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Traffic Service Position System No. 1:

Station Signaling and Announcement Subsystem: Hardware for Automated Coin Toll Service

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A new subsystem, Station Signaling and Announcement Subsystem (SSAS), *was added to* TSPS *to provide automated coin toll service. Presented here are descriptions of how this new subsystem generates announcements from digitally stored speech samples, how it responds to coin deposit signals from coin stations, how the announcement circuits and coin tone detection circuits are automatically tested, and how the subsystem is physically packaged.*

I. INTRODUCTION

The new functions needed in TSPS for Automated Coin Toll Service are provided by the newly designed Station Signaling and Announcement Subsystem (SSAS). SSAS delivers voice announcements to customers at coin stations and responds to the coin deposit signals generated at the coin stations.

SSAS can be described from two perspectives, that of a coin toll customer and that of the TSPS processor. From the coin toll customer's viewpoint, it should sound and react the same as or better than the human operators the customer is accustomed to. From the standpoint of the TSPS processor, it operates as an "intelligent peripheral," using the existing instruction and data buses. In response to TSPS instructions, it constructs announcements to request and acknowledge coin deposits. It keeps track of each customer's coin deposits and then reports the amount of the completed deposit to the processor, which then sets up the call. If the customer does not deposit enough coins, SSAS delivers requests for the balance, or finally sends a time-out

report to the processor so an operator can be brought in to assist the customer. To provide reliable service, the SSAS control circuits are duplicated, with one control circuit active and the other standby. They contain self-checking features so faults can be detected promptly and reported to the TSPS processor, enabling a smooth switchover from the active to the standby SSAS controller.

The interface of SSAS with customers is through a number (up to 239 per system) of Coin Detection and Announcement circuits (CDAS). Each CDA provides service to one customer at a time. Each CDA contains a coin tone receiver that recognizes the nickel, dime, and quarter deposit signals from dual-frequency, single-slot, coin stations. Each CDA also contains a digital-to-analog decoder that converts bits at 31,250 b/s into natural-sounding voice announcements. To provide for connecting an operator if the customer has difficulty and to reduce the possibility that operator or automated announcement speech will interfere with correct coin recognition, each CDA also includes a 4-wire, voice-frequency network with an extra port for the operator. Each network contains 4-wire terminating sets and amplifiers to isolate the coin-tone receiver and digital-to-analog decoder from one another. In addition to the customer-serving CDAS, each SSAS contains one unique CDA circuit that functions as a built-in test set.

Figure 1 shows the essential parts of a connection from a customer to an SSAS CDA.

Before the advent of SSAS, a coin call needing TSPS operator service would be connected through a TSPS trunk and the TSPS network to an operator position or to a service circuit for ringing or busy tone. With SSAS, a call identified as eligible for automated coin detection handling is immediately connected to a CDA. If it later develops that an operator is needed, one can be connected to speak to the customer or to listen to the automated announcements and coin signals.

Figure 2 shows the principal parts of SSAS along with the input and output data bus connections to the TSPS processor.

The coin-tone receivers in the CDAS deliver detected coin data to digital registers, also in the CDAS. These registers are scanned periodically, and the data are ultimately relayed back to the TSPS processor. The digital-to-analog decoders that deliver the announcements were adapted from an earlier Bell Laboratories design, Subscriber Loop Carrier 40 (*SLC*™-40). They are preceded by serial buffers that are loaded sequentially, with bursts of 40 bits transmitted at a 1-mHz rate. The bits are decoded at a steady rate of 31,250 b/s.

As mentioned earlier, as many as 239 CDAS can be associated with one SSAS. Since the holding time needed to request and collect coin deposits for a typical call is relatively short, 239 is expected to be enough CDAS to handle the coin toll traffic in large metropolitan TSPS offices. The CDAS are operated by a controller frame and an associated

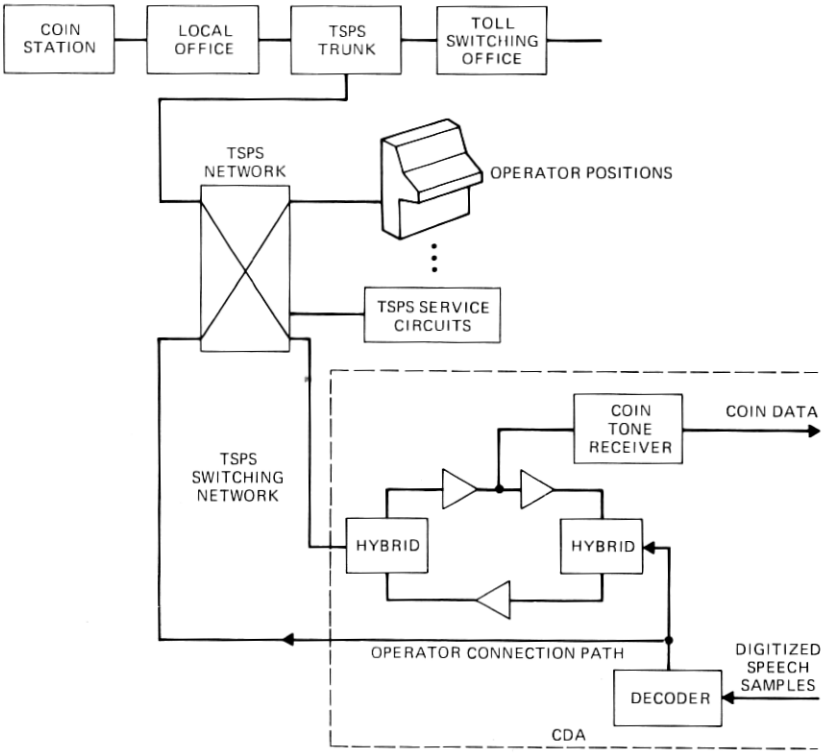


Fig. 1—Connection of SSAS CDA into TSPS.

semiconductor announcement store. For backup in case of failure, there is an identical controller frame/announcement store pair. The announcement store, except for minor modifications to make it accessible either from the SSAS controller or the TSPS processor, is the same design as the TSPS processor main store frames. It may contain up to six memory modules, each containing 32K 47-bit words. Forty bits of each word are data; seven are used for error detection and correction.

The controller frame contains a programmable controller (PROCON) and wired logic which, in response to instructions from the TSPS processor, retrieves samples of digitized speech from the announcement store and distributes them in a multiplexed scheme, with a fixed sequence, 40 bits at a time, to the CDAs. The announcement distribution sequence has 256 time slots, of which 16 are used for test instructions and 240 are used to deliver bits to the 239 CDAs and the one test channel. The distribution sequence is repeated every 1.28 ms, so that each CDA, using bits out of its serial buffer at a rate of 31,250 b/s, for announcement generation, is supplied with precisely enough data to produce uninterrupted announcements consisting of 512-ms segments joined together.

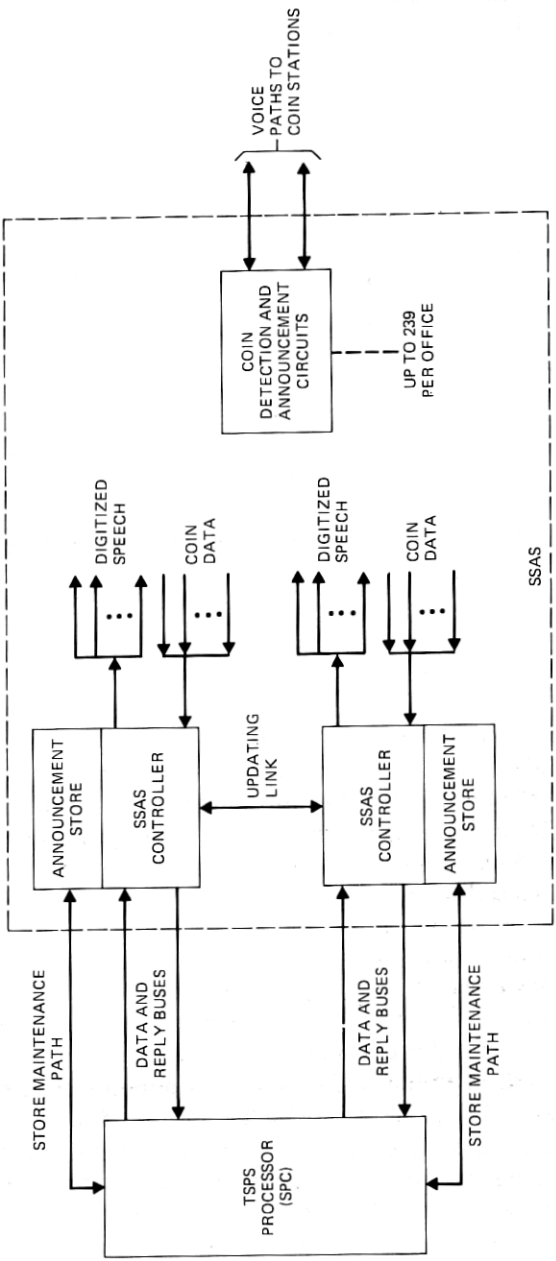


Fig. 2—SSAS block diagram.

If an office were equipped with the full complement of 239 CDAs, it could deliver announcements to 239 customers simultaneously. When there are not 239 CDAs installed, or when not all installed CDAs are in use, a bit pattern representing silence is placed in each inactive time slot.

At the same time that the PROCON in the SSAS controller is distributing 40-bit digitized speech segments to the CDAs, it is sequentially scanning, over separate data paths, registers connected to the outputs of the coin tone receivers in the CDAs to gather data on coin deposits. The coin deposit data, including the time when the deposits occurred, is stored by the PROCON in "scratch pad" memory. The deposit and time data are used to determine future actions, i.e., additional announcements or reports to the TSPS processor when the deposits are sufficient.

Both the active and standby controllers have access (one at a time) to all CDAs. The two controllers do not operate synchronously with matching for error detection. Each, however, contains a close tolerance crystal-controlled clock, so any time difference between them would be only a few microseconds, a difference not noticeable to customers in the event of a switchover. The maintenance and initial loading of the announcement stores takes place over the store maintenance paths shown in Fig. 2. These paths, in fact, are extensions of the existing TSPS processor store buses.

The updating link shown between the two SSAS controllers is a parallel, 17-bit (16 plus parity), 1-mHz link interconnecting the PROCONs in the two controller frames. This link provides two very powerful features. First, if one announcement store is powered down for maintenance, reloading over the store bus would require human action to set up a tape drive and many minutes of loading time. With the updating link, however, the PROCON in the active controller can, interleaved with normal handling of announcements and coin data, transmit in a few seconds the entire contents of the active announcement store to the just-restored inactive announcement store.

Second, while the active controller is dealing with the ever-changing coin collection data stored in its "scratch pad" memory, the same data are being continuously relayed through the updating link to the memory of the standby controller. This makes it possible to perform a planned or unplanned switchover to the standby controller, usually without interrupting announcements or losing track of the coins that as many as 239 customers may be in the process of depositing.

II. DETAILED HARDWARE IMPLEMENTATION

The development of SSAS includes several areas that are felt to be of some general interest and will be discussed further here. These are:

1. Storage, retrieval, and decoding of announcements.

2. Coin deposit signaling and detection.
3. Automated testing of coin detection and announcement circuits.
4. Physical design.

2.1 Announcement storage and processing

The continuing orders-of-magnitude decrease in the cost of digital memories made it clear that the storage of announcements for SSAS should be digital rather than analog. A major decision for SSAS was whether to use writable store (RAM) or read-only memory (ROM) to store the announcement vocabulary. For some recently developed or proposed "talking" systems, ROM is clearly the better choice. For personal calculators for the blind, for example, the vocabulary is well defined to include just the digits zero through nine and the names of the arithmetic operations. Reloading a volatile memory in a portable calculator would be clearly impractical. Also, ROMs can be packaged more densely. For SSAS, however, although the vocabulary for coin traffic might appear to be constant, it is subject to change when call-handling practices change. There may have to be vocabulary differences among operating companies because of differences in their practices concerning overtime collection. More important, when new features are added to SSAS, a significant amount of new vocabulary will have to be added. If the SSAS vocabulary were stored in read-only-memory, the logistics and cost of managing spares, repairs, and additions appear to be objectionable. With a writable memory of the type already in use in TSPS, no special handling of memory units will be needed. New vocabulary can be distributed to operating companies as needed on reels of magnetic tape, using administration procedures already established for distribution of TSPS software updates. Although data in a writable store are subject to loss in the event of a power failure, the back-up power arrangements in Bell System central offices make a shutdown of both announcement memories unlikely; if it does occur, their contents can be restored from a tape stored in the office.

The SSAS announcement vocabulary presently includes 80 512-ms speech segments and the equivalent of 15 more speech segments containing test tones and timing data for automatic self-testing. Each 512-ms segment requires 16,000 bits, stored in the 40-bit data portion of the words at 400 consecutive addresses in the announcement store.

The semiconductor program/data store recently developed for use in TSPS was selected for use with some modification as the SSAS announcement store. Figure 3 is a photograph of this store. This store frame can be equipped with up to six modules, each holding 32,000 47-bit digital words. The 95 presently used vocabulary segments require 38,000 digital words, so the frame presently used in SSAS is equipped

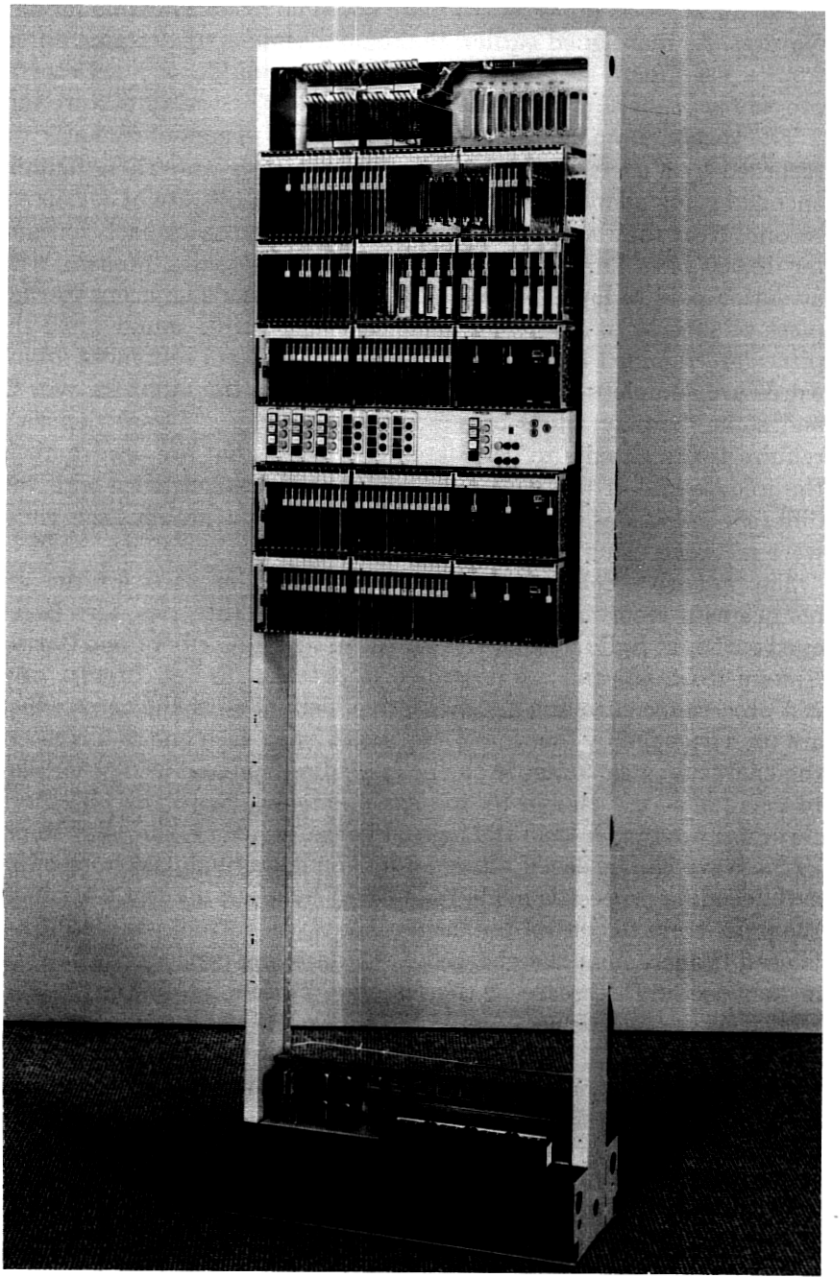


Fig. 3—Announcement store frame.

with only two memory modules. A store frame fully equipped with six modules would accommodate 480 512-ms segments. Since 95 are now in use for ACTS, as many as 385 more could be made available for new features. As mentioned earlier, the announcement store frame differs from a TSPS main store frame only by the addition of a selector to provide access either from the SSAS controller or the TSPS store bus.

The vocabulary of 80 words needed for the SSAS announcements was recorded by a professional announcer. The words were then digitally encoded using adaptive delta modulation with a bit rate of 31,250 per second. Next they were edited into 80 512-ms segments, each containing 16,000 bits. The editing was a subjective listening process, with attention paid to level, pitch, and the silent periods adjacent to each piece of speech, to assure the most natural possible sound when the pieces are rejoined in various combinations to form sentences. Many words are complete in a single 512-ms segment; the numbers over 20 and some common parts of announcements (e.g., "Please deposit") require two segments to complete. The words that are used both in the middle and at the end of sentences are included twice with two different inflections. The 15 equivalent segments containing test tones were recorded using laboratory signal generators.

The adaptive delta modulation (ADM) encoder used for the announcement recording and the decoders used in the CDAS were developed earlier at Bell Laboratories for use in the Subscriber Loop Carrier System (*SLC*-40) and are described in detail in Ref. 1. Briefly, ADM is a process for encoding a signal into a train of ones and zeros which are then decoded by the simple process of using each one to increment the charge on a capacitor in the positive direction and using each zero to decrement the charge by the same amount. Since the bit rate is several times higher than the highest voice frequency, the "stairsteps" in the wave can be easily filtered out. The delta modulation encoding and decoding process is made "adaptive" by using the last few bits in the pulse train to control the magnitude of the current generator that is used to increment the charge on the decoding capacitor. The rates of increase and decrease of the adaptive current generator are controlled by R-C networks tailored to the average parameters of speech syllables.

Adaptive delta modulation produces thoroughly adequate announcement quality using 31,250 bits per second, about half the bit rate that would be needed by 7- or 8-bit pulse code modulation (PCM) using an 8-kHz sampling rate.

The announcement decoder for each of the SSAS CDAS is on a single 6-by-8-inch circuit pack. Each pack includes the decoder circuit from the *SLC*-40 design (adapted for slightly different power supply voltages), a "silence" generator, and a serial input buffer. The silence generator is a flip-flop controlled by a clock to produce alternating

ones and zeros. It is intended to be brought into operation in midword to silence an announcement quickly when a customer starts to deposit coins. This feature allows a substantial speedup in service for customers who already know the charges for calls they are making. The serial input buffer is a self-shifting, first-in/first-out (FIFO) shift register device, available commercially from several manufacturers. It is loaded at a 1.0-mHz rate each time the 40-bit data bursts arrive. It is unloaded continuously into the decoder circuit by the 31,250-Hz clock distributed to all the CDAs.

The sequential distribution of 40-bit announcement segments to all the CDAs is controlled by the PROCON and by wired logic that automatically steps through the 400 store addresses for each speech segment and distributes the data to the 239 CDAs and one test circuit. The retrieval of the words from the 400 consecutive announcement store addresses is controlled from a pair of 256-word recirculating shift registers. These shift registers are used in an alternating fashion. One is loaded by the PROCON with the 256 initial addresses of the announcement segments needed for the next upcoming 512-ms period. One particular address is used to represent silence for inactive or unequipped CDAs. The second shift register, which was previously loaded with the initial addresses for all the announcements (or 512-ms silence segments) in progress, is recirculated 400 times, and each time a one is added to all the addresses. Thus the set of 256 starting addresses is altered at each recirculation to step through the 399 addresses that follow each initial address. These addresses are used to retrieve the announcement data words, which are then distributed in sequence to the CDAs for decoding. After the 400 recirculations, the roles of the two recirculating shift registers are reversed. The recirculation and incrementing begins with the new set of starting addresses, and the just-exhausted shift register is loaded with the still newer set of starting addresses for the next 512 ms of announcements. Each 512-ms interval, when a new set of announcement addresses is loaded, is referred to as a "base period."

2.2 Coin deposit signaling and detection

Coin deposits were reported to an operator for many years through a largely mechanical system. In the widely used 3-slot coin station, the coins rolled and bounced against gongs to produce "bing" for a nickel, "bing-bing" for a dime, and "bong" for a quarter. To provide added flexibility for changes in the initial deposit on local calls and to provide substantially more protection against counterfeit coins and slugs, a new single-slot coin station was introduced in 1966. In this coin station, the coins, after passing through a mechanism that tests them for dimensions, mass, and conductivity, trigger an electromechanical device called a totalizer. After each coin passes, the totalizer resets itself,

and in so doing, momentarily switches on a pulsed-electronic oscillator that produces one "beep" for a nickel, two for a dime, and five for a quarter. In principle, single-frequency "beeps" from such a coin station could be recognized by a tuned electronic detector and counter. However, Bell System experience with multifrequency and *TOUCH-TONE*® signaling indicated that adequate protection against errors caused by speech or noise could be provided only by using dual-frequency "beeps" to represent coin deposits. Accordingly, a low-cost dual-frequency oscillator assembly was designed and introduced into the manufacture and refurbishment of coin stations starting in 1975. This was done deliberately well in advance of the service cutover of SSAS (late 1977) so that a minimum of coin station modification visits would be needed when Automated Coin Toll Service is introduced to an area.

2.2.1 Coin tone receiver operating environment

Coin tone signaling may take place in the presence of ambient speech and noise. Speech interference, for example, may be due to a synthesized announcement in progress, customer speech, an operator talking, or background noise at the coin station at the same time that coins are being deposited. The SSAS coin tone receiver is required to respond correctly to these coin tone signals in the presence of such speech or noise interference. The human ear (and mind) usually has no problem identifying tone signals in the presence of speech and can easily differentiate tone signals from speech. Electronic detection of tone signals, if it involved only receivers tuned to the specific frequencies, would be vulnerable to errors from speech signals since vowel sounds in speech frequently contain frequency components in the recognition band of the coin tone receiver.

The speed of operation of the electromechanical totalizers in the coin stations is affected by temperature, by the dc current available from the loop to the central office, and by wear of the totalizer parts. Consequently, the coin tone receiver must accept a coin deposit signal whose timing varies over a considerable range.

2.2.2 Coin tone receiver overall design philosophy

The basic design requirements can be summarized as follows. The coin tone receiver should:

(*i*) Recognize coin tones from widely ranging coin stations.
(*ii*) Identify a coin station whose performance is outside of requirements.
(*iii*) Operate in the presence of speech.
(*iv*) Reject coin simulations.

The first two requirements are met by accurate timing of the received signal to identify both valid coin deposit sequences and those

from coin stations with defective timing mechanisms. The third and fourth requirements, operating in the presence of speech while rejecting coin simulations, are major considerations and have a significant impact on the receiver's design. As was mentioned earlier, speech may frequently contain sufficiently sustained tone components that simulate coin deposits. By using dual-frequency coin signaling for ACTS, where both tones have to be present simultaneously for a signal to be valid, the coin simulation rate is reduced by a considerable degree. A simple detector that looks only for the presence of the two required frequencies, however, still does not provide adequate simulation immunity. Further receiver protection against coin simulations by speech is obtained by looking at other energy (called guard energy) besides the signal frequencies. If the guard energy is sufficient, the "signal" is assumed to be speech, and tone detection is blocked even though signaling energy may also be present. However, speech from the operator, announcement, or the calling station may be present while coins are being deposited. Thus receivers designed to give good coin simulation protection may be blocked or "talked down" when speech or noise is superimposed on tone signals. This can be seen in Fig. 4, where ambient speech interferes with and partially blocks tone detection and at the same time causes false detection (coin simulation) during the silent interval between bursts. Since the cure for one problem makes the other worse, a compromise but exacting choice must be made in establishing receiver operating parameters.

To reduce the effect of "talkdown" and coin simulation due to the operator and/or announcement, a four-wire terminating set is used to isolate the receiver from speech signals directed toward the originating station. However, because of nonideal return losses associated with trunks, loops, and various terminations, some portion of this speech energy is reflected back to the coin tone receiver. The returned signal

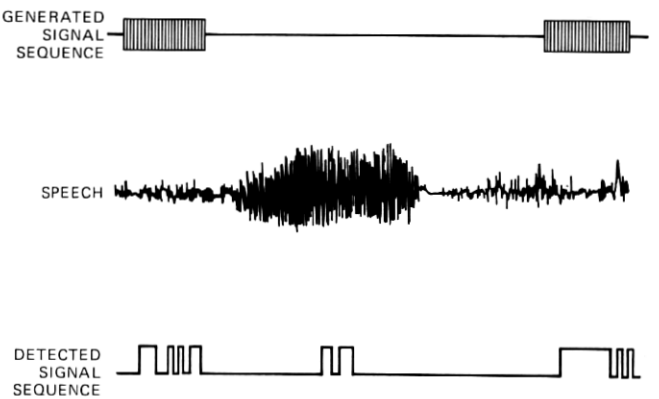


Fig. 4—Coin signal in the presence of speech.

is usually at a considerably lower level so that the probability of interference with signal reception is substantially reduced.

The interfering effect of the announcement is reduced even further by truncating it at the earliest indication of a received coin tone signal. The receiver sends to the ADM circuit pack in the CDA a command to truncate the announcement even before the minimum duration legitimate coin burst is timed. Hence, if a false detection were due to signaling frequency components within the announcement itself, the signal would disappear before a coin simulation could be produced. If the detection were legitimate, truncation would prevent any further talkdown by the announcement.

2.2.3 Coin tone receiver subdivision

Notwithstanding the coin simulation and talkdown protection provided by the four-wire terminating sets and announcement truncation, the receiver itself must have additional safeguards to distinguish between speech and coin tones, yet recognize tones in the presence of speech. This is accomplished in a two-phase processing approach: tone recognition and tone validation. The front-end analog tone recognition portion of the receiver "detects" the signal while providing the initial balance between coin simulation protection and "talkdown" protection; the digital tone validation timing portion then applies different validity standards to various portions of the "detected" signal to determine the coin denomination.

The analog portion (Fig. 5) is similar in principle to existing receiver designs for *TOUCH-TONE* signaling. (*TOUCH-TONE* signaling and receiver design considerations are described in Ref. 2.) It consists of filters, limiters, and detectors which produce a logic 1 output to the timing circuitry when both signal frequencies are simultaneously detected. As was mentioned earlier, tone detection is blocked when sufficient "guard" energy is present. The input bandpass filter (BPF) controls the total frequency range of signals entering the receiver. If this filter is broad, a considerable spectrum of the speech energy entering the receiver will be applied to the limiters. If the speech contains components at the signaling frequencies, it is likely that these components will be dominated by the other speech components, which will "capture" the limiters. Thus the signaling components passing through the bandpass filters, which follow, will not be of sufficient amplitude to operate the detectors. This method of preventing coin simulation is known as "limiter-guard action" and is the technique employed in *TOUCH-TONE* signaling to reduce the incidence of digit simulations. Therefore, a broad input BPF provides good coin simulation protection. If, however, legitimate coin signals are being transmitted while speech is present, they may also be blocked by speech.

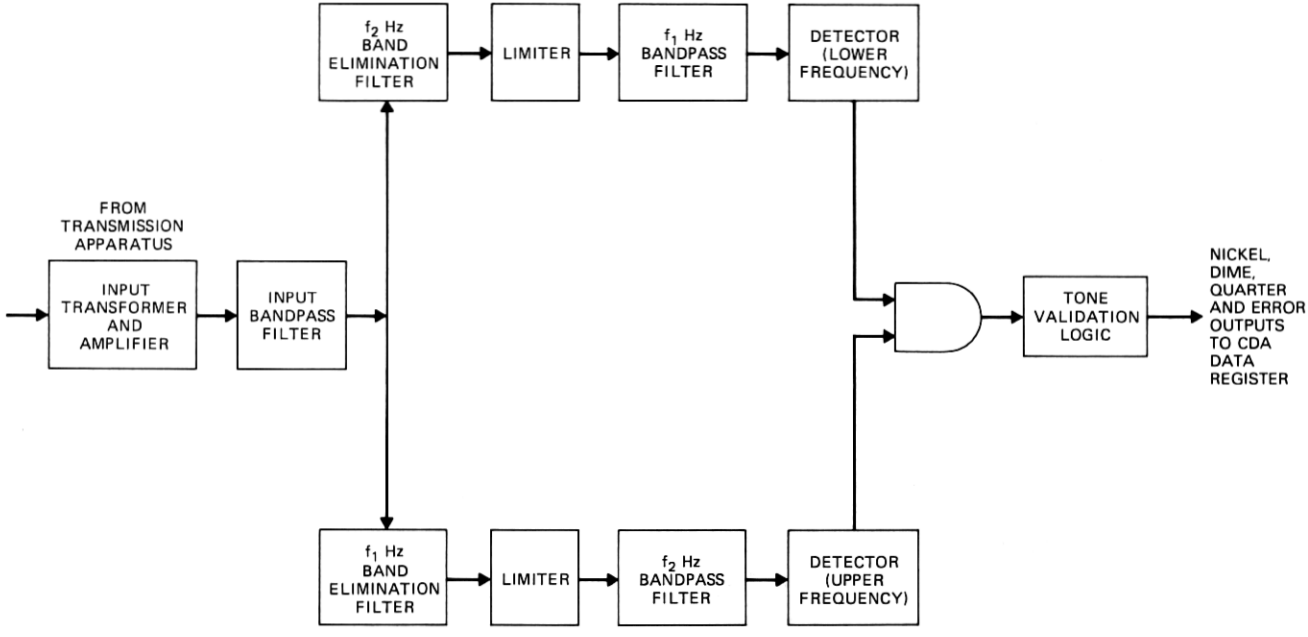


Fig. 5—Coin tone receiver.

Hence, "talkdown" protection will be poor. If the input BPF is narrowed (the input BPF must be at least wide enough to pass the two signaling frequencies), less speech energy can get through and, while "talkdown" is improved, less protection is provided against coin simulation. Based on laboratory and field tests, a filter was selected to optimize the tradeoff between the detector's coin simulation and "talkdown" protection.

The logic signal indicating dual-tone detection is applied to the receiver's tone validation timing circuitry which performs the following functions:

(*i*) Processes the detected signal (refer to Fig. 4 for a sample detected signal) to form "discrete" burst and silent interval logic signals in accordance with the timing algorithm by filling in some gaps while ignoring some burst portions.

(*ii*) Totalizes the number of "discrete" bursts received.

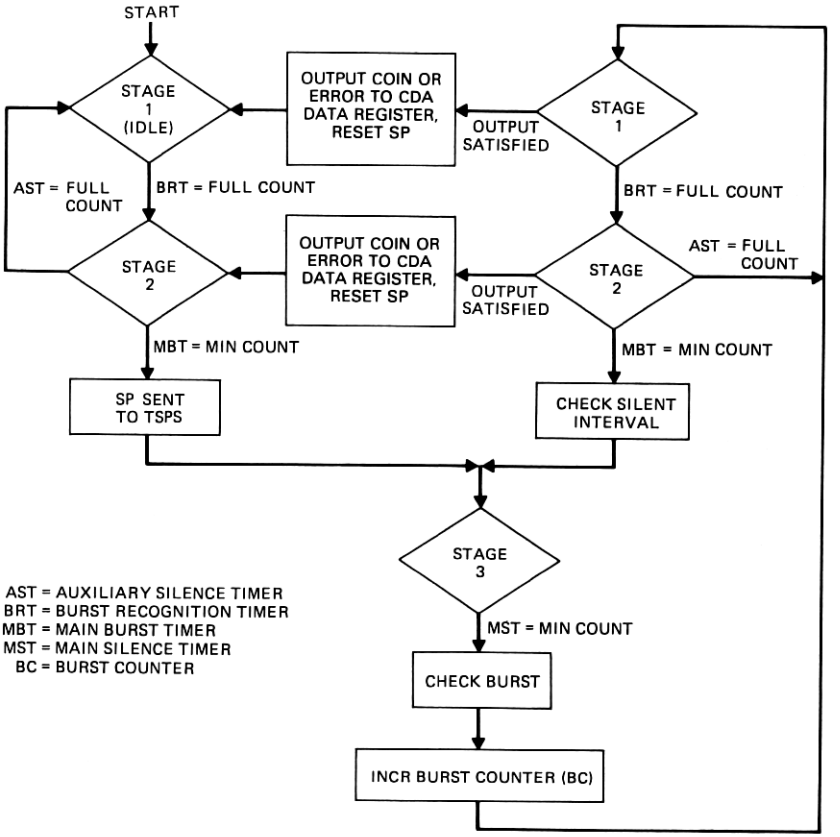
(*iii*) Categorizes each "discrete" burst or silent interval after it is formed and makes a preliminary determination of the coin denomination at that time.

(*iv*) Checks for consistency with previous burst and silent intervals to narrow the denomination possibility for that coin and also check for coin station timing malfunctions.

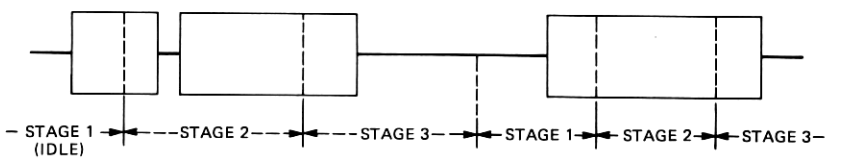
(*v*) Outputs the coin denomination or timing error signal when certain conditions are satisfied regarding the number of bursts received, the apparent coin category, and the amount of silence since the end of the last burst.

2.2.4 Receiver outputs

As the receiver performs signal timing in accordance with the timing flow diagram in Fig. 6a, certain output conditions may be satisfied and an output representing one of the coin denominations or a timing error (representing an out-of-tolerance coin station) will be delivered to a CDA data register. Before any coin or timing error outputs can be sent, however, the receiver must first deliver a Signal Processing (SP) signal. The SP signal is sent when the timing of the first burst of a suspected coin deposit reaches a certain minimum value. It remains active until a coin identification or timing error output signal is transmitted or the suspected coin deposit is deemed to be a coin simulation. At that time processing for the coin is assumed to be completed. The SP signal is used in the announcement decoder to truncate the announcement (see Section 2.2.2) by switching in the silence generator. The receiver also sends a DST (data strobe) signal along with the outputs, which gates the coin denomination or timing error indication into a data register in the CDA.



(a)



(b)

Fig. 6—Timing algorithm. (a) Algorithm flow. (b) Sample detected signal sequence.

2.2.5 Circuit implementation

The tone detection portion of the receiver (see Fig. 5) is based on existing receiver designs for *TOUCH-TONE* signaling. The input bandpass filter, which is critical to the detector's response to speech and also to its performance when tones are being received in the presence of speech, was discussed in detail in Section 2.2.3.

Following the bandpass filter are two band-elimination filters (BEFs) in parallel. The width of these filters is tailored to the tolerances of the coin station oscillators. The first filter rejects the higher of the two signaling frequencies, and the second filter rejects the lower. Thus the output of the high BEF will contain the lower of the two signaling frequencies, and the output of the low BEF will contain the upper signaling tone. The limiters that follow convert the signals to square waves. Hence, at this point, there are two square waves, one out of each limiter.

These signals now pass through bandpass filters centered at the two signaling frequencies. The square wave out of the low frequency limiter passes through a filter centered at the low frequency and a sine wave output is produced. The same occurs for the upper frequency square wave. Following the filters are threshold detectors that detect the sine waves if they are above a certain threshold level. The limiter employs a feedback arrangement to control the limiter operating threshold. The two detector outputs are combined to produce a logic output that is timed by the receiver's tone validation circuitry to determine the denomination of the coin.

Wherever possible, components originally designed for *TOUCH-TONE* signaling are used for design implementation. These include the limiter-threshold generator circuit module, STAR (standard tantalum active resonator) filter circuit modules similar to those for *TOUCH-TONE* signaling, and the detector modules. These circuit modules are hybrid integrated circuits. The analog tone detector circuitry occupies two 4- by 8-inch printed wire boards. The filters are on one board, and the remaining detector circuitry is on the other.

Tone validation timing is done digitally, with the circuitry consisting primarily of small scale integration (SSI) and medium scale integration (MSI) TTL devices. A 1-kHz clock signal synchronizes all tone validation timing operations within the receiver. This clock sets the rate at which the tone detect signal from the analog circuitry is sampled. Based upon whether the dual tone detector is high or low at the sample instant, the various gates, counters, flip flops, etc., are operated in accordance with the tone timing validation algorithm. This tone validation circuitry takes up four circuit packs, making a total of six packs for the entire receiver. Subsequent to deployment of the random logic timing circuitry, a cost reduction was made by having a microprocessor perform the timing algorithm. The entire tone timing validation circuit was placed on one circuit pack, lowering the overall circuit pack count to three.

2.3 Automated testing of announcement and coin detection circuits

The use of digital speech storage and PROCON control in SSAS made it possible, with a very small amount of added hardware, to provide

automated testing of the speech decoding and coin tone receiver circuits.

The adaptive delta modulation decoding circuits in the CDAs are tested by using four single frequency tones digitally stored in the announcement store. Three of the tones are within the frequency band of the voice announcements, and the fourth is just above that band. The three in-band tones verify the flatness of response of the decoder and the transmission network associated with it. The out-of-band tone verifies correct roll-off response of an active low-pass filter included in each CDA to filter out the 31,250-Hz "stairsteps" that result from the decoding process.

Under control of a diagnostic program, each CDA is periodically taken out of service, and the digitized test tones are distributed to it from the standby SSAS controller frame. The TSPS processor simultaneously sets up a network connection from the output of the CDA circuit under test to the CDA test circuit. The CDA test circuit connections for decoder testing are shown in Fig. 7. The CDA test circuit contains a bandpass filter that passes all the test frequencies, followed by a level detector that delivers "go/no-go" responses to indicate when the detected levels are in or out of tolerance. Also included in the CDA test circuit are four active "notch" filters followed by a detector and a smoothing filter. The notch filters remove the fundamental of each test frequency, and the detector responds to the residue, which includes harmonics and noise resulting from the adaptive delta modulation encoding/decoding process. The detector delivers a logic level "no-go" output if the residue is higher than normal. The smoothing filter is needed because, after the fundamental has been removed, the residual combination of harmonics and decoding products is partly random,

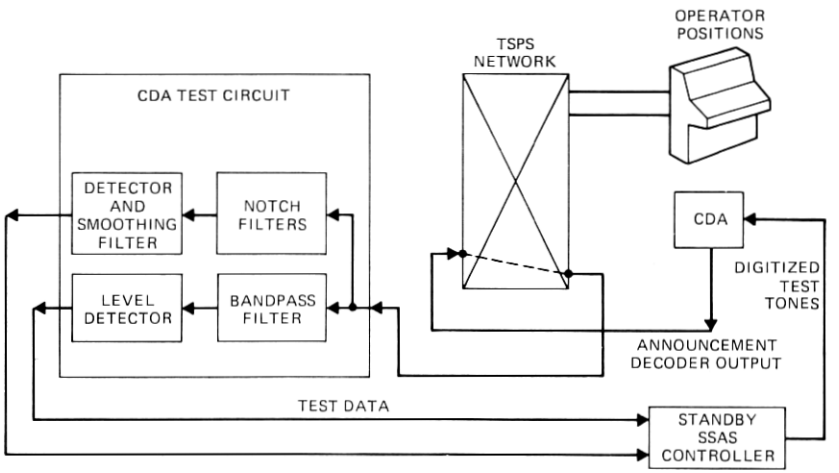


Fig. 7—Testing CDA decoders.

and without smoothing it would cause occasional "false alarm" responses at the detector output.

Testing CDA decoder circuits in the way described above verifies the integrity of the logic circuits and wiring that retrieve and distribute digitized speech segments, and it checks for continuity and proper alignment of the voice frequency transmission apparatus that connects the CDAs to the TSPS trunks.

The coin tone receivers are also tested by using tones stored in the announcement memory. The diagnostic program for the coin tone receivers directs the digitized coin test tones to a CDA decoder circuit pack that is dedicated for this purpose. The output of this decoder is routed through a solid-state switch controlled to produce tone bursts that simulate the coin station output signals that represent nickels, dimes, and quarters. The tone bursts are passed through switchable attenuators and through TSPS network connections to each coin tone receiver in turn. CDA test circuit connections for coin tone receivers are shown in Fig. 8.

A very comprehensive test sequence is applied to the coin tone receivers using the scheme described above. The coin test tones are recorded and stored with nominal frequencies and frequencies just inside and just outside the operating tolerances on both sides of the nominal frequencies. The solid-state switch is operated to produce the nominal tone bursts that check the receiver's detection of the various nominal and edge band frequencies and a variety of non-nominal durations and sequences that exercise the receiver's timing logic. The switchable attenuators control the levels of the tone bursts in the test sequence to provide verification that the coin tone receivers operate over the range of levels that result from coin station and transmission

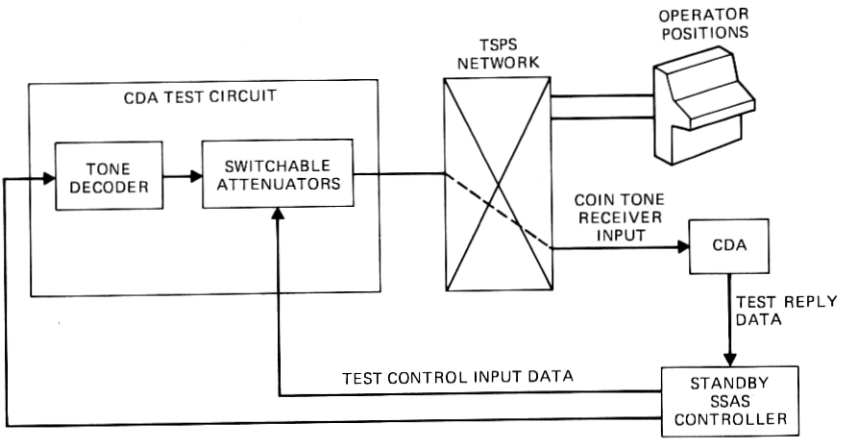


Fig. 8—Testing CDA coin tone receiver.

loss variations. The test sequence for each coin tone receiver is completed automatically in a few seconds.

The CDA test circuit includes four circuit packs identical to a set of four used in each CDA, and five additional packs unique to the test circuit. The CDA test circuit also has a self-test mode. In this test mode, the output of the tone generation and control circuits of the CDA test circuit are temporarily fed back to the input of the filter/detector circuits and a "wrap-around" test sequence is executed.

2.4 Physical design considerations

A complete SSAS installation includes two controller frames, two announcement store frames, from 2 to 15 pairs of frames containing coin tone receivers, announcement decoding circuits, voice frequency terminating sets and amplifiers. The coin tone receivers and announcement decoding circuits are mounted in service circuit frames (up to a maximum of 16 sets per frame) and the voice frequency circuits are similarly mounted in transmission frames.

2.4.1 Controller frame

The controller frame (Fig. 9) is a single-bay frame, 2-ft 2-in. wide and 7-ft high, using a 12-in. deep framework, as do most other TSPS frames. This frame is compatible with all other TSPS frames and requires no special hardware, mounting, or installation arrangements.

The communication bus and interconnection unit at the top of the controller frame contains multi-pin terminal strips for terminating cables from connecting frames. The connections to the announcement store are also made through this unit. Transformers are furnished for connection to the TSPS buses. Bus connectorization for growth is provided, and is compatible with existing office arrangements.

The logic unit in the upper part of the controller frame includes six levels of circuit packs and a control panel unit. Five-volt power and ground return for the circuit packs are provided by a double-sided, printed-wiring back plane for each of the six levels. Each level is split into two halves for power distribution. Five levels can accommodate up to 37 circuit packs on ½-in. centers. The sixth level can accommodate 28 circuit packs on ½-in. centers. A very large percentage of the backplane wiring is automated. The type of circuit pack used is a double-sided printed wiring board, 6 in. by 7 in. in size, with 80 pins. An example of this circuit pack is shown in Fig. 10.

The control panel unit contains the various keys, lamps, and jacks for maintenance and frame control functions.

The memory and control unit provides mounting arangements for the PROCON and its associated memory packs. Connectorized cables are provided within this unit and between parts of the logic unit.

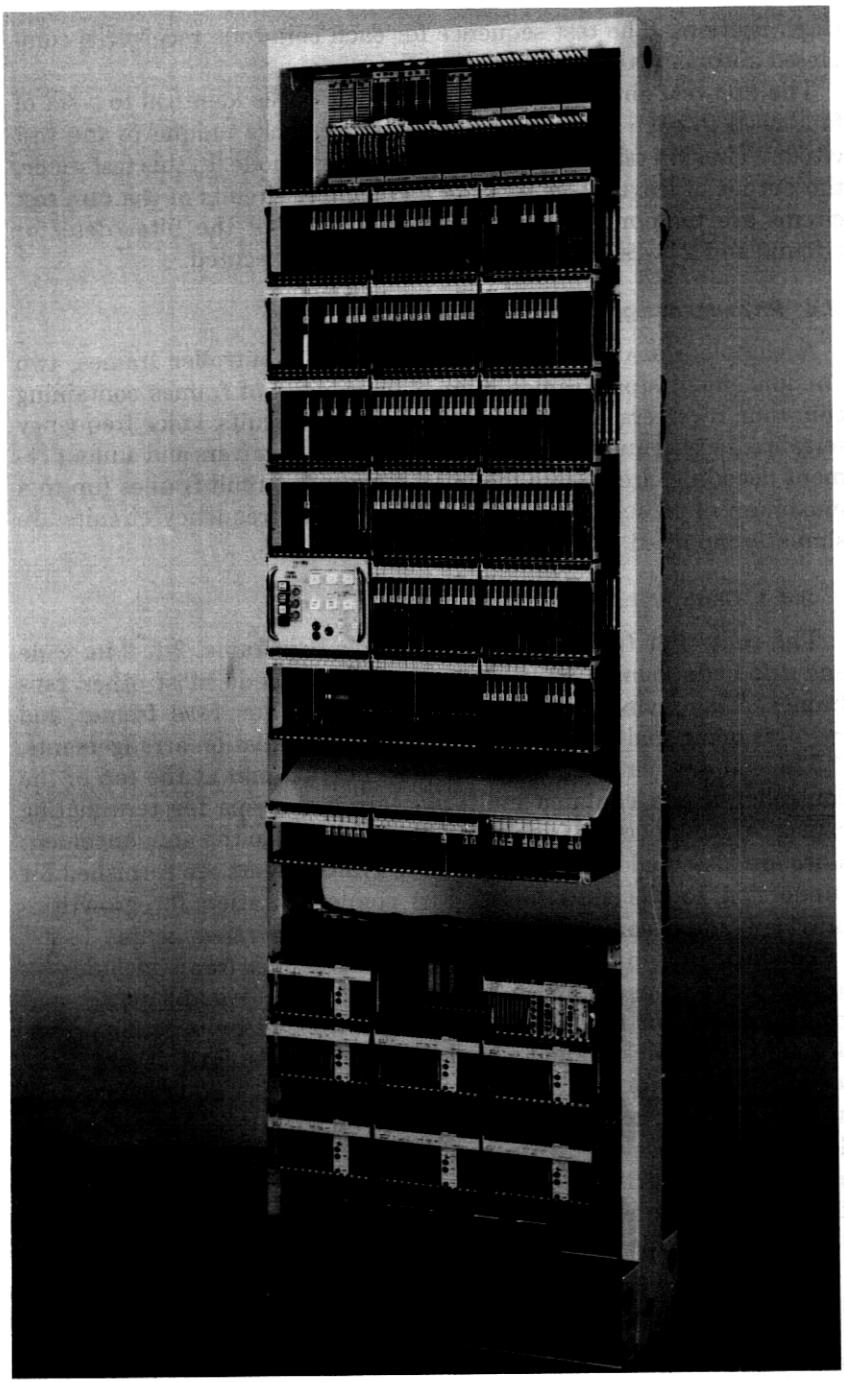


Fig. 9—Controller frame.

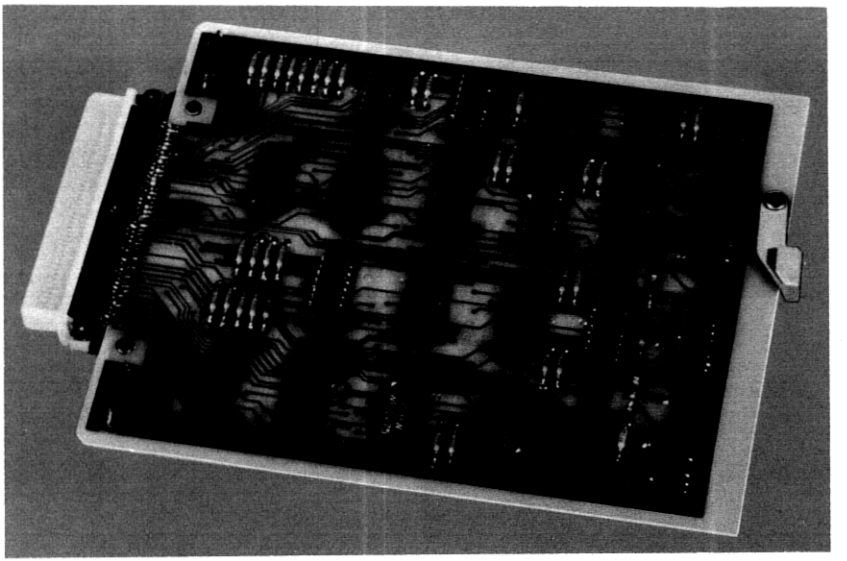


Fig. 10—Controller frame circuit pack.

The power converter unit contains +5 V and −12 V dc-to-dc converters and fuses. These power units are pluggable for easy replacement. A +5 V load fuse and a pilot fuse are provided for each half of the circuit pack levels and for the memory and control units.

The fuse panel unit contains −48 V and +24 V fuses, alarm relays, and power control relays. The −48 V is used to supply the dc/dc converters. The +24 V is used in the circuit packs that contain bus drivers.

2.4.2 Service circuit frame

The service circuit frame (see Fig. 11) is a single-bay frame, 2 ft, 2 in. wide and 7-ft high, using a 12-in. deep framework. Each frame may contain as many as 16 CDAs. A maximum capacity SSAS installation would include 15 service circuit frames to hold 239 CDAs plus one CDA test circuit.

The service circuit frame uses multi-pin terminal strips and bus coupling transformers for terminating cables from other connecting frames. In addition, the unit is arranged to hold three levels of circuited packs. These packs are associated with the 16 CDAs and the circuits that provide switchable access to either controller frame. The +5 V power is supplied individually to each service circuit and to each of the group controllers. Printed-wiring back planes provide +5 V ground return for each pack. A large part of the unit wiring is automated. This unit is always wired for 16 circuits and is equipped by plugging in circuit packs as determined by traffic requirements.

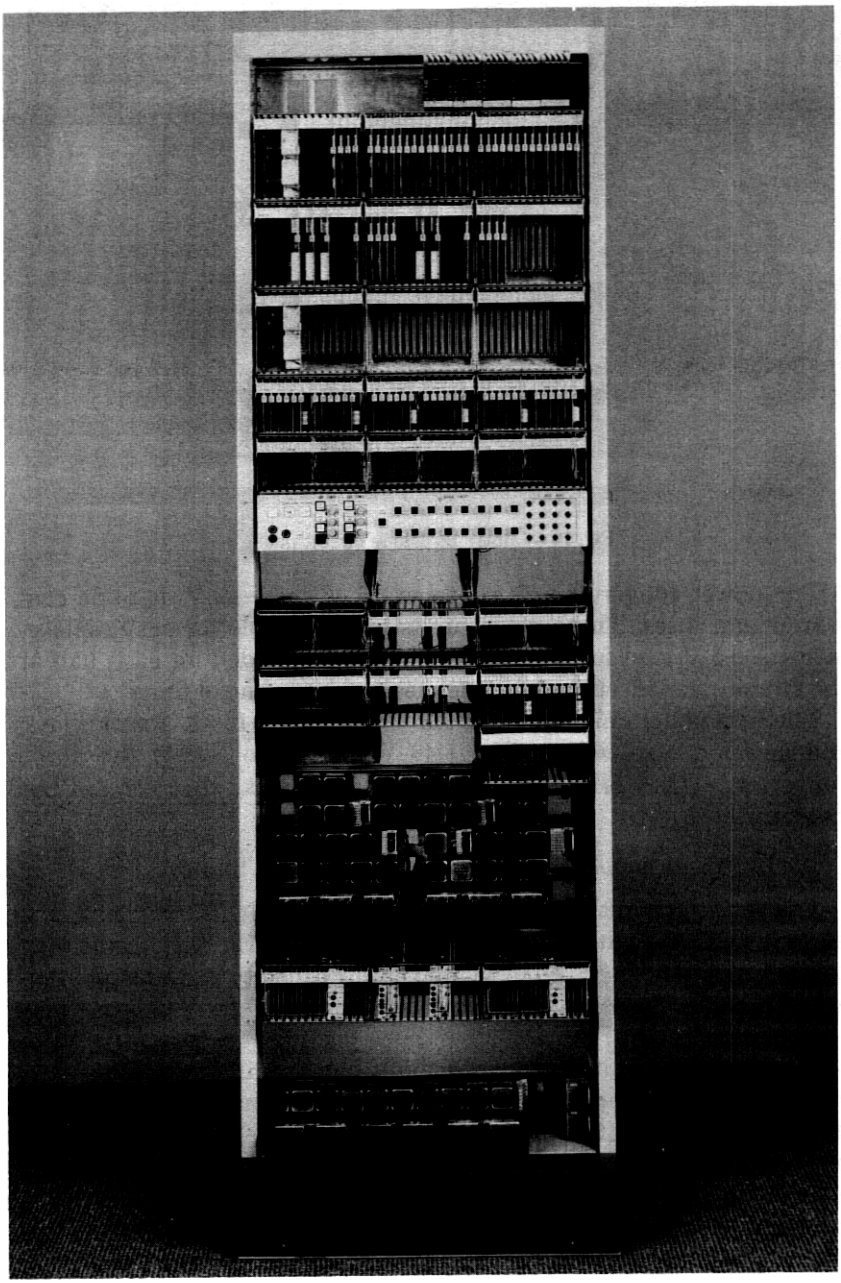


Fig. 11—Service circuit frame.

The control panel unit contains the various keys, jacks, lamps, and switches associated with maintenance and frame control functions. Each CDA is controlled individually.

The power converter unit contains +5, +6, and −6 V dc-to-dc converters and fuses for the +5 V distribution. These power units are pluggable for easy removal. A +5 V load fuse and a +5 V indicator fuse is provided for each service circuit.

The fuse panel unit contains −48 and +24 V fuses, alarm relays, and power control relays. The −48 volt is used to supply the dc/dc power units. The +24 V is used for bus drivers.

Even-numbered frames and odd-numbered frames are fused from separate power distribution frames.

Space for up to 16 coin-tone receivers is provided on all frames except the first frame of the subsystem, where the CDA test circuit unit replaces one of the coin-tone receivers. The coin-tone receivers are connected to their associated CDA circuits by plug-ended cables to facilitate growth and rearrangement due to changes in traffic patterns.

2.4.3 CDA transmission frame

Associated with each service circuit frame is a single-bay frame (see Fig. 12) containing voice frequency transmission equipment.

Growth and rearrangements are accomplished with pluggable apparatus.

2.4.4 Announcement store frame

Associated with each controller frame is an announcement store frame (see Fig. 3) that provides storage for the digitally encoded announcement segments.

The bus unit at the top of the store frame contains terminal strips for interconnecting cables from connecting circuits in the office. Transformers are furnished as part of this unit to connect to the TSPS processor store bus. Store buses are connectorized to facilitate growth.

As mentioned earlier, two memory modules are required for Automated Coin Toll Service. Additional memory modules up to a total of six may be added to provide storage for additional vocabulary words if required by future features.

III. ACKNOWLEDGMENTS

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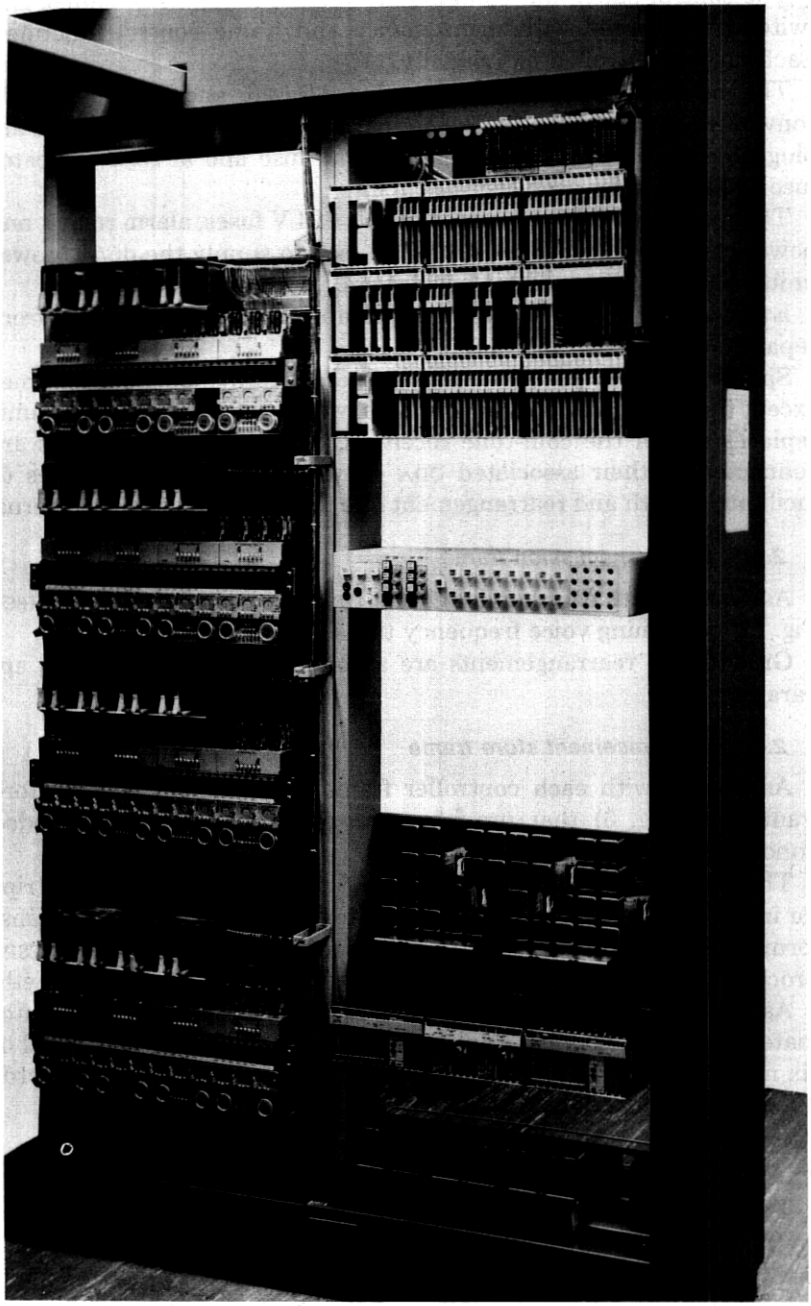

Fig. 12—Transmission frame.

M. Schmidt; for guidance and assistance in physical design, R. D. Garside, H. A. Hilsinger, and W. J. Proetta; for skillful electrical design and testing of SSAS circuits, J. O. Croswell, R. L. Grenzow, J. O. Hardy, D. C. Peterson, T. L. Roush, and B. G. Ruel.

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