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Equivalent Circuits for the Analysis and Synthesis of Switched Capacitor Networks

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An extensive library of z-domain building block equivalent circuits is derived to facilitate the analysis and synthesis of switched capacitor (SC) networks. These SC building blocks, typically comprised of a single capacitor and from one to four switches, serve as basic circuit elements for SC networks in much the same spirit that resistors and capacitors serve analog networks. This building block library facilitates the derivation of canonic z-domain equivalent circuits for complex SC networks and the application of well-established mathematical network analysis and synthesis tools. What has been sought are easily applied techniques for achieving the same insights for SC networks that we have long enjoyed with analog networks.

I. INTRODUCTION

Over the past several years, many researchers[1-15] have searched for the means to realize monolithic analog recursive filters, particularly for voice frequency applications. Initial attempts to realize a monolithic filters technology led to the development of active-R or resistor-only active filters.[1-6] By removing the large external capacitors (C ~ 5000 pF), such filters are, in principle, highly suited to integration with standard bipolar processing. The frequency dependence for these filters is derived[1-5] from the single-pole rolloff due to a compensation capacitor (C ~ 30 pF) to achieve a unity gain frequency of 1 MHz. This method of operation posed two significant barriers to the practical application of active-R filters; namely, large resistor ratios[1-5] are required to reach audio frequencies and the unity gain frequencies are not sufficiently stable[1-4] for precise filter realization. Although these barriers have to some degree been overcome,[5,6] it has become clear that the future of integrated circuits is in MOS large-scale integration and very large-scale integration processing. LSI has substantially reduced the cost of digital logic and memory, and VLSI will bring even further cost reductions.

With the overwhelming success of digital MOS LSI and the promises of VLSI as motivation, much productive effort[7-15] has been spent on the development of a compatible MOS LSI sample data technology. This work culminated in the development of compact operational amplifiers[12] with acceptable noise and power specifications, charge transfer device (CTD) transversal filters,[14, 15] and switched capacitor (SC) recursive filters[7-11] which fully utilize the advantages provided by MOS LSI. The transfer function coefficients[7-11] of an SC recursive filter are determined by a highly stable clock frequency and capacitor ratios which can be held to very tight tolerances (measured[13] errors of less than 0.2 percent have been achieved for binary valued capacitor ratios). Furthermore, MOS capacitors are nearly ideal, with very low dissipation factors and temperature coefficients[13] of less than 100 ppm/°C. This process of inherent precision and quality is sufficient to meet many filter and system specifications.

Considering the growing interest in MOS switched capacitor networks, the need is obvious for analytical and computer-aided tools[16-21] for the analysis and synthesis of SC networks. The pioneering work[16, 17] of Kurth and Moschytz provided a rigorous, network-theoretic foundation to the characterization of SC networks. They considered the analysis of SC networks comprised of capacitors and periodic, bi-phased switches. These networks, which are sampled data in nature, were shown to be characterized by nodal charge difference equations with periodically time-varying coefficients. This system of equations can be transformed into the z-domain[22, 23] to obtain the frequency response of the SC network. To reduce the analytical complexity, a building block approach was introduced[17] with the six basic building blocks: (*i*) shunt capacitor, (*ii*) series capacitor, (*iii*) shunt capacitor in parallel with a switch, (*iv*) series capacitor in parallel with a switch, (*v*) shunt switch, and (*vi*) series switch. These building blocks were expressed as four-port equivalent circuits with each two-port pair accounting for each of two signal paths which result from the two switch phases. The two signal paths, denoted even and odd, were shown to be linked by a common link two-port (LTP)[17] network. Any SC network, comprised of bi-phase switches, can be transformed into a z-domain equivalent circuit by interconnecting the appropriate combination of these building-block equivalent circuits. This equivalent circuit then provides the network designer with a pictorial representation of the circuit from which transfer relations can be derived between any pair of node voltages and provides the instant insight to circuit innovations we have long enjoyed with analog, linear, time-invariant networks.

The primary objective of this paper is to extend the Kurth-Moschytz[17] library of building blocks to include those higher-order SC elements which occur frequently in complex SC networks. These elements are typically comprised of one capacitor and from one to four

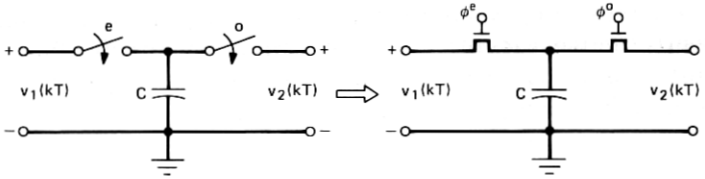
switches. With this expanded library of equivalent circuits, one can efficiently derive canonic z-domain equivalent circuits for any SC network. It is shown that, by manipulating the equivalent circuit for a toggle-switched four-port element one can derive all the equivalent circuits in the library. Alternative interpretations of the Kurth-Moschytz LTP are also provided which facilitate the derivation of canonic equivalent circuits. Finally, several examples are given which demonstrate the ease in which equivalent circuits are constructed and the insight derived therefrom.

II. APPLICATION OF Z-TRANSFORM TECHNIQUES TO THE ANALYSIS OF SC NETWORKS WITH BI-PHASE SWITCHES

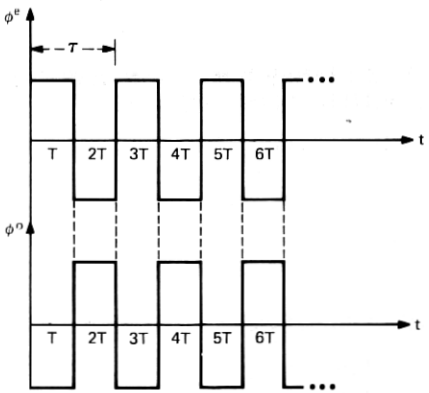
This section briefly reviews the basic assumptions[16, 17] regarding the sampled data nature of SC networks and the fundamentals germane to the derivations and procedures given in the succeeding sections. This review also provides an opportunity to define symbols and to acquaint the reader with the notation employed.

2.1 Operation of ideal SC networks

Consider now the operation of an ideal SC network, comprised of ideal capacitors, ideal switches, and ideal voltage-controlled voltage sources (i.e., ideal operational amplifiers) when excited by sampled data voltage inputs. Typically, the switches are controlled by a two-phase, nonoverlapping clock of frequency $f_c = 1/2T$, as shown in Fig. 1. Note that ϕ^e is used to denote the even clock phase that instantaneously closes the e-switch on the even $2kT$ times. Similarly, ϕ^o denotes the odd clock phase that instantaneously closes the o-switch on the odd $(2k + 1)T$ times. The switches are assumed to have a 50-percent duty cycle with equal (T-second) on- and-off time periods. It is further assumed that both the input and output of the SC network are sampled data signals which change in value only at switching instants kT. Thus, in their most general form, the voltage sources and internal circuit voltages are assumed to be sampled at times kT and held over a one-half clock period interval (T) as shown in Fig. 2a. With this assumption, we can apply[16-19] z-transform techniques to the general analysis and synthesis of SC networks. The z-transform, $z = e^{s\tau}$, where s is the complex analog frequency variable and τ is the clock period, then provides us with a convenient means for performing frequency domain analysis. Of course, the z-domain transfer functions obtained from this procedure relate the input and output samples of switched capacitor networks. Thus, to obtain the response, the input must also be characterized in the z-domain. Furthermore, if the output is considered as a held[24] (staircase) signal, this computed response must be modified[24] by $(\sin x)/x$. When continuous inputs are applied directly[20, 21] to SC networks, the analysis can become considerably more complex.



(a)



(b)

Fig. 1—(a) Simple switched capacitor network with (b) two-phase nonoverlapping clock.

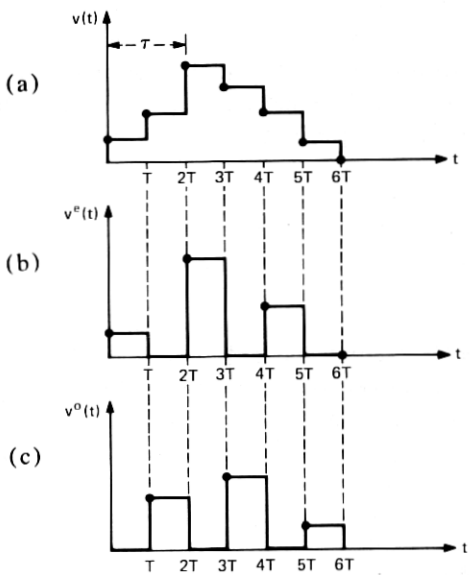


Fig. 2—(a) Sampled data voltage waveform portioned into its (b) even and (c) odd components.

As pointed out in Ref. 16, the switching action described in Fig. 1 provides a time-varying nature to the SC network. That is, as the switches open and close, the network graph changes, alternating between two topologies. One topology corresponds to the even clock phase and a second topology to the odd clock phase. Thus, one can view the time-varying SC network, with bi-phase switches, as two interrelated time invariant networks.[16–21] In lieu of this fundamental approach, it is mathematically convenient to partition[16] the sampled data voltage waveform in Fig. 2a into its even and odd components as shown, respectively, in Figs. 2b and 2c. Comparing v^e and v^o to the clock waveforms ϕ^e and ϕ^o, we observe that v^e is only nonzero when the e-switch is closed and v^o is only nonzero when the o-switch is closed. This fundamental observation[16, 17] has opened the door to a rigorous understanding of switched capacitor networks and has resulted in several methods for their analysis.

One way to interpret the relationship between the even and odd topologies is to consider them topologically decoupled, with the states of one determining the initial conditions for the other.[18, 19] This interpretation results in two distinct circuits coupled together via dependent sources which establish the initial conditions mentioned previously. This formulation has been found[18, 19] to be particularly convenient for computer-aided analysis. Another interpretation[16, 17] is to combine the even and odd networks topologically into a single z-domain equivalent circuit. In general, an n-port SC network[16, 17] will require a $2n$-port equivalent circuit, i.e., n-ports for the even clock phase and n-ports for the odd clock phase. It is this interpretation that provides the kinds of valuable insight that Laplace transform techniques have provided for analog linear-time invariant networks.

Since SC networks can be most rigorously characterized[16, 17] in terms of charge transfer operations, discrete time voltages $v_i(kT)$ and discrete time charge variations $\Delta q_i(kT)$ are used as port variables. At the switching times kT, charges are instantaneously redistributed with the principle of charge conservation maintained at every node in the network. It is this principle that allows us to write nodal charge equations in the same spirit with which we apply Kirchoff's current law to continuous networks. In general, due to the bi-phase switching operation, two distinct, but coupled, nodal charge equations are required to characterize the charge conservation condition at a particular node for all time instants kT. Namely, one equation for the even $2kT$ times and a second equation for the odd $(2k + 1)T$ times are required. These equations are written, for some node p, as

$$\Delta q_p^e(kT) = \sum_{i=1}^{M_{ep}} q_{pi}^e(kT) - \sum_{i=1}^{M_{ep}} q_{pi}^o((k-1)T)$$

for k an even integer, (1a)

and

$$\Delta q_p^o(kT) = \sum_{i=1}^{M_{op}} q_{pi}^o(kT) - \sum_{i=1}^{M_{op}} q_{pi}^e((k-1)T)$$

for k an odd integer, (1b)

or equivalently in the z-domain

$$\Delta Q_p^e(z) = \sum_{i=1}^{M_{ep}} Q_{pi}^e(z) - z^{-1/2} \sum_{i=1}^{M_{ep}} Q_{pi}^o(z) \tag{2a}$$

and

$$\Delta Q_p^o(z) = \sum_{i=1}^{M_{op}} Q_{pi}^o(z) - z^{-1/2} \sum_{i=1}^{M_{op}} Q_{pi}^e(z), \tag{2b}$$

where q_{pi}^e, q_{pi}^o and Q_{pi}^e, Q_{pi}^o denote, respectively, the instantaneous charges stored on the ith capacitor connected to node p for the even, odd kT time instants and their z-transforms. Also M_{ep} and M_{op} denote respectively the total number of capacitors connected to node p during the even and odd clock phases.

For single capacitor sc blocks, z-transformed nodal charge equations[16] lead directly to the desired equivalent circuits as described in Section III. To characterize a complex sc network one simply substitutes, one-for-one, the appropriate z-domain block equivalent circuit for each sc element in the network schematic. As demonstrated in Section IV, transformed nodal charge equations for each node in the network are then written by inspection from the equivalent circuit. The desired voltage transfer function(s) is then obtained by algebraically manipulating these z-domain equations in the usual manner.

2.2 Sample data waveforms

It should be noted that there are several sample data waveforms that can be modeled as special cases of the waveform depicted in Fig. 2. These waveforms and their respective even and odd components are shown in Fig. 3. One can immediately invoke the z-transform to mathematically describe these waveforms. The return-to-zero waveforms in Figs. 3a and 3b can be expressed mathematically as

$$V_a(z) = V_a^e(z) + V_a^o(z), \tag{3a}$$

where

$$V_a^o(z) = 0 \tag{3b}$$

and

$$V_b(z) = V_b^e(z) + V_b^o(z), \tag{4a}$$

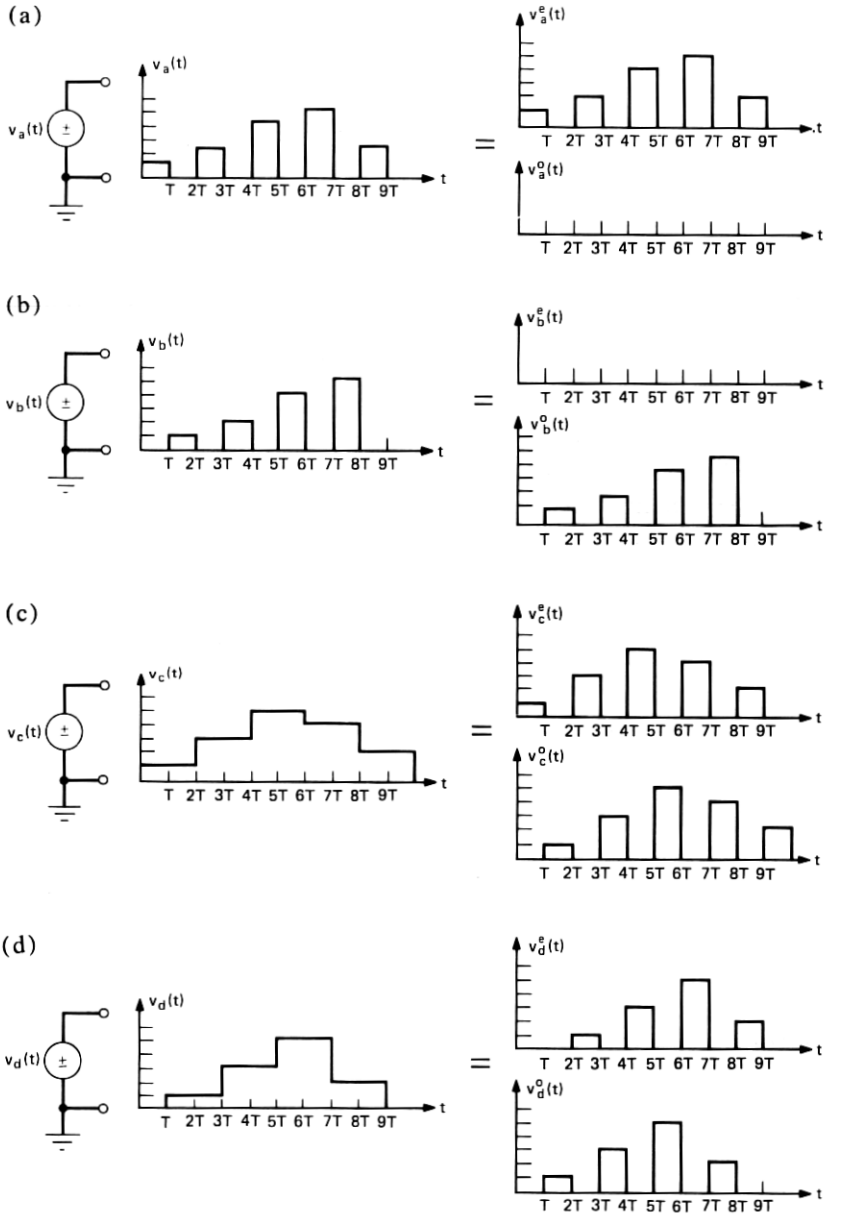


Fig. 3—Common special-case sampled data voltage waveforms and their respective even and odd components.

where

$$V_b^e(z) = 0. \tag{4b}$$

In a similar manner, we can characterize the full clock period sampled and held (S/H) waveforms in Figs. 3c and 3d as

$$V_c(z) = V_c^e(z) + V_c^o(z), \tag{5a}$$

where

$$V_c^o(z) = z^{-1/2} V_c^e(z) \tag{5b}$$

and

$$V_d(z) = V_d^e(z) + V_d^o(z), \tag{6a}$$

where

$$V_d^e(z) = z^{-1/2} V_d^o(z). \tag{6b}$$

If a capacitor of value C is placed across the terminals of the voltage source $v_c(t)$, we observe that the charge on the capacitor changes in value only once per clock cycle, i.e., at the even $2kT$ time instants when $v_c(t)$ changes. At the odd $(2k + 1)T$ time instants $v_c(t)$, the capacitor voltage is unchanged, thus, the charge remains constant. This phenomenon is described analytically, for the even and odd clock phases, in the following manner:

$$\Delta Q_c^e(z) = CV_c^e(z) - Cz^{-1/2} V_c^o(z) = C(1 - z^{-1}) V_c^e(z) \tag{7a}$$

and

$$\Delta Q_c^o(z) = CV_c^o(z) - Cz^{-1/2} V_c^e(z) = 0. \tag{7b}$$

It is noted that the condition $\Delta Q_c^o(z) = 0$ can also be obtained by disconnecting V_c from the capacitor with a switch which is open during the odd clock phase. Thus, in the sense that no charge is transferred, this open circuit condition also implies a full cycle sample and hold operation. Corresponding relations can also be written for the full cycle S/H waveform in Fig 3d.

It is useful to note that the return-to-zero waveforms $v_a(t)$ and $v_b(t)$ can be obtained by processing $v(t)$ in Fig. 2 with simple switch networks as shown in Fig. 4. When the switches in Fig. 4 are ideal, v_a and v_b are ideal, zero-impedance voltage sources with waveforms as depicted in Figs. 3a and 3b, respectively.

The various sample data waveforms considered in this section can be generated externally (i.e., an independent voltage source) and at any internal node by an appropriate combination of switches and capacitors. It is often crucial, particularly at the network output where one may either resample or couple to another SC network, to identify the waveform type of internal node voltages. From the properties

described in this section, this identification process is usually straightforward.

2.3 SC network transfer function relations

The voltage transfer function is well recognized as a convenient mathematical tool for the analysis and synthesis of continuous, linear, time-invariant networks. The value of the voltage transfer function is not expected to diminish with SC networks. At this point, it should be obvious that SC network transfer functions are most conveniently written in the z-domain.

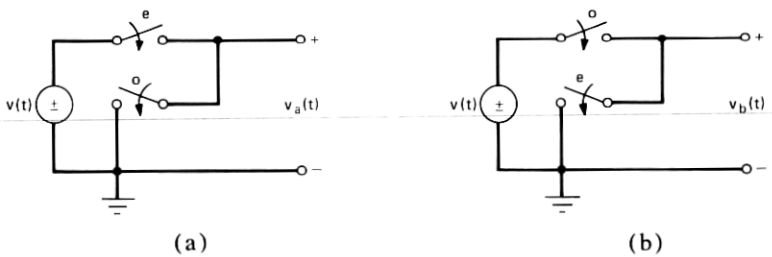
Let us, for simplicity, confine the discussion in this subsection to two-port SC networks with one input and one output. As noted previously, the two-port can be represented by an equivalent four-port, as shown in Fig. 5. In general, a 2×2 transfer matrix is required to fully characterize the input-output relations for this four-port network, i.e.,

$$\begin{bmatrix} V^e_{out}(z) \\ V^o_{out}(z) \end{bmatrix} = \begin{bmatrix} H_1(z) & H_2(z) \\ H_3(z) & H_4(z) \end{bmatrix} \begin{bmatrix} V^e_{in}(z) \\ V^o_{in}(z) \end{bmatrix} \tag{8}$$

where, by superposition,

$$V_{in}(z) = V^e_{in}(z) + V^o_{in}(z) \tag{9a}$$

$$V_{out}(z) = V^e_{out}(z) + V^o_{out}(z). \tag{9b}$$



(a) (b)

Fig. 4—Switch networks for return to zero voltage generation.

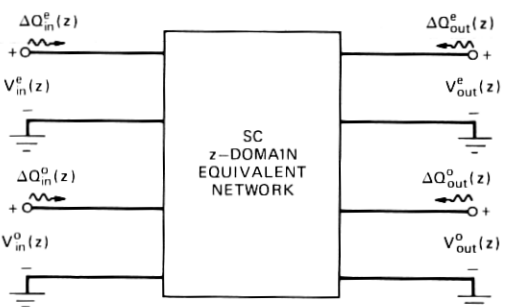


Fig. 5—Four-port z-domain equivalent circuit.

In many cases, the signal conditioning performed at the input and output imposes constraints on the form of the transfer relations. For example, consider the application of the return-to-zero source in Fig. 3a to the SC network in Fig. 5. Substituting $V_{in}^{o}(z) = 0$, obtained from eq. (3b), into eq. (8) yields the following transfer relations

$$V_{out}^{e}(z) = H_1(z)\, V_{in}^{e}(z) \tag{10}$$

and

$$V_{out}^{o}(z) = H_3(z)\, V_{in}^{e}(z). \tag{11}$$

Thus, depending on whether $v_{out}(kT)$ is sampled at the even $2kT$ times or the odd $(2k+1)T$ times, the voltage transfer function is either $H_1(z)$ or $H_3(z)$, respectively. However, if v_{out} is sampled at all kT times, then

$$V_{out}(z) = (H_1(z) + H_3(z))\, V_{in}^{e}(z). \tag{12}$$

In general, $H_1(z) \neq H_3(z)$; however, they are obviously interrelated. Therefore, one is not able to independently synthesize $H_1(z)$ and $H_3(z)$.

In practice, by appropriately conditioning the input and output signals, one can realize an SC network which is completely characterized by a single transfer function. Equations (10) and (11) describe examples of this class of SC network. One can in principle synthesize SC networks of this type directly in the z-domain using digital filter[22, 23] synthesis techniques. Several examples of multi-transfer function and single transfer function SC networks are provided in Section IV.

III. EQUIVALENT CIRCUIT MODELS FOR SC BUILDING BLOCKS

In this section, multi-port z-domain equivalent circuits will be derived for several SC building blocks. It has been shown[17] that any SC network can be constructed from the six blocks mentioned in Section I and voltage controlled voltage sources. The objective here is to facilitate the application of this approach by deriving a library of higher order building blocks which, when interconnected, lead to canonic z-domain equivalent circuits. SC elements comprised of one capacitor and from one to four switches are treated as basic circuit elements much like passive R's, L's, and C's in analog circuits. As noted in the previous section, the z-domain transfer relations can be derived from the equivalent circuit using familiar network analysis techniques.[25]

Figures 6 and 7 contain listings of the commonly occurring SC elements and their respective z-domain equivalent circuits or building blocks. In addition to the SC building blocks, z-domain models are also given for each of the sample data sources discussed in the previous section. This library is sufficiently general to accommodate all the

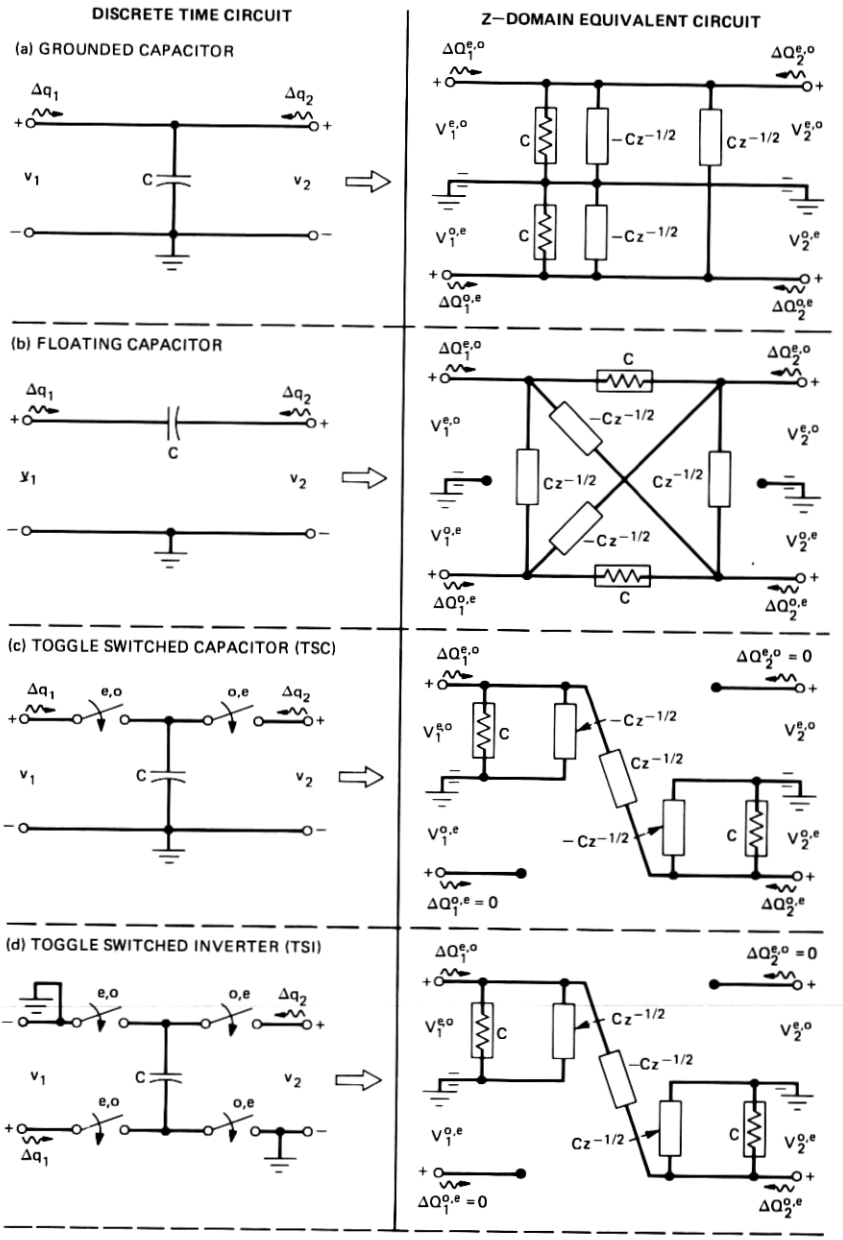


Fig. 6—General library of 2n port z-domain equivalent circuits for switched capacitor building blocks (*continued on pp 740–743*).

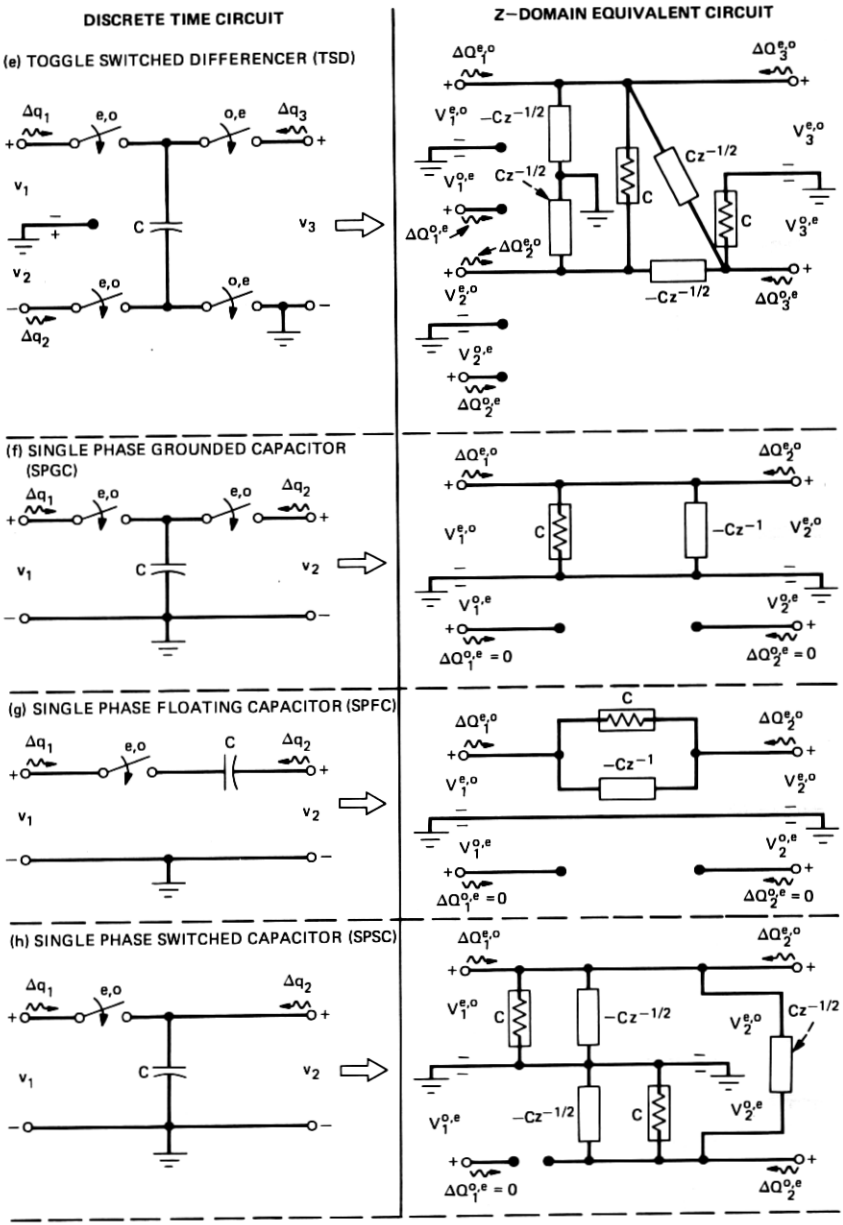


Fig. 6—(*continued*).

published[7-11, 17, 26, 27] SC networks which use nonoverlapping bi-phase switches. The equivalent circuits in Fig. 6 are derived in their most general $2n$-port form, assuming that all voltages update at one-half clock cycle intervals, as per $v(t)$ in Fig. 2. The e, o notation refers to the switch phasings as noted in the previous section. Similarly, super-

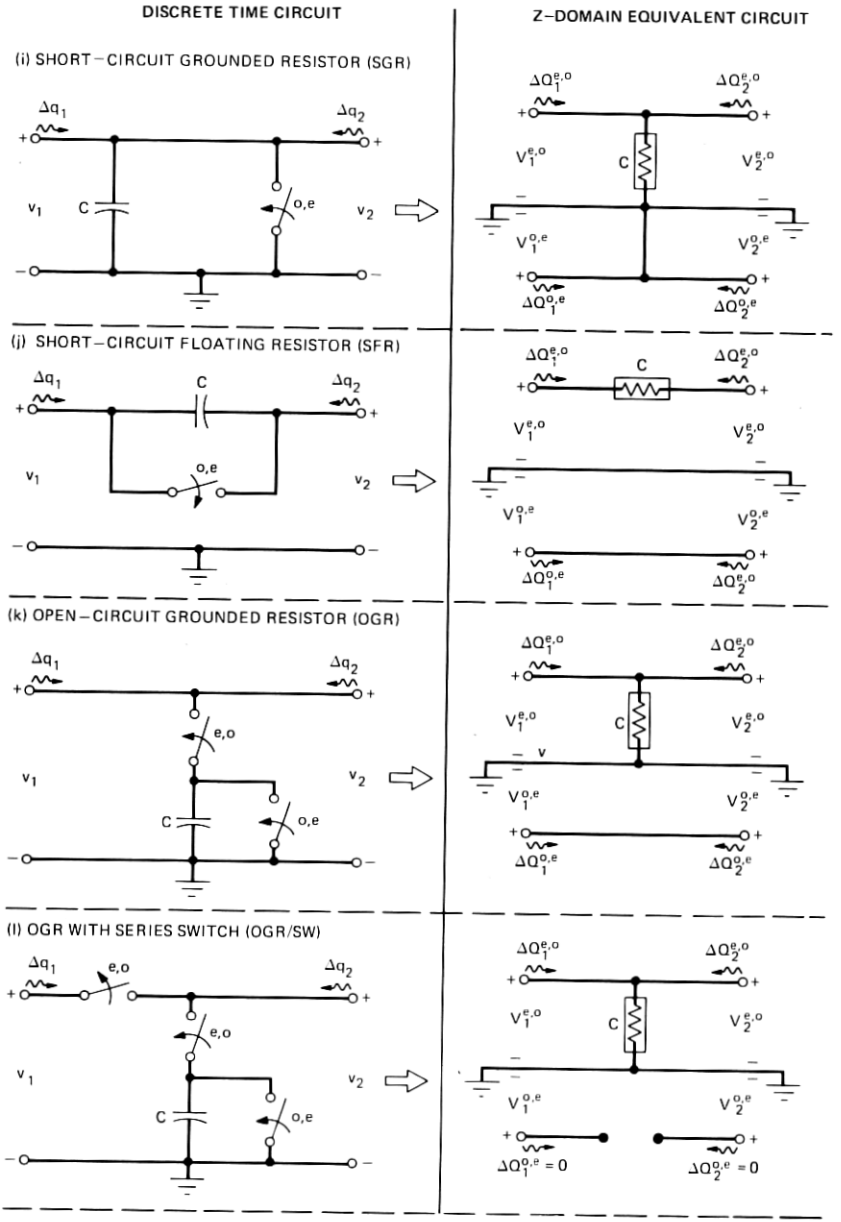


Fig. 6—(*continued*).

scripts e, o and o, e are used to denote the even or odd port variable (V_i, ΔQ_i) components and the complement odd or even port-variable components, respectively. This e, o notation conveniently provides the connectivity information for interconnecting the building blocks.

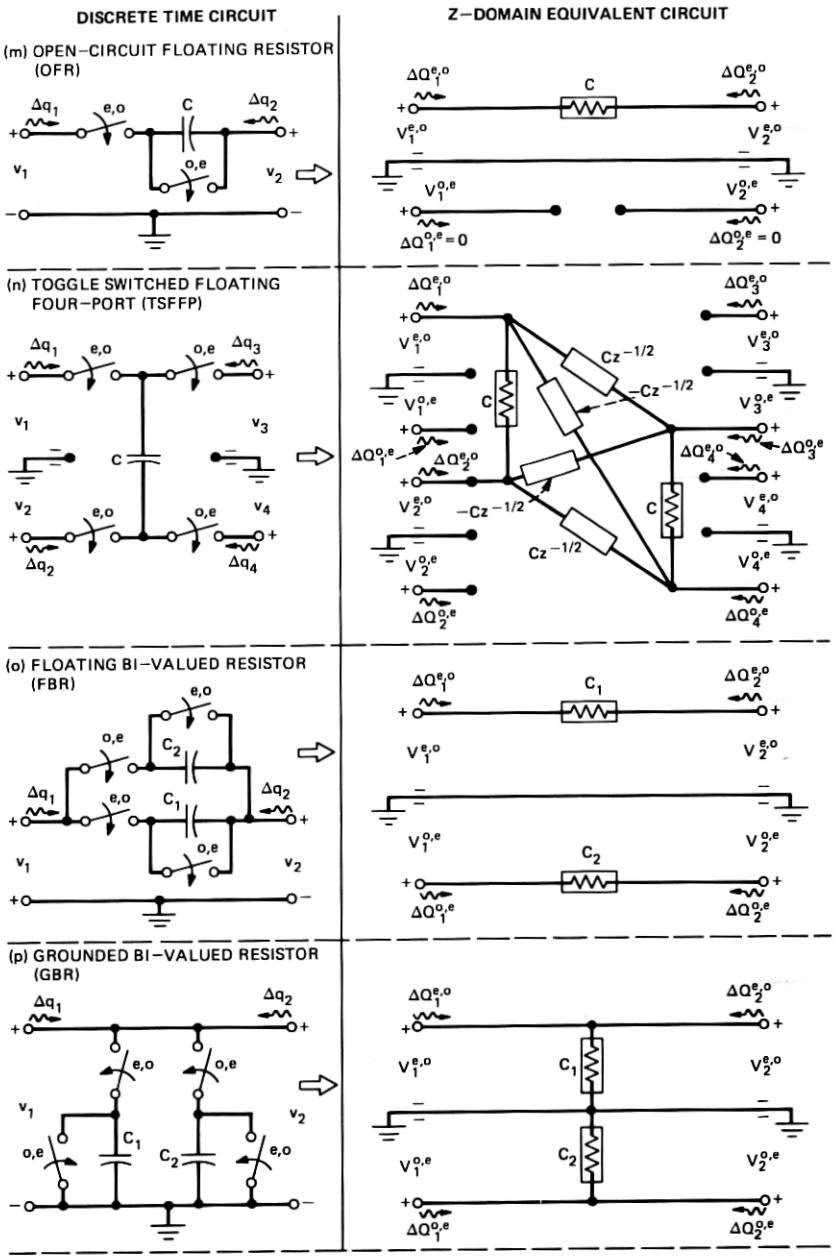


Fig. 6—(*continued*).

In practice, there are many sc networks in which the charges and voltages update, due to the internal switching action of the sc network, only on full clock cycle intervals. This behavior, which is readily identified on a block-by-block basis, results in $2n$-port equivalent circuits with n open ports. Many of the sc blocks in Fig. 6 fall within

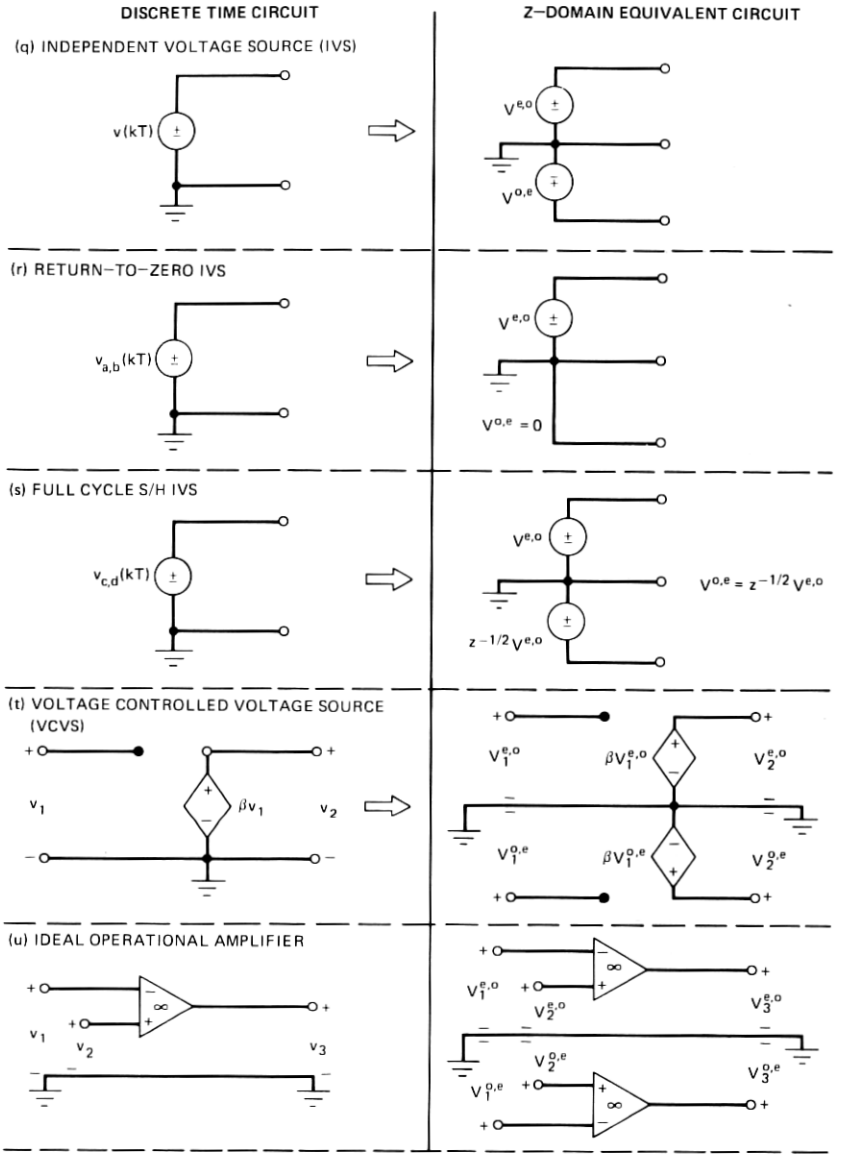


Fig. 6—(*continued*).

this category. When properly interconnected,[17] these $2n$-port equivalent circuits can be reduced to the n-port equivalent circuits in Fig. 7.

3.1 2n-port SC building block equivalent circuits

In this section, derivations are given for several of the SC equivalent circuits in Fig. 6. These derivations will be based on z-transformed nodal charge equations which can be derived by inspection from the

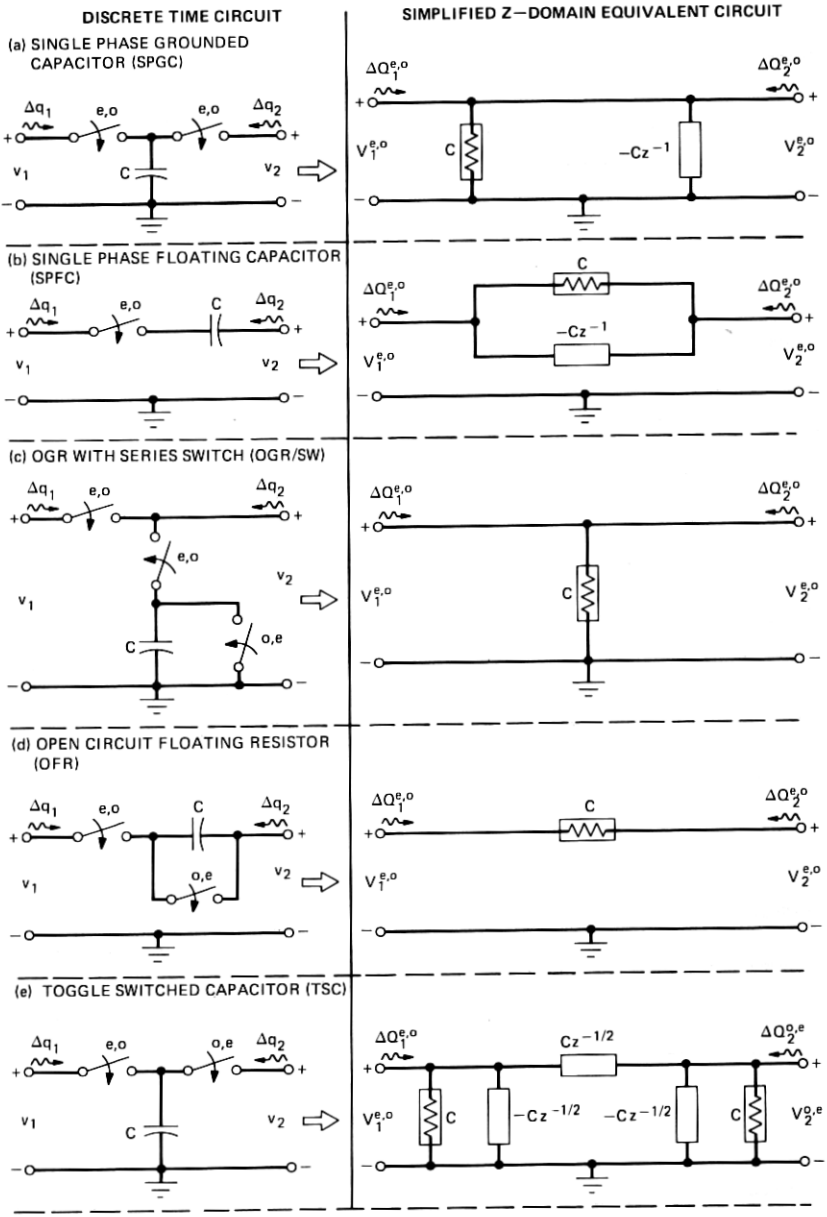


Fig. 7—Simplified library of n port z-domain equivalent circuits (*continued on pp. 745–746*).

sc circuit. As noted in the previous section, one can write a distinct nodal charge equation for each switch phase. Therefore an n-port sc block is characterized by $2n$ nodal charge relations. The desired $2n$-port z-domain equivalent circuit evolves directly from these relations.

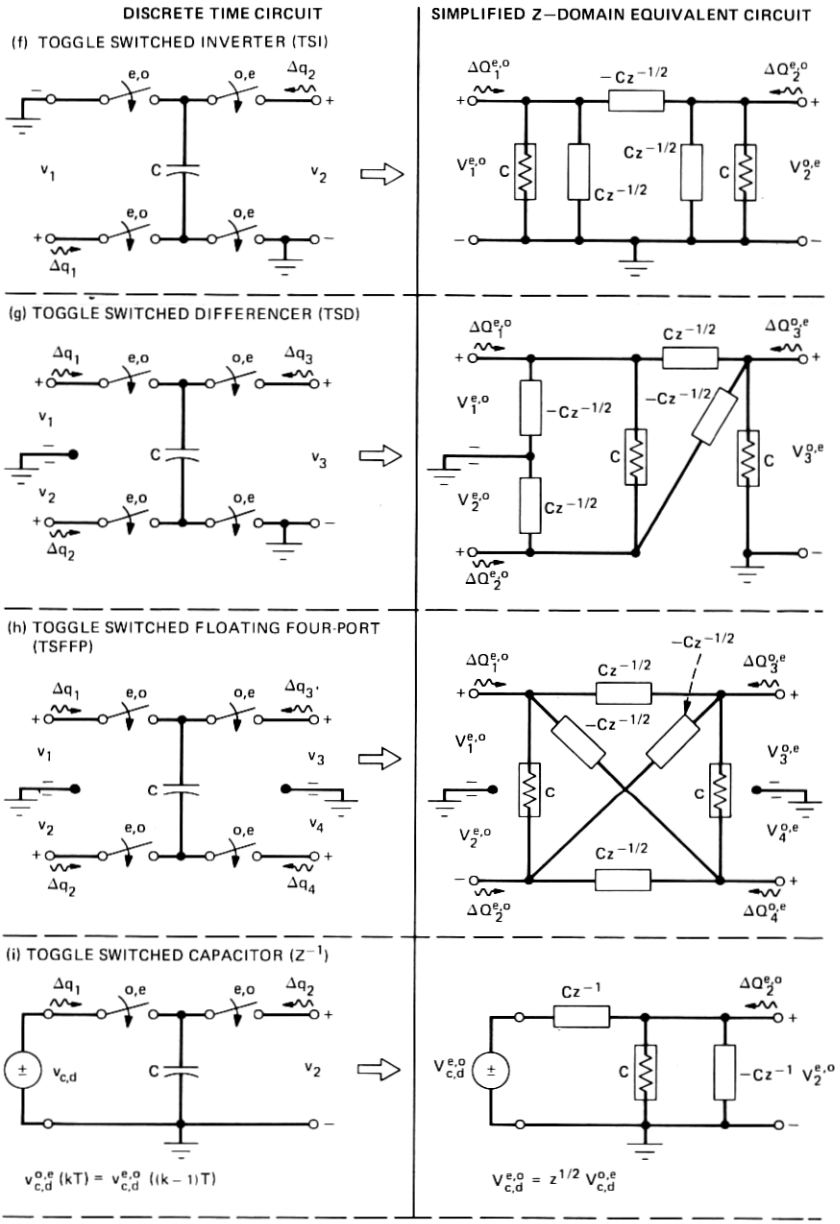


Fig. 7—(*continued*).

The equivalent circuit for a complex SC network is derived by properly interconnecting the appropriate block equivalent circuits. To avoid boring the reader with excessive repetition, derivations will only be provided for blocks b through f and l of Fig. 6. Once these derivations

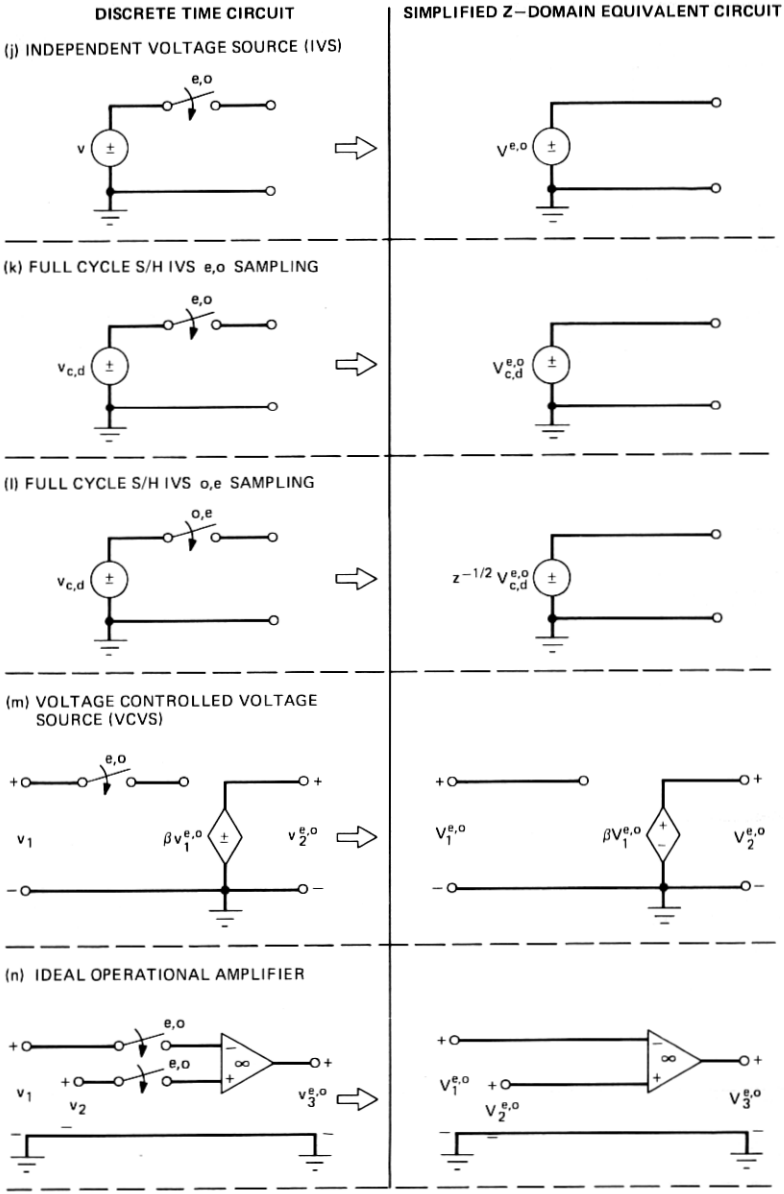


Fig. 7—(*continued*).

are understood, the validity of the remaining equivalent circuits can be established by inspection. The independent and dependent voltage source equivalent circuits are obtained directly from the relations in the previous section.

3.1.1 Floating capacitor equivalent circuit

One can derive the desired equivalent circuit in a straightforward manner directly from the nodal charge equations. In these equations, the even and odd voltage components (V^e and V^o) serve as independent variables and the even and odd charge variation components (ΔQ^e and ΔQ^o) serve as the dependent variables. Since the floating capacitor block in Fig. 6b contains no switches, the z-transformed nodal charge equations, where V^e, V^o, V_2^e and V_2^o are independent voltage excitations, are instantly written as

$$\Delta Q_1^{e,o}(z) =$$

$$CV_1^{e,o}(z) - Cz^{-1/2}V_1^{o,e}(z) - CV_2^{e,o}(z) + Cz^{-1/2}V_2^{o,e}(z), \quad (13a)$$

$$\Delta Q_2^{e,o}(z) =$$

$$CV_2^{e,o}(z) - Cz^{-1/2}V_2^{o,e}(z) - CV_1^{e,o}(z) + Cz^{-1/2}V_1^{o,e}(z), \quad (13b)$$

$$\Delta Q_1^{o,e}(z) =$$

$$CV_1^{o,e}(z) - Cz^{-1/2}V_1^{e,o}(z) - CV_2^{o,e}(z) + Cz^{-1/2}V_2^{e,o}(z), \quad (13c)$$

and

$$\Delta Q_2^{o,e}(z) =$$

$$CV_2^{o,e}(z) - Cz^{-1/2}V_2^{e,o}(z) - CV_1^{o,e}(z) + Cz^{-1/2}V_1^{e,o}(z). \quad (13d)$$

There are perhaps several circuit interpretations for this set of equations. One convenient interpretation is the balanced lattice equivalent circuit shown in Fig. 6b. Another circuit interpretation[17] for these equations is a four-port network comprised of an unbalanced floating LTP coupled to the even and odd transmission paths via ideal transformers. By interpreting eqs. (13) as a balanced lattice, one can eliminate the transformers. This balanced lattice is referred to in this paper as a balanced floating LTP; in contrast, the Kurth-Moschytz circuit is referred to as an unbalanced floating LTP. Both circuits are equivalent and valid under all port termination conditions.

3.1.2 Toggle switched capacitor[7] (TSC) equivalent circuit

Due to the switching action of the toggle switch, the capacitor C receives charge from v_1, only on the even (odd) times and charge from v_2 on the odd (even) times. When the switches are open, the corresponding ports are open and $\Delta Q = 0$. These observations are consistent with the z-transformed nodal charge equations:

$$\Delta Q_1^{e,o}(z) = CV_1^{e,o}(z) - Cz^{-1/2}V_2^{o,e}(z) \quad (14a)$$

$$\Delta Q_2^{e,o}(z) = 0 \quad (14b)$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{14c}$$

$$\Delta Q_2^{o,e}(z) = CV_2^{o,e}(z) - Cz^{-1/2}V_1^{e,o}(z). \tag{14d}$$

These equations lead directly to the four-port equivalent circuit in Fig. 6c. As described in Ref. 17, an unbalanced LTP is seen to bridge the 1-*e,o* and 2-*o,e* ports. Note that ports 1-*o,e* and 2-*e,o* are always open; therefore, no transmission occurs at these ports. This is a property common to all bi-phase toggle switched SC blocks (e.g., equivalent circuits 6d and 6e in Fig. 6).

3.1.3 Toggle switched inverter[11] (TSI) equivalent circuit

The operation of this circuit is similar to the TSC element; with the exception that in the TSI the voltage is inverted as the charge on C is transferred from port 1 to port 2. This process is described by the following z-transformed nodal charge equations:

$$\Delta Q_1^{e,o}(z) = CV_1^{e,o}(z) + Cz^{-1/2}V_2^{o,e}(z) \tag{15a}$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{15b}$$

$$\Delta Q_2^{e,o}(z) = 0 \tag{15c}$$

$$\Delta Q_2^{o,e}(z) = CV_2^{o,e}(z) + Cz^{-1/2}V_1^{e,o}(z). \tag{15d}$$

These equations are readily interpreted by the four-port equivalent circuit in Fig. 6d. Note for this block the 1-*e,o* and 2-*o,e* ports are bridged by an unbalanced LTP-like network in which the storage elements ($Cz^{-1/2}$) are all premultiplied by (-1). Since this network serves both as a link between even and odd transmission paths and as a signal inverter, it is referred to as an unbalanced inverting LTP.

3.1.4 Toggle switched differencer[11] (TSD) equivalent circuit

In this element, the charge on C is determined by the voltage difference $v_1^{e,o}(kT) - v_2^{e,o}(kT)$ during the *e,o* switch phase. When the *o,e* switches close this voltage, difference appears directly across port 3. This operation is described by the following z-transformed nodal charge equations:

$$\Delta Q_1^{e,o}(z) = CV_1^{e,o}(z) - CV_2^{e,o}(z) - Cz^{-1/2}V_3^{o,e}(z) \tag{16a}$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{16b}$$

$$\Delta Q_2^{e,o}(z) = CV_2^{e,o}(z) - CV_1^{e,o}(z) + Cz^{-1/2}V_3^{o,e}(z) \tag{16c}$$

$$\Delta Q_2^{o,e}(z) = 0 \tag{16d}$$

$$\Delta Q_3^{e,o}(z) = 0 \tag{16e}$$

and

$$\Delta Q_3^{o,e}(z) = CV_3^{o,e}(z) - Cz^{-1/2}V_1^{e,o}(z) + Cz^{-1/2}V_2^{e,o}(z). \tag{16f}$$

The six-port equivalent circuit representation for these equations is given in Fig. 6e. Note that three of the six ports are open. The TSD element exhibits yet another form of LTP. In this element two *e,o* transmission paths are linked to a single *o,e* path through a differencing operation. It is perhaps appropriate to refer to this LTP as an unbalanced differencing LTP.

3.1.5 Single phase grounded capacitor (SPGC)

This SC element occurs frequently in SC networks, particularly in low-pass SC filters. In a sense, it serves as a companion element for the grounded capacitor in Fig. 6a. It is also a special case of the grounded capacitor. The nodal charge relations for this block are readily written as

$$\Delta Q_1^{e,o}(z) = C(1 - z^{-1})V^{e,o}(z) \tag{17a}$$

$$\Delta Q_2^{e,o}(z) = C(1 - z^{-1})V^{e,o}(z) \tag{17b}$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{17c}$$

$$\Delta Q_2^{o,e}(z) = 0, \tag{17d}$$

where $V^{e,o}(z) = V_1^{e,o}(z) = V_2^{e,o}(z)$. It is noted that one can derive eqs. (17) from the grounded capacitor equivalent circuit in Fig. 6a by setting $\Delta Q_1^{o,e} = \Delta Q_2^{o,e} = 0$, which implies $V^{o,e}(z) = z^{-1/2}V^{e,o}(z)$. For the SPGC block, $V^{o,e}(z)$ represents the voltage stored and held on capacitor C and no longer refers to port voltages $V_1^{o,e}$ and $V_2^{o,e}$. As noted in Section II, this condition is equivalent to a full clock period S/H.

Equations (17a) through (17d) lead directly to the four port equivalent circuit in Fig. 6f. Due to the switches, two of the ports are open as described by eqs. (17c) and (17d). This network is equivalent to the open circuit LTP described in Ref. 17. The equivalent circuit for the floating capacitor is seen to similarly reduce to that in Fig. 6g when a series switch is added. Since these blocks occur frequently in complex SC networks, their recognition results in substantially simplified equivalent circuits.

3.1.6 Open circuit grounded resistor with series switch (OGR/SW) equivalent circuit

This block performs a function similar to the SGR in Fig. 6i, except that capacitor C is discharged while it is totally disconnected from the circuit. Therefore the shorted capacitor does not load the circuit during the discharging switch phase. The equivalent circuit, in Fig. 6l, for this block is obtained from the following z-transformed nodal charge equations

$$\Delta Q_1^{e,o}(z) = CV^{e,o}(z) \tag{18a}$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{18b}$$

$$\Delta Q_2^{e,o}(z) = CV^{e,o}(z) \tag{18c}$$

and

$$\Delta Q_2^{o,e}(z) = 0, \tag{18d}$$

where

$$V^{e,o}(z) = V_1^{e,o}(z) = V_2^{e,o}(z).$$

This block is memoryless, and it is an open circuit during the *o,e* clock phase when capacitor C discharges. Thus during the *e,o* clock phase, the block serves as a resistor and during the *o,e* clock phase it does nothing. In many SC network arrangements, where it is only necessary to transmit during one clock phase, this block serves as an excellent resistor equivalent.

Equivalent circuits 6o and 6p represent straightforward, nevertheless useful, generalizations of circuits 6l and 6m. These SC networks are seen to provide, for the even and odd clock phases, different value resistor-like components. This type of component suggests the possibility of time-sharing capacitors and operational amplifiers to achieve different even and odd circuit behaviors.

This concludes the derivations for equivalent circuits in Fig. 6. At this point, the interested reader should be able to derive the remaining SC equivalent circuits easily.

3.2 Simplified SC building block equivalent circuits

In the previous section, it was observed that many of the four-port equivalent circuits result in n (of $2n$) open circuit ports. Obviously, any signals applied to one or more of these open ports will neither be processed nor transmitted. Therefore, SC networks comprised of these blocks will only provide transmission and filtering, when the switches are phased such that the blocks interconnect to provide one nonopen signal path[17] from input to output. Assuming this connection rule, the open ports are nonfunctional and can be removed from the equivalent circuits. The immediate identification of these blocks in a complex SC network results in much labor-saving equivalent circuit simplification. More specifically, $2n$-port equivalent circuits reduce directly to n-port equivalent circuits. To emphasize this point, the appropriate four-port equivalent circuits in Fig. 6 have been reconfigured as two-port equivalent circuits in Fig. 7. Many complex SC networks[9,11] can be modeled exclusively with these simplified equivalent circuits. For this class of SC networks, circuit analysis is no more complex than that for continuous (linear) time-invariant networks. Since the blocks listed in Fig. 7 perform all the necessary network functions, it is expected that one can synthesize general z-domain transfer functions using only these blocks. This restriction, with little sacrifice in generality, should lead to efficient z-domain synthesis procedures for SC networks.

In addition to the reconfigured equivalent circuits from Fig. 6, Fig.

7 contains two additional building blocks. These blocks are shown in Fig. 7h and 7i. Let us briefly discuss each of these blocks on an individual basis.

3.2.1 Toggle switched floating four-port (TSFFP) equivalent circuit

This element is the most general of the toggle switched (single) capacitor elements. Thus the equivalent circuits for the TSC, TSI, and the TSD can be derived directly from the equivalent circuit in Figure 7h, by simply shorting to ground the appropriate port or ports. The z-transformed nodal charge equations for the block are expressed as

$$\Delta Q_1^{e,o}(z) = CV_1^{e,o}(z) - CV_2^{e,o}(z) - Cz^{-1/2}V_3^{o,e}(z) + Cz^{-1/2}V_4^{o,e}(z) \tag{19a}$$

$$\Delta Q_1^{o,e}(z) = 0 \tag{19b}$$

$$\Delta Q_2^{e,o}(z) = CV_2^{e,o}(z) - CV_1^{e,o}(z) - Cz^{-1/2}V_4^{o,e}(z) + Cz^{-1/2}V_3^{o,e}(z) \tag{19c}$$

$$\Delta Q_2^{o,e}(z) = 0 \tag{19d}$$

$$\Delta Q_3^{e,o}(z) = 0 \tag{19e}$$

$$\Delta Q_3^{o,e}(z) = CV_3^{o,e}(z) - CV_4^{o,e}(z) - Cz^{-1/2}V_1^{e,o}(z) + Cz^{-1/2}V_2^{e,o}(z) \tag{19f}$$

$$\Delta Q_4^{e,o}(z) = 0 \tag{19g}$$

and

$$\Delta Q_4^{o,e}(z) = CV_4^{o,e}(z) - CV_3^{o,e}(z) - Cz^{-1/2}V_2^{e,o}(z) + Cz^{-1/2}V_1^{e,o}(z). \tag{19h}$$

To be completely general, eqs. (19) describe an eight-port equivalent circuit with four open ports. Such an eight-port description is shown in Fig. 6n. The more useful four-port equivalent circuit in Fig. 7h is obtained by deleting the open ports.

Comparing Figs. 6b and 7h, one observes that the four non-open ports of the TSFFP are coupled together via a 90-degree rotated, balanced floating LTP. In fact, if the TSFFP is rotated 90 degrees with ports 1 and 3 serving as the incoming ports and ports 2 and 4 as the outgoing ports, we indeed have the equivalent circuit for the floating capacitor in Fig. 6b. If ports 2 and 4 are then shorted to ground, one can then easily derive the equivalent circuit for the grounded capacitor in Fig. 6a. All the toggle-switched (the TSC, TSI, and TSD) elements can be readily derived from the TSFFP. For example, if ports 2 and 4 are shorted to ground, the TSFFP equivalent circuit reduces to that of the TSC in Fig. 7e. Also, the TSI in Fig. 7f is obtained when ports 1 and 4 are shorted to ground. In summary, by providing the proper termina-

tion conditions, one can derive the equivalent circuits for any of the single capacitor SC elements in Figs. 6 and 7 with the TSFFP.

3.2.2 Toggle switched blocks driven by full clock cycle S/H voltage sources

Equivalent full-cycle time delays can be experienced when toggle-switched SC blocks are driven with full cycle S/H voltage sources. A situation of this type is illustrated in Fig. 7i. The behavior of this circuit can be described in the following manner. When source $v_{c,d}(t)$ changes to value $v_{c,d}^{e,o}$, the o,e switch is open; thus, the charge on capacitor C remains unchanged. One-half clock period later when switch o,e closes, capacitor C acquires the charge $Cv_{c,d}^{e,o}$. Another one-half clock period later, the o,e switch opens, the e,o switch closes, and $v_{c,d}^{e,o}$ appears at the output with a net time delay of one full clock period. Obviously, when the source changes value in synchronism with the initial o,e switch, the net time delay is one-half of a clock period. The SC circuit in Fig. 7i can be modeled according to the equivalent circuit in Fig. 8. Writing a nodal charge equation at node 2 yields

$$CV_2^{e,o}(z) = Cz^{-1/2}(z^{-1/2}V_{c,d}^{e,o}(z)) = Cz^{-1}V_{c,d}^{e,o}(z). \tag{20}$$

The equivalent circuit in Figure 7i conveniently characterizes this relationship. Similar equivalent circuits can be derived for the TSI and TSD blocks as shown in Figs. 9a and 9b respectively. Full cycle time delays can readily[11] occur when appropriately phased toggle switched blocks are driven by operational amplifier integrator circuits.

IV. APPLICATIONS TO THE ANALYSIS AND SYNTHESIS OF SC NETWORKS

In this section, the concepts developed in the previous sections are applied to the analysis of several passive and active SC networks. Many examples are simple, to emphasize the insight provided by the equivalent circuits.

4.1 Passive SC networks

In this section we examine two single pole passive SC networks. The equivalent circuits in Figs. 6 and 7 allow one to examine a given SC network under an assortment of input-output conditions, as in Fig. 3. As we will see, such an examination can reveal some rather interesting circuit behavior that is not immediately obvious.

4.1.1 First-order, low-pass SC networks

As the initial example, consider the simple first-order, low-pass network depicted in Fig. 10a. An equivalent circuit for this network can be obtained by simply cascading blocks 6c and 6f, as shown in Fig. 10b. This circuit can obviously be reduced to that in Fig. 10c. One could have immediately written the equivalent circuit in Fig. 10c by

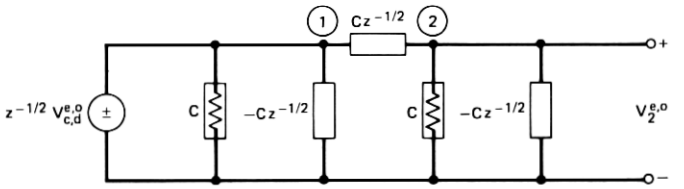


Fig. 8—Toggle switched capacitor driven by a full clock period S/H voltage source.

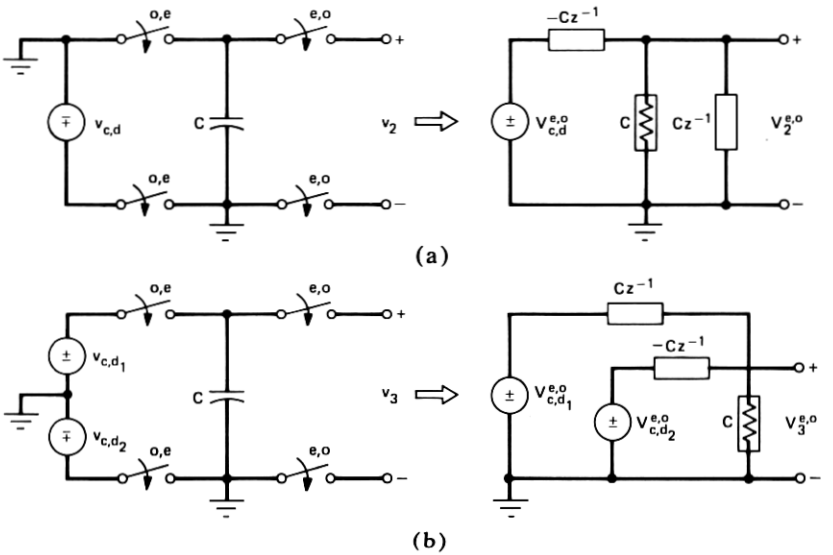


Fig. 9—(a) Toggle switched inverter and (b) toggle switched differencer, driven by full clock period S/H voltage sources.

cascading the simplified block equivalent circuits 7a and 7e. Writing a single nodal charge equation at node 2, namely,

$$(C_1 - C_1 z^{-1/2} + C_1 z^{-1/2} + C_2 - C_2 z^{-1}) V^o_{out}(z) = C_1 z^{-1/2} V^e_{in}(z) \quad (21)$$

yields the familiar low-pass z-domain transfer function

$$H_3(z) = \frac{V^o_{out}(z)}{V^e_{in}(z)} = \frac{C_1 z^{-1/2}}{C_1 + C_2 - C_2 z^{-1}}. \quad (22)$$

Note that V^o_{in} and V^e_{out} are removed by sampling operations at the input and output respectively. Thus, the transmission through this network is completely described by a single transfer function, namely H_3.

4.1.2 First-order, high-pass SC network

The simple first-order, high-pass circuit shown in Fig. 11 is a rather interesting circuit, as we shall soon see. Its interesting behavior stems from the input-to-output switch free path which permits both V^e_{in} and

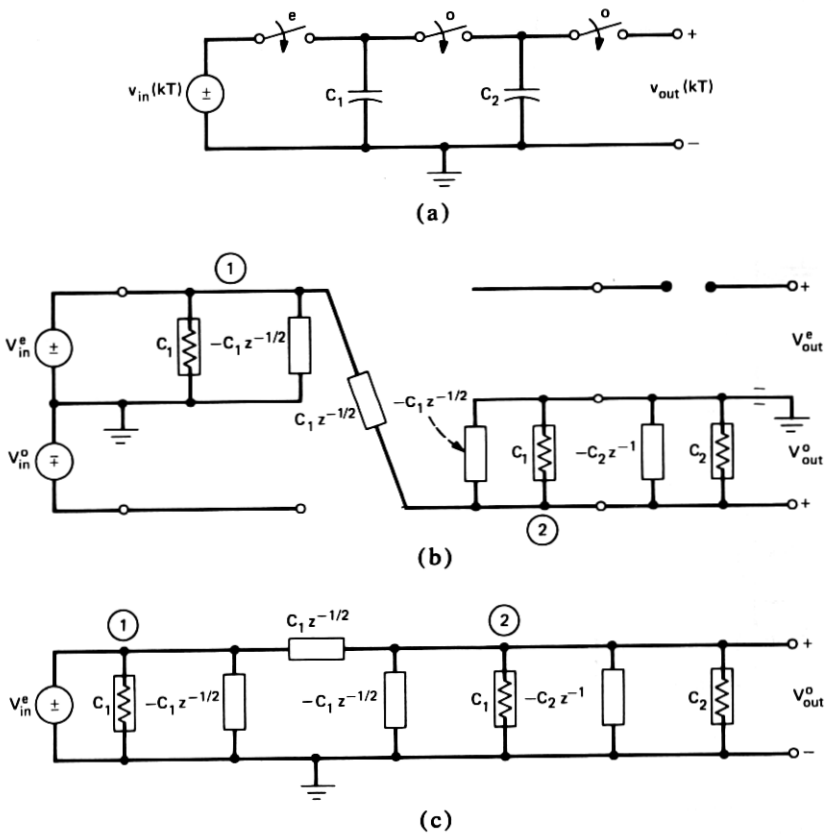


Fig. 10—Single pole "passive" sc low-pass network.

V^o_{in} to determine the e and o components of V_{out}. To study this circuit, we write the equivalent circuit in Fig. 11b by cascading blocks 6b and 6k.

Analysis of the equivalent circuit yields the following relations:

$$V^e_{out}(z) = \frac{C_1(1 - z^{-1})}{C_1 + C_2 - C_1 z^{-1}} V^e_{in}(z) + OV^o_{in}(z) \tag{23a}$$

$$= H_1(z) V^e_{in}(z) \tag{23b}$$

and

$$V^o_{out}(z) = \frac{-C_2 z^{-1/2}}{C_1 + C_2 - C_1 z^{-1}} V^e_{in}(z) + V^o_{in}(z) \tag{24a}$$

$$= H_3(z) V^e_{in}(z) + H_4(z) V^o_{in}(z). \tag{24b}$$

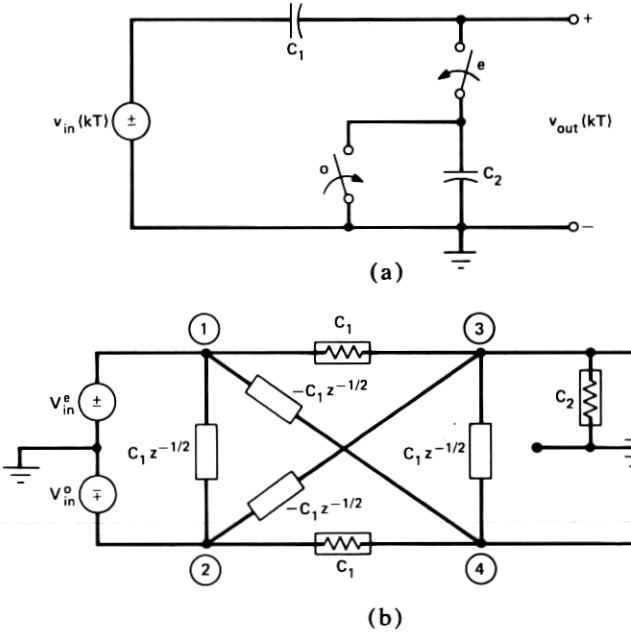


Fig. 11—Single pole "passive" SC high-pass network.

Note:

$$H_1(z) \triangleq \left.\frac{V^e_{out}(z)}{V^e_{in}(z)}\right|_{V^o_{in}=0} = \frac{C_1(1-z^{-1})}{C_1 + C_2 - C_1 z^{-1}} \tag{25a}$$

is a first-order, high-pass function, while

$$H_3(z) \triangleq \left.\frac{V^o_{out}(z)}{V^e_{in}(z)}\right|_{V^o_{in}=0} = \frac{-C_2 z^{-1/2}}{C_1 + C_2 - C_1 z^{-1}} \tag{25b}$$

is a first-order, low-pass function. This is a most interesting result, indeed. From eqs. (24), we observe that by forcing $V^o_{in} = 0$, as in Fig. 12a, this circuit behaves like a first-order, high-pass filter when the output is sampled on the even times and behaves like a first-order, low-pass filter when the output is sampled on the odd times. A circuit that achieves this bifunctional characteristic is shown in Fig. 12b. To achieve this behavior, a simple return-to-zero source of the form shown previously in Fig. 3a, or equivalently in Fig. 4a, is used to drive the high-pass circuit depicted in Fig. 11.

4.2 Active SC networks

Due to obvious reasons, much of our interest is in active[8-11,26,27] SC networks. These networks are typically[8-11,26,27] comprised of capacitors,

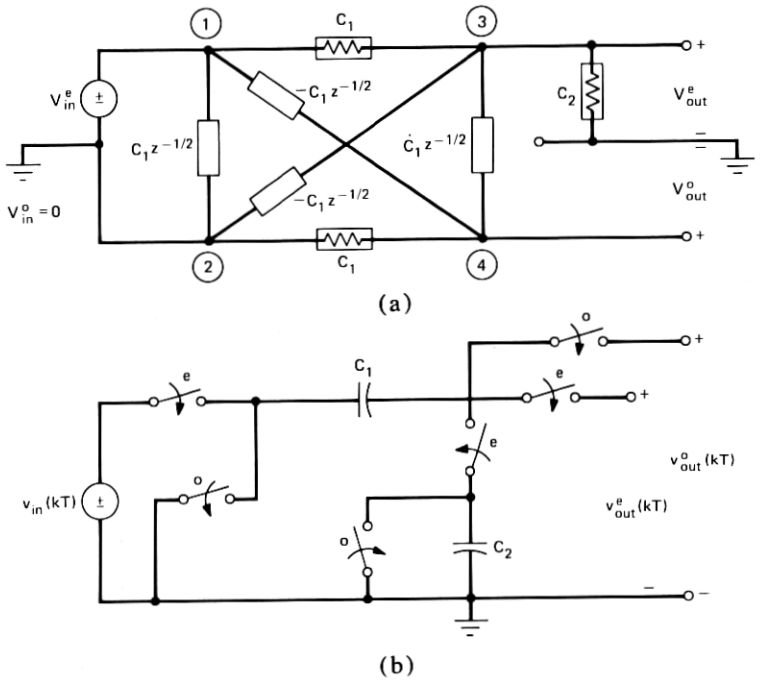


Fig. 12—Single pole "passive" SC high-pass/low-pass network.

switches and operational amplifiers. Many of the active SC networks appearing[8-11] in the literature are comprised of simple SC building blocks, of the form listed in Fig. 7, buffered by operational amplifiers. When these operational amplifiers can be assumed to be ideal, the virtual grounds result in further simplifications in the equivalent circuits. In the voltage-charge domain, a "virtual" ground at the input of an ideal operational amplifier shall be defined by the condition $\Delta Q = 0$, $V = 0$. Let us now consider the equivalent circuit representations for the following selection of first-order active SC networks.

4.2.1 Lossless integrator

The equivalent circuit for the lossless integrator in Fig. 13a is derived, in full generality, using blocks 6b, 6c, and 6u as shown in Fig. 13b. Of course, one may accommodate the finite gain of an actual operational amplifier using the voltage-controlled voltage source, cited in Fig. 6 as block 6t. The rather unwieldy circuit depicted in Fig. 13b can be immediately simplified by removing all elements shunting virtual ground points and voltage sources. This network is then redrawn in the form shown in Fig. 13c, which can be again reconfigured to yield the circuit in Fig. 13d. Finally, the second stage of Fig. 13d is noted to be a voltage-controlled voltage source with $\beta = z^{-1/2}$ as in

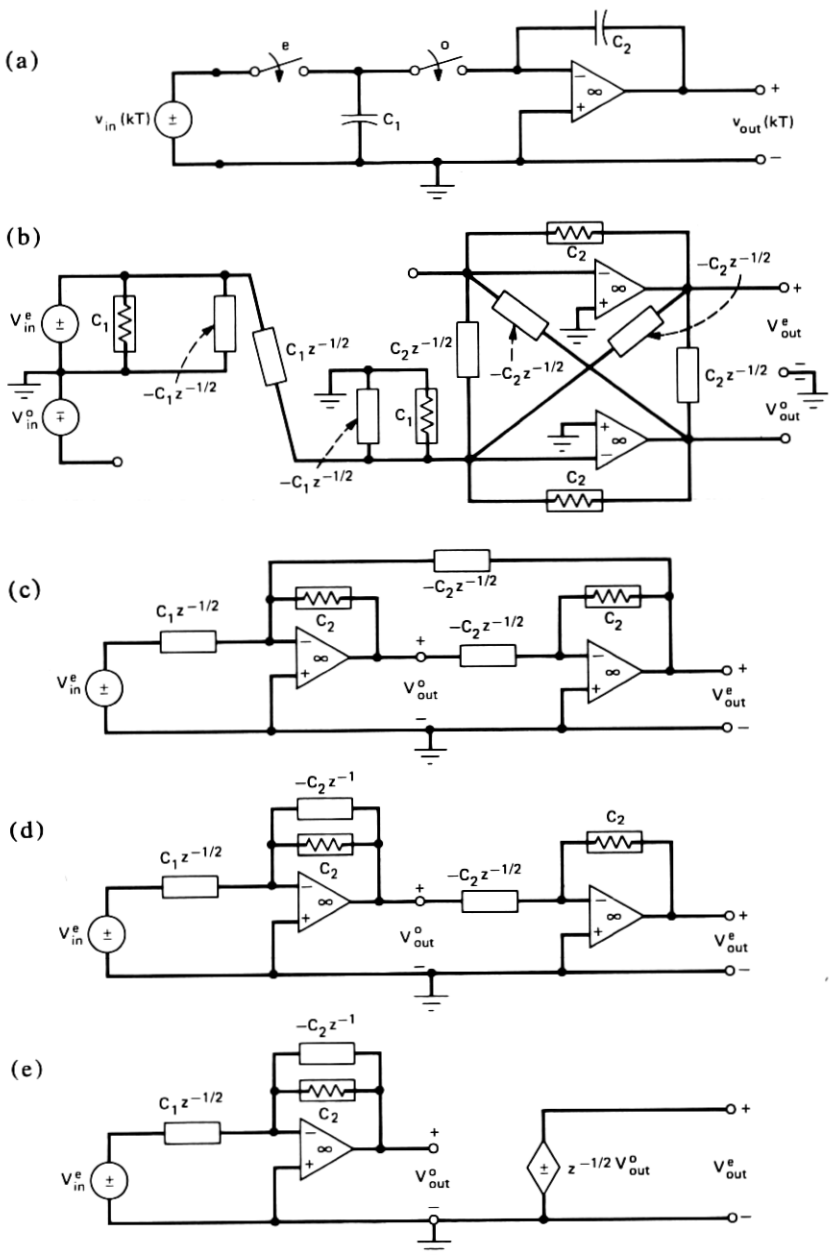


Fig. 13—Active-sc integrator.

Fig. 8. The final equivalent circuit in Fig. 13e implies that the lossless integrator could have been derived directly from the simplified equivalent circuits in Fig. 7.

The transfer functions for the lossless integrator are then readily

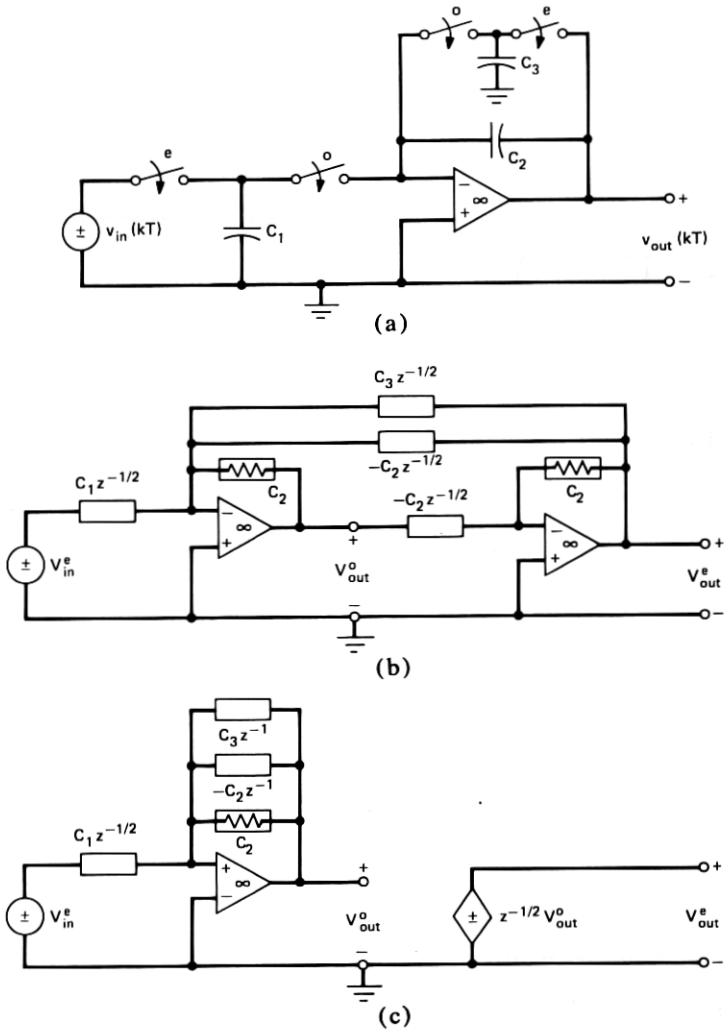


Fig. 14—Active-sc lossy integrator with TSC damping.

determined to be

$$H_3(z) = \frac{V^o_{out}(z)}{V^e_{in}(z)} = \frac{-(C_1/C_2)z^{-1/2}}{1 - z^{-1}} \tag{26a}$$

and

$$H_1(z) = \frac{V^e_{out}(z)}{V^e_{in}} = \frac{-(C_1/C_2)z^{-1}}{1 - z^{-1}}. \tag{26b}$$

Note that when the output of the lossless integrator is sampled at the odd times, the transfer function is H_3 and when sampled on the even times the transfer function is H_1.

4.2.2 Lossy integrator with TSC

As should be expected, the equivalent circuit for the lossy integrator, shown in Fig. 14a, is similar to that derived for the lossless integrator. To shift the pole to the left of $z = 1 + j0$, a toggle-switched capacitor (TSC) has been placed across the feedback capacitor. Obviously, the intent is for the TSC to play a role comparable to a resistor in active-RC lossy integrators. To analyze this network, let us first derive the equivalent circuit. This equivalent circuit can be derived step by step, as was done for the lossless integrator and shown successively in Figs. 14b and 14c, respectively. The final equivalent circuit in Fig. 14c, like that in Fig. 13e, can be readily derived from the simplified equivalent circuits in Fig. 7 by direct substitution. This result simplifies tremendously the equivalent circuits for complex, high-order active SC networks.

The transfer functions for the lossy integrator are then readily obtained from the circuit in Fig. 14c, namely,

$$H_3(z) = \frac{V_{out}^o(z)}{V_{in}^e(z)} = \frac{-(C_1/C_2)z^{-1/2}}{1 - [1 - (C_3/C_2)]z^{-1}} \tag{27a}$$

and

$$H_1(z) = \frac{V_{out}^e(z)}{V_{in}^o(z)} = \frac{-(C_1/C_2)z^{-1}}{1 - [1 - (C_3/C_2)]z^{-1}}. \tag{27b}$$

It is interesting to examine $H_3(z)$ for different values of C_3. Consider the following three conditions $C_3 = C_2$, $C_3 = 2C_2$, and $C_3 > 2C_2$. For $C_3 = C_2$:

$$H_3(z) = -\frac{C_1}{C_2} z^{-1/2} \tag{28}$$

an ideal half-delay element. For $C_3 = 2C_2$,

$$H_3(z) = \frac{-(C_1/C_2)z^{-1/2}}{1 + z^{-1}}, \tag{29}$$

and the circuit is no longer stable. Finally, when $C_3 > 2C_2$ the pole of $H_3(z)$ lies outside the unit circle and the circuit is clearly unstable. Obviously, the TSC is much more than a resistor; a point which has been illustrated[17] in other ways.

Let us look briefly at the effect of alternating the phases of the switches which make up the feedback TSC. This SC network along with its equivalent circuits are shown in Fig. 15. The transfer functions are then readily written

$$H_3(z) = \frac{V_{out}^o(z)}{V_{in}^e(z)} = \frac{-(C_1/C_2)z^{-1/2}}{1 - [1 - (C_3/C_2)]z^{-1}} \tag{30a}$$

and

$$H_1(z) = \frac{V^e_{out}(z)}{V^e_{in}(z)} = \frac{-(C_1/C_2)[(C_2 - C_3)/C_2]z^{-1}}{1 - [1 - (C_3/C_2)]z^{-1}}. \qquad (30b)$$

Comparing the pole location for $H_i(z)$ in eqs. (27) and (30), one observes that the TSC switch phasing has no effect on this parameter. However, the dc gain for the even component V_{out} is altered by the factor $(C_2 - C_3)/C_2$. It should be noted that these observations were not totally expected.

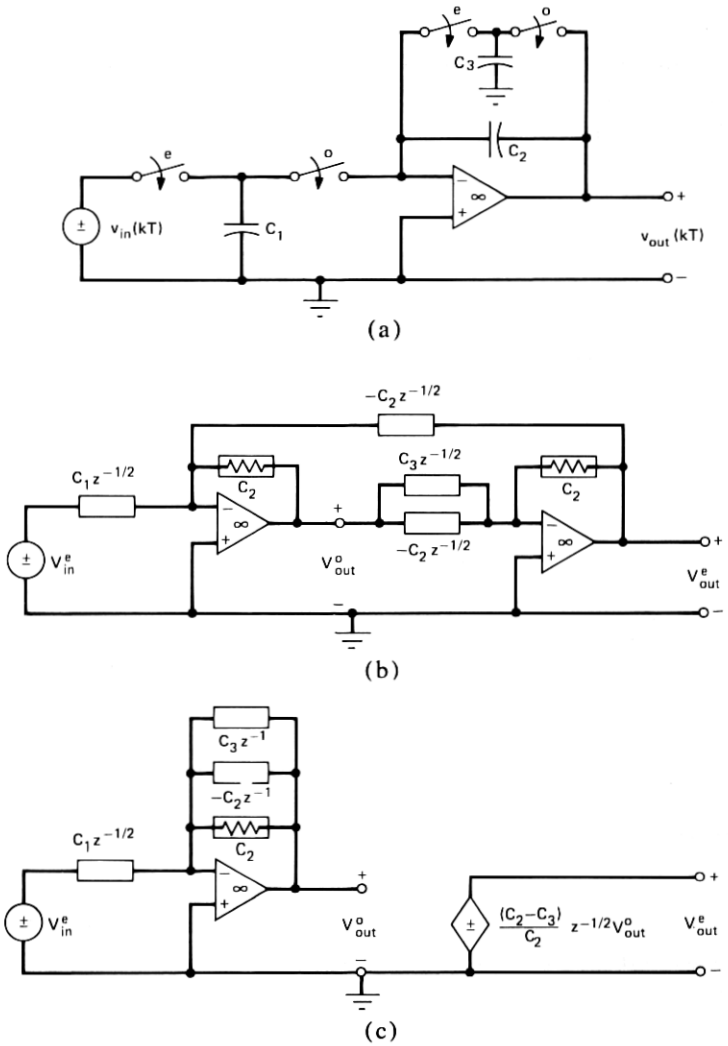


Fig. 15—Active-SC lossy integrator with TSC damping. The switches of the feedback TSC are phased opposite to that shown in Fig. 14.

4.2.3 Lossy integrator with OFR

Another lossy integrator realization is shown in Fig. 16a. Of perhaps only theoretical interest is the comparison of the behavior of this circuit with its counterpart in Fig. 14a. The equivalent circuit, shown in successive stages of simplification in Figs. 14b and 14c respectively, can be derived directly from the simplified block equivalent circuits in Fig. 7. The transfer functions for this circuit are

$$H_3(z) = \frac{V_{out}^o(z)}{V_{in}^e(z)} = \frac{[-C_1/(C_2 + C_3)]z^{-1/2}}{1 - [C_2/(C_2 + C_3)]z^{-1}} \tag{31a}$$

and

$$H_1(z) = \frac{V_{out}^e(z)}{V_{in}^e(z)} = \frac{[-C_1/(C_2 + C_3)]z^{-1}}{1 - [C_2/(C_2 + C_3)]z^{-1}}. \tag{31b}$$

The transfer functions expressed in eqs. (31) are seen to be truly representative of lossy integrators. $H_3(z)$ and $H_1(z)$ are absolutely stable for all finite values of C_1, C_2 and C_3.

4.2.4 Bilinear lossless integrators[26, 27]

Previously, in Section 4.1.1, an integrator was analyzed which achieved integration in the sample-data sense according to the transformations[28]

$$\frac{1}{s} = \tau \frac{z^{-1/2}}{1 - z^{-1}} \tag{32a}$$

or

$$\frac{1}{s} = \tau \frac{z^{-1}}{1 - z^{-1}}. \tag{32b}$$

It is well known[26, 28] that eq. (32b) only adequately approximates the function of an analog integrator for frequencies satisfying $w\tau \ll 1$. Although eq. (32a) overcomes[28] this difficulty, it cannot always be rigorously applied.[11, 28] An accurate and mathematically convenient integrator implementation is obtained via the well-known bilinear transform [22, 26, 28]

$$\frac{1}{s} = \frac{\tau}{2} \frac{1 + z^{-1}}{1 - z^{-1}}. \tag{33}$$

There are several ways bilinear integration can be realized[26, 27] with active-SC networks, as demonstrated in Figs. 17, 18, and 19. It is interesting to examine the behavior of each of these circuits.

Let us initially consider the bilinear integrator[26] shown in Fig. 17a. The z-domain equivalent circuit, obtained by interconnecting blocks 6b, 6c, 6m, and 6u, is shown in Fig. 17b. By straightforward nodal-

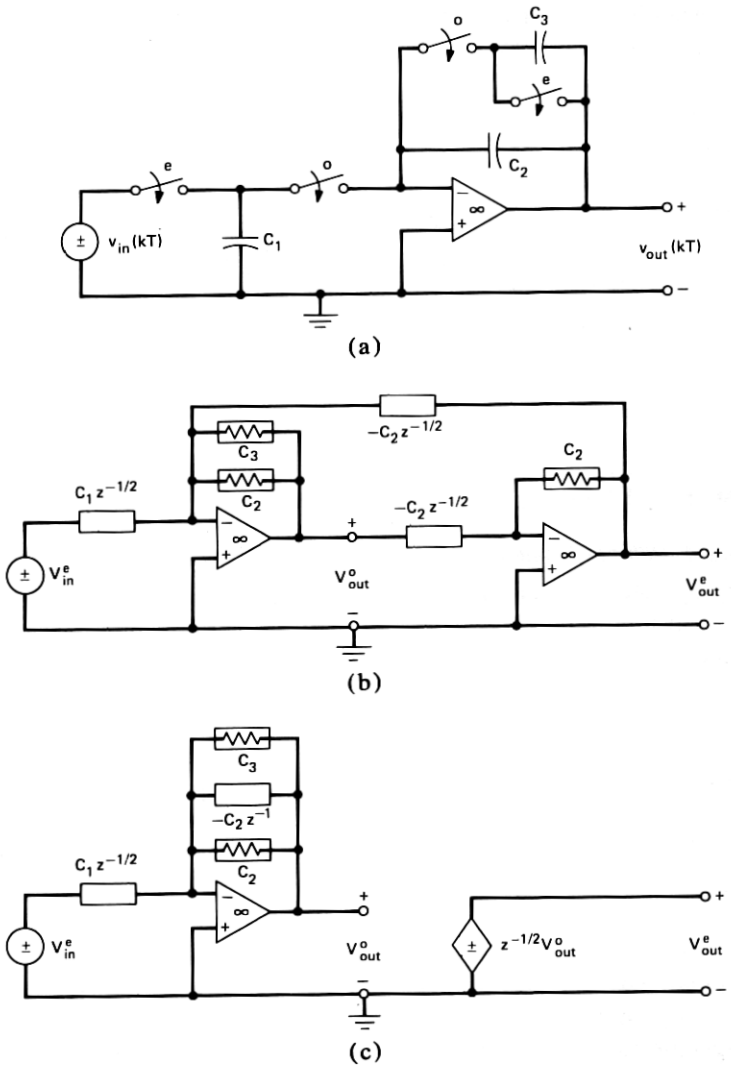


Fig. 16—Active-SC lossy integrator with OFR damping.

charge analysis, the following relations are easily obtained:

$$V_{out}^{o} = \frac{-(C_1/C_2)z^{-1/2}}{1 - z^{-1}} V_{in}^{e} - \frac{(C_1/C_2)}{1 - z^{-1}} V_{in}^{o} \tag{34a}$$

and

$$V_{out}^{e} = z^{-1/2} V_{out}^{o} . \tag{34b}$$

From eq. (34a), we observe that the desired bilinear integration is only

obtained when

$$V_{in}^{e} = z^{-1/2} V_{in}^{o} . \tag{35}$$

Substituting eq. (35) into eq. (34a) yields the desired result

$$H_4(z) = \frac{V_{put}^{o}}{V_{in}^{o}} = \frac{-(C_1/C_2)(1 + z^{-1})}{1 - z^{-1}} ; \tag{36a}$$

also,

$$H_2(z) = \frac{V_{out}^{e}}{V_{in}^{o}} = \frac{-(C_1/C_2) z^{-1/2}(1 + z^{-1})}{1 - z^{-1}} . \tag{36b}$$

In summary, this circuit, with the switches phased as shown in Fig. 17a, will provide bilinear integration only when the input and output are sampled at the odd $(2k + 1)T$ times and the input is held for the entire clock period.

A second bilinear integrator realization[27] is shown in Fig. 18a. The z-domain equivalent circuit, shown in Fig. 18b, is obtained by interconnecting blocks 6b, 6e, and 6u. The transfer relations for this circuit are readily determined to be

$$V_{out}^{o} = \frac{-(C_1/C_2)(1 + z^{-1})}{(1 - z^{-1})} V_{in}^{o} - \frac{2(C_1/C_2) z^{-1/2}}{1 - z^{-1}} V_{in}^{e} \tag{37a}$$

and

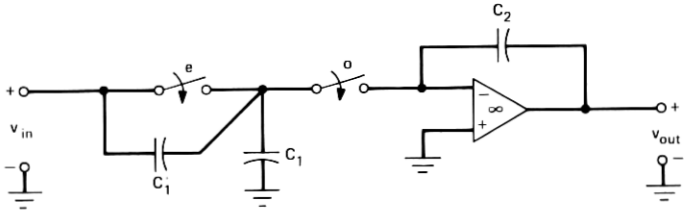
$$V_{out}^{e} = \frac{-(C_1/C_2)(1 + z^{-1})}{(1 - z^{-1})} V_{in}^{e} - \frac{2(C_1/C_2) z^{-1/2}}{1 - z^{-1}} V_{in}^{o} . \tag{37b}$$

The output, sampled at all (both even and odd) kT times, is obtained by summing eqs. (37a) and (37b) according to eq. (9) and cancelling the common factor $(1 + z^{-1/2})$; i.e.,

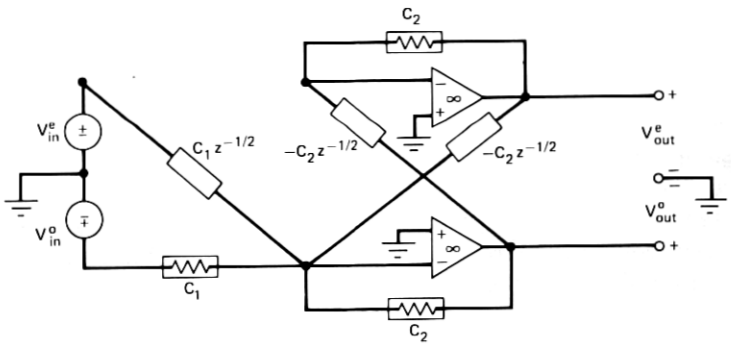
$$H(z) = \frac{V_{out}}{V_{in}} = \frac{V_{out}^{e} + V_{out}^{o}}{V_{in}^{e} + V_{in}^{o}} = \frac{-(C_1/C_2)(1 + z^{-1/2})}{1 - z^{-1/2}} . \tag{38}$$

Comparing equations (38) and (36a), we see that the effective sampling rate has been doubled with the circuit in Fig. 18a. Also, bilinear integration is obtained independent of the input sampling conditions. It is noted that sampling the output of this circuit at only the even $2kT$ times or only the odd $(2k + 1)T$ times will result in an erroneous output.

A third bilinear integrator is obtained by simply deleting one TSD from Fig. 18a, as shown in Fig. 19a. It is interesting to analyze this circuit and compare the results with that given in eqs. (37) and (38) for the integrator in Fig. 18a. The z-domain equivalent circuit in Fig. 19b is readily obtained by deleting the appropriate elements from the



(a)



(b)

Fig. 17—Active-sc bilinear integrator (Copeland, Ref. 26).

equivalent circuit in Fig. 18b. The transfer relations for this circuit are

$$V^e_{out} = \frac{-(C_1/C_2)(1 + z^{-1})}{1 - z^{-1}} V^e_{in} \tag{39a}$$

and

$$V^o_{out} = \frac{-2(C_1/C_2)z^{-1/2}}{1 - z^{-1}} V^e_{in} . \tag{39b}$$

Summing eqs. (39a) and (39b) yields

$$V_{out} = V^e_{out} + V^o_{out} = \frac{-(C_1/C_2)(1 + z^{-1/2})}{1 - z^{-1/2}} V^e_{in} . \tag{40}$$

Note that bilinear integration is obtained when the output is either sampled at the even $2kT$ times or at all (both even and odd) kT times. Again, bilinear integration is obtained independent of the input sampling conditions. This concludes the first-order active SC network examples. It should be noted that circuits similar to those in Figs. 13 through 16 could have been derived using the TSI and TSD elements shown in Figs. 6d and 6e or Figs. 7f and 7g. To further illustrate the procedure, the equivalent circuit for the fourth-order low-pass, leap-

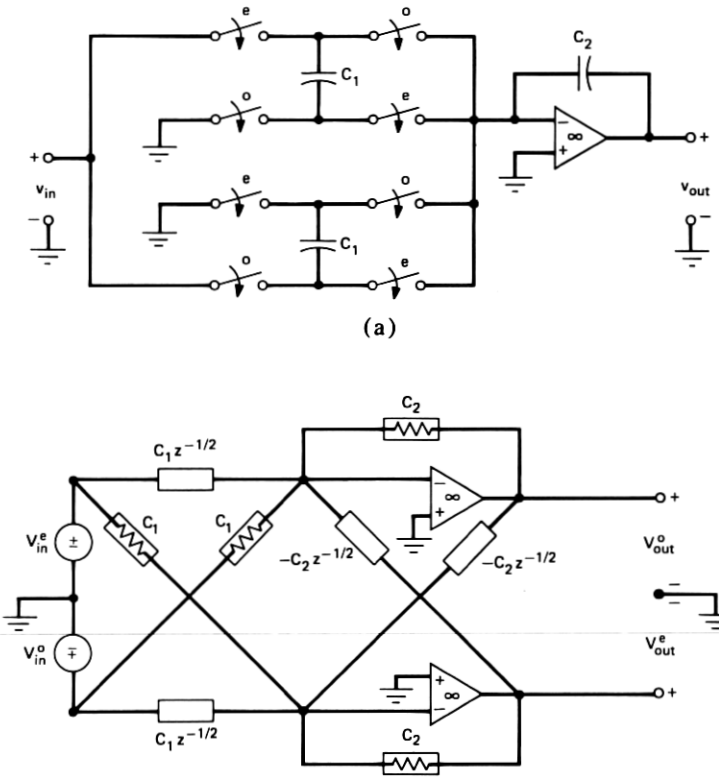
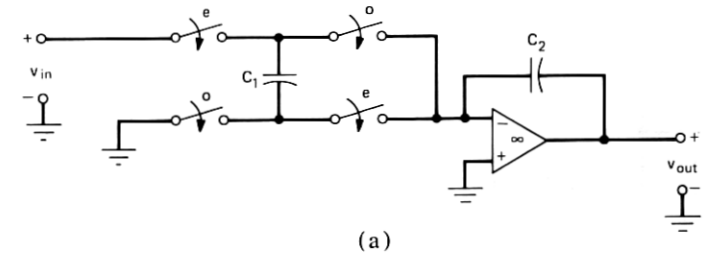


Fig. 18—Active-SC bilinear integrator (Temes and Young, Ref. 27).

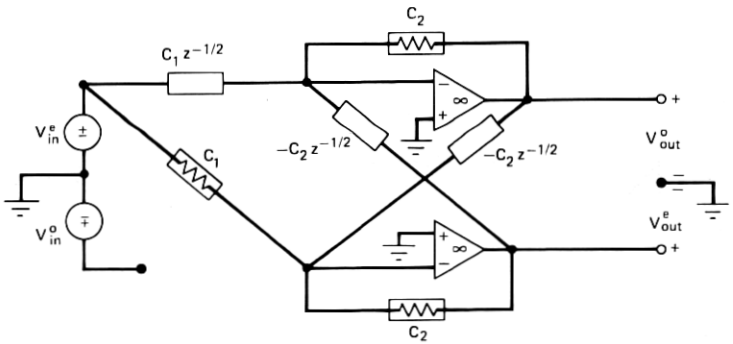
frog, active-SC filter, depicted in Fig. 20a, is given in Fig. 20b. This equivalent circuit is readily derived from the equivalent circuit blocks in Fig. 7 and the principles discussed in this section. The equivalent circuit in Fig. 20b is seen to be no more complex than the equivalent active-RC circuit. Note that, in the absence of the output even switch, the only modification to the z-domain equivalent circuit in Fig. 20b is an additional voltage-controlled voltage source at the output. This voltage-controlled voltage source defines the relation $V^o_{out} = z^{-1/2}V^e_{out}$, as shown previously in Fig. 14c. The verification of this circuit is left as an exercise for the reader.

V. CONCLUDING REMARKS

The powerful tools which we commonly refer to as network or circuit theory have been indispensable in advancing the analog filter art to its present level of quality and sophistication. Such fundamental concepts as transfer functions, poles, and zeros have provided the filter designer with quick insight as to the behavior of a given filter. He can then



(a)



(b)

Fig. 19—A reduced version of the bilinear integrator in Fig. 18.

efficiently design the filter by relating pole-zero movements to specific circuit elements. It is interesting, in this era of high-speed computers and sophisticated analysis programs, that many of the classical networks tools still maintain their important role in filter design. The objective of this work has been to make tools[16, 17] of this kind more accessible to the designers of switched capacitor filters.

In keeping with this goal, a comprehensive library of building-block equivalent circuits has been given. This library extends that given in Ref. 17 by providing equivalent circuits for higher order SC elements and a variety of sampled data sources. These SC elements, typically comprised of one capacitor and from one to four switches, serve as circuit elements for SC networks much in the spirit in which resistors and capacitors serve analog circuits. Viewing switched capacitor elements in this way facilitates the derivation of canonic z-domain equivalent circuits for complex SC networks and the application of classical networks tools to their analysis and synthesis.

In deriving the equivalent circuits, it is pointed out that there are several interpretations and types of link two ports or LTPs. The interpretation of the floating LTP as a balanced lattice network, in lieu of an unbalanced structure, results in the elimination of two transformers in the equivalent circuit for a floating capacitor. In addition,

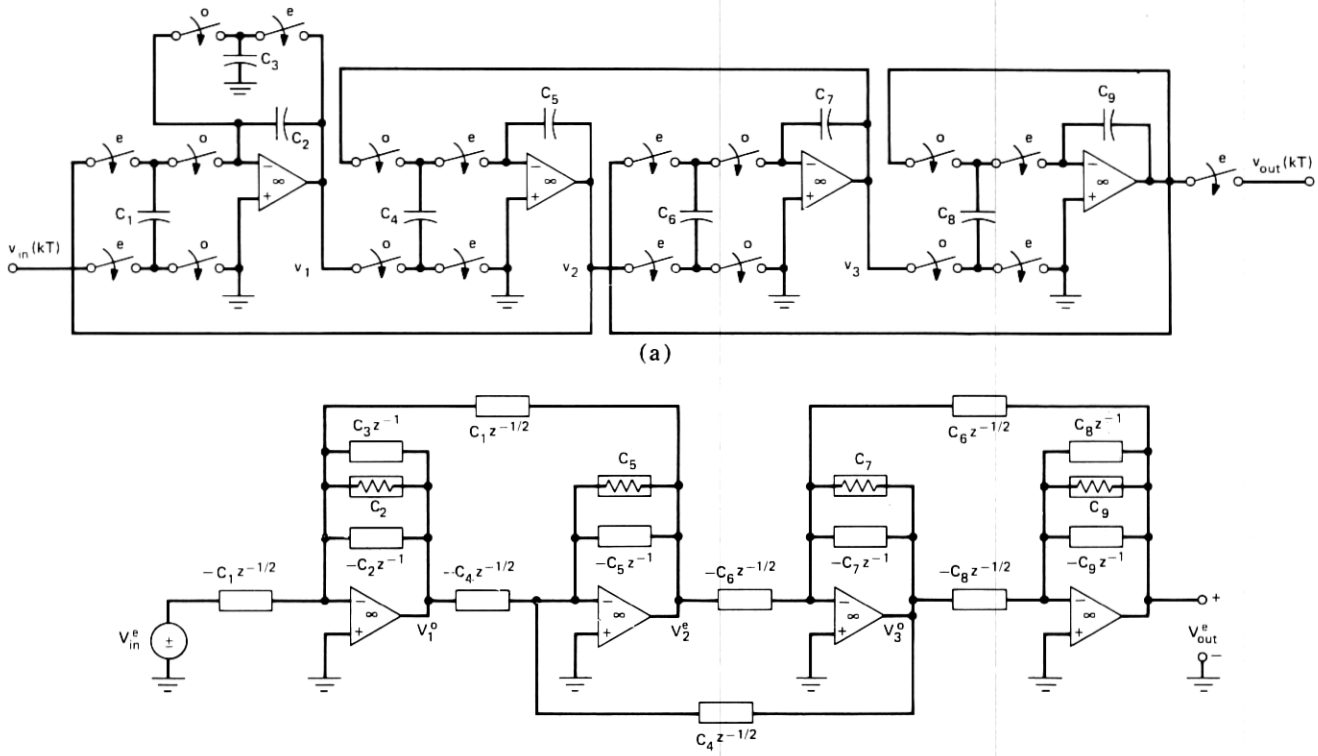


Fig. 20—Fourth-order, low-pass, leapfrog active-sc filter.

unbalanced inverting and differencing LTPs are also identified. An equivalent circuit is provided for a general toggle switched floating four port (TSFFP) element. The functioning ports are shown to be linked via a 90-degree rotated, balanced floating LTP. By applying the appropriate termination conditions to the TSFFP, its equivalent circuit can be used to derive the equivalent circuit for any single capacitor element in the library.

Several examples were worked out and discussed illustrating the case of application of the proposed equivalent circuits and the insight gained. Most interesting was the novel circuit depicted in Fig. 12 which exhibits a bifunctional capability; namely, a high-pass function at the even ($2kT$) times and a low-pass function at the odd ($2k + 1)T$ times. The application to active-SC networks of various complexities was also discussed. Particularly noteworthy were the various subtle differences among the circuits shown in Figs. 17, 18, and 19, all professed to realize bilinear integration.

VI. ACKNOWLEDGMENTS

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