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WT4 Millimeter Waveguide System:

Semiconductor Devices for the WT4 Repeater

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Design, fabrication, performance, and reliability information is provided for three types of millimeter-wave diodes developed to operate over the 40–110 GHz WT4 band. A family of silicon IMPATT diodes generate the transmitter and local-oscillator power. These diodes use an ion-implanted double drift impurity profile. A hermetically sealed package was developed to achieve high reliability. A diamond heat sink provides a low thermal resistance. A silicon PIN subnanosecond switching diode phase modulates the transmitted power. The passivated mesa of the PIN diode chip is fabricated from thin, high-resistivity epitaxial material to achieve low capacitance and fast switching. A gallium arsenide Schottky-barrier mixer diode down-converts the signal in the receiver. The beam-lead Schottky diode is fabricated using molecular beam epitaxy, which provides a novel junction-isolation technique. Also, a brief description is given of the salient features of other active devices which operate in the IF (1.371 GHz) and baseband (dc to 300 MHz) circuitry. They consist of a family of both transistors and diodes (step recovery device, PIN variolosser, and Schottky mixer).

I. INTRODUCTION

Three new solid-state diodes were developed to generate, modulate, and down-convert millimeter-wave signals over the 40–110 GHz WT4 band. Silicon IMPATT diodes generate the transmitter and local oscillator power, a silicon PIN switching diode phase-modulates the transmitted power, and a gallium arsenide Schottky-barrier mixer diode down-converts the signal in the receiver.

Also, numerous other devices were either specifically developed for or found usage in WT4. These devices operate in the IF (1.371 GHz) or baseband (dc to 300 MHz) circuitry.

Table I—WT4 system requirements for IMPATT diodes

Frequency, GHz	Power output, mW		Efficiency,† percent		Figure of merit*		Thermal impedance, °C/W	Total capacitance, pF
	2-phase	4-phase	2-phase	4-phase	2-phase	4-phase		
43	170	340	4.3	6.4	173	86	30	0.41
50	130	260	4.1	6.1	173	86	40	0.35
59	100	200	4.0	5.8	173	86	55	0.30
70	75	150	3.8	5.5	173	86	70	0.25
80	55	110	3.6	5.2	86	43	84	0.21
90	45	90	3.3	4.9	86	43	97	0.19
105	35	70	2.9	4.5	86	43	112	0.17

* Local oscillator only: power output ≥ 16 mW.
† Junction temperature not to exceed 230°C at rated power output.

This paper provides a detailed description of the design, characterization, and performance of the three millimeter-wave diodes. The salient features of the most significant lower-frequency devices will be discussed briefly.

II. MILLIMETER-WAVE IMPATT DIODES

2.1 System requirements

The IMPATT diodes developed for the WT4 system are used to provide the local oscillator and the transmitter power. Several diode codes are necessary to cover the broad frequency range. In addition to providing power, these devices also must meet stringent requirements for noise, modulation sensitivity, and reliability. The system requirements were met by using double-drift silicon IMPATT diodes hermetically encapsulated using a novel packaging approach.

The device performance characteristics necessary to satisfy the two-phase and proposed four-phase WT4 system requirements are listed in Table I. The power output, efficiency, and thermal impedance pertain to the transmitting oscillator. The efficiency and thermal impedance requirements are those needed to provide the desired power output and reliability (junction temperature) and are compatible with the heat-removal designs. The figure of merit is defined as the ratio of noise ($Hz/\sqrt{KHz}$) to modulation sensitivity (MHz/mA). It is a measure of the diode noise performance and should be independent of the circuit characteristics. This requirement pertains to both the local oscillator and transmitter diodes to assure acceptable noise performance. The capacitance values listed are those required to provide the proper impedance match to the individual oscillator housings.

2.2 Device design

The design of the IMPATT diodes evolved through several different stages. Gallium arsenide and germanium IMPATT diodes were eliminated

because theoretical analysis indicated that these materials exhibited inadequate power-frequency products.[1] Silicon IMPATT diodes, however, do not display this shortcoming. For silicon IMPATTs there remained the choice of the design of the drift region and the physical configuration that the device would assume.

2.2.1 Avalanche-drift region

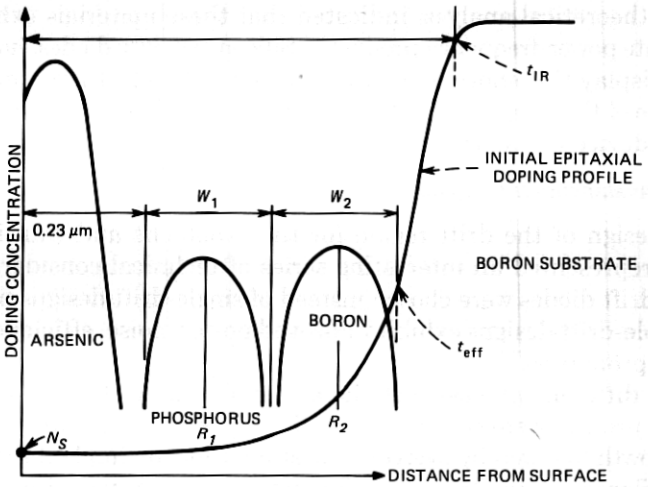
The design of the drift region for the avalanche and transit-time process represented an interesting series of technical considerations. Double-drift diodes were chosen instead of single-drift designs because the double-drift designs exhibit improved power, noise, efficiency, and thermal properties.[2,3]

Three different process techniques for obtaining the desired double-drift profiles were considered: (*i*) double-epitaxial growth, (*ii*) epitaxial growth followed by overcompensation using ion implantation, and (*iii*) a tailored ion-implanted doping profile into π-type epitaxy on p^+ substrates. The last was chosen since it represents the most controllable technique.[4] Because IMPATT diodes display a negative-admittance characteristic over a wide frequency range, three doping profile designs were adequate to provide oscillators covering the WT4 frequency range. These doping profiles provide devices with overlapping frequency bands.

The "all-implanted" double-drift n^+npp^+ structure was designed for use at 55, 75, and 105 GHz center frequencies. The design is shown in Fig. 1. The selection of a π on p^+ substrate structure takes advantage of boron's greater implant range compared with phosphorus or arsenic. Use of ν on n^+ substrates would require much higher implant energies.

The dose values were estimated empirically using previous experimental results and scaling laws. The ion dose is based upon a particular active number of carriers/cm^2 ($\int N\,dx$) establishing the desired drift width for the frequency of interest. An arsenic implant provides the high surface doping necessary to obtain an ohmic contact. The "all-implanted" design at all frequencies satisfied a system need for a single-polarity, single-process technology of IMPATT diodes.

To take advantage of the control inherent in ion implantation, it is necessary to carefully characterize the thin material used in this device. The most important parameter in the epitaxial concentration profile is the effective thickness, t_{eff}. This is the depth to which the active region is to be implanted and is measured by the spreading resistance (SR) technique.[5] After the dopant has been implanted and annealed, the slice is thinned, metallized, and separation-etched. Diodes are next bonded onto millimeter-wave bases and tailor-etched to the desired capacitance. Figure 2 shows the layout of the wafer, bonding tape, and package housing.



$W_{1,2}$ — DRIFT AND AVALANCHE, μm
R_1 — RANGE OF PHOSPHORUS IMPLANT, μm
R_2 — RANGE OF BORON IMPLANT, μm
t_{eff} — EFFECTIVE EPITAXIAL THICKNESS
t_{IR} — IR MEASUREMENT OF EPITAXIAL THICKNESS
0.23 μm — CONSTANT DEPTH INTRODUCED TO ACCOMMODATE SURFACE IMPLANT
N_S — SURFACE DOPING OF π LAYER

Fig. 1—Ion-implanted doping profile of millimeter-wave IMPATT.

2.2.2 Millimeter-wave IMPATT package

The package for the IMPATT diodes evolved to satisfy several needs that became apparent during the development of the diodes. These needs were to provide a controlled ambient for the surface of the silicon, protection for the wafer during handling, and a load bearing surface for the circuit probe contacting the top surface of the diode. The diamond heat sink was included to provide the low thermal impedance necessary to maintain sufficiently low operating temperatures to assure the desired reliability. It was embedded into the base to further reduce thermal impedance and to control the configuration of the diode base.

The package developed for the IMPATT diode applications provides low electrical parasitics and low thermal impedance. A package capacitance of 0.1 pF, inductance of 0.07 nH and the thermal impedance values listed in Table I were obtained.

The microminiature hermetic diode encapsulation shown in Fig. 2 is constructed on a metallized diamond embedded in a gold-plated copper base. The encapsulation is based on the use of a metallized quartz insulator having a hole in the center for the silicon wafer. The wafer is contacted and a top cover is thermocompression-bonded to the quartz, providing a hermetic package for the IMPATT chip.

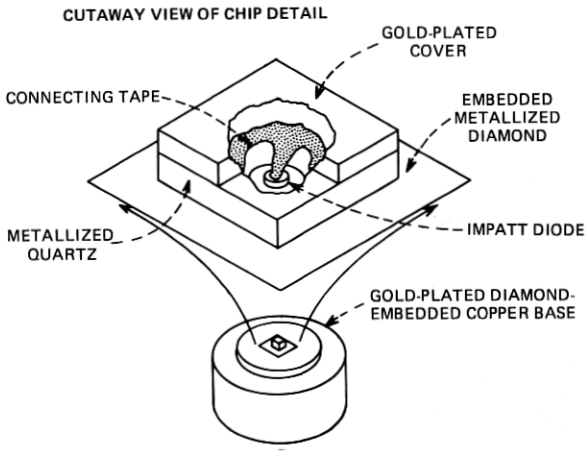


Fig. 2—IMPATT diode structure and package.

Since the package volume was too small to test hermeticity using conventional techniques the diodes were given an autoclave leakage test to evaluate both hermeticity and reliability.[6]

Instead of using a hermetic encapsulation to provide surface stability, we considered a passivated mesa approach. But calculations indicated that there were penalties in thermal impedance associated with the process. At 50 GHz the thermal impedance is 20 percent higher and would increase even more at higher frequencies. Also, the ability to tailor etch to obtain diodes for the desired frequency would be compromised and no mechanical protection would be provided.

2.3 System performance

The two-phase and four-phase power output requirements are plotted in Fig. 3. The dashed curve represents the median power output mea-

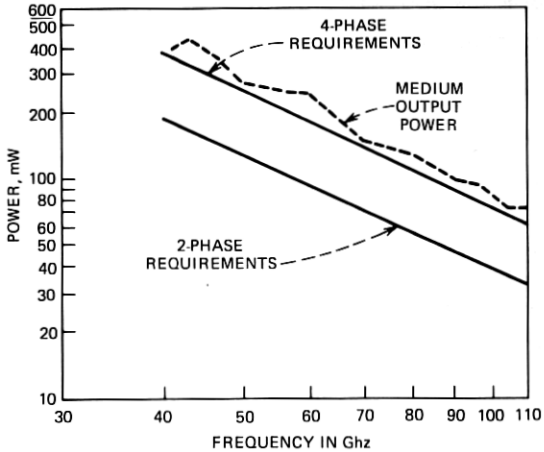


Fig. 3—IMPATT power output vs. frequency.

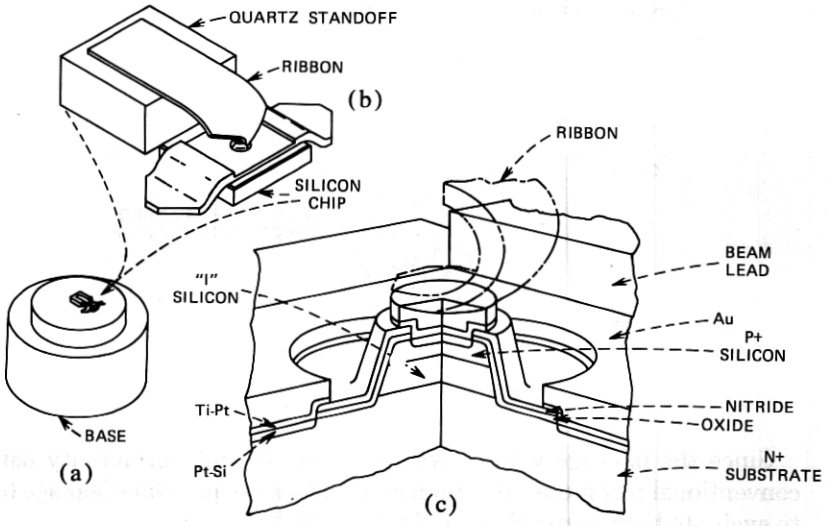


Fig. 4—Millimeter-wave PIN diode structure. (a) Assembled diode. (b) Diode chip, quartz standoff, and connecting gold ribbon. (c) Cut-away view of diode chip.

sured on groups of diodes at several of the WT4 design frequencies. The design has the ability to meet all two-phase requirements. However, to achieve a reasonable yield for the four-phase requirements the power output performance would have to be increased. Also, to meet the stringent noise and consequent figure-of-merit requirements of the local oscillator for the four-phase mode of operation, additional circuit/device/system evaluation is required.

III. PHASE SHIFT MODULATOR SWITCHING DIODE

3.1 Diode description and application

A low-loss, subnanosecond PIN switching diode was developed for WT4. It is used in the Phase Shift Modulator (PSM) of the transmitter over the 40–110 GHz frequency band. The quasi-beam-leaded (substrate only) diode chip is bonded on a gold-plated copper base as shown in Fig. 4a and 4b. A gold ribbon connects the oxide-nitride passivated mesa junction to the metallized top of an adjacent quartz standoff which is centered on the base. In the PSM the assembled diode terminates a coaxial line that couples into the waveguide. Switching the diode between forward- and reverse-bias states phase-modulates the incident waveguide signal.[7]

For proper circuit behavior a low and equal return loss is necessary in both bias states. The junction capacitance must be small to achieve the needed change in device impedance upon switching. Any parasitic

Table II—PIN diode electrical specification

Parameter	Condition	Limit	Typical
Balanced return loss	I_F = 10 mAdc V_R = 10 Vdc f = 54.2 GHz	≤1.2 dB	~0.7 dB @ 40 GHz ~1.0 dB @ 55 GHz ~1.5 dB @ 80 GHz ~2.5 dB @ 108 GHz
Total capacitance	V_R = 0 V	≤0.10 pF	0.06–0.08 pF
Total capacitance	V_R = 10 V	≤0.07 pF	0.04–0.05 pF
Breakdown voltage	10 μAdc	≥30 Vdc	~35 V
Storage time	$I_F = I_R$ = 10 mA	≤5.0 nsec	~4 nsec
Fall time		≤0.5 nsec	~0.4 nsec

reactive elements are present for both bias states and tend to mask the change in junction impedance, in addition to reducing the bandwidth. The time of switching between bias states must be short in comparison to the period of the modulating signal from the PSM driver. The stored charge injected during forward bias causes a delay in the switching action from the forward to reverse bias states and must be limited to avoid excessive timing errors.[8] The resulting electrical requirements that the PSM imposes on the PIN diode are shown in Table II.

At this time, it seems probable that two diode designs will be necessary to provide adequate circuit performance over the entire 40–110 GHz band. Different diode capacitances are needed for the low and high end of the frequency range. Further characterization is needed for frequencies >70 GHz, in particular, to firmly establish the diode loss as a function of frequency. The increased incident power of the four-phase system would not require any changes in diode design to meet either electrical or reliability specifications.

3.2 Device design

A thin-base epitaxial PIN diode fabricated using high resistivity ν-type silicon epitaxial material is most suitable for meeting the PSM switching diode specifications.[9] A "doping well" is formed by the shallow p^+ in-diffusion and steep doping tail from the n^+ substrate. This constitutes an optimum structure from the standpoint of maximum breakdown voltage, minimum capacitance per unit area, low resistance, and fast switching speed.

At very low reverse voltages (≲2 V) the junction depletion region extends completely to the substrate. The breakdown voltage is therefore essentially determined by the base width and the critical electric field at breakdown which for silicon is ~30V/μm. The base width was chosen to achieve a breakdown voltage of ~36 V. Similarly, the junction capacitance at −10 V can be determined in terms of a parallel plate capacitor model and was calculated to be 0.027 pF. The parasitic capacitance of the quartz standoff adds ~0.014 pF. The zero bias capacitance

specification is readily met due to the high resistivity of the base and is necessary to prevent varactor action and thereby undesirable modulation.

A mesa containing a plane junction was chosen to physically confine the stored charge injected during forward bias. During the forward-to-reverse bias switching transient, the majority of the charge is removed during a storage time interval before the device impedance switches to the high-impedance state. Switching occurs during the fall time interval when the residual stored charge is removed. In the usual planar diffused junction, part of the injected charge is distributed parallel to the surface. Removal of this charge component is diffusion-limited, and this results in slow switching speeds. The amount of stored charge injected during forward bias, is controlled by the mobile carrier lifetime. The lifetime is a direct function of base width and an inverse function of current density.[10] The exact functional relationship is processing dependent and must be established experimentally.

The forward-bias resistance of the base region is essentially fixed by the stored charge and its geometrical dimensions. The remaining diode series resistance is contributed by the metallurgical contacts and substrate. Spreading resistance from the small junction diameter and skin depth effects at millimeter-wave frequencies are important. To reduce these resistance contributions, a heavily doped n^+ substrate was used. The contact to the substrate was placed on the front of the chip, as close as possible to the base of the mesa—Fig. 4c. Beam leads for the substrate contact logically follow. The use of beam leads also permits the fabrication of a chip size sufficiently large to be manufacturable, while maintaining the small active diode region. The chip size, including beam leads, was determined by the minimum outer diameter of the coaxial line which the diode terminates.

3.3 Fabrication

Oxide-nitride passivation and a sealed-junction overlay PtSi-Ti-Pt-Au metallurgical contact was chosen for high reliability.[11] The low barrier height of PtSi (~0.25 eV) is needed to minimize the contact resistance of the small-diameter p^+ contact. The mesa height must be sufficient to assure that the substrate contact is made to material which has the bulk substrate resistivity. The epitaxial material was grown using chemical vapor deposition of $SiCl_4$. However, to achieve a sharp epitaxial-to-substrate doping profile, a heat treatment was performed after HCl *in situ* etching, but before deposition of the epitaxy.[12]

3.4 Characterization and results

Typical values achieved for the various electrical characteristics of the device are also listed in Table II. The storage time was within the

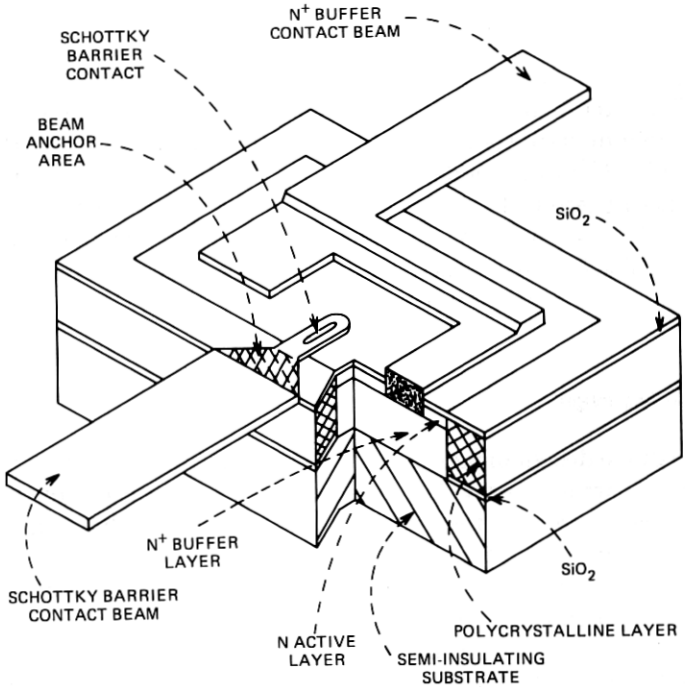


Fig. 5—Cross-sectional view of low parasitic capacitance Schottky-barrier mixer diode.

specification limit for the diode dimensions chosen, which were based upon breakdown voltage and capacitance requirements. If the storage time had been too high, the use of gold or platinum doping would have been considered. The fall time was found to be a function of the base width, the shape of the epi-to-substrate doping tail, and the junction depth. The first factor is basically a transit-time effect. The last two factors decrease the degree to which the stored charge is confined and are diffusion-limited. The switching path of the diode impedance was found to be close to resistive.[8] This permits a relaxation of transient and error timing requirements in the system.

IV. GALLIUM ARSENIDE MIXER DIODE

4.1 Device description and application

The WT4 receiver uses planar, isolated, gallium arsenide, beam-leaded diodes to down-convert the millimeter wave signal. One diode design is adequate to cover the entire 40–110 GHz WT4 frequency band and meet the two-phase receiver noise requirements. Low parasitic capacitance (~0.02 pF) between the Schottky-barrier beam and the n^+ epitaxial layer (see Fig. 5) is achieved by the simultaneous deposition of both

single-crystal and high-resistivity polycrystalline gallium arsenide by the Molecular Beam Epitaxy (MBE) technique.[14,15]

The diodes are thermocompression-bonded to millimeter-wave thin-film circuits in either the orthomode double balanced down-converter (four diodes)[16] or the half-frequency pumped down-converter (two diodes).[17–19] Typical diodes selected for these circuits have a total capacitance at zero volts less than 0.08 pF and an excess series resistance (R_{SF}), calculated from the dc forward-bias junction characteristics, less than 8 Ω. The final zero bias total capacitance and excess series resistance limits have not been established.

4.2 Diode Design

The diode design makes use of the majority-carrier current flow in a Schottky barrier to provide a nonlinear impedance at millimeter-wave frequencies for mixing the local oscillator and signal voltages in the WT4 receiver down-converter.

A major consideration in the design of the beam-lead diode was the overlay capacitance between the Schottky-barrier beam and the n^+ substrate—Fig. 5. This capacitance provides a shunt path for current across the Schottky barrier and lowers the local oscillator and signal voltage swing across the active metal-to-semiconductor junction.

The first diode design was a planar structure fabricated on an n-type epitaxial layer deposited on a heavily doped n^+ substrate. The performance of these diodes met the two-phase system conversion-loss requirements at the lower frequency end of the band, but the shunting capacitance degraded their high-frequency performance. The dielectric (deposited oxide) thickness could be increased to reduce the overlay capacitance. However, the definition of the junction window would deteriorate. Or the high-frequency performance could be improved by reducing the anchor area, but the diodes became mechanically fragile and difficult to handle and bond.

The development of MBE techniques, to produce simultaneously low-resistivity single crystal and high-resistivity polycrystalline gallium arsenide on semiinsulating substrates, provided the means whereby the overlay capacitance could be reduced. It was possible to simultaneously decrease the anchor area over the n^+ layer and to increase the dielectric isolation with respect to the remaining anchor area. In addition, the planar diode design was retained, along with adequate total anchor area.

For two-phase operation the planar polyisolated technique is capable of achieving the WT4 requirements over the complete frequency band. Further development is necessary to meet the four-phase objectives.

Table III—Typical diode characteristics for planar-isolated diodes

Parameter	Condition	Typical
Junction capacitance	$V = 0$ $f = 1$ MHz	0.04 to 0.06 pF
Parasitic overlay capacitance		~0.02 pF
Forward bias series resistance	$I_F = 5$ mAdc	4 to 8 Ω
Diode quality factor, n*		1.1 to 1.3
Reverse voltage	V_R @ 10 μAdc	5 to 12 Vdc
Reverse current	I_R @ −3.0 Vdc	$<1 \times 10^{-9}$ A

* $I_F = I_S$ [exp $(qV/nkT) - 1$]

4.3 Fabrication

Chromium doped semiinsulating substrates are polished and covered with a thin layer of deposited SiO_2 into which the isolation patterns are etched. The n^+ buffer and n active layers are deposited by MBE techniques and form into single-crystal gallium arsenide on the exposed gallium arsenide surface, and into high-resistivity polycrystalline gallium arsenide over the oxide-covered areas.

An n^+ ohmic contact pattern, centered in the single crystalline area, is defined in a second SiO_2 layer and etched to remove the n epitaxial layer down to the n^+ buffer layer. A low resistance ohmic contact to the n^+ buffer layer is formed by spike-alloying layers of gold, tin, and nickel.

After defining the junction window in the second SiO_2 layer, the Schottky barrier is formed by sequentially depositing titanium and platinum. The metallization pattern is Au plated and elsewhere the titanium and platinum are removed. Areas of the beam outside the active area of the diode and extending outside the region of the chip receive a heavy gold plate. The completed wafer is back-lapped, masked with photoresist, and etched to separate the diodes.

4.4 Characterization and results

Completed planar-isolated diodes are tested for 1-MHz zero-bias total capacitance, forward and reverse junction characteristics. The dc forward bias series resistance, R_S, is calculated from the forward bias characteristic. Diodes with typical characteristics as shown in Table III are suitable for mixer circuits.

The feasibility of using 1-MHz zero bias total capacitance and forward series resistance data to select diodes for mixer circuits is demonstrated by the curve shown in Fig. 6. Close agreement is found between the measured and calculated conversion loss plotted for a set of four diodes in a double-balanced down-converter.[16] In the original n/n^+ diode design the dc forward-bias series resistance was lower than the equivalent

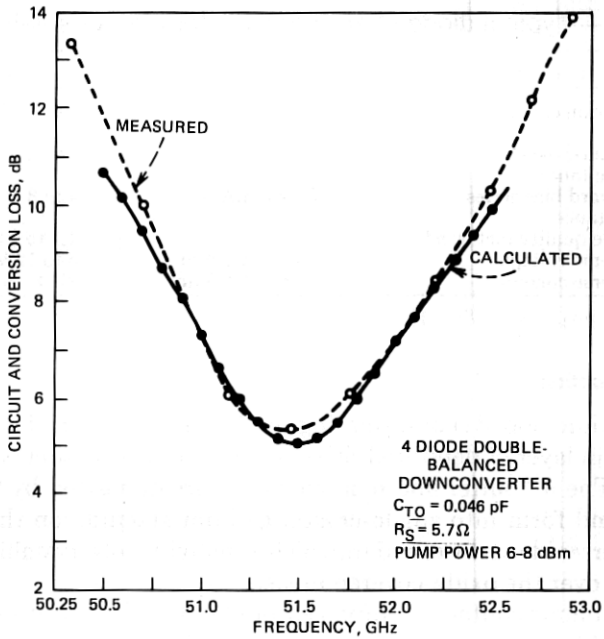


Fig. 6—Measured and computed conversion loss for a balanced mixer.

high-frequency resistance due to skin effects. This is not a major factor with the planar-isolated diode structure since the buffer layer is approximately the same thickness as the skin depth. Hence, the path along which both the dc and high-frequency currents must flow is approximately the same.

V. OTHER SEMICONDUCTOR DEVICES FOR WT4

5.1 Silicon surface PIN diode

A beam-lead PIN variolosser diode was developed for application in the AGC circuit of the receiver IF amplifier. The diode is fabricated from high resistivity n substrates using planar processing. The p^+ and n^+ regions were both formed on the front surface.[20] The diode features a low forward-bias resistance ($\leq 4\ \Omega$ at 20mA, 1.5 GHz) and low total reverse-bias capacitance (≤ 0.2 pF at -0.8V). A thick dielectric is used to reduce the parasitic junction beam capacitance.

5.2 Silicon step-recovery diode

A beam-lead step recovery diode is used at baseband frequencies in both the regenerator circuit and as a ×5 multiplier. The diode is fabricated from thin, high-resistivity ν on n^+ epitaxy, and is similar to the millimeter-wave PIN diode. Again, a passivated mesa junction confines

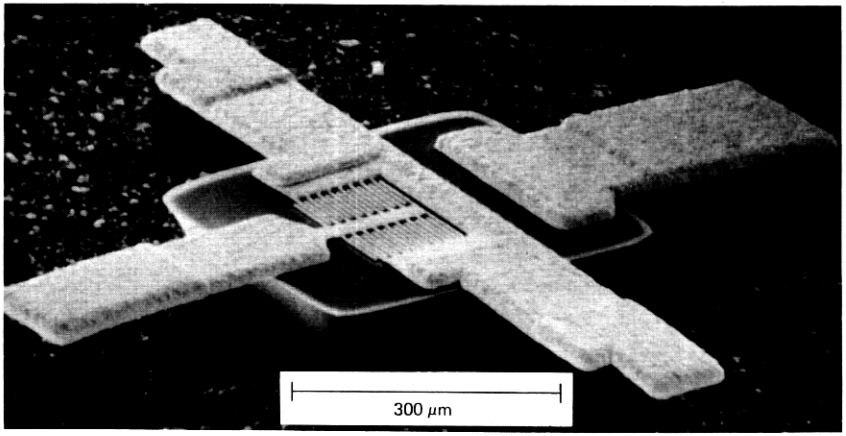


Fig. 7—Large area microwave transistor.

the stored charge to minimize the fall time (≤0.7 nsec). The higher storage time of ≥7.0 nsec is met by increasing the junction diameter. The storage and fall times were measured for a drive condition of $I_F = I_R =$ 10 mA.

5.3 Gallium arsenide Schottky diode

A second beam-lead GaAs Schottky diode was developed for use in the IF detector and amplifier, PSM driver circuit, and various baseband circuits. This diode is fabricated using n on n^+ epitaxy and planar processing. The barrier metal is titanium. The diode has a zero bias capacitance of ≤0.5 pF and a series resistance of ≤3Ω.

5.4 Silicon microwave transistors

A family of beam-lead npn microwave transistors was developed for numerous applications in both the IF and baseband circuitry. The interdigitated emitter and base stripes have a 2.5 μm width and 2.5 μm separation between stripes. A 0.25 μm base width is achieved using ion implantation to introduce both the emitter and base dopants.[21] The transistor was designed to operate at a current level of ~10 mA and has a typical collector-base capacitance of 2.5 pF at −3 V. One of the transistors must meet tight specifications on both magnitude and phase of all *s* parameters. In particular, the forward insertion gain is 9.7–11 dB at 1.4 GHz. Also, a transistor with four times the emitter area was also developed for the higher power needed in the PSM driver—Fig. 7.

VI. DEVICE RELIABILITY

Accelerated life tests were performed on all the devices developed for WT4 to establish their reliability. The median time to failure for each

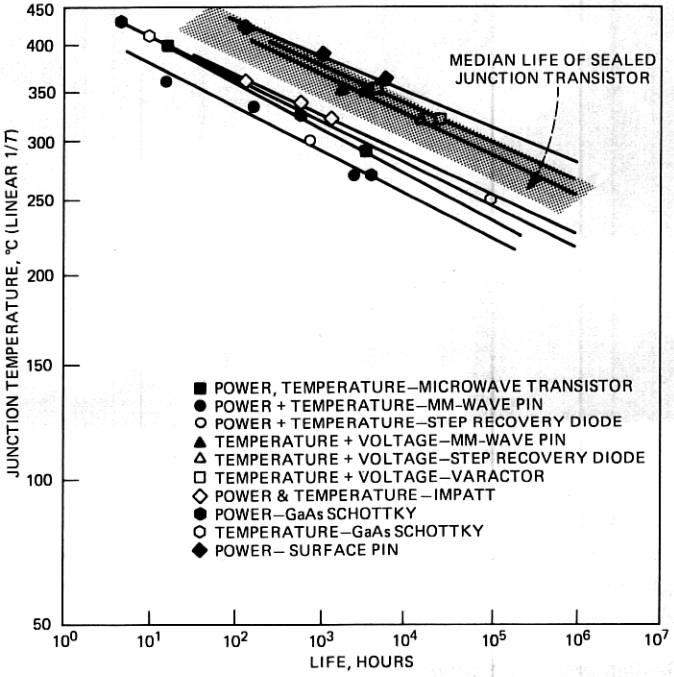


Fig. 8—Device reliability: median time to failure as a function of junction temperature.

device is shown plotted in Fig. 8 as a function of junction temperature. The shaded area on the figure represents extensive data of the median life of sealed-junction transistors as established by Peck.[22]

All the devices except the IMPATT have a projected reliability of less than 10 FIT when extrapolating the aging data to user condition. The IMPATT reliability is 600 FIT at the maximum operational junction temperature of 230°C.

The observed activation energies for the devices are characteristic of a metallurgical failure mechanism as opposed to a surface charge migration mechanism. The dominant failure mode was a degradation of the reverse characteristic and excessive leakage current, with some catastrophic failures showing evidence of contact metal alloying into the silicon.

Temperature aging at 350°C, with and without reverse bias, and dc forward-bias power aging were performed on the millimeter-wave PIN diode. Bias had little effect on the mean time to failure. Power dissipation was the more severe aging condition. Data for the step-recovery diode matches that of the PIN diode quite well. Both devices have a thermal impedance of approximately 600°C/Watt. An activation energy of 1.7 eV was calculated for the regression curve of the aging data.

For the beam-leaded millimeter-wave GaAs Schottky both ac power aging and temperature aging fit the same regression line. The beam-leaded microwave GaAs Schottky data also fell on this regression line. This was equally true for a third device, a packaged GaAs chip, not reported on in this paper. All three devices use titanium as the barrier metal and have an activation energy of 1.8 eV.

The beam-leaded surface PIN diode was subjected to forward-bias dc power aging at elevated temperature. A 2.3 eV activation energy was established. Temperature aging with reverse bias data was also available for a silicon beam-leaded varactor diode used in WT4. It has an activation energy of 1.9 eV.

DC and 50-GHz power aging at elevated temperature was performed on the millimeter-wave IMPATT diode. For the microwave transistor both temperature and power aging data fit the same regression curve. Activation energies of 1.9 eV and 1.6 eV, respectively, were calculated.

VII. SUMMARY

Three unique devices were developed to generate the millimeter-wave power, phase-modulate the carrier, and down-convert the signal of the WT4 system. These devices represent a wide application of state-of-the-art materials and fabrication development and millimeter-wave characterization. Reliable devices were provided that meet the two-phase requirements of the WT4 system over the frequency band 40–110 GHz. To meet the four-phase system objectives would require further device and circuit development. Numerous other devices were also developed for operation in the IF and baseband circuitry.

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