The Bell System Technical Journal
Vol. 53, No. 10, December 1974
*Printed in U.S.A.*

## *L5 SYSTEM:*

# Jumbogroup Frequency Supply

By J. F. BARRY, S. NARAYANAN, and J. F. OBERST

(Manuscript received November 8, 1973)

*The jumbogroup frequency supply (JFS) provides accurate and reliable synchronization signals to L5 jumbogroup multiplex carrier supplies. The JFS output-signal frequency is held to within several parts in $10^{10}$ of an input reference frequency. This extraordinary accuracy is achieved by digital frequency control of a precision quartz oscillator. The excellent reliability required when the JFS serves over 100,000 two-way voice circuits is achieved by redundant power and signal feeds, one-for-one protection of key circuits, and automatic protection switching.*

*In addition to its L5 application, the JFS will also serve as a regional frequency supply in a new synchronizing frequency distribution network that will upgrade the entire Bell System transmission plant.*

## I. INTRODUCTION

It is the goal of the Bell System to maintain frequency offset in any transcontinental circuit to within ±2 Hz. This requirement is imposed by the most sensitive message signals, such as those in programming, telegraph signals, and data signals. In an analog amplitude-modulated system, such a frequency offset can be introduced into the message signal if the transmitting and receiving multiplex carriers are not synchronized. In a single-sideband suppressed carrier multiplex format as used in jumbogroup multiplex[1] terminals (JMX), the multiplexing carriers are not transmitted. Thus, precision frequencies must be provided for the multiplex terminal at each geographical location.

The top channel frequency of the long-haul, analog, frequency-division multiplex system has been steadily increasing. With the increase in top channel frequency ($F$), the frequency precision required of the multiplex carriers increases. This is because the frequency offset

($\Delta F$) is limited to 2 Hz, whereas the ratio $\Delta F/F$ decreases as $F$ increases. In the L5 coaxial system, the top channel frequency is at 60 MHz, and the 2-Hz requirement results in a ratio of 3.3 parts in $10^8$ ($3.3/10^8$). Because a typical signal may traverse through several JMX terminals, carrier frequencies must be synchronized with an accuracy of about 1 part in $10^8$.

The frequency precision demanded by the L5 system could not be provided by the synchronizing network existing at the time L5 design work was initiated. Several alternatives were studied. One alternative was to provide a cesium frequency standard at each multiplex location. The cost of the cesium standard, the need for providing at least two such standards for reliability at each location, and the need for training personnel to maintain them made this option unattractive. An alternative was to provide a primary frequency standard at a central location and transmit reference-frequency signals to different locations. Such a primary frequency standard, called the Bell System Reference Frequency Standard[2] (BSRFS), has been designed. It comprises three cesium standards and provides highly accurate reference signals (better than one part in $10^{11}$).

At the receiving location, several alternatives were open. One option was to use a precision voltage-controlled crystal oscillator, whose frequency drift could be manually corrected periodically. The manual control implied trained personnel and periodic maintenance. Moreover, frequency-control circuitry is required for alarming and switching purposes in case of oscillator failure. Thus, it was decided to control and monitor frequency automatically, and the precision frequency supply so designed (the jumbogroup frequency supply, or JFS) is the subject of this paper.

The reference-frequency signal, even though highly accurate, may suffer short term impairment like noise, switching transients, etc. It may even be lost completely due to transmission difficulties. Because of the large number of circuits (more than 100,000) dependent upon one JFS, it is imperative that precision frequencies be supplied to the JMX even when the reference signal is lost or impaired. To accomplish this objective, a precision crystal oscillator capable of accurately free-running for a short period of time is employed in the JFS. The precision oscillator is loosely coupled to the reference signal such that it can automatically correct itself when the unimpaired reference signal is present and disconnect from the reference signal if the reference signal is impaired or lost. A digital memory is provided in the digital frequency-control circuit so that the oscillator can remain at the correct

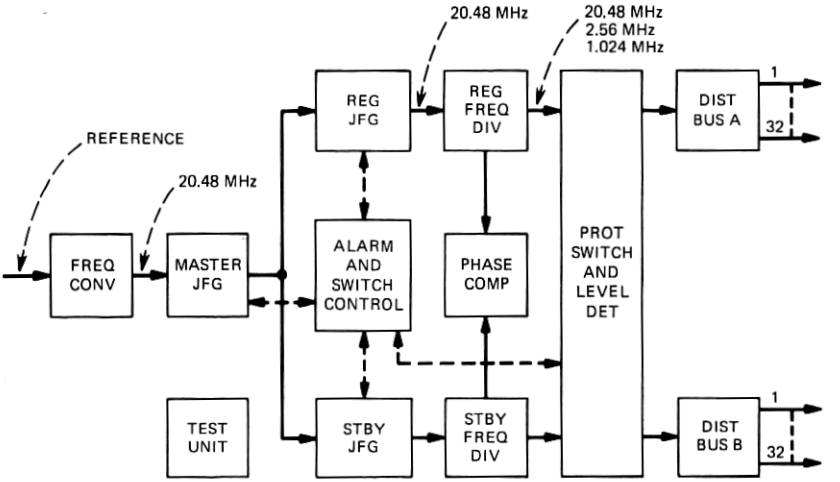


Fig. 1—Block diagram of jumbogroup frequency supply.

frequency even when the reference signal is disconnected. The precision oscillator and the precision digital frequency-control circuits are housed in a unit called the jumbogroup frequency generator (JFG).

An important consideration in the design of the JFS is reliability. More than 100,000 two-way voice circuits may depend upon one JFS. To ensure reliability, automatic protection switching is provided for its key circuits. Several visual alarms are provided so that preventive action can be taken before protection switching is needed. The working of the frequency-control circuitry can be checked without any interruption of service. Redundant power feeds connect each JFS to the office battery and two cables are provided to each JMX.

Human engineering has been given careful consideration. A precision test unit to measure accurately the difference between two signals has been incorporated in the JFS. This will enable the craftsperson to troubleshoot the bay if necessary. A manual patching arrangement and manual override have been provided to ensure that the craftsperson can take full control of the bay if needed.

## II. SYSTEM DESCRIPTION OF JFS

The JFS furnishes three precision frequencies to the JMX carrier supply, where further processing occurs to generate all the carriers needed for frequency multiplexing. The three frequencies are at 20.48 MHz, 2.56 MHz, and 1.024 MHz. An overall block diagram of the JFS is shown in Fig. 1. It consists of three JFG's arranged in a master-

slave configuration, two frequency dividers, switch and alarm circuitry, two output buses, and a precision frequency-measuring test unit.

The master JFG directly receives the 20.48-MHz reference signal. In some locations, the reference signal will be at 2.048 MHz; a frequency converter has been designed to convert 2.048 MHz to 20.48 MHz. The master JFG compares its precision-oscillator frequency with the incoming reference signal and corrects its oscillator based on the long-term average of the frequency difference. The master JFG output signal is at 20.48 MHz and is fed to the regular and standby JFG's.

The incorporation of three JFG's in a JFS ensures detection of a JFG failure even when the reference signal is noisy or absent. Such a detection would quickly initiate alarm and switching circuits to take appropriate action. If only two JFG's were provided in a JFS, the failed JFG could not be isolated if the failure occurred when the reference signal was absent or noisy.

The regular and standby JFG's use the output of the master JFG as their reference. In this master-slave arrangement, the input signal to the regular and standby JFG's should be good all the time unless the master JFG fails. In contrast, the master JFG reference signal, while highly accurate when present, may be absent or noisy at times. For this reason the master JFG does not produce frequency alarms unless the frequency offset exceeds $1/10^8$ and lasts at least two hours; the regular and standby JFG's produce frequency alarms if the offset exceeds $2/10^9$ and lasts for several hundred milliseconds (see the JFG description in Section III).

As shown in Fig. 1, the output of the regular JFG (20.48 MHz) is fed to the regular frequency divider; similarly, the standby JFG feeds the standby frequency divider. The function of the frequency divider is to generate 2.56-MHz and 1.024-MHz signals and combine all three frequencies (20.48 MHz, 2.56 MHz, and 1.024 MHz) together for transmission on one coaxial cable. The output of the regular divider is transmitted to the two output buses through two coaxial switches. The coaxial switches are operated by the alarm-and-switch-control unit which processes information from the three JFG's and the level detectors. The output bus has 32 taps, and because of reliability considerations one JFS may serve up to 22 JMX's. Each JMX is connected by two cables, one from bus A and the other from bus B. Thus, the regular divider feeds both sides of the JMX. The output of the standby divider is fed to the two coaxial switches. If a regular JFG or frequency divider fails, the alarm and switch control unit will operate the coaxial switches so that the standby JFG and divider will supply signals to

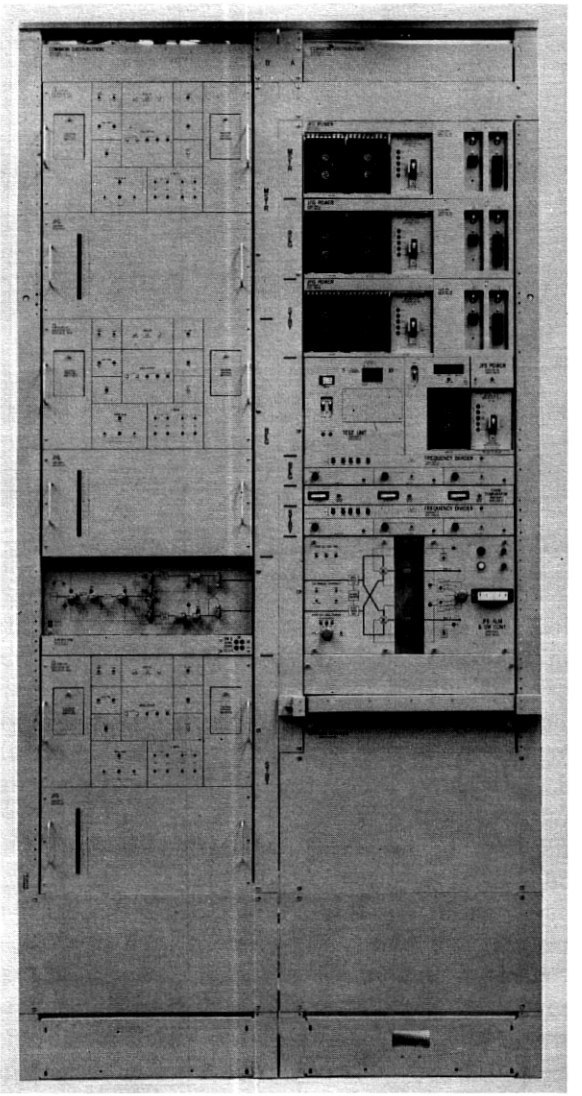

Fig. 2—Jumbogroup frequency supply bay.

both sides of the JMX. A phase comparator is provided to compare the phases of signals from the regular and standby dividers; this enables the craftsperson to manually transfer output signals from the regular JFG to the standby JFG with minimal disturbance.

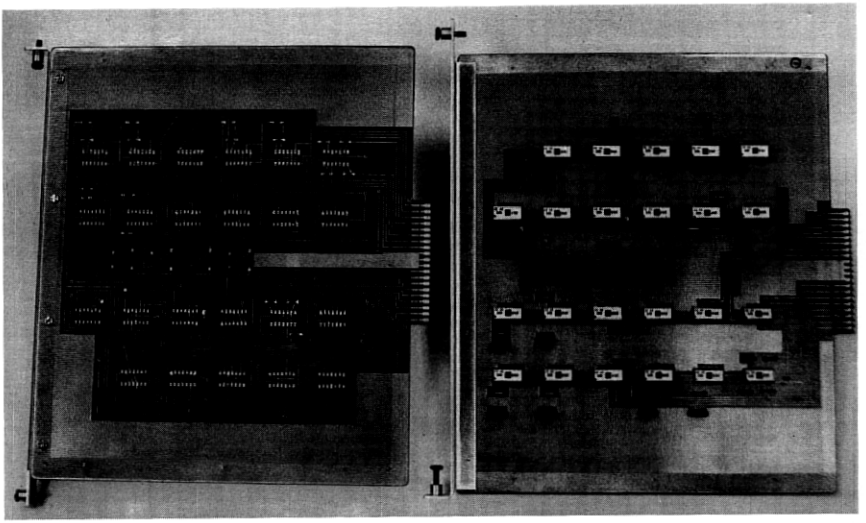

Fig. 3—Typical printed-wiring board for jumbogroup frequency supply.

Several features have been included in the JFS to facilitate trouble-shooting and maintenance. A precision frequency-measuring test unit has been designed and incorporated as a part of the JFS. A patch panel has been included to provide a convenient and non-service-affecting way to rearrange the remaining JFG's if a JFG fails. Several test points and a level meter have been provided. The coaxial switches can be patched around without affecting service; the alarm and switch control circuit could then be exercised for routine checkup of the coaxial switches and control circuitry.

The JFS is shown in Fig. 2 in a double 9-foot bay. A 7-foot-bay arrangement is also available. At the top of each side is a distribution bus; these buses provide 32 redundant (64 total) outputs. The three JFG's are on the left side with the master on top and below it the regular and standby JFG's with the JFG patch panel between them. Each JFG has its alarm display panel above its oscillator panel on which the 14 bits of the oscillator frequency-control word are displayed. On the right side, from top to bottom, are shown: three sets of dc-dc converters, test unit and associated dc-dc converters, regular frequency divider, phase comparator, standby frequency divider, and alarm and switch control unit.

Most of the JFS circuitry consists of digital integrated circuits (IC's) and various discrete components mounted on two- or four-layer

printed-wiring boards. Additional apparatus such as thin-film, hybrid, integrated-circuit amplifiers and crystal filters are also employed.

The wide use of digital IC's in the JFS made it possible to achieve sophisticated control and alarm functions that would be impractical with discrete components. Western Electric-manufactured 101-type emitter-coupled logic (ECL) was chosen for reasons of speed and availability. Since only small-scale integration (SSI) members of this logic family were available during the JFS design phase, a large number of "chips" was necessary to implement all JFS functions—about 1100 logic chips in a full JFS. A typical two-sided printed-wiring board is shown in Fig. 3.

The JFG is discussed in detail in the next section. The frequency divider, protection switching, and test unit are discussed in the succeeding sections.

## III. JUMBOGROUP FREQUENCY GENERATOR

### 3.1 General description

The JFG produces an accurate 20.48-MHz sinusoidal output signal with a $\Delta F/F$ normally less than $1/10^{10}$ relative to its input signal. This small $\Delta F/F$ is achieved by combining an extremely stable crystal oscillator with precision frequency-control circuitry. Frequency accuracy is provided by reference to a signal whose ultimate source is the BSRFS.

The oscillator is the 39A digitally controlled crystal oscillator.[3] It has a drift rate less than $1/10^{10}$ per day, low enough to operate without correction for several weeks and still meet JFS frequency-accuracy requirements. This oscillator's frequency is controlled by a 14-parallel-bit binary-control word developed by the JFG frequency-control circuit. The control word is changed when comparison of the JFG input and output signals indicates a need to correct the oscillator frequency.

Figure 4 is a block diagram of the JFG showing the relationship between oscillator, input, output, and frequency-control circuits. The 39A digitally controlled crystal oscillator (DCXO) has a 5.12-MHz output which is multiplied to 20.48 MHz in the JFG output circuit. The 20.48-MHz input signal, after being filtered and amplified in the JFG input circuit, is compared with the 20.48-MHz output signal in the frequency-control-and-alarm circuit, which produces the frequency-control word and frequency alarms. The logic-interface circuit processes frequency, level, and voltage alarms generated within the JFG for transmission to the JFS alarm-and-switch-control circuit and for dis-

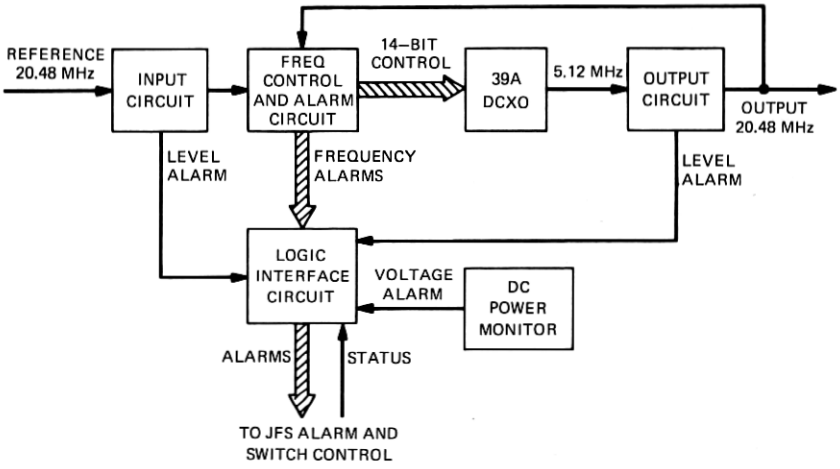


Fig. 4—Jumbogroup frequency generator.

play on the JFG itself. This alarm processing is controlled by a status input from the JFS alarm and switch control.

These frequency-control and alarm features will be described in some detail in the following sections, along with a number of other features designed to facilitate the operation and maintenance of the JFG.

### *3.2 Frequency control*

The major consideration in designing the JFG was the character of the signal supplied to the JFS as a frequency reference. As mentioned earlier, this signal could be intermittent, noisy, or absent due to transmission difficulties. Furthermore, at the time of JFG development, the proposed reference-signal-transmission path contained phase-locked oscillators that could introduce frequency offsets as great as several parts in $10^6$ if they lost phase-lock. These phase-locked oscillators were not used in the final BSRFS distribution network. Because of these reference transmission difficulties, the JFG was designed to rely on only one characteristic of the reference signal—its average frequency as measured during times of good transmission.

The low drift rate of the 39A DCXO allows a JFG to ignore the reference during times of poor transmission. Although this drift rate is low, it is not zero and cannot be ignored. In the JFG the DCXO frequency-control word is held constant until the average of a large number (256 minimum) of short (16 seconds), valid frequency comparisons

between input and output signals indicates a frequency offset greater than $1/10^{10}$. Then the control word is changed to move the DCXO frequency $2/10^{10}$ in a direction opposite to the offset. This frequency-control operation can be separated into three functions: frequency-offset detection, averaging, and frequency correction.

#### *3.2.1 Frequency-offset detection*

Figure 5 shows, in general terms, the basic portion of the circuit by which the JFG detects small values of $\Delta F/F$ between two frequencies $A$ and $P$. In the first portion of this circuit, divider $D$ and the two mixer-bandpass filter circuits develop a frequency $A/D + \Delta F$. The final portion of the circuit consists of a frequency divider $N$ whose output controls a gate, allowing the frequency $A$ to be counted for one gate period, resulting in the count $C$. $C_o$ is the count when $\Delta F = O$. The count $\Delta C$ contains the $\Delta F/F$ information obtained in the time $T$.

Implementation of this circuit involves the selection of values for $D$ and $N$ and the number of stages in the counter. To maximize the $\Delta C/T$ ratio, $D$ is made as large as possible within the constraints imposed by the bandpass filter requirements and the short-term frequency stability of the signals. In the JFG, $D = 320$; hence, $A/D = 64$ kHz. $N$ is selected to provide the necessary precision ($\Delta C$) in a reasonable time ($T$). $N$ is also considered in the counter design. A counter large enough to count to $C$ would be larger than necessary. In the JFG frequency-control circuit the largest $\Delta F/F$ that must be measured by the counter is $1/10^8$; this limits $\Delta C$. If one selects $N$ and the number of

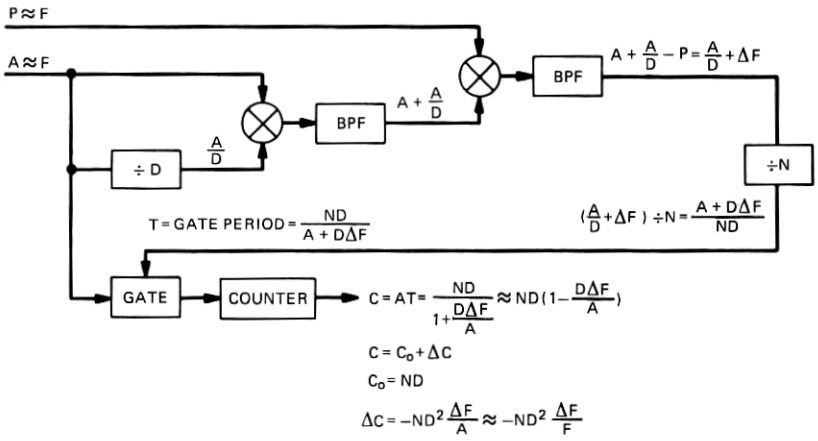


Fig. 5—Frequency-offset detection.

counter stages so that after multiple overflowings $C_o$ leaves a remaining count of all zeros, the number of counter stages need only be sufficient to detect the sense and magnitude of $\Delta C$. In the JFG, $N = 2^{20}$ and the counter has 19 stages. This results in a circuit capable of detecting sense and magnitude of frequency offsets in the $1/10^{11}$ to $2/10^{6}$ range.

Figure 6 shows the application of this circuit in the JFG. During the 16.384-second gate period provided by GATE 1, the COUNT signal (the JFG output frequency) is counted. At the end of that period, $\Delta C$ is examined and if it indicates a $\Delta F/F > 1/10^{10}$, high or low, a pulse is sent to the high or low input of the ACCUMULATOR. The INHIBIT 2 signal will interrupt this process and reset the circuit should other, quicker-acting circuits determine that the frequency comparison is not acceptable for frequency control.

#### 3.2.2 Measurement averaging

Averaging of the results of the 16.384-second frequency comparisons is done in the ACCUMULATOR. This circuit is a nine-stage up-down binary counter. Starting from its midrange, or reset, position, this counter counts up or down depending on the sense of $\Delta F/F$. When this counter has received 256 more pulses in one direction than in the other, it sends two pulses to the MEMORY by way of the FREQ CONT MODE SELECTOR.

#### 3.2.3 Frequency correction

The normal position of the FREQ CONT MODE SELECTOR will connect the ACCUMULATOR to the MEMORY. The MEMORY provides the 14-bit frequency-control word to the 39A DCXO. In the 39A a $D/A$ converter plus varactor diode circuit provide a linear relationship between oscillator frequency and digital control word. The least significant bit (LSB) of the control word corresponds to $\Delta F/F = 5/10^{11}$; so the 14-bit word provides a frequency-control range of $\pm 4/10^{7}$. The MEMORY keeps the LSB at 0 and increases the higher bits by one for each pulse it receives. Thus, the two pulses from the ACCUMULATOR result in a $2/10^{10}$ frequency change.

The maximum correction rate of the frequency-control circuit is $2/10^{10}$ per 256 frequency comparisons made at a rate of one every 20.48 seconds; this converts to $3.4/10^{9}$ per day.

### 3.3 Frequency alarms

Figure 6 shows a number of frequency alarms being generated. The circuits generating these alarms are interconnected to utilize the inverse relation between the value of $\Delta F/F$ and the time needed to detect it.

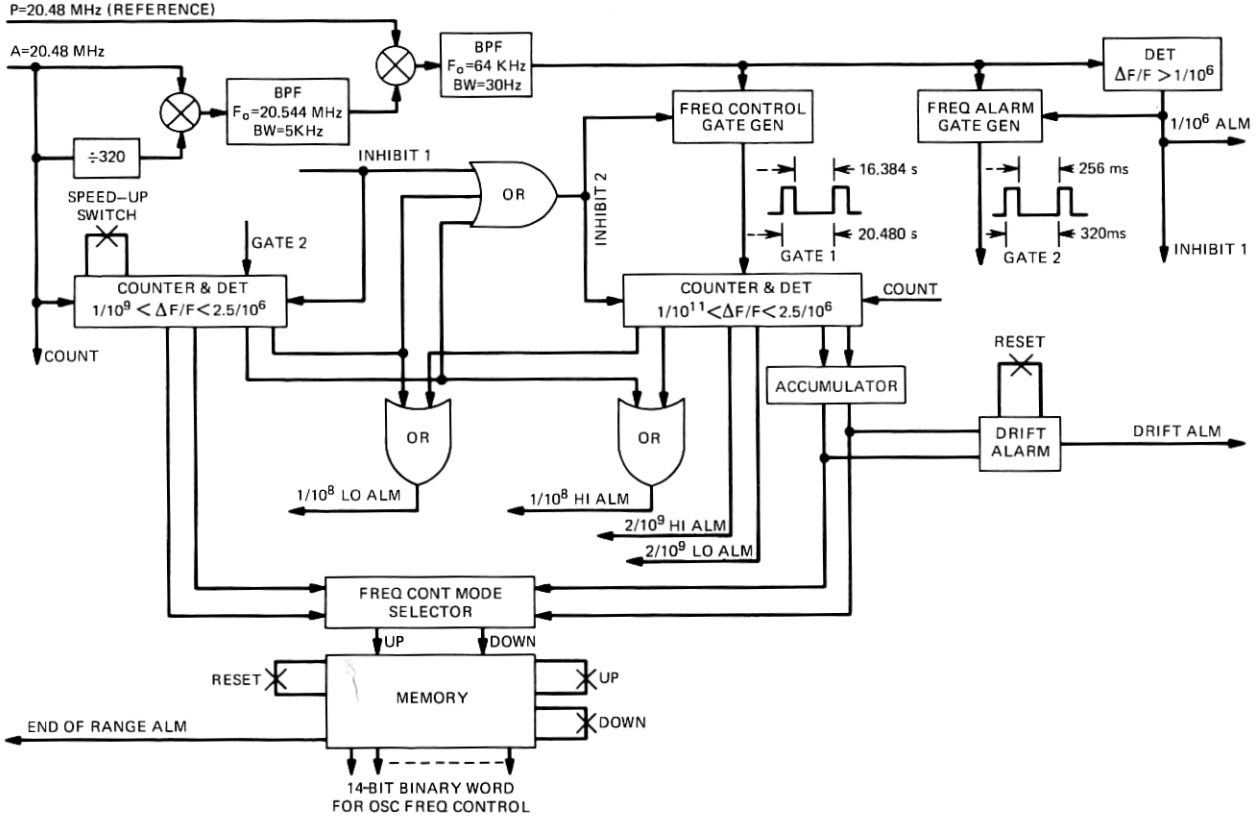


Fig. 6—Frequency-control-and-alarm circuit.

#### 3.3.1 $1/10^6$ alarm

This is the coarsest frequency alarm and utilizes the 30-Hz bandwidth of the 64-kHz bandpass filter. At the output of this filter a $\Delta F$ of 15 Hz or greater causes a 3-dB or greater drop in signal level. This drop corresponds to a $\Delta F/F$ of $7.5/10^7$ or greater. A level-detector circuit, DET, detects this and produces the $1/10^6$ ALM and INHIBIT 1 signals. (The $1/10^6$ designation is nominal.)

#### 3.3.2 $1/10^8$ alarms

GATE 2 is called the frequency-alarm gate, and the circuits generating it and using it comprise the frequency-alarm circuit. This circuit uses the frequency offset detection scheme shown in Fig. 5. $N = 2^{14}$ and the counter has 12 stages; so the circuit has a range from $1/10^9$ to $2.5/10^6$. The INHIBIT 1 signal interrupts and resets this circuit which makes a $\Delta F/F$ measurement every 320 ms. The main function of this circuit is to produce the $1/10^8$ HI ALM and $1/10^8$ LO ALM and shut down the frequency-control circuit when $\Delta F/F > 1/10^8$.

Since the counter used in the frequency-control circuit can detect $1/10^8$ offsets, it is also used to produce the $1/10^8$ HI ALM and $1/10^8$ LO ALM. This provides protection in case of frequency-alarm-circuit failure.

#### 3.3.3 $2/10^9$ alarms

The $2/10^9$ HI and LO alarms are produced in the frequency-control circuit. These alarms alert maintenance personnel to problems before they affect service.

#### 3.3.4 Drift alarm

A frequency drift less than $3.4/10^9$ per day can be compensated for in the JFG. An oscillator with a drift rate greater than $3.4/10^9$ per day will eventually produce a frequency alarm. An oscillator with a lower drift rate will not cause such an alarm and no action would be taken until the oscillator reached the end of its control range and had to be replaced. The DRIFT ALARM forestalls this. The DRIFT ALARM circuit notes each frequency-correction pulse from the ACCUMULATOR, and generates the DRIFT ALM signal when the MEMORY has received 64 more pulses in one direction than in the other. The DRIFT ALM signal notifies maintenance personnel, who manually reset the circuit and record the alarm. The record of DRIFT ALM times and oscillator frequency-control words indicates oscillator drift rate.

#### 3.3.5 End of range alarm

If the oscillator is at the end of its control range; i.e., its control word is all ones or all zeros, the MEMORY produces the END OF RANGE ALM and inhibits itself from further changes. The oscillator must then be replaced. However, long before this happens, maintenance personnel should have predicted it from the drift-alarm records.

### 3.4 Operational features of the JFG

Most functions within the JFG are automatic, but installation and maintenance operations must be performed manually. The JFG design has tried to facilitate these operations.

#### 3.4.1 Rapid correction of frequency

At time of installation, or following a loss of power, the oscillator frequency might need to be changed so much that the $3.4/10^9$ per day rate would be far too slow. Shown in Figs. 6 and 7 are three features to provide more rapid frequency correction. First, there is the MEM RST switch which can put the frequency control word in its midrange position. Second, there are the $1/10^{10}$ UP and DOWN switches which change the oscillator frequency by $1/10^{10}$ with each operation. Third, there is the speed-up circuit which uses the 320-ms period of the

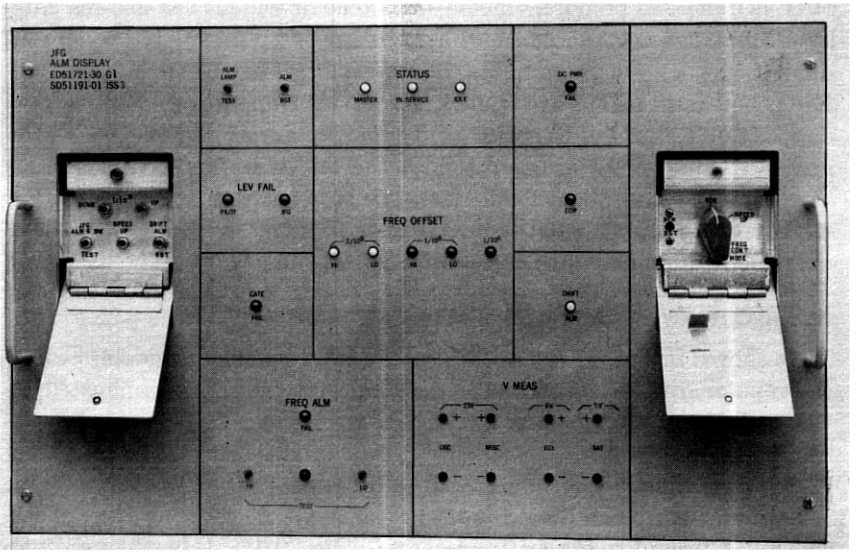


Fig. 7—Alarm-display panel for jumbogroup frequency generator.

frequency-alarm circuit to correct the oscillator at a $6/10^{10}$ per second rate. To operate the speed-up circuit, the FREQ CONT MODE switch is moved from the NOR to SPEED-UP position and then the SPEED-UP pushbutton switch is operated. The frequency-alarm circuit automatically stops sending pulses to the MEMORY when the $\Delta F/F$ is reduced below $1/10^9$. Figure 7 shows that all these controls are located behind covers to forestall their misuse. Note the angle bracket on the cover of the FREQ CONT MODE switch; this bracket forces one to return the switch to its NOR position before the cover can be closed.

#### 3.4.2 Alarm lock-up

Intermittent alarms have always been the bane of maintenance personnel. In the JFG, alarm indications are held until they can be noted or until their cause has been corrected, whichever comes later. Figure 7 shows the ALM RST switch which will extinguish an alarm lamp if the trouble has gone. If the trouble still exists, the lamp cannot be extinguished. An exception to this lock-up is that all alarms associated with the JFS reference signal do not lock up.

#### 3.4.3 Frequency alarm test

A failure of the frequency-alarm circuit could go unnoticed. The JFG provides a simple way of checking this. Operation of the FREQ ALM TEST switches, HI or LO, artificially shortens or widens the 256-ms gate by 1.6 ms, causing the effect of a $1/10^8$ HI or LO offset. If the circuit detects this, a green lamp lights; if it does not, the red FAIL lamp lights. No other indications are generated in this operation. But if one desires to check the interaction of this alarm circuit and the JFS alarm and switching circuits, operation of the JFS ALM & SW TEST switch (see Fig. 7) simultaneously with the HI or LO switch will allow $1/10^8$ alarms to be transmitted from the JFG to the JFS. Note that these operations do not disturb the JFG output frequency.

## IV. FREQUENCY DIVIDER AND PHASE COMPARATOR

As shown in Fig. 1, the JFS contains two frequency dividers. Called the regular divider and standby divider, these units are connected to the outputs of the regular JFG and standby JFG, respectively. Each frequency divider provides as an output 1.024-MHz, 2.56-MHz, and 20.48-MHz signals multiplexed onto one coaxial cable.

Figure 8 is a block diagram of the basic circuit showing that phase control is provided for all frequencies. The 20.48-MHz phase-adjust networks provide a 180-degree control range. The fine phase adjust-

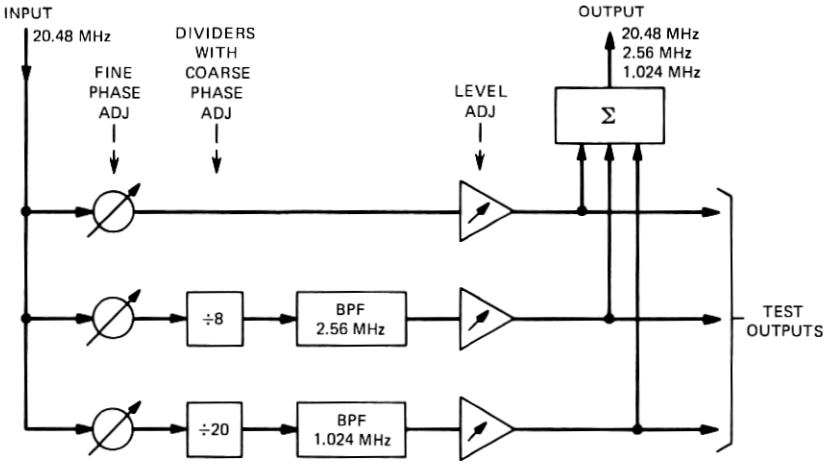


Fig. 8—Frequency divider.

ment for the 1.024-MHz and 2.56-MHz output signals is done at 20.48 MHz to avoid component problems associated with lower-frequency-phase-adjust networks. The 180-degree phase adjust at 20.48 MHz yields 22.5 degrees at 2.56 MHz and 9 degrees at 1.024 MHz. Coarse-phase-adjust circuits are included in the two dividers to increase the range of phase adjustment at the two lower frequencies. Each divider skips a single input pulse for each push of its associated pushbutton, thus producing a step change in its output phase. From each divider, the test outputs, shown in Fig. 8, are connected to the phase-comparator panel, which provides one meter for each frequency. A meter null is an indication of phase coincidence. All three meters must be nulled to indicate that the signals from the two dividers are in phase. In adjusting phase to produce these nulls, the coarse-phase adjust of the in-service divider should not be used.

## V. PROTECTION SWITCHING

### *5.1 General description*

Protection switching plays a vital role in ensuring the continuity of JFS output signals. Figure 9 shows the switching arrangement; the switches are fabricated with coaxial, dry-reed contacts. The normally closed contacts of these switches are magnetically biased so there is no need for switch coil current while the switch is released. Since the switch is normally released, a loss of switch power will normally not affect the JFS output signal. As shown in Fig. 9, with the switches

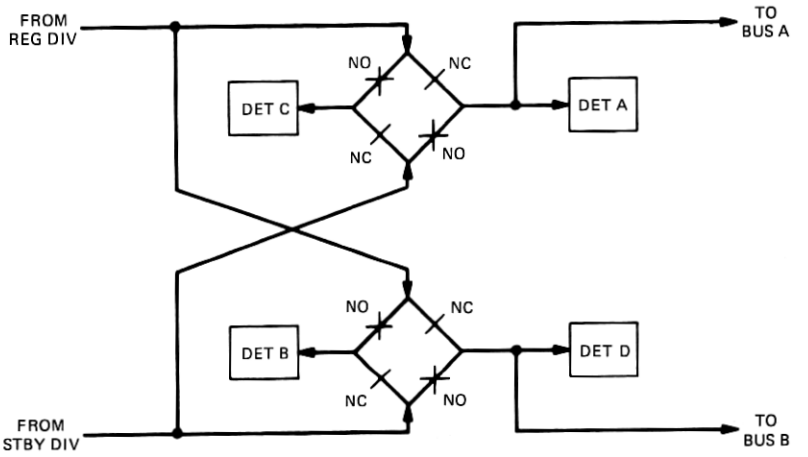


Fig. 9—Protection switch and level detectors.

released, the regular divider feeds detectors A and D and output buses A and B, while the standby divider feeds detectors B and C. When the switches are operated, the standby divider feeds detectors A and D and output buses A and B, while the regular divider feeds detectors B and C.

The switch-control circuit energizes (to operate) or deenergizes (to release) the switch coils in a "make before break" sequence. This feature has little importance if the switching is being done automatically due to a signal fault. However, if the switching is being done manually for any nonemergency reason, the switch input signals can be adjusted to be of equal phase and level; this combined with the "make before break" feature minimizes perturbations of the JFS output signal caused by nonemergency switch operation.

### *5.2 Manual control*

Manual control is provided in the JFS alarm-and-switch-control panel by means of pushbuttons. Accidental manual switching is prevented by requiring multiple simultaneous pushbutton operations for switching. It is possible to override automatic-switch-control signals manually.

### *5.3 Automatic control*

The alarms received from the four level detectors (Fig. 9) and the JFG's are processed by the switch-control circuit, which sends a com-

mand to the switches if an automatic switch is warranted. The switch will operate if detector A or D indicates an unusual change in signal level or if the regular JFG indicates it is impaired sufficiently to require being switched out of service. Should detector B or C indicate an unusual change in signal level or the standby JFG indicate it is impaired, switch operation will be inhibited.

### *5.4 Manual rearrangement*

If a JFG failure occurs, the JFS may have to operate for some time with only two JFG's. Patching facilities are provided for restructuring the JFG interconnections (Fig. 10). For example, if the master JFG fails, the standby JFG temporarily serves the master JFG function. The alarm-and-switch-control circuit must be modified to recognize the new arrangement. This modification is achieved by selecting a position on a rotary switch corresponding to the new arrangement, and then operating an associated pushbutton switch. Because the JFS can function for some time with only two JFG's, the JFG is spared on a regional rather than a per-office basis. For most of the other units in the JFS, spares are included either in the JFS itself or in each office.

A jack-and-patch-plug arrangement has been provided in the alarm-and-switch-control panel so that the JFS output signals can be routed around the coaxial switches. Using this arrangement to take the switches out of service produces small phase and amplitude "hits" on

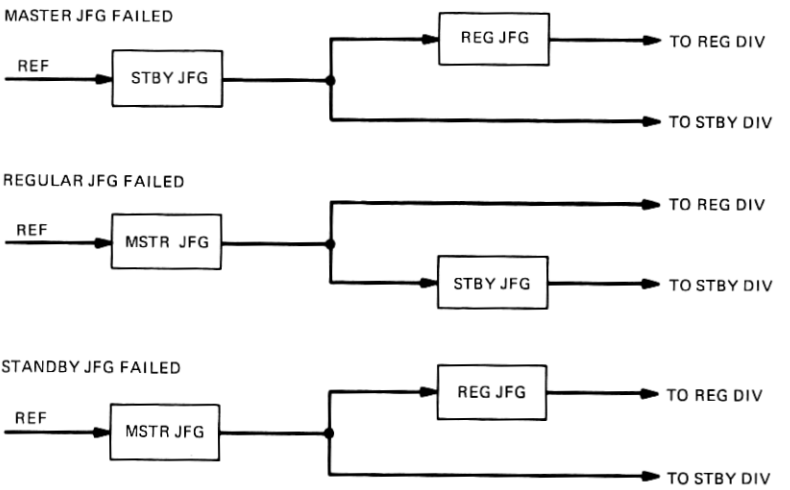


Fig. 10—Jumbogroup frequency supply operation using two jumbogroup frequency generators.

the JFS output signals. When the patching operation has been completed, the signal through the patched path is within 2 degrees and 0.2 dB of what it had been through the switch path.

A rotary-switch-and-power-meter arrangement has been provided on the alarm-and-switch-control panel to enable the craftsperson to read the level of each frequency (1.024, 2.56, and 20.48 MHz) at detectors A and B shown in Fig. 9.

## VI. TEST UNIT

The JFS incorporates a test unit to measure small frequency offsets, since a typical office does not have precision-frequency-measuring equipment.

The test unit can compare two frequencies of approximately 20.48 MHz, and display on numeric indicators the fractional frequency offset in parts in $10^{10}$ or $10^{11}$. The test unit has two modes of operation, either of which can be selected by a switch on the front of the panel. The 6 SEC, or normal, mode measures frequency differences of parts in $10^{10}$. The 30 SEC, or extended precision, mode measures frequency differences of parts in $10^{11}$. The frequency-offset information is displayed on LED numeric readouts.

Signals to be compared must have a level greater than $-30$ dBm into 75 ohms, and the frequency difference must be less than one part in $10^6$. If either of these conditions is not met, the OUT OF RANGE indicator will light, and the test unit will not operate. The COUNTING indicator is lit while the test unit is counting. When the COUNTING indicator goes off, information is transferred from the counter to the numeric readouts. After approximately six seconds, a new count is taken.

The internal functions of the test unit can be divided into three sections: gate generator, counter, and display. The gate generator provides a gate whose period is a function of $\Delta F$, the frequency difference between the two input signals. In the counter, the duration of the gate is measured by counting proportional to the fractional frequency offset ($\Delta F/F$). This is similar to the frequency-offset-detection technique used in the JFG. The information in the detection counters is transferred to a digital display unit.

## VII. CONCLUSION

The first JFS production unit was shipped from the factory in June 1973. There are presently more than ten JFS bays installed at L5 main

stations. The operational performance of these units has been excellent, and they have met all of their design objectives.

The availability of these accurate and reliable frequency supplies has stimulated the modernization of the entire Bell System synchronization network.[4] Beginning in 1974, the United States will be divided into approximately twenty synchronization regions, and telephone offices in each region will receive their synchronization signals from a regional frequency supply (RFS). Certain L5 main stations will become regional sync centers, with the L5 JFS serving as the RFS and providing 64-kHz and 512-kHz sync signals to telephone offices in its region. In areas where no L5 facility exists, a special two-JFG version of the JFS will serve as the RFS. Thus, the entire frequency-division multiplex plant, including both radio and coaxial transmission systems, will soon be synchronized through JFS equipment.

In addition to serving L5 and the Bell System synchronization network, the JFS has sufficient frequency precision to serve future systems having ten times the bandwidth of L5.

## VIII. ACKNOWLEDGMENTS

The authors acknowledge the many contributions of R. E. Benjamin to the JFS development; he has been involved with the JFS since its inception. Several others contributed to the development of the JFS, in particular, W. W. Brown, L. J. Finelli, D. A. Lane, W. G. Albert, D. M. Pierce, and W. C. Schmidt. Special mention is due W. L. Smith and H. S. Pustarfi whose expertise in the field of precision frequency sources led to the development of the 39A oscillator.

## REFERENCES

1. R. E. Maurer, "L5 System: Jumbogroup Multiplex Terminal," B.S.T.J., this issue, pp. 2065–2096.
2. J. F. Oberst, "Keeping Bell System Frequencies on the Beam," Bell Laboratories Record, *52*, No. 3 (March 1974), pp. 84–89.
3. A. F. Flint and H. S. Pustarfi, "L5 System: 39A Precision Oscillator," B.S.T.J., this issue, pp. 2097–2107.
4. R. E. Powers, "Reference Frequency Transmission Over Bell System Radio and Coaxial Facilities," Proc. of 28th Annual Frequency Control Symposium, Fort Monmouth, N.J., U.S. Army Electronics Laboratories, May 29–31, 1974.