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A Doped Surface Two-Phase CCD

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The successful operation of an n-channel two-phase charge-coupled device has been achieved. The asymmetry in the surface potential profile necessary to force the charge to move unidirectionally was obtained by ion implanting a nonuniform doping distribution in the Si substrate under each gate. An eight-stage shift register with a length per stage of 80 μm was made, and was operated as both a digital and an analog device. There are two ways to clock the device. Either both clock lines are driven with square waves, out of phase by one half of a period, or one clock is held at a fixed DC potential while the other is driven with a square wave. Using the latter method, the charge transfer efficiency was better than 99.9 percent per transfer over the clock frequency range of 10^3 Hz to 6.5 × 10^6 Hz.

I. INTRODUCTION

In a charge-coupled device, as described by Boyle and Smith,[1] charge moves successively from the semiconductor region under a given electrode to the region under the next electrode. For information to be transferred from one end of the resulting shift register to the other, it is necessary that the charge always move in the same direction. Until now, the way this directionality has been typically achieved is by the use of three or more clock lines.[2-4] In this type of structure, when charge is transferred from one electrode to the next, the electrode behind the one transferring charge is kept at a potential which repels the free charge and thereby prevents backward flow. The electrode to receive charge, meanwhile, is made more attractive to charge than the one giving up its charge. It can be seen that this arrangement requires three electrodes (at least) for each packet of charge and that each one must be driven by a different clock line.

The use of three clock lines (as opposed to two) has significant topological disadvantages because with three clock lines there must be crossovers. These have been fabricated by a diffusion into the semiconductor surface.[2] This diffusion must be contacted once for every bit which is undesirable from the standpoint of yield and packing density.

This problem is exacerbated when connection is made to a three-phase shift register in a serpentine layout. Since the serpentine layout typically provides the most compact register, the three-phase device is normally limited to applications in which a straight layout is permissible, as for example, in an imaging device.

The serpentining problem can be overcome if a CCD with four clock lines is employed;[3,4] however, this device requires two layers of metallization, and fabrication problems may occur due to the present state of development of that technology.

In view of these difficulties, the fabrication of a two-phase CCD is considered an important goal in the development of charge-coupled devices; it requires no crossovers, utilizes only one layer of metallization, and can be easily laid out in a serpentine configuration.

The design, fabrication and operation of a simple eight-bit two-phase shift register will be discussed in the following three sections of this paper. A final section is devoted to conclusions.

II. DEVICE DESIGN

In a two-phase CCD, when an electrode is giving up its charge, both adjacent electrodes are biased to attract that charge. Moreover, they must be equally attractive to the charge because every other electrode is tied together; consequently, directionality must be achieved by associating a potential barrier with each electrode. The directional transfer imposed by such a barrier is shown schematically in Fig. 1. The potential barrier near the left end of the region under each electrode prevents backward flow of charge. While its asymmetrical location under the electrode is important, the shape of the barrier is not critical in determining whether charge flow will be directional or not, but higher speed would be expected if the right side of the barrier is sloped to encourage charge flow in the forward direction.

The desired surface potential barrier can be obtained by implanting into the p-type silicon substrate a shallow layer of boron ions in a narrow stripe geometry as shown in Fig. 2. Charge-coupled device operation requires that the entire region under each gate be in deep depletion, so the boron implant must be light enough to be totally ionized and depleted. The resulting negative charge layer assures that, for a given value of applied voltage V_A, the surface potential, φ_s, has a lower value in the implanted region than in the unimplanted region. The height of the potential barrier $\Delta\varphi_s$ is simply the difference between these values.

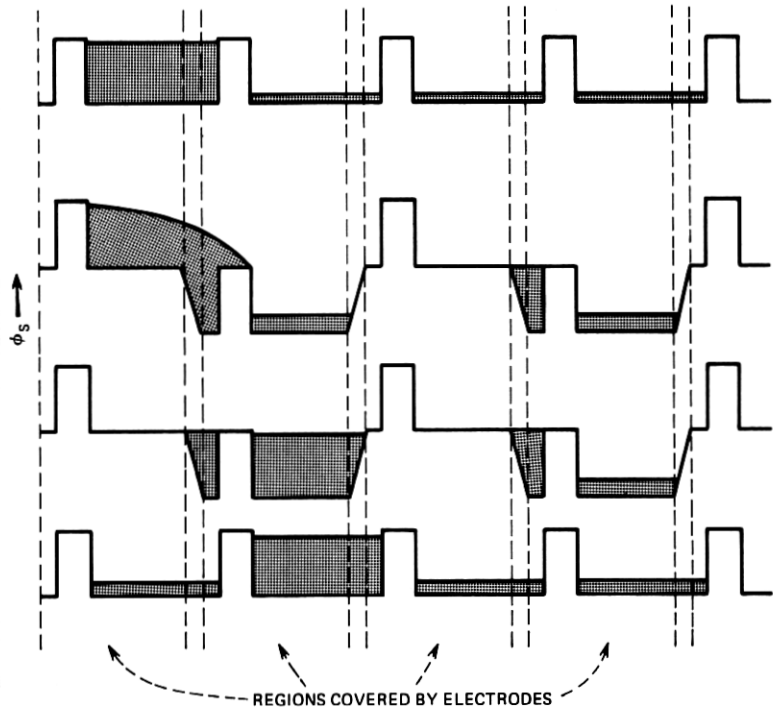

Fig. 1—Sequence of plots of surface potential vs position with free carrier density shown cross hatched. The height of the barrier is typically ~5V. One complete transfer is shown.

A one-dimensional solution of Poisson's equation can be obtained to give ϕ_s as a function of V_A for the deep depletion condition. It is assumed here that the doping profile is characterized by a constant density N_{A1} highly doped region to a well defined depth x_1, and the background density, N_{A2} (see Fig. 3). This approximate profile is sufficient to show the major consequences of a shallow charge layer. The results of the calculations are

$$V_A - V_{FB} = \varphi_s + V_1\left(\frac{\varphi_s}{\varphi_{s1}}\right)^{\frac{1}{2}}, \qquad x_d \leqq x_1$$

$$V_A - V_{FB} = \varphi_s + V_1 - V_2\left\{1 - \sqrt{1 + \frac{N_{A1}}{N_{A2}}\left(\frac{\varphi_s}{\varphi_{s1}} - 1\right)}\right\}, \qquad x_d \geqq x_1 \qquad (1)$$

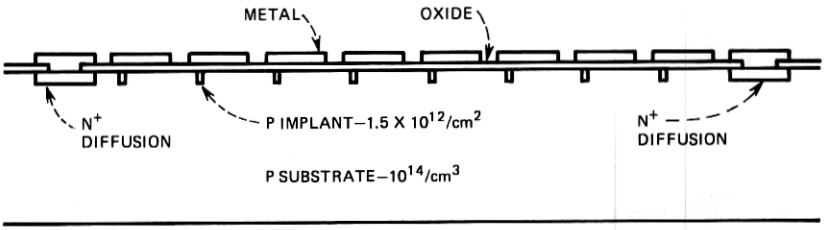

Fig. 2—Cross section of the two-phase charge-coupled device which was fabricated (the actual device made has 8 bits, only 4 are shown here).

where V_{FB} is the flat-band voltage and

$$V_1 = \frac{ex_1\, dN_{A1}}{\epsilon_{ox}}$$

$$V_2 = \frac{ex_1\, dN_{A2}}{\epsilon_{ox}}$$

$$\varphi_{s1} = \frac{ex_1^2 N_{A1}}{2\epsilon_s}$$

where ϵ_s and ϵ_{ox} are the permittivities of the Si substrate and the SiO_2 film respectively and d is the SiO_2 thickness.

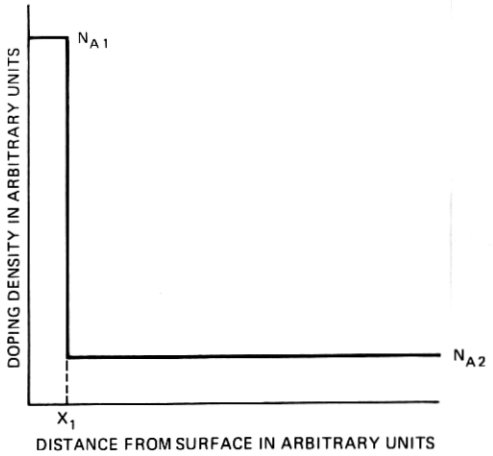

Fig. 3—Doping density vs distance from semiconductor surface.

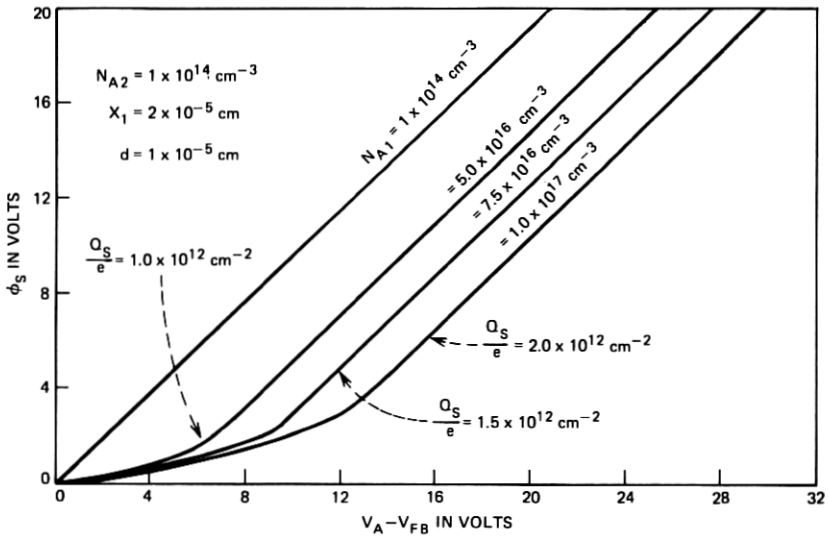

Fig. 4—Curves of surface potential vs applied voltage for various values of surface doping.

The parameters φ_{s1} and V_1 are the voltage drops across the Si depletion region and SiO_2, respectively, when the depletion layer width x_d is the same as x_1. The results of eq. (1) are plotted in Fig. 4 for several values of N_{A1}; it was assumed that $N_{A2} = 1 \times 10^{14}$ cm^{-3}, $x_1 = 2 \times 10^{-5}$ cm and $d = 1 \times 10^{-5}$ cm. Each curve has two regions of distinctly different behavior: the first extends from the origin to the knee, shows φ_s varying slowly with respect to V_A, and corresponds to the condition $x_d \leqq x_1$; beyond the knee, the curve is nearly linear and corresponds to $x_d > x_1$. The point indicated on each curve corresponds to $x_d = x_1$, and the associated value of $Q_s = ex_1N_{A1}$ is the total charge per unit area in the heavily doped region.

The effect of increasing N_{A1} for a given x is to increase the height of the barrier between implanted and unimplanted regions. The barrier height also depends on applied voltage. It is zero for an applied voltage equal to the flat-band voltage, but it is essentially constant for voltages large enough to insure $x_d > x_1$. Operation with V_A dropping into the region where the barrier is lower than its maximum is permissible, even though an instantaneous decrease in V_A (and consequently V_B) during the transfer process, would permit some of the charge to flow backwards over the shrinking barrier. Actually, V_A has a finite time derivative so some charge is transferred forward before V_A reaches its minimum. This

initial transfer of charge is extremely fast. Using calculations made by Strain and Schryer[5], an n-channel device with 25μ electrodes, half of the charge is transferred in 5 ns. For a 10μ electrode, only 1 ns is required. Therefore, if the pulse generators driving the clock lines have rise times of several ns, the barrier can shrink by at least a factor of two with no loss of charge. This is because the amount of charge being held back by the barrier decreases faster than the barrier height decreases.

Typical surface potential values during operation are illustrated in Fig. 5. Two curves are shown; one is for the unimplanted region (1×10^{14} cm^{-3} p-type), and the other is for the implanted area (7.5×10^{16} cm^{-3} p-type, $x_1 = 2 \times 10^{-5}$ cm). The circled points A, B, C and D determine the operating parameters of the CCD: the peak-to-peak variation in the clock voltage is determined by the voltage difference ΔV_A between points B and C, while the potential well depth $\Delta\varphi_s$ is determined by the separation of points A and B or of C and D.

The lower value of applied voltage ($V_A - V_{FB} = 3$ volts) was chosen to make the barrier approximately half of its maximum value. The larger value of V_A($V_A - V_{FB} = 11$ volts) was chosen to make the surface potential at the top of the barrier under the receiving electrode equal to the surface potential in the unimplanted region under the

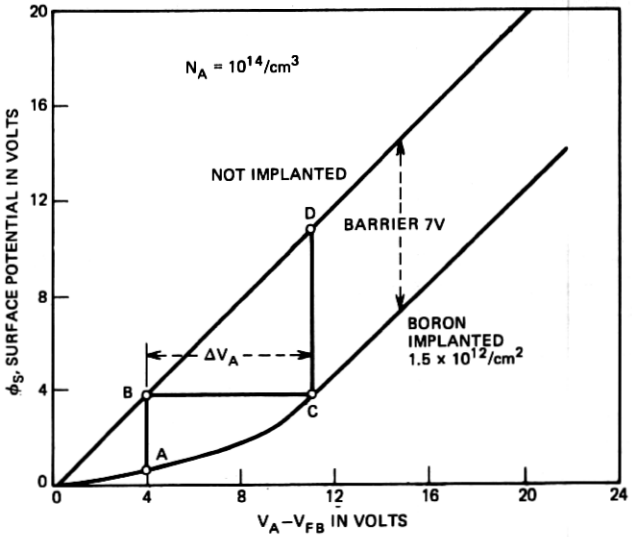

Fig. 5—Curves of surface potential vs applied voltage for both implanted and unimplanted regions (implant 7.5×10^{16}/cm^3, depth 0.2μ). Also indicated are the driving voltage used and corresponding surface potentials. These are the parameters of the device fabricated.

electrode giving up charge. Any value of $V_A - V_{FB}$ greater than 11 volts could also be used. Since these values of V_A are convenient, the values of N_{A1}, N_{A2}, and x_1 (10^{14}, 7.5×10^{16}, 2×10^{-5} cm) used for Fig. 5 were also used in the device that was fabricated.

In the design of the device, transfer across the spaces between the electrodes had to be considered also. Calculations made by Krambeck[6] have shown that for a p substrate with a doping of $10^{14}/cm^3$ and a thermally grown SiO_2 insulator, the gaps should not interfere with transfer. The interelectrode spacings were made 5μ, and the width of the electrodes was made 35μ. The implanted regions were offset from the left edges of the gates by 5μ and were 5μ wide. These parameters give a device which is practical to fabricate and is capable of moving useful amounts of charge at high rates. The construction, testing and operation of this CCD will be described in the next section.

III. EXPERIMENTAL RESULTS

3.1 *Processing*

The fabrication of the device involves five steps requiring photolithography. Four of these use standard planar processing: diffusing the input and output diodes, diffusing the channel stop, etching the contact holes and etching the metallization. The fifth photolithographic step is needed to obtain the ion implanted pattern. For this, the photoresist is used as the mask and $1.5 \times 10^{12}/cm^2$ of boron is implanted. The boron is activated with a high temperature anneal.

A photograph of a completed device is shown in Fig. 6. Along with the shift register itself, several test structures have been fabricated as well. Two MOS capacitors appear in the lower left-hand corner of the photo, one in which the entire region under the gate has been subjected to the ion implantation, and the other which is completely devoid of any implant.

3.2 *Pretest*

The MOS capacitors were used to determine the operating characteristics of the shift register. The three major measurements that are required are: (*i*) surface potential φ_s as a function of applied voltage V_A; (*ii*) generation time T_g for the buildup of an inversion layer in the Si and (*iii*) surface state density N_{ss}. The first measurement gives information regarding the height of the potential barrier, the second gives an indication of the low frequency limit of device operation, and the third relates to the charge transfer efficiency.[4]

The measurement techniques are based on the use of ramps for

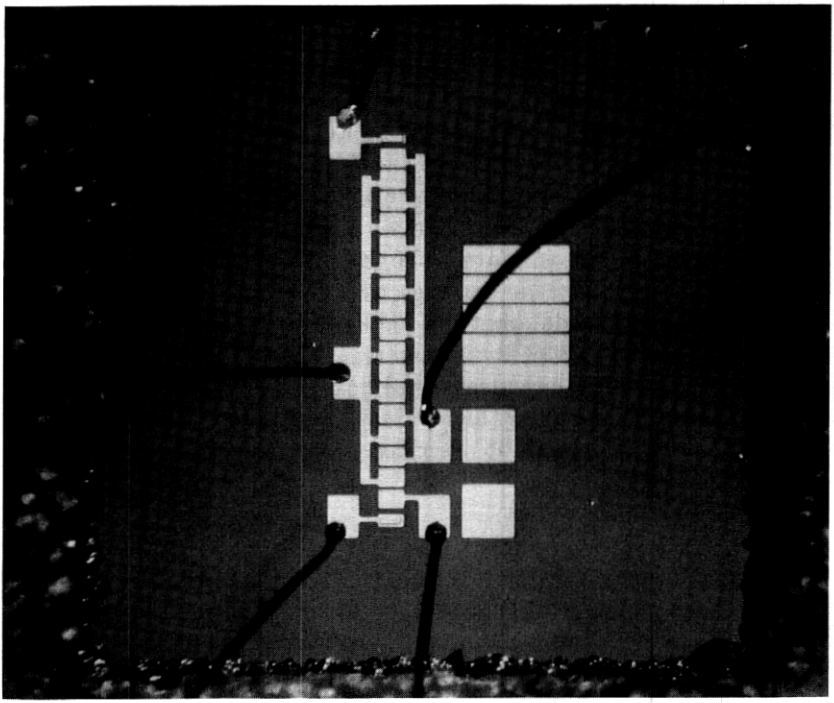

Fig. 6—Photograph of a completed device.

capacitance measurements. Surface potential as a function of applied voltage is obtained by integrating the deep depletion C-V curve as is indicated in the following equation[7]

$$\varphi_s(V_A) - \varphi_s(V_{\text{REF}}) = \int_{V_{\text{REF}}}^{V_A} \left(1 - \frac{C(V)}{C_{\text{ox}}}\right) dV \tag{2}$$

where V_{REF} is some convenient reference voltage and $C(V)$ and C_{ox} are the capacitance at some voltage V and the oxide capacitance respectively. The deep depletion C-V curve is obtained using the "fast ramp" technique[8] and the integration is done by simply operating the electrometer used to measure the displacement current as a coulombmeter. Surface potential curves for the test structures are shown in the photographs in Fig. 7. The curve in Fig. 7a is for the unimplanted sample, and that in Fig. 7b for the implanted specimen. These curves are similar in appearance to the calculated curves in Fig. 5. At large positive values of V_A, the difference in surface potential $\Delta\varphi_s$ for a given V_A is essentially constant and equal to 6.3 volts. This value for the potential barrier

height corresponds to a total implanted charge density of approximately 1.3×10^{12} cm^{-2} which is 80 percent of the original dose.

In order to obtain a value for the generation time T_g, the square wave response of the surface potential was measured. The positive-going portion of the square wave causes the MOS capacitor to be driven suddenly into deep depletion, and φ_s assumes a large value, then while the applied voltage remains at its peak value, an inversion layer builds up at the silicon surface, causing φ_s to decay toward its equilibrium level. The negative-going portion of the square wave drives the sample into accumulation, and φ_s is a constant throughout this half cycle at a level which is approximately one volt below the inversion equilibrium value. Photographs of φ_s as a function of time are displayed in Fig. 8. The response curves show the decay of φ_s followed by an abrupt change to a constant value corresponding to the accumulation condition. The signals for both capacitors to $1/e$ of their initial value in $T_g = 0.1$ s which implies a lower frequency operating limit of a few hundred Hz.

The surface state density N_{ss} in the implanted test capacitor was determined by the method of comparison of high frequency (10^6 Hz) and low frequency (quasistatic) C-V curves.[9] The derived distribution is shown in Fig. 9. As shown in the Appendix, this surface state density is too low to cause visible loss in an 8-bit CCD.

The above tests showed that while the properties of the oxide-silicon interface were not ideal, they were good enough to permit operation of the CCD. In particular, the tests of φ_s, vs V_A showed that a 6-volt potential barrier does exist between implanted and unimplanted regions under the same electrode. Also the -3-volt flat band voltage indicated that the positive charge in the oxide ($\sim 5 \times 10^{11}$/cm^2) was in the range

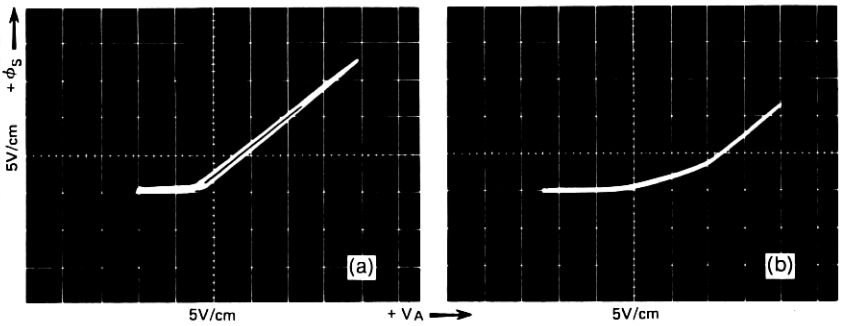

Fig. 7—Measured curves of surface potential vs applied voltage. (a) unimplanted, (b) implanted 1.5×10^{12}/cm^2 boron.

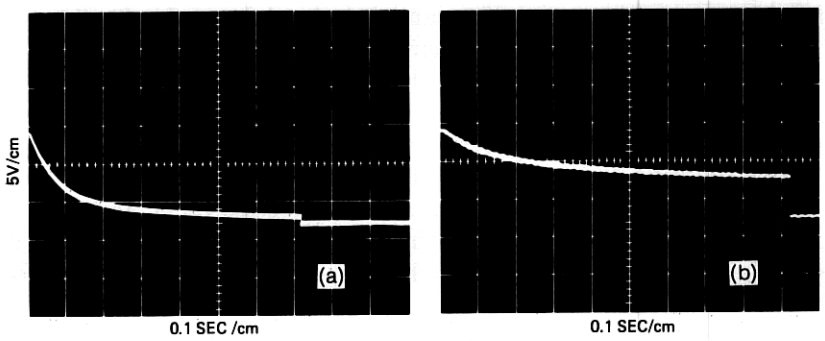

Fig. 8—Surface potential vs time after application of a step in voltage applied. (a) implanted, (b) unimplanted.

which insured transfer across the gap between electrodes.[6] The value of flat-band voltage is quite convenient since, from Fig. 5, it permits the use of 0 volt as the lower value of V_A .

3.3 *Shift Register Operation*

To find if the device actually worked as predicted, the circuit of Fig. 10 was used. This circuit includes two diodes; one at each end of the shift register. These provide a convenient way of introducing minority carriers at one end, and of removing and sensing that charge after it has passed through the entire register. The operation of the device is as follows: the two diodes are normally held in reverse bias

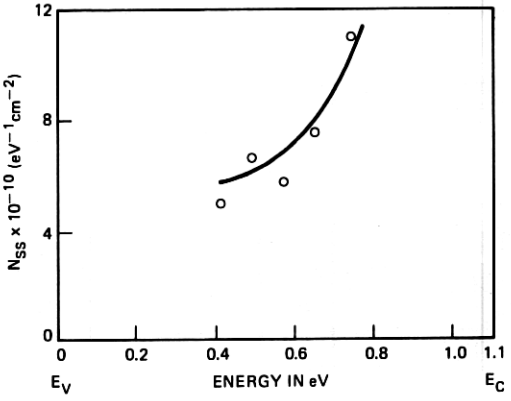

Fig. 9—Calculated values of surface state density vs position in the forbidden gap.

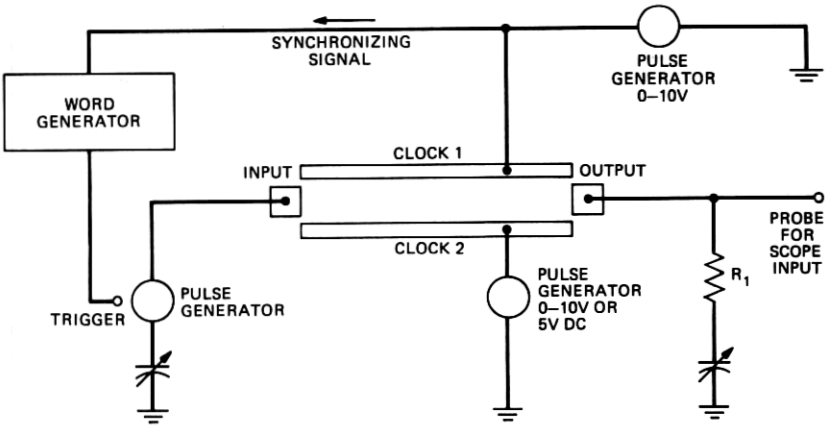

Fig. 10—Circuit used to test the device.

of about 15 volts to prevent injection of charge. The clock bias can be driven in either of two ways. These are shown in Figures 11a and 11b respectively. In one of these modes, both clock bias are driven with square waves, while in the second, only one square wave is used. This latter mode has the obvious advantage that no synchronization is necessary. The two modes give the same operation because charges move in response to differences in potential. Inspection of Figure 11a and 11b shows that the difference between voltages on the two clock lines as a function of time is essentially the same for both. As long as the input diode is held at a fixed voltage of 15 volts, no charge is injected, and ZERO's are sent through the shift register. The only output is that caused by capacitive coupling between the clock lines and the output diode pad.

To provide charge input, a negative pulse is applied to the input diode while a positive pulse is being applied to the first electrode in the shift register. Electrons will flow out of the *n*-diffusion into the region under the electrode at a rate dependent on the relative voltage between the two. The process is illustrated in Fig. 12. The surface potential under the first electrode ultimately becomes equal to that in the diode. When the negative pulse ends, any excess charge flows back into the diode. The resulting packet of charge is then transferred step by step to the other end of the shift register, and is finally transferred into the second diode when the last electrode is driven to the substrate potential. This charge changes the diode voltage by an amount dependent on the total capacitance between the diode and ground. This

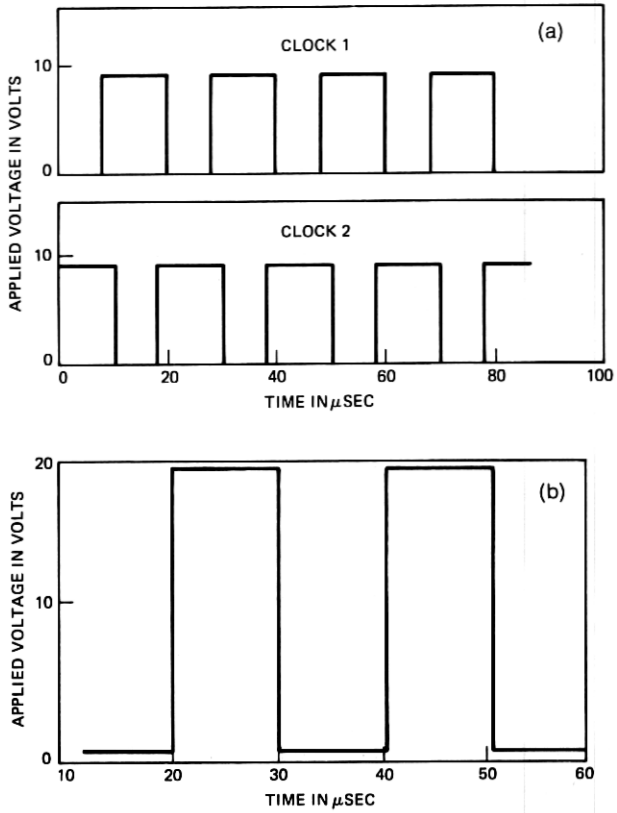

Fig. 11—Voltages used to drive the clock lines. (a) Two clock method and (b) One clock method (this was actually used to drive the device).

voltage decays to zero with a time constant dependent on the resistor R_1 in Fig. 10.

If a series of intermixed ONE's and ZERO's is fed into the shift register, the output should show a temporary voltage drop $\Delta V = Q/C$, where Q is the stored charge and C is the output capacitance. For this device, Q is determined by the activated implant density ($1.2 \times 10^{12}/\text{cm}^2$) and the area of the region which stores charge (10^{-5} cm^2). Therefore, Q is 1.9×10^{-12} coulombs and change in output voltage should be $1.9/C$ volts where C is in pF.

The results, with a clock frequency of 1.5 MHz, are shown in the top photograph in Fig. 13. The lower trace shows the pulses applied to the input diodes, and the upper trace is the output voltage. The output

swing caused by Q is 0.02 volt. It is clear that shift register action has been obtained since the output is delayed 8 cycles as it should be. This confirms the feasibility of guiding charge in a charge-coupled device by the implantation of properly chosen amounts of boron.

Measurements of transfer efficiency were carried out at several frequencies, two of which are shown in Fig. 13, and the results are shown in Fig. 14. The loss is too small to measure at 6.5 MHz, and it is estimated that a loss of 0.1 percent per transfer. Thus the loss increases from less than 0.1 percent per transfer below 6.5 MHz to 2 percent per transfer at 17 MHz.

So far the device has only been discussed as a digital shift register. However, intermediate amounts of charge may also be injected to demonstrate operation as an analog shift register. To accomplish this,

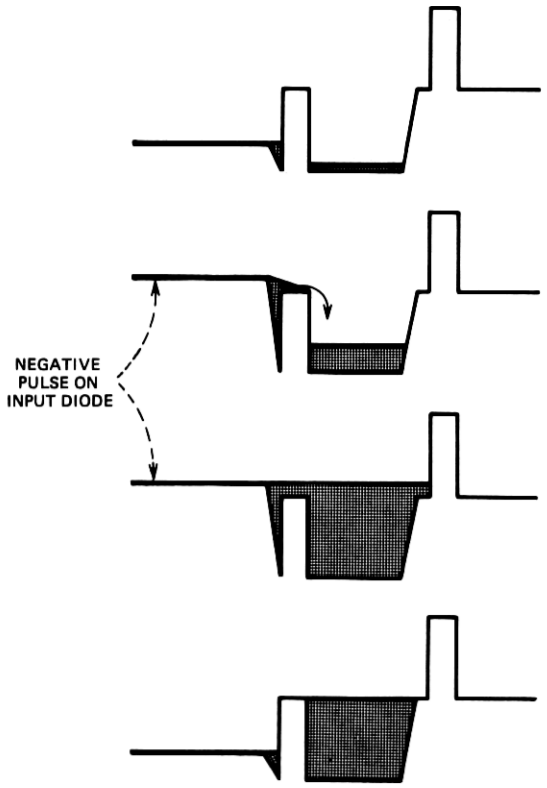

Fig. 12—Surface potential at input of shift register during injection of charge.

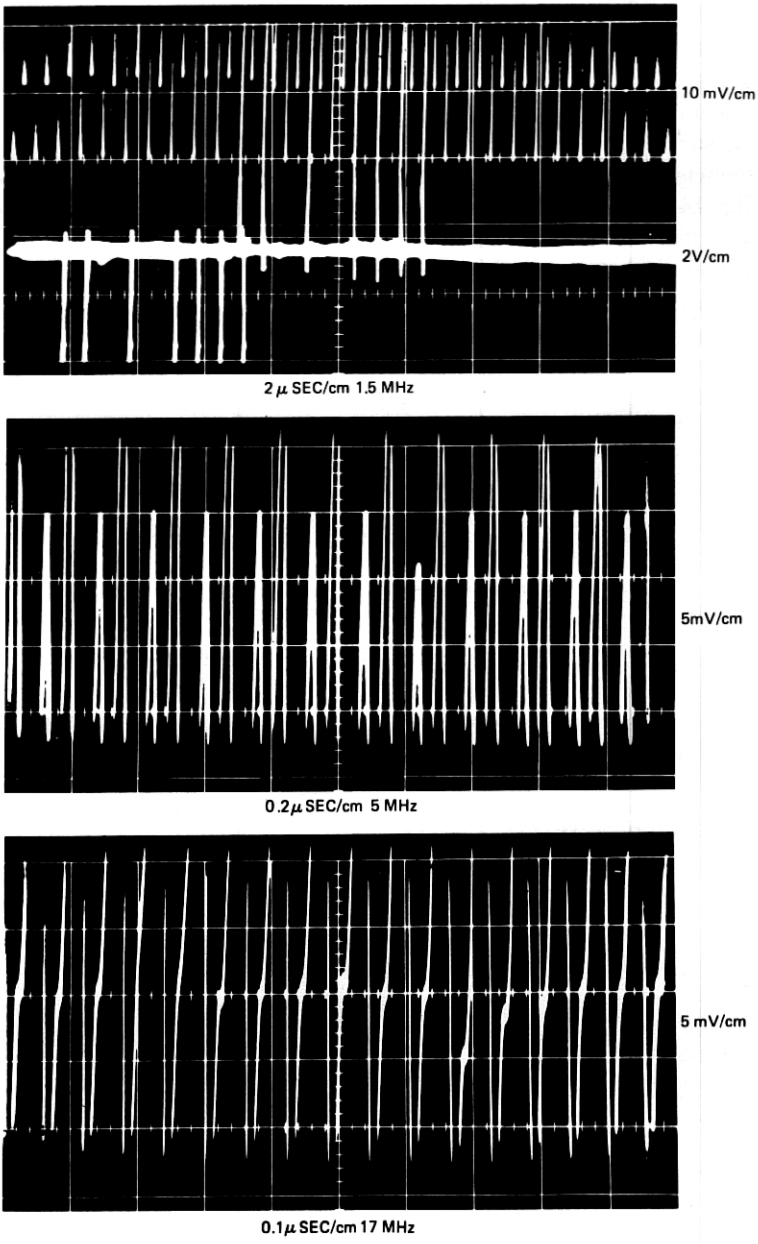

Fig. 13—Top photo: Input (lower trace) and output (upper trace) during operation of the shift register at 1.5 MHz. Middle and lower photos are output of a single ONE at 5MHz and 17 MHz respectively.

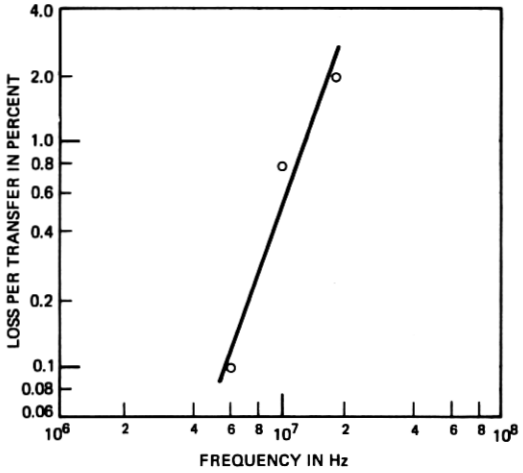

Fig. 14—Loss per transfer vs frequency (measured).

it is necessary to modulate the height of the input pulses so the rate of charge flow and the total amount of charge injected during each cycle have values between those previously used. This modulation was accomplished by placing a ramp generator in parallel with the input pulse generator. The resulting input waveform is shown on the bottom trace of Fig. 15. The output shows a ramp delayed eight periods of the clock frequency.

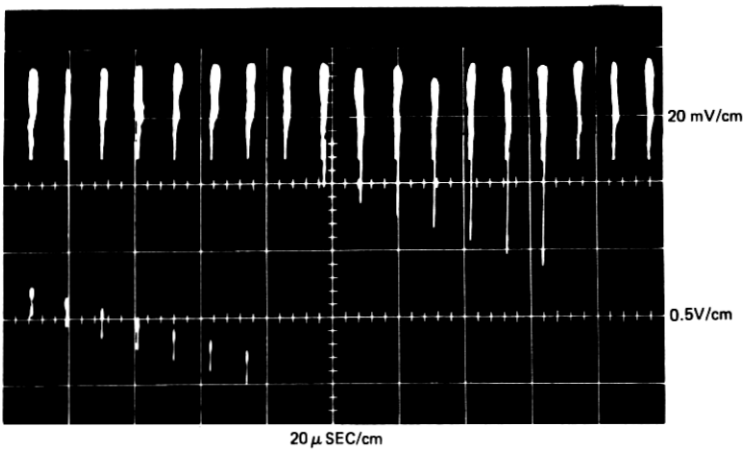

Fig. 15—Input and output (top trace) during operation as an analog device.

IV. CONCLUSION

The successful operation of an 8-bit n-channel two-phase CCD fabricated using ion implantation has been achieved. The device performed in the frequency range of 1 kHz to 6.6 MHz with no discernible loss ($\lesssim$0.1%/transfer). At 17 MHz, it was 2%/transfer. The shift register was also operated as an analog delay line.

The surface potential barrier under a portion of each gate necessary for unidirectional charge transfer was realized by ion implanting 1.5×10^{12} boron ions/cm^2. This gave rise to a measured barrier height of approximately 6 volts.

The use of the ion-implanted barrier makes possible considerable simplification of the structure. There is only one layer of metallization and no crossovers or crossunders. Moreover, the simplification caused no sacrifice in performance, since the device showed more efficient high-frequency operation than any previously reported CCD.

V. ACKNOWLEDGMENT

The authors are grateful to H. F. Hamilton for his invaluable assistance in fabricating the devices used in this study.

APPENDIX

Previous calculations[4] have shown that when the charge in a ZERO is a substantial fraction of the charge in a ONE, and square waves are used to drive the clock lines, there is virtually no loss caused by surface states. However, the implanted barrier represents a new feature with respect to surface state loss analysis.

The region that was implanted, and as a result contains a potential barrier, is exposed to a high concentration of free carriers only when transferring a ONE. There is essentially no free charge in this region at other times (refer to Fig. 1). As a result, when a ONE passes the barriers, some of the surface states in that region capture charge. This charge may be divided into three parts. Part one is charge which is re-emitted before the ONE has completed its transfer. This charge rejoins that in the ONE, and has no effect on loss. Part two is charge which is emitted too late to catch up, and is therefore dropped into the ZERO or ZERO's following the ONE. The remaining charge is still trapped when the next ONE arrives. The charge lost by this second ONE is the difference between the charge in the traps when it arrives, and the trapped charge when it leaves. This is the charge referred to as part two above.

Let us follow what happens to the charge which is trapped as a ONE crosses the barrier. The charge rejoining the ONE needs no further consideration. Charge which is emitted during the succeeding half cycle can travel either forward or backward, since the barrier region in question is at a potential maximum. As a result, one half of the charge emitted during this half cycle is lost. The amount of this charge can be determined as follows: Assume that all of the traps, the time constants of which are between $\tau/2$ and τ (where τ is the period of the clock frequency), will emit their captured charge during this half cycle. The number of such traps is $N_{ss}(E) \cdot kT \cdot ln(\tau/0.5\tau)$, where $N_{ss}(E)$ is the density of traps, per eV and per cm^2, the position of which in the forbidden gap makes their emission rate $1/\tau$. (It will be assumed that $N_{ss}(E)$ does not vary significantly for a few kT.) Then the charge lost per unit area of potential barrier during this half cycle is

$$\tfrac{1}{2} \cdot N_{ss}(E) \cdot kT \cdot ln\ 2. \tag{3}$$

The formula to convert position in the gap to period of the clock line is

$$f = N_c c_n \exp\left[-(E_c - E)/kT\right]$$

or

$$f = 3 \times 10^{10} \exp\left[-(E_c - E)/kT\right], \tag{4}$$

where N_c is conduction band effective density of states, c_n is the capture probability, and $E_c - E$ is the depth of the state below the conduction band edge. Formula (4) can be used to determine the appropriate value of E in formula (3).

Suppose n ZERO's now follow the ONE. During the n cycles required for these to pass, no free carriers cross the barrier. However, the surface states continue to emit trapped charge. This goes on from $t = \tau$ to $t = (n + 1)\tau$. The total amount of charge emitted during this period is therefore

$$N_{ss}(E) \cdot kT \cdot ln\ ((n + 1)\tau/\tau)$$

or

$$N_{ss}(E) \cdot kT \cdot ln\ (n + 1).$$

Not all of this charge is lost however, because the charge can flow backward or forward. The charge which flows backward during the time between $(n + \frac{1}{2})\tau$ and $(n + 1)\tau$ will join the ONE following the n ZERO's and therefore does not contribute to loss. This backward flowing charge is

$$\tfrac{1}{2} N_{ss}(E) \cdot kT \cdot ln((n + 1)\tau/(n + \tfrac{1}{2})\tau).$$

The net loss per unit area of potential barrier is

$$L_n = \tfrac{1}{2}N_{ss}(E)\cdot kT\cdot ln2 + N_{ss}(E)\cdot kT\cdot ln(n+1) - \tfrac{1}{2}N_{ss}(E)\cdot kT\cdot ln(n+1/n+2)$$

or

$$L = \tfrac{1}{2}N_{ss}(E)kT[ln(2n+1)(n+1)]. \tag{5}$$

Equations (4) and (5) can now be used to calculate expected loss per transfer vs frequency. For the experimental measurements of loss per transfer, $n = 1$. Therefore

$$L = 1.3N_{ss}(E)kT.$$

As an example at $E_c - E = 0.3\ eV$, from Fig. 10, $N_{ss} = 10^{11}/cm^2 - eV$. Therefore $L = 0.33 \times 10^{10}/cm^2$. From (4), the frequency is 2.7×10^5 Hz. Since the area of the potential barrier is 2.5×10^{-6} cm^2, the charge lost per transfer is 0.13×10^{-14} coulombs. The charge storage capacity is 2×10^{-12} coulombs which gives a loss per transfer figure of 0.07 percent. This compares to the "measured" loss of less than approximately 0.1 percent. This low loss is directly attributable to the two-phase structure, since only a small fraction of the surface states (those in the implanted region) can cause any loss.

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