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D2 Channel Bank:

Digital Functions

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This article describes the generation of timing signals and processing of digital information in the D2 Channel Bank. The transmitting portion of the D2 Channel Bank, which has four digital outputs, operates under the control of a single synchronous timing circuit. Because the four digital inputs to the receiving section of the D2 Bank are generally asynchronous, independent timing circuits are used for each of the four inputs. In addition, a separate clock is used in the receiver section to operate a single decoder shared by the four digital inputs.

Digital processing of the transmitting terminal includes the serializing of the coder output, inserting of signaling and framing information, and converting the binary code into a bipolar format for transmission over the T1 digital line. To perform the inverse operation just mentioned, the receiving portion of the D2 Bank must extract timing information from the received digital signal and recover the framing information so that the decoded PCM words can be properly demultiplexed. In addition, queuing logic must be performed to permit sharing a single decoder among four asynchronous inputs.

I. INTRODUCTION

The digital functions necessary in the D2 Channel Bank include the generation of control signals and the processing of digital information. The four digital outputs, called digroups, of the D2 Channel Bank are synchronous. A single crystal oscillator followed by a countdown chain is used to provide timing information for the operation of the entire transmitting section. The four incoming digital signals, however, are not expected to be synchronous. Independent extractions of the line clock for each of the four incoming digroups must be provided. This is followed by four independent countdown chains. Since a single decoder will be shared among the four incoming digroups, an independent timing supply is used for decoder operation.

Signals to be processed in the transmitting section of the D2 Bank include the PCM words from the coder which must be serialized and separated into four outgoing digital streams, and signaling information from the channel units which must be multiplexed along with the PCM code words. To provide for the proper demultiplexing of the information at the distant receiver, framing information must also be added to the signal. Automatic search and verification of the framing pulse is performed by each of the countdown chains to insure the proper demultiplexing of the digital signals. Asynchronous sharing of a single decoder and a fast framing search procedure represent unconventional approaches taken in the system design of the D2 Channel Bank. This article will describe circuits that perform the above two functions as well as the more straightforward operation of timing and digital processing.

II. TRANSMITTING SECTION TIMING

2.1 *Requirements*

Operationally, the 96 channels are divided into four independent digroups of 24 channels each. However, the four digroups of the D2 Channel Bank are treated synchronously on the transmitting side. They share a single timing generation circuit. The requirements for transmitting timing are dictated by both the output format and circuitry requirements. First, channel pulses occurring at an 8-kHz rate are necessary for the operation of the sampling gates. Four channels, one from each digroup, are sampled simultaneously. Thus 24 channel pulses, staggered in time and placed on separate leads, are required for the first stage of multiplexing. The first multiplexing stage results in eight groups of 12 channels each. The samples of four of these groups are staggered with those of the other four. Second, these samples are sequentially transferred to the coder by transfer gates operated by group pulses. Thus eight group pulses are needed for this final multiplexing with each of the eight group pulses repeating at a 96-kHz rate. Third, the digit-at-a-time sequential nature of coder operation requires control pulses. Six coder control pulses, each on separate leads, and each repeating at 772 kHz are necessary. In order to provide for proper phasing of the coder control pulses, a crystal clock of 6176 kHz is used at the head of the countdown chain. Fourth, the output format requires the insertion of the framing pulses at a 2-kHz rate, and requires the insertion of signaling framing pulses repeating at 667 Hz. Finally, the output bit streams applied to the four transmission lines require a clock of 1544 kHz.

2.2 *Timing Circuitry*

Figure 1 is a block diagram of the countdown chain used to produce the clocks in the transmitting section. The major use of each frequency is also indicated in the figure. Combinations of pulse trains produced by this chain are used wherever necessary to provide proper phases and duty cycles. The lowest frequency of 667 Hz provides for the

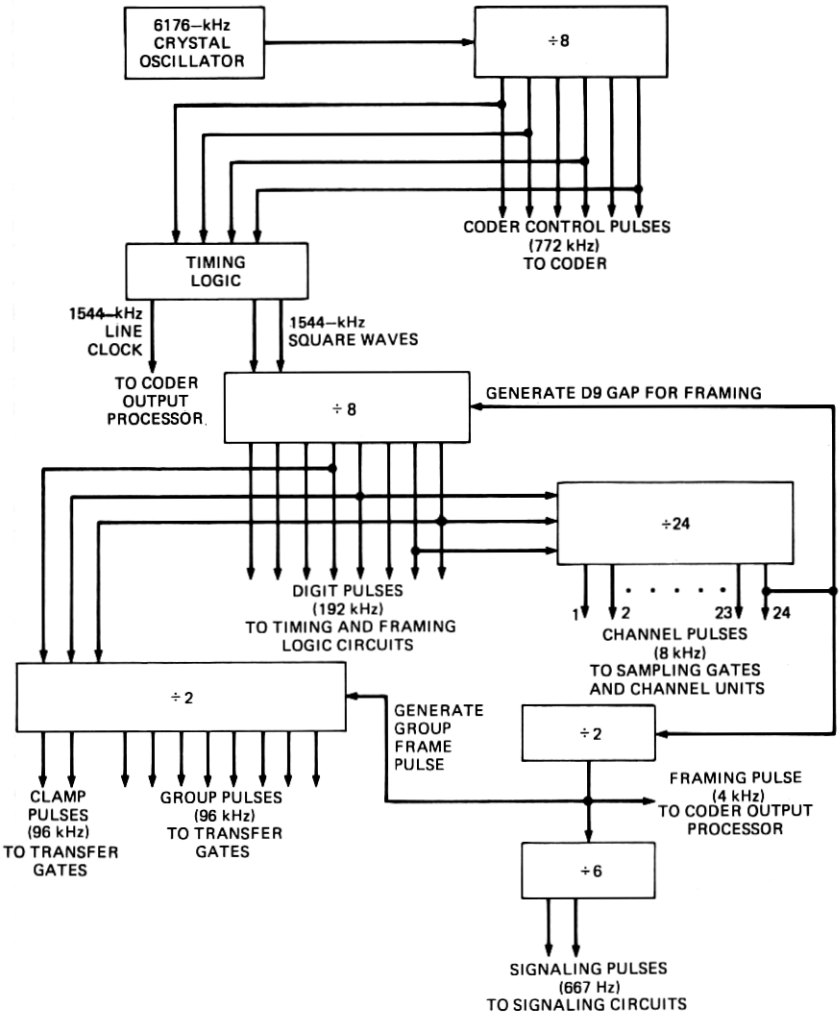

Fig. 1—Transmitting timing: a block diagram of the countdown chain used to produce the clock in the transmitting section.

insertion of the signaling framing bit, which is a repeating pattern of 111000, and controls the insertion of the signaling bits for all 96 channels. The 4-kHz signal controls the insertion of the main framing pulses which have the alternating pattern of 1010. The main framing bit and the signaling framing bit alternately occupy the 193rd bit in each 125-microsecond frame of each of the four digroups.

Even though the first stage of multiplexing is accomplished in groups of 12, 24 channel pulses are necessary because while a sample from one channel is obtained and held for further multiplexing, the sample from another channel must be clamped in preparation for a new sample. This requires that two staggered sets of 12 channel pulses be generated. Figure 2 indicates a portion of the timing near the framing pulse. The straightforward counting down of the frequency is modified by the insertion of a gap for zero setting of the coder. As mentioned in a companion article,[1] accuracy of the coding is achieved in part by a zero-setting circuit operating on the output of the coder when the coder is connected to a known reference signal. The time for this housekeeping chore is the gap which is present in the output frame format when the framing pulses are being inserted. This time, which is about 650 nanoseconds, is only half the interval that the coder normally takes to code a sample. To provide for a full 1300-nanosecond gap for the zero-setting circuit, the coding operation is offset in time by 650 nanoseconds every other frame so that two framing intervals can be lumped together. This also requires that the timing offset must be removed at the output so that framing pulses can be properly inserted for transmission.

III. RECEIVING SECTION TIMING

Much of the receiving section timing is similar to the transmitting section timing to the extent that channel pulses, framing pulses, and signaling framing time must all be derived. Since the receiving timing chain should be synchronous with the incoming signal, and since four independent incoming digroups are expected, four independent countdown chains are used in the receiver. Each of these four countdown chains is driven by a 1544-kHz clock extracted from the incoming line (Fig. 3). Unusual aspects of the receiving timing circuitry are the framing search procedure, and the operation of a shared decoder.

3.1 *Framing*

Framing is necessary at the receiver to bring the timing generation at the receiver into phase with respect to the incoming line, so that the digits can be properly identified for decoding and demultiplexing.

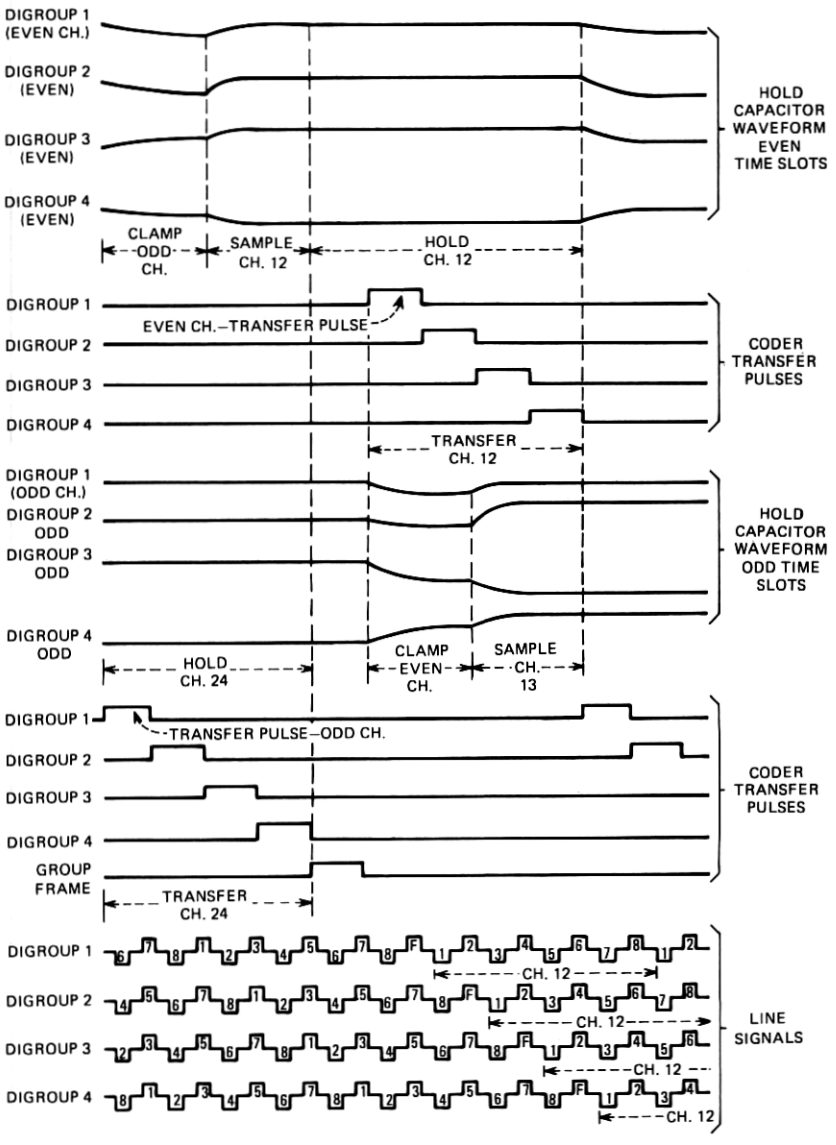

Fig. 2—Transmitting timing: a portion of the timing near the framing pulse.

Framing is accomplished by searching and verifying the framing pattern which was inserted at the transmitting end. The requirement on a framing circuit is that it should accomplish the search for the framing pulse within a certain time. Whenever the synchronization

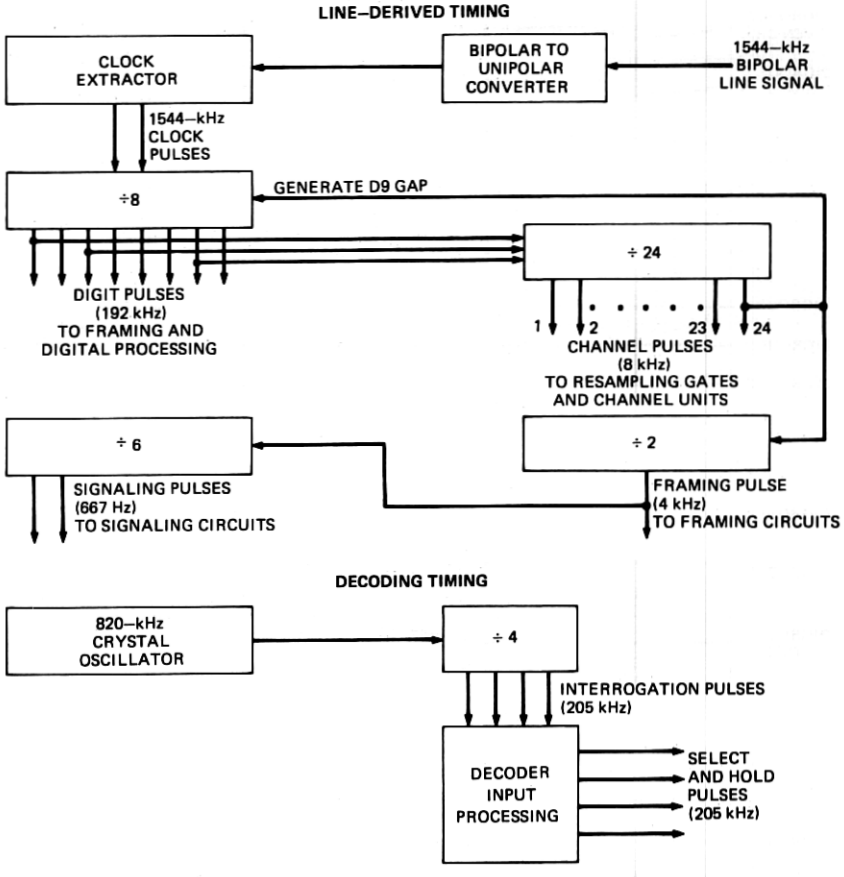

Fig. 3—Receiving timing: each of four countdown chains is driven by a 1544-kHz clock extracted from the incoming line.

of the receiver with the incoming signal is inadvertently lost due to error conditions, the signaling information will be incorrect. The requirement that reframes be accomplished within 50 milliseconds insures that although the telephone customer will receive no useful signal during this 50 milliseconds, at least he will not be disconnected. Because framing pulses in D2 are inserted every 250 microseconds as compared to every 125 microseconds for D1, a simple bit-by-bit search strategy, such as that used in D1, will result in a reframe time up to 200 milliseconds long. Therefore, a more sophisticated reframe procedure is used in D2.

As is usual in framing circuits, there are two modes of operation. The normal mode is the in-frame mode where the framing bit is checked for the alternating 1010 pattern. Occasional deviations from this pattern are ignored so that isolated line errors will not cause the framing circuit to initiate a false search. This flywheel action is achieved in the form of a capacitor store where about four closely-spaced errors are necessary to cause the framing circuit to enter the out-of-frame mode.

When a framing circuit enters the out-of-frame mode, the search procedure is initiated. Two 8-bit registers are used by the framing circuit in order that eight bits of the received stream may be examined at a time for possible candidates for the framing pulses (Fig. 4). Normally, these two 8-bit registers are used by the decoder input processor for the queuing operation. This will be discussed later in this article. During the out-of-frame mode, these registers are transferred for use by the reframe circuit. One register is used to store the incoming information bits. This is called the I register. The second register is used to note which of the bits in the I register are still suitable candidates for the framing pulse. This is called the S register. At the start of the reframe procedure, eight consecutive incoming bits are stored in the I register. These saved bits are then compared with eight consecutive incoming bits occurring two frames (0.25 milliseconds) later. A true framing bit should exhibit the alternating 1010 pattern. Any other bit position is assumed not to have this property on the long term but may or may not exhibit this property on the short term. The new eight bits replace the old eight bits in the I register. A comparison is made during this replacement between the old and the new to see if

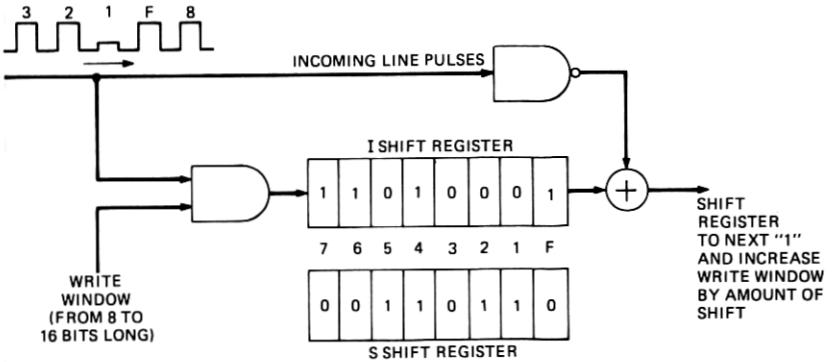

Fig. 4—Two 8-bit registers which are used by the framing circuit so that eight bits of the received stream may be examined at a time for possible candidates for the framing pulses.

any of these pulses are still candidates for the framing pulse. The result is stored in the S register. If the first of the eight pulses fails to qualify as the framing pulse, both the I and the S registers will shift one position allowing the second pulse to occupy the first position and making room for the next pulse at the end. It is thus possible for the registers to shift up to eight bit positions if all eight bits fail to meet the test. No shift takes place, however, if the first position exhibits the 10 alternation, even though the succeeding positions do not. This fact, though, is noted in the S register. In so doing, as soon as the first position fails the test, the succeeding bit positions could be rapidly passed over.

During the out-of-frame mode, a single detected violation of the alternating pattern will disqualify a particular bit position as a possible framing pattern. Thus line errors could cause a legitimate framing pulse to be passed over. The reframe time will exceed 50 milliseconds when this happens. With the expected line error rates of 10^{-6} or better, such incidences will not be frequent enough to cause concern. When an alternating pattern has persisted for about 2.5 milliseconds during its examination, the corresponding bit position will be considered as the framing pulse. The in-frame mode will then be entered. Again isolated errors will be ignored, and the I and S registers returned to their former function in the decoder input processor. By testing the framing position for 2.5 milliseconds in which time ten checks are made, the incidence of falsely returning to the in-frame mode due to information pulses exhibiting the alternating pattern on the short term will be small. When it happens, the penalty is a slightly increased reframe time since the out-of-frame mode must be re-entered.

By using a window of eight bits, the reframe time of about 43 milliseconds is achieved. The standard deviation is about 5 milliseconds. Increasing the number of bits stored and compared at one time would, of course, reduce the reframe time further. For example, with a pair of 16-bit registers, the reframe time is calculated to be 26 milliseconds. However, the 43 milliseconds of reframe time is adequate, and permits the sharing of these registers with the decoder processor.

IV. CODER OUTPUT AND DECODER INPUT PROCESSING

4.1 *Coder Output Processor*

The coder output processor is basically a parallel to the serial converter. In the D2 Channel Bank the coder output must first be split into four outgoing streams. Thus, there is a coder output processor for each of the four digroups. Parallel outputs from the coder are written

sequentially into one of four shift registers from which the serial information stream is read out. In addition, after 24 channels have been processed, the framing bit is added to the register following the last bit of the 24th channel. As mentioned previously, the coder operates with a timing offset between the even and odd frames to provide for zero-setting. This offset is absorbed by the shift register where extra storage is provided. Signaling information is inserted at the proper frames in the eighth bit position of each word. This insertion takes place in the coder from which it enters one of the four coder output processors.

4.2 *Decoder Input Processor*

A single decoder is shared by four incoming digroups for decoding the PCM code words into analog samples. A simple queuing logic is used. The decoder has its own clock which operates at a rate higher than four times the incoming rate of each line. Each incoming digroup has a decoder input processor associated with it. These processors use two 8-bit registers. A complete 8-bit word is stored in one of the registers to wait for decoding. During this wait, the second register will be receiving the following serial 8-bit code word. The decoder timing circuit causes the decoder to poll each of the four decoder input processors. Whenever the decoder cycles to a particular processor and there is a complete 8-bit word ready for decoding, these eight bits are transferred to the input register of the decoder.

Since the decoder timing is faster with respect to any of the incoming lines, the decoder will at times find only partly filled serial-to-parallel registers. In this case, the decoder processor will not transfer any code words, and the decoder will rest for that period before moving on to the next processor. This variation in time between the arrival of a complete code word and the decoding time is one complete queuing cycle. Thus, at least two registers must be used in each processor to accommodate this delay (Fig. 5). It can be shown that even with a very sophisticated queuing logic, two registers are still needed for each digroup because the maximum delay cannot be less than three decoding times.

Removal of this delay variation is accomplished in the analog store of the select-and-hold circuit. Channel pulses derived from the incoming line sample the output of the select-and-hold circuit at the proper time position in the demultiplexing process, and thus provide uniformly spaced PAM pulses to the receiving lowpass filter.

Timing for the decoder is provided by a separate 820-kHz oscillator.

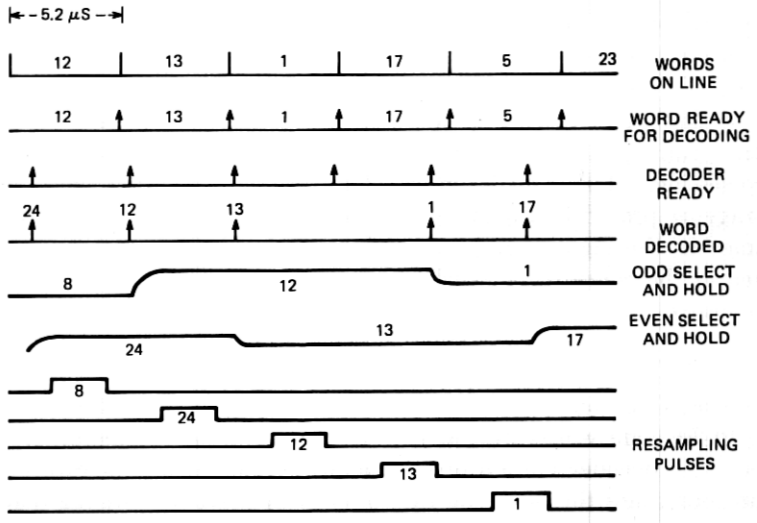

Fig. 5—Asynchronous decoding.

This is divided down to provide four phases of 205 kHz for use in polling the decoder input processors. This frequency must be high enough above the expected incoming word rate of 192 kHz to avoid queuing overflow during higher than normal incoming word rates caused by line jitter, and low enough to provide ample time for decoder settling. Another factor affecting the choice of the rate is the desire to minimize the effects of any beating frequencies between the incoming word rate and the decoding rate. The choice of 205 kHz meets these criteria.

Whenever the decoder becomes idle because an 8-bit word has not yet fully arrived at the input processor for digroup 4, the decoder will use this interval for zero setting.[1] With a line rate of 192 kHz, and a decoder cycling rate of 205 kHz, the rate of occurrence of no decoding is approximately 13 kHz for each digroup.

V. TRANSMITTING AND RECEIVING COMMON SIGNALING

Common signaling circuits in both the transmitting and receiving sections of the D2 Bank control the routing of signaling information from the channel units to the output bit stream and back. The signaling states of a particular channel are sampled by the appropriate channel pulse at the channel unit. Two signaling paths, allowing up to four

signaling states for each channel, result in two samples from each channel unit. These samples are multiplexed on two buses and sent to the transmitting common signaling circuit. The above action repeats every frame. During the sixth frame of a twelve-frame cycle, and only then, samples on one of the buses are sent to the coder where they take the place of digit 8, the least significant information pulse. During the twelfth frame, samples from the second bus are similarly sent to the coder.

To allow the receiving end to properly identify these signaling digits, signaling framing information must also be inserted in the 193rd position of every other frame. These bits follow the pattern 111000, completing a cycle every twelve frames. The frame following the signaling framing bit change from zero to one is defined as the frame containing signaling information in the eighth bit of every word for signaling path A. The frame following the one-to-zero change contains signaling information for signaling path B. In this manner, two signaling paths per channel are provided, each with a signaling capacity of 667 Hz.

At the receiving end, the frames containing the signaling bits are identified by testing the signaling framing bit. The locations of the signaling framing bit are indicated by the main framing pulse which shares the 193rd time slot in alternate frames. As with other receiving timing circuits, each digroup contains a separate receiving common signaling circuit. Each circuit extracts the eighth digit of each word during the appropriate frame, and places it on one of two buses, one for signaling channel A and the other for signaling channel B. The appropriate channel pulse gates the information on the buses to the individual channel-unit flip-flops which, in turn, drive the relays to reproduce the signaling information of the transmitting end.

The receiving common signaling circuit also controls the operation of the decoder during the signaling frame. Since only seven of the eight digits contain PCM information, the decoder is prevented from using the eighth digit for decoding. During these frames the decoder operates as a seven-digit decoder.

The transmitting and receiving common signaling circuits are designed so that they may be replaced by common-channel interoffice signaling (CCIS) plug-in units. When this is done, the CCIS bit stream will take the place of the signaling framing bits directly. This provides for a 4-kilobit per second channel. At the same time, the substitution of the eighth bit for signaling information will not take place and the full potential of eight-bit coding will be realized. At the receiving end, the decoder will no longer be asked to perform seven-digit decoding.

VI. SUMMARY

This article has discussed the system and circuit aspects of the digital functions in the D2 Channel Bank. The unique features of the D2 Channel Bank in this respect are:

(*i*) Circuitry to accomplish fast framing by use of storage,
(*ii*) Asynchronous operation of a single decoder shared by four incoming lines, and
(*iii*) Signaling circuits that can later be changed for common-channel interoffice signaling systems.

REFERENCE

1. Dammann, C. L., McDaniel, L. D., and Maddox, C. L., "D2 Channel Bank: Multiplexing and Coding," B.S.T.J., this issue, pp. 1675–1699.