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D2 Channel Bank:

Multiplexing and Coding

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Analog multiplexing and coding in the D2 Channel Bank is discussed in this article. Multiplexing of the message signals is accomplished in two stages. In the first stage, groups of 12 channels are multiplexed together using resonant transfer gates. The resulting eight buses, each carrying pulse-amplitude-modulated signals of 12 channels, are then multiplexed in the second stage. The samples of all 96 channels are presented to a single coder. The demultiplexing plan follows the inverse of the multiplexing plan. The output of the decoder is first divided into eight buses, and the final demultiplexing is accomplished in groups of 12 channels. Because the decoding is accomplished by an asynchronous time-shared decoder, storing and stretching of the analog samples is necessary to permit removal of the time jitter due to the queuing process.

The coder used in D2 is a nonlinear coder using a compression characteristic called the 15-segment approximation to the $\mu = 255$ law. To ensure the success of the coder development, a stage-by-stage binary coding plan was chosen. The first stage determines the polarity of the signal, and the succeeding binary stages determine the amplitude of the compressed signal one digit at a time. To achieve accuracy in the coder with available devices, automatic zero-setting circuits are used in a feedback loop to control offset deviations. This is in addition to the use of precision resistors and precision power supplies for the remaining critical parts of the coder. In order to achieve comparable accuracy in the decoder, the same stage-by-stage arrangement is also used. Again, automatic zero-set feedback loops are used to control drifts. The performance of the coder/decoder combination has met the objectives.

I. INTRODUCTION

This paper is concerned with the analog multiplexing and the coding processes in the D2 Channel Bank. Economies in a digital channel bank

are mostly due to the ability to share complex equipment such as the coder among all of the channels. To permit such sharing to take place, it is necessary to time-division multiplex the message signals from all the channels. This is accomplished by the multiplexing circuits. Because of the fragile nature of pulse-amplitude-modulated signals, it is here that most of the degradations, other than quantizing noise, are introduced. Great care must be exercised in the electrical and mechanical design of the multiplexing and demultiplexing circuits.

The bulk of this paper is devoted to coding. The presence of a coder is characteristic of digital channel banks, since it converts analog signals into digital form. The choice of the compression law will be discussed here. The method used to achieve the chosen compression law will be described. The speed and accuracy achieved by the D2 coder represented a significant technical advance in the art of analog-to-digital conversion. The success in developing and manufacturing this coder to the required speed and accuracy proved the basic soundness of the approach taken.

II. MULTIPLEXING

It was recognized early in the system design of the D2 Channel Bank that time-division multiplexing of the analog signals of all 96 channels in one step would present a difficult electrical and physical design problem. This is because it would be very difficult to control crosstalk and signal interference with a fan-in of 96 to 1. With two stages of multiplexing, the fan-in is reduced for the first stage. Greater care can then be exercised in the circuits used for the second stage of multiplexing since these will be fewer in number and their cost will be shared over many channels. Although the number 96 can be factored into many different combinations, it was decided to use the 12-8 multiplexing plan because the Bell System has traditionally used 12 channels to form a basic group in the frequency division multiplexing plan. (See Fig. 1.) Two such groups consisting of 24 channels are called a digroup meaning two groups. Digroup has also been construed to mean digital groups. The second meaning gained popularity because digroups appear predominately in digital channel banks.

2.1 *The First Stage of Multiplexing*

For the first stage of multiplexing the channels must be sampled as well as multiplexed. The sampling rate is 8 kHz. The basic cycle for sampling one of the 12 channels is 10.4 microseconds. The resonant

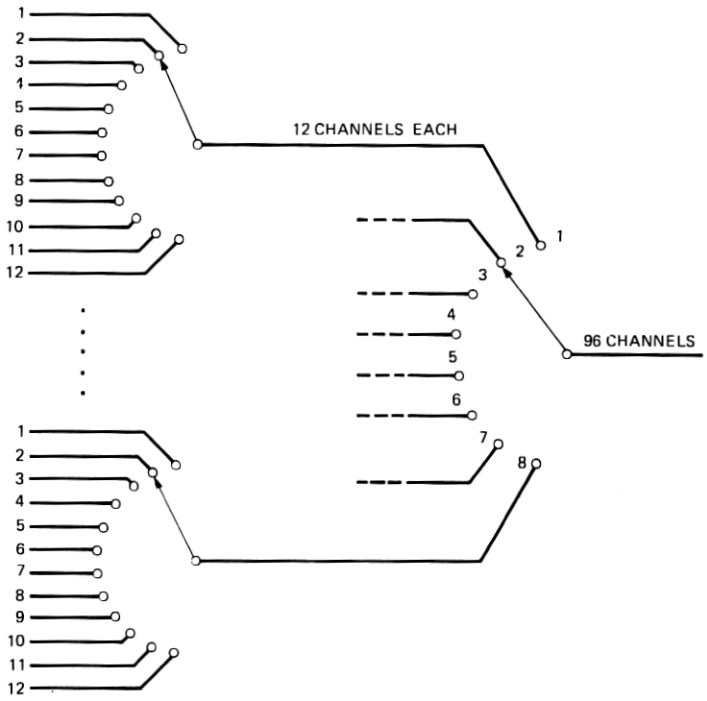

Fig. 1—Multiplexing plan.

transfer technique is used to perform the sampling. This transfer is accomplished in 2.2 microseconds (Fig. 2a). The result of resonant transfer is stored in the hold capacitor of the multiplexing bus for 5.2 microseconds (Fig. 2b). During this time the held sample is available for the second stage of multiplexing. After the hold period, clamping takes place for the rest of the 10.4-microsecond time to prepare the hold capacitor for the next resonant transfer. It is seen that on each multiplexed bus of 12 channels the samples are available only half the time. It is thus necessary to stagger the operation of sampling in pairs so that when a sample is available on one bus ready for the next stage of multiplexing, clamping followed by resonant transfer takes place on the other bus.

In a fully-equipped channel bank, there are eight buses, each with a holding capacitor, one for each group of 12 channels. Resonant transfer and the clamping occur in four of the eight buses simultaneously. This permits the use of a single channel counter to drive four resonant

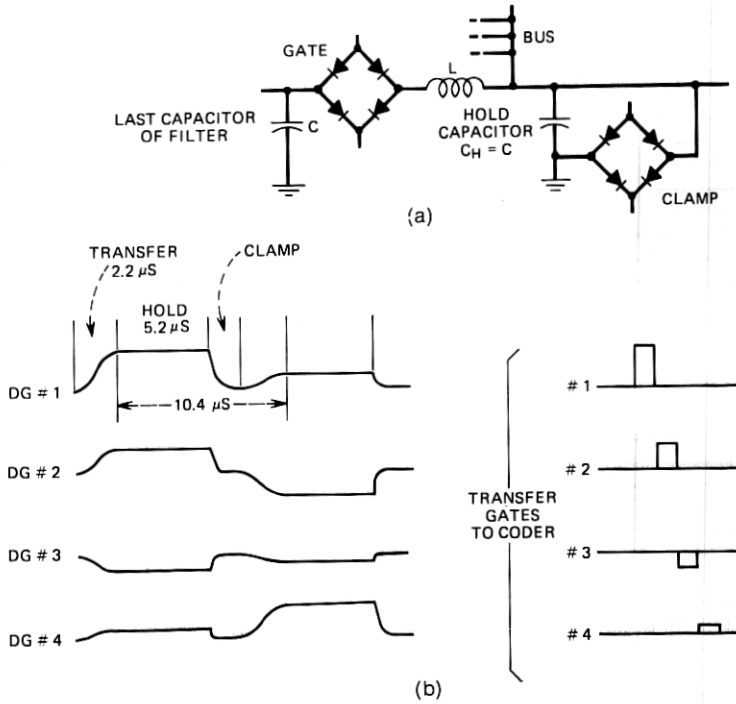

Fig. 2a—Resonant transfer.
Fig. 2b—First stage sampling and multiplexing.

transfer gates. A shift register of 24 stages is thus shared by 96 channels. Resonant transfer is used for this first stage of multiplexing because the resultant higher signal levels are more immune to noise and interference. This is particularly important because the multiplexing bus is physically spread over a large area on the D2 bay.

2.2 *Second Stage of Multiplexing*

The second stage of multiplexing combines the sample values from each of the eight holding capacitors, and feeds them to the coder for conversion into digital form. (See Fig. 3.) This multiplexing is accomplished by the use of balanced diode gates that follow the holding amplifiers associated with each of the eight holding capacitors. An operational amplifier is used for each pair of the diode gates. Thus four operational amplifiers are required. The outputs of these operational amplifiers are summed at the input of the coder. This arrangement permits equipping a channel bank with one digroup at a time and has

the further advantage that in the event of a failure of a single amplifier or gate, all channels do not have to be disabled to replace the defective one. The holding time of the first stage of multiplexing is divided into four 1.3-microsecond intervals and four samples are read sequentially into the coder during these intervals of coding. As will be explained in Section V, in order to provide a full 1.3-microsecond interval for zero setting the coder, the transfer gate operation has a timing offset every other frame. To permit this timing offset, the holding time at the first stage of multiplexing is made slightly longer than 5.2 microseconds. This delays the clamping operation by 0.65 microsecond.

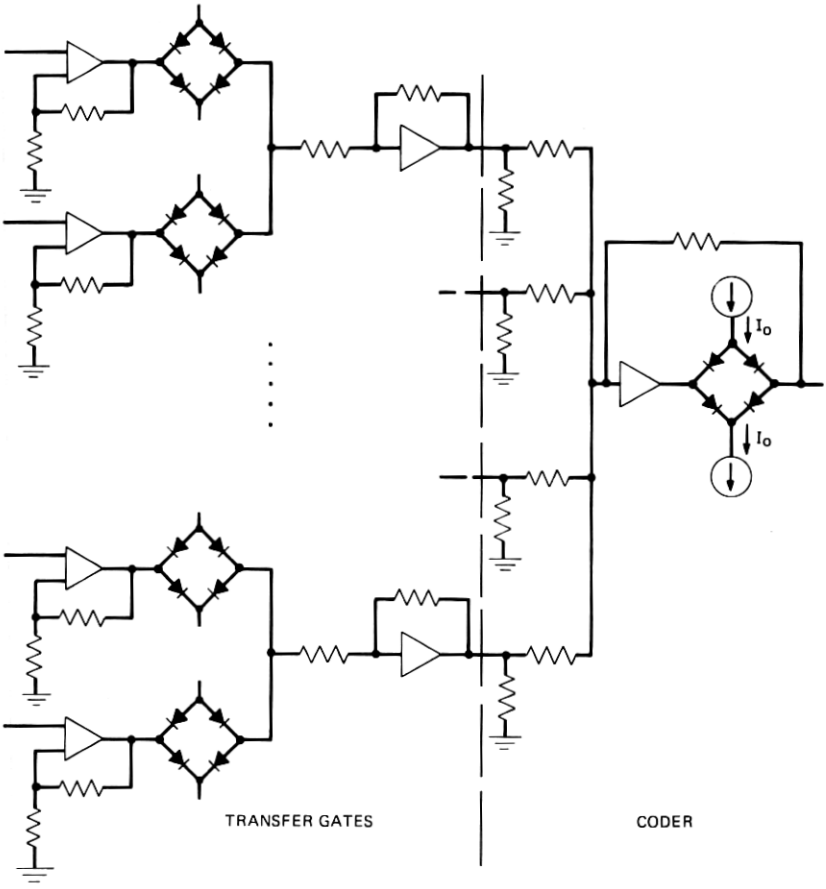

Fig. 3—Transfer gates.

III. DEMULTIPLEXING

On the receiving side after the incoming PCM code words are decoded by a common decoder, the PAM samples are demultiplexed in a two-stage operation following the inverse pattern of the multiplexing operation. First, the PAM samples are demultiplexed into eight groups of 12 channels each. Second, the groups of 12 channels are broken down into individual voice-frequency channels.

3.1 *Select and Hold*

Because the single decoder in a D2 Channel Bank is shared by four asynchronous incoming digroups, queuing takes place at the digital input to the decoder.[1] Consequently, the PAM samples, as delivered by the decoder, are jittered in time with respect to the derived incoming clock. This jitter can be as large as 5 microseconds. Removal of this jitter is accomplished in the select-and-hold circuit which also acts as the first stage of demultiplexing. The details of queuing are discussed in the next article.

At the same time that a digital word is transmitted to the decoder, the appropriate selection gate is turned on to steer the decoded PAM sample to one of the eight holding capacitors (Fig. 4). The samples are then ready for the channel pulses to steer them for the second demultiplexing stage. The time constant of this capacitor in parallel with the input impedance of the holding amplifier is made long so that the result of variable holding time will not add any detectable noise to the signal.

In each of the holding capacitors there is a sequence of PAM samples representing signals from the group of 12 voice frequency channels. Crosstalk can be caused by residual charge from the sample from a previous channel. Clamping the capacitor is one way to reduce this crosstalk. It is obvious that the same crosstalk performance can be achieved by precisely charging the hold capacitor to the new sample value. This is accomplished by making the time constant of the hold capacitor in combination with the output impedance of the driving amplifier very small. To protect the amplifier from the high currents that would result for such short-time constants, a current limiting diode bridge is interposed between the amplifier and the selection gates.

3.2 *Final Demultiplexing*

Each select-and-hold circuit is connected to the 12 voice frequency receiving filters through balanced diode transmission gates. These

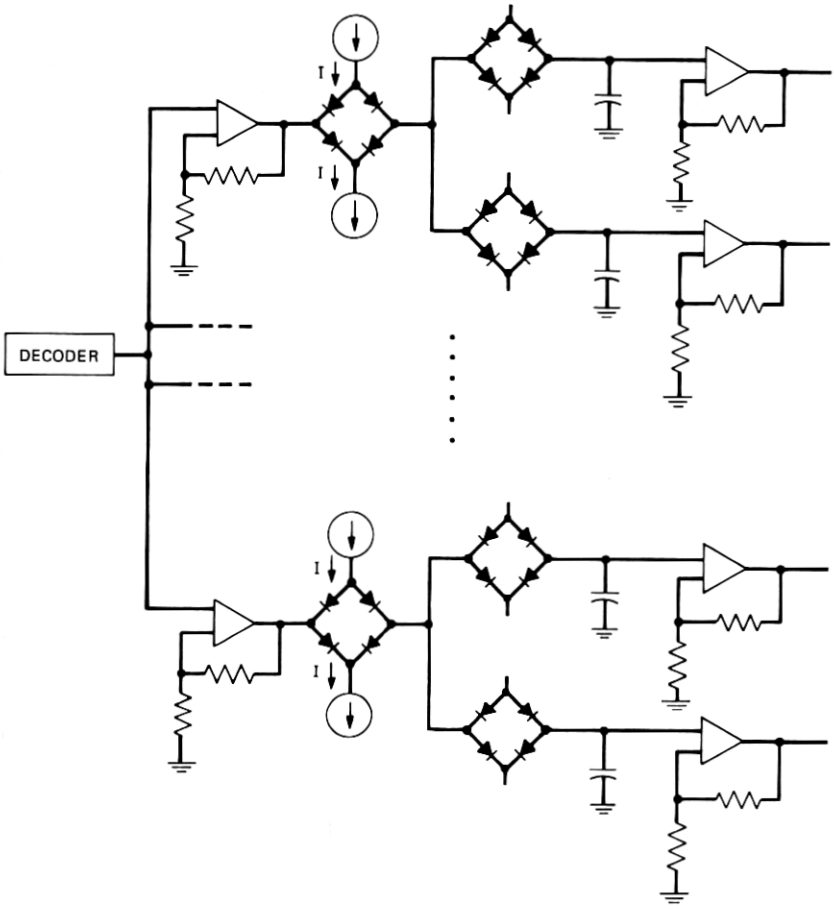

Fig. 4—Select and hold.

gates are under the control of the receiving channel counters and they demultiplex the 12 sequential PAM samples held by the select-and-hold. Voice frequency filters then reconstruct the signal from the PAM sample. Since the four incoming digroups are expected to be asynchronous, there are four sets of receiving channel counters of 24 stages each–one set for each digroup. The receiving channel pulses generated by the channel counters are derived from the incoming line. Thus they are not influenced by the asynchronous queuing logic of the decoder.

IV. CODING PLAN

For PCM coding of message signals, it is well known that a nonuniform assignment of code words to various amplitudes is necessary. This is because message signals can be expected to have a dynamic range of over 40 dB.[2] In the D1 Bank, this nonuniform coding step size is achieved by compressing the signal with a nonlinear circuit before coding and expanding the signal after decoding. The nonlinear circuit that does the compression and expansion is called the compandor and the transfer characteristic of the compressor is called the compression (or companding) characteristic. For uniform signal-to-distortion ratio over a wide dynamic range, a logarithmic compression characteristic is required. A pure logarithmic function cannot be used since the function approaches minus infinity at zero. Various approximations to the logarithmic characteristic have been proposed. The one proposed by the Bell System is called the μ-law,[2] and the one proposed by the British is called the A-law.[3,4] Both of these laws become linear at the origin. The D1 Channel Bank uses the nonlinear properties of diodes to approximate the μ-law characteristic. The resultant compression characteristic falls somewhere between the μ- and A-laws. During the initial planning of the D2 Channel Bank a new family of compression laws was proposed. These are called the digitally linearizable compression laws. These laws are piecewise linear approximations to the logarithmic laws. Furthermore, coders using these transfer characteristics have step sizes that are related to each other in powers of

TABLE I—CODER SEGMENTS

Coder Input	Segment	Step Size
8159	000	256
4063	001	128
2015	010	64
991	011	32
479	100	16
223	101	8
95	110	4
31	111	2
0		

two. It is thus possible to take the resultant binary code words representing the compressed signal amplitudes, to translate them easily into binary code words representing the linear or uncompressed signal, and to do so without incurring any additional quantizing noise degradations and with the linear step sizes no smaller than the smallest step sizes of the compressed code words.

There was some disagreement as to the exact detail of these digitally linearizable laws. The Bell System proposed a 16-segment law, symmetrical about the origin, with the center two segments having the same step size, and each succeeding outer pair of segments having step size double that of the previous pair of segments. This is called the 15-segment approximation of the $\mu = 255$ compression law. The definition of the 15-segment compression law is shown in Table I and also illustrated in Fig. 5. At the same time CCITT in Europe favored a similar 16-segment approximation where the inner *four* segments are made to have the same step size and the next succeeding pairs of outer segments doubling in step size. This is called the 13-segment approximation to the A-law. In comparing the two compression laws, one can find that the smallest step size used by the 15-segment approximation is about one half the step size used by the 13-segment approximation. This tends to give the 15-segment law better idle channel noise and crosstalk performance. However, for the same number of digits, the 15-segment law necessarily has slightly larger step sizes in the outer segments. It has been argued that the potential performance

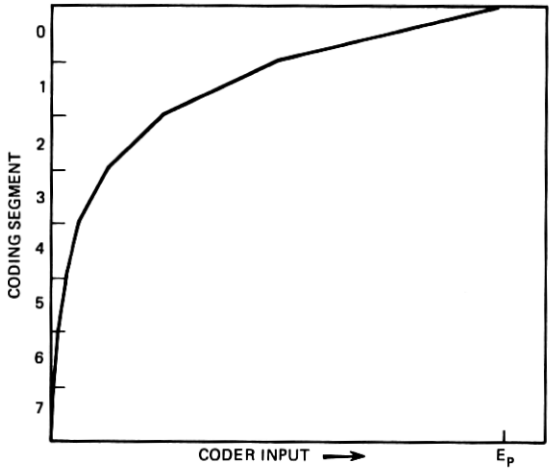

Fig. 5—15-segment $\mu = 255$ compression characteristic.

capabilities of the 15-segment law cannot be achieved with present technology. This is largely true as can be seen by the performance of the production D2 Channel Banks. The 15-segment law was chosen for the D2 coder because (*i*) the slightly lower signal-to-distortion performance at mid-to-upper signal levels as compared to the 13-segment law is not significant, and (*ii*) it allows the potential for future improved performance so that the 15-segment law can be made to be the standard for future digital channel banks as well.[5]

4.2 *Output Code Format*

The choice of the output code format is important because of the desire to make this the standard for future channel banks also. The D1 Channel Bank used the ordinary binary code where negative signals are expressed as the complement of the corresponding positive signals. An alternative to the ordinary binary code is the signed binary code or folded binary code where the first digit indicates the polarity of the signal, and the following digits indicate the magnitude. It has been shown that the folded binary code is superior to the ordinary binary code in masking transmission errors when a speech signal is carried.[6] This is because, with the ordinary binary code, an error in the first or most significant digit will always cause an amplitude error of half range, whereas with the folded binary code, a transmission error in the first or sign digit causes an error which is proportional to the signal. Since speech signals have the highest probability at zero, the average error voltage caused by a transmission error would also tend to be small.

A second choice concerning the output code format is whether magnitude should be transmitted in straight binary or its complements. For the folded binary code, the two choices result in different densities of pulses on a transmission line. When the magnitude is transmitted straight, small signals or no signal results in a very low density of ones being transmitted on the line. This could cause timing problems in the repeatered line. When the inverted binary code is transmitted, small or no signal would cause a very high density of ones on the transmission line. This would result in a strong timing signal in the repeater line. However, in a cable containing many digital transmission systems, a dense pattern of pulses would result in greater amounts of crosstalk from one system to another. For the ordinary binary code, there is no reason to make a choice since negative values have code words which are the exact complement of positive values.

The inverted folded binary code was chosen as the output code

format because it is thought that maintaining good timing performance in the repeatered line is important. The reduced timing error in the repeatered line would then leave more margin for amplitude degradations due to crosstalk. Compromise alternatives have been considered. For example, it is possible to invert every other bit at the output. This was proposed for the 13-segment approximation to the A-law. Compared with the inverted folded binary code it has both advantages and disadvantages, and the net difference was not considered significant.

V. THE CODER DESCRIPTION

Many methods are available that can be used to code an analog sample into a compressed binary code according to the 15-segment approximation to the $\mu = 255$ compression law. The nonlinear characteristics of diodes used in the D1 Bank are not suitable because they do not yield a piecewise-linear approximation. The digitally linearizable property permits the sample to be initially coded into a linear code which can then be followed by digital processing to achieve the compressed code. A desirable property designed into either the 15-segment or 13-segment code is that it permits a coder design using either the feedback arrangement or the stage-by-stage coding arrangement. For the feedback arrangement a local decoder is used, and the digits are determined sequentially by a single comparator. The local decoder consists of a linear binary decoder which determines the steps within each linear segment, followed by a ladder attenuator which determines the slope of the compression law.* The stage-by-stage coding method was chosen for D2 primarily because transmission gates and control logic in integrated-circuit form were not available at the time of development. Stage-by-stage coding does not use transmission gates. It is more complex, but within a D2 Bank the coder constitutes a very small fraction of the total cost.

5.1 *Coding Method*

The nonlinear coder consists of an arrangement of tandem stages, one stage for each of the eight digits.[8] Each coding stage produces two outputs, a digit output and a residue output. The residue is the input to the next tandem stage. This arrangement is illustrated in Fig. 6. The tandem stage method can be applied to any logarithmic compression coding characteristic including linear coding and piecewise-linear approximation to logarithmic compression laws.

* A more detailed discussion of coder types can be found in Ref. 7, pp. 583–592.

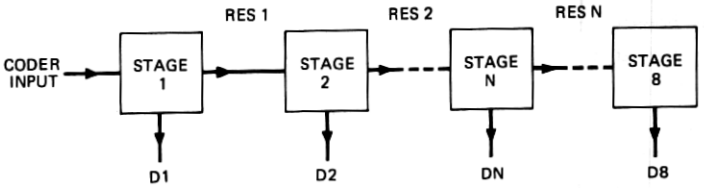

Fig. 6—Tandem stage coder.

Residue and digit output characteristics for the first three coding stages are plotted versus the amplitude of the PAM sample, E_{in} , in Fig. 7. Stage 1 determines the polarity of the sample, D1. Its residue is proportional to the magnitude of the sample. Each of the remaining

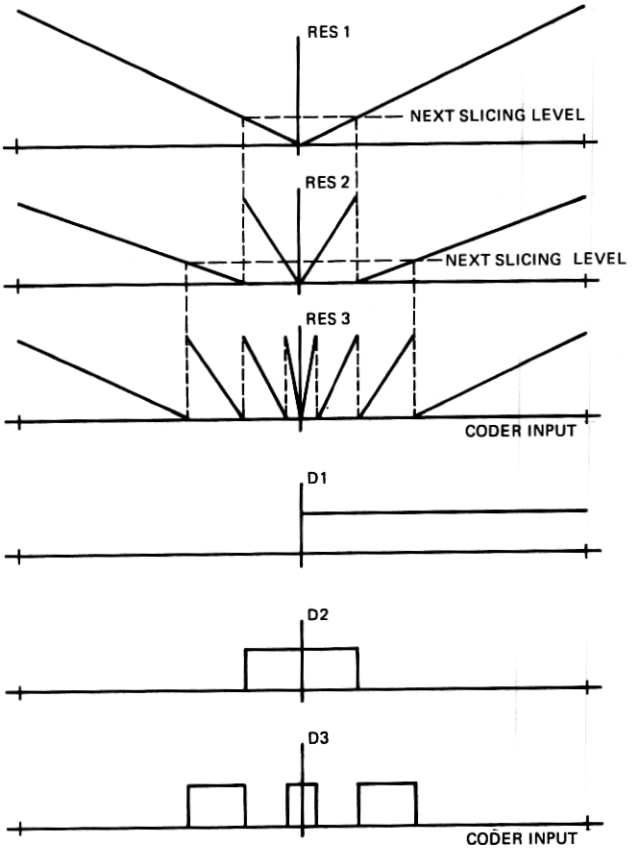

Fig. 7—Residue and digit characteristics.

stages produces one digit of the binary code representing the magnitude of the sample. The compression characteristic is generated by controlling the break-points and relative slopes of the residue segments.

Logarithmic compression coding is possible with this technique because the logarithmic curve has the property that it is congruent to itself by magnification and translation.

5.2 *Polarity Stage*

The first coding stage, the polarity stage, determines the polarity of the sample to produce the sign digit D1, and full-wave rectifies the PAM sample amplitude to produce the residue. The configuration of this stage is shown as Fig. 8. The stage consists of a high-gain inverting amplifier with nonlinear feedback and a digit detector. It is a combination half-wave rectifier and precision slicer. Assuming the high-gain inverting amplifier and no reverse conduction in the diodes, any input current, $I_{in} = E_{in}/R$, at the summing node of the amplifier, must result in conduction through one of the two feedback paths which contains either diode D_1 or D_2 . Any input voltage E_{in} greater than zero results in conduction through D_2 while an input voltage less than zero results in conduction through D_1 . The voltage and current relationships for the stage are shown in Fig. 8. The very steep slope of E_d in the vicinity of zero E_{in} results from the V–I characteristic of the feedback diodes. For the silicon diodes used in the

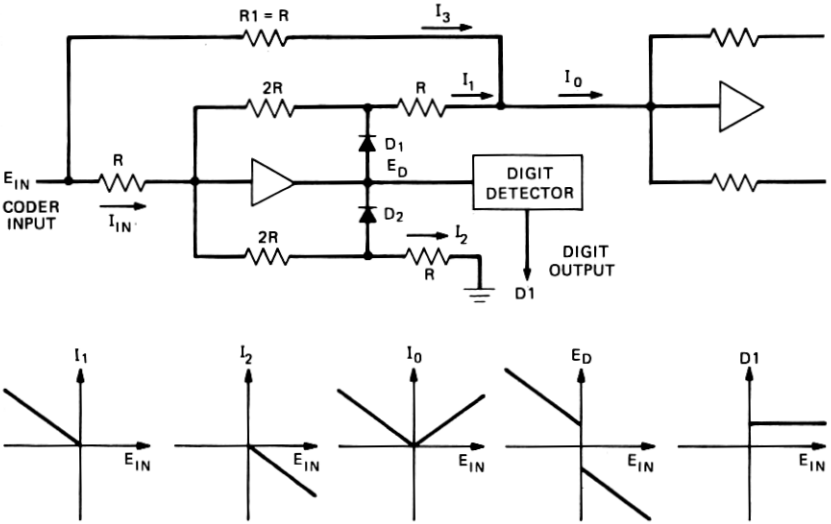

Fig. 8—Polarity stage.

coder, this slope is greater than 200 mv per microamp of diode current. The digit detector, which is a coarse threshold detector, senses the polarity of the voltage E_d and produces the one or zero code output for D1. The full-wave rectifier characteristic is produced by combining the current I_3 transmitted through the path of resistor R1 with the half-wave rectified current I_1 at the summing node of the next coding stage.

5.3 *Binary Stage*

A typical binary coding stage is shown in Fig. 9. The input current I_{in} (I_{in} is the output current or residue of the previous tandem stage) is combined with a reference current I_{ref} . I_{ref} defines the slicing level of the half-wave rectifier stage. As in the polarity stage, any net current at the summing node must result in conduction through one of the two feedback paths. Input currents greater than the reference current result in conduction through D_2 while input currents less than the reference result in conduction through D_1 . Voltage and current relationships for the stage are shown in Fig. 9. As in the polarity stage, a digit detector senses the polarity of the voltage E_d , and produces the one or zero code output for the digit. The digit detector also controls the switching of a reference current, I_p , which, when added to I_1 and I_2 at the summing node of the next stage, produces the required residue characteristic for binary coding.

The binary coding stage is a precision slicer producing a binary digit with one-zero transitions at $I_{in} = I_{ref}$, and producing a sawtooth

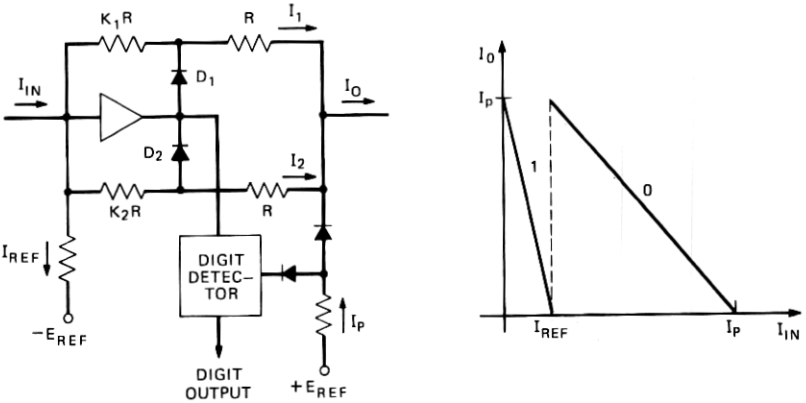

Fig. 9—Binary coding stage.

residue with different slopes to give the desired compression characteristic. For an arbitrary μ, the gain ratio and reference current for the first stage after the polarity stage are given by:

$$\text{gain ratio} = \sqrt{1 + \mu}$$

$$I_{\text{ref}} = I_{\text{p}} \frac{1}{1 + [\text{gain ratio}]}$$

where I_{p} is the peak current.

For the next stage, the gain ratio is the square root of that of the previous stage or

$$(1 + \mu)^{\frac{1}{4}}.$$

and

$$I_{\text{ref}} = I_{\text{p}} \frac{1}{1 + (1 + \mu)^{\frac{1}{4}}}$$

and so on. The gain ratios and reference currents for the 15-segment $\mu = 255$ compression characteristic are summarized in Table II.

The recurrence relationship between each succeeding gain ratio described above is discontinued at the fifth stage. Had this been continued, an exact $\mu = 255$ compression law would result. By forcing the gain ratios to be one for stages five through eight, a piecewise linear approximation to the μ-law results. Since the only gain ratios used are powers of two, the resulting coder step sizes are related to each other also by factors that are powers of two. This is due to the choice of μ such that

$$1 + \mu = 2^{2^N}. \quad \text{For } \mu = 255, N = 4.$$

5.4 *Coder Timing*

The step discontinuities in the residue output of each binary coding stage correspond to transitions of the binary digits. These discontinuities

TABLE II—CODING STAGE PARAMETERS

Stage	Reference $I_{\text{ref}}/I_{\text{p}}$	Gain Ratio K_1/K_2
2	1/17	16
3	1/5	4
4	1/3	2
5–8	1/2	1

are produced by the digit detectors switching reference currents I_p during the coding interval. Sample amplitudes near a transition are likely to cause a change in digit output, and a switching of the reference current at the last coding instant. All succeeding stages must then respond to this transient and settle to new outputs. Use of the resultant code word during this transient interval would result in coding errors. It is this response time that limits coding speed.

These errors are prevented by sequentially clocking digit detectors for the binary stages to define the time during the coding interval when each digit output can change state. These times are indicated in Fig. 10. The 1.3 μs coding interval is divided into eight 163-ns phases defined by the 6.176-mHz clock. Coder control (CC) pulses of various widths clock the digit detectors: when a coder control pulse is high, the digit output can change state, and when it is low, the digit output is inhibited from changing state.

The detector for D2 is allowed two clock phases to makes its digit decision and is then inhibited by CC2 from making further changes, the detector for D3 is given three clock phases to make its digit decision and is then inhibited by CC3 from making further changes, the detector for D4 is given four clock phases to make its digit decision and is then inhibited by CC4, etc. This clocking sequence is followed through D6. D7 and D8 are inhibited simultaneously at Phase 7. Since the polarity

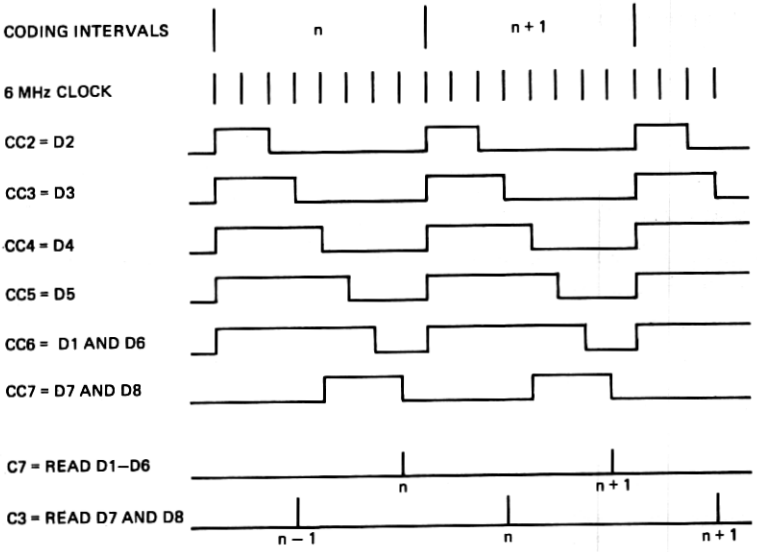

Fig. 10—Coder timing diagram.

digit, D1, has no effect on the residue passed forward to the binary coding stages, it is given until Phase 6 to make its digit decision and is clocked by CC6.

Digits are read into the appropriate coder output processor by phases of the 6-mHz clock. D1 through D6 are read out at Phase 7 by C7. At that time, D7 and D8 have just been inhibited by CC7 and may not have settled to a solid one or zero logic status. Read out of these digits is delayed until the next available processor read time, C3 (each of the four processors operates at one fourth of the 6-mHz clock rate). D7 and D8 are stored in the digit detectors until Phase 4 of the next coding interval by inhibiting them with CC7.

5.5 *Coder Accuracy*

Numerous coder parameters determine the accuracy to which input samples are coded. Among these are:

(*i*) reference voltage supplies,
(*ii*) reference resistors,
(*iii*) ratio of amplifier gain resistors,
(*iv*) summing node bias current and offset voltage.

The significance of the coding error introduced by these parameters depends on which coding stages are affected and the amplitude of the sample being coded. Obviously, errors introduced in the input coding stages are more significant than comparable errors in the latter stages, and a given error is most significant when the coding step size is smallest.

The effect of coding errors can be illustrated by a simple example. Current levels in the coder are chosen such that the peak input voltage to the coder, E_p, results in a peak residue current $I_p = 7$ ma. At the input to the second coding stage, the smallest step sizes, those on the inner segment, correspond to a residue current of approximately 1.7 μa. The effect of a current error of 3.4 μa, which could be introduced by summing node offset at the input of this stage, is illustrated in Fig. 11. This error has resulted in the omission of four code words at the origin of the transfer characteristic. This abrupt step in the characteristic would result in excessive idle channel noise and crosstalk as well as degraded gain tracking and distortion performance in message channels.

The magnitude of coding errors could be controlled by placing stringent and costly stability requirements on reference voltage supplies, resistors, and summing node offset. Instead, two simple automatic zero-set loops are used to maintain alignment of the coding segments adjacent to the origin.

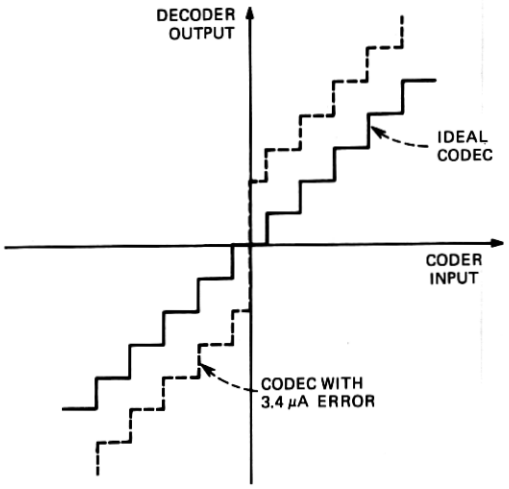

Fig. 11—Coding errors.

Automatic zero-set loops are operated in a housekeeping coding interval set aside at the end of every two frames, or 250 μs. The coder input during this interval is taken to be zero (although the input from the transfer gates need not be zero volt). The first loop, AZS1 in Fig. 12, samples D1. If the digit is a one, the zero set current into the polarity stage is adjusted to move the digit toward a zero. When the digit output

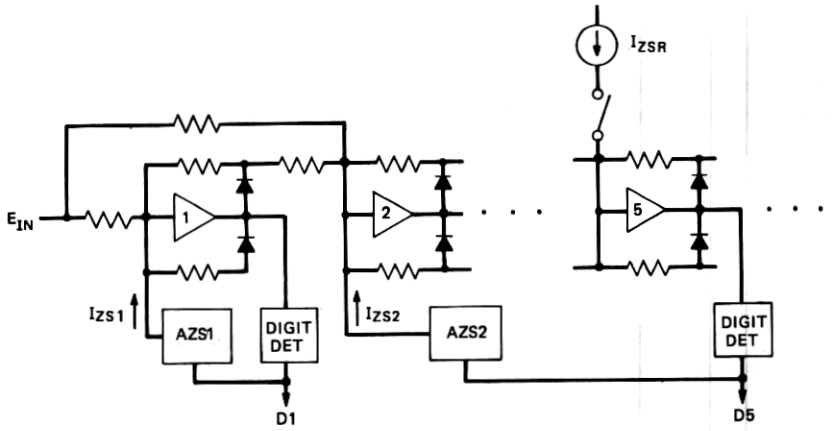

Fig. 12—Automatic zero-set loops.

is zero in the zero set interval, the current is adjusted to move the digit toward a one. The change in I_{zs1} between sampling intervals (250 μs) is held to a fraction of the smallest coding step. Thus, this loop dithers the polarity stage at its one-zero transition.

Since the polarity stage is at its transition, the residue is at the tip or folding point of the full-wave rectifier "vee" characteristic. This information is vital to the operation of the second loop, AZS2. During the zero-set interval a reference current, I_{zsr} , equal to 7-1/2 steps, corresponding to the transition of D5, is switched into the node of stage 5. This current is not present during normal message channel coding intervals. With this input current and the polarity stage at its transition, stage 5 *should* be at its one-zero transition. By injecting a correction current, I_{zs2} , at the second stage the AZS2 loop, sampling D5 and functioning similar to AZS1 dithers stage 5 around this transition.

During the zero-set interval, the coder is forced to the digit-five transition at the middle of the innermost segment independent of any errors introduced by stages two through four. When I_{zsr} is removed during normal coding intervals, the segments adjacent to zero input are aligned. Any error in coding on these segments is due to stages five through eight. These stages resolve the residue input to stage five into 16 uniform steps, a task requiring only modest accuracy. Coding errors that would have resulted from static imperfections in stages one through four without the zero-set loops have been shifted from the inner segments to the segments where the step sizes are larger and a fixed coding error is less significant relative to the step size. The current I_{zs1} serves the function of the slicing reference for stage 2 and precisely cancels any summing node bias current of this stage.

Each zero-set loop (Fig. 13) is a simple bang-bang servo with an integrator. The state of the digit is clocked as the input to a one-shot multivibrator during the zero-set interval. If the one-shot does not

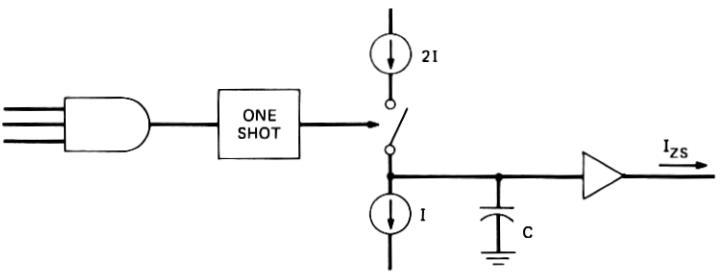

Fig. 13—Zero set.

operate, current source I discharges the voltage on capacitor C. When the one-shot does operate, current source $2I$ is connected to charge C with a net current equal to I. Loop parameters I and C are chosen such that the change in I_{zs} between sampling intervals is a fraction of the smallest coding step.

Precision resistors determine the gains of the coding stages and, with reference voltage supplies, determine fixed and switched reference currents. These resistors define the coder compression characteristic. Thin-film tantalum nitride resistor networks are used to ensure coding accuracy. The ratio of two resistors determines the gain of each path of a coding stage. These gain resistors are fabricated in networks consisting of four resistors, two for each gain path of the stage. A typical resistor network is shown in Fig. 14. Gain resistors are specified to have a ratio tolerance of ± 0.1 percent for the input stages to 2 percent for the latter stages. Reference resistors are fabricated as networks consisting of the fixed and switched reference for each summing node. Absolute tolerance requirements range from ± 0.25 percent to 2 percent. Computer simulations and actual measurements have confirmed the necessity and the adequacy of these requirements.

5.6 *Zero Code Suppression*

In order to insure adequate timing information for the T1 line repeaters, the D1 Channel Bank suppresses the all zeros code. In so doing, the density of ones is at least one eighth, and the longest run of zeros is fourteen. To comply with the same constraint, the all zeros code in D2 is also suppressed and replaced by the code word 00000010.

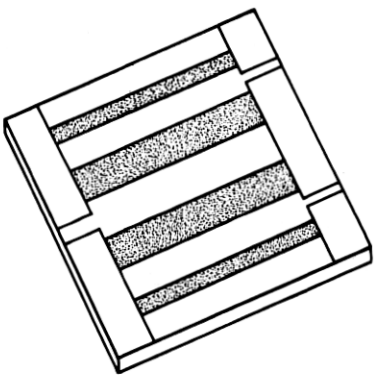

Fig. 14—Thin-film gain-resistor network.

The next to the last digit is changed to a one because the last digit is reserved for signaling in one sixth of the frames.

It has been argued that, since the average density of ones in D2 is higher than that in D1, and since the probability of code words with sparse ones following one another is much smaller than that in D1, zero code suppression is not really necessary. It is included because the additional complexity is very small.

VI. DECODER

The nonlinear decoder has an expansion characteristic that is the inverse of the 15-segment approximation to the $\mu = 255$ compression characteristic of the coder. The decoder is time-shared over four asynchronous digroup inputs. Words to be decoded are written in parallel into a register in the decoder by one of four decoder input processors. The word remains in the store for the approximately 1.2 μs decoding interval until reset by the decoder clock. Digits D1 through D5 are decoded in tandem stages very similar to those used in the coder. Because these digits represent linear divisions within segments, and because accuracy is no longer critical, digits D6 through D8 are decoded by summing binary-weighted currents at the node of the first tandem stage, which is for D5.

A typical decoding stage is shown in Fig. 15. The binary state of the digit controls a switched reference current, I_D, at the input of the

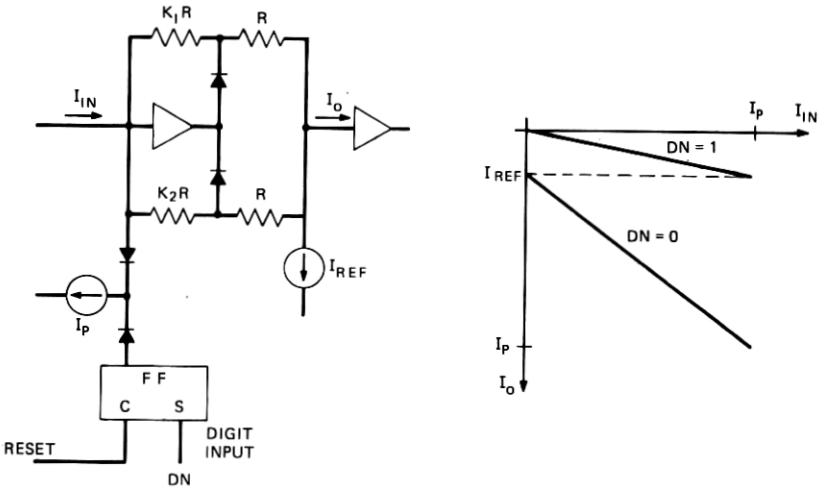

Fig. 15—Typical decoder stage.

stage and determines which gain segment is used for the stage. The gain ratios of these stages are the inverse of the gain ratios for the corresponding coder stages given in Table II. A fixed reference current, I_{ref}, shifts the output to produce a residue of constant polarity. This output, I_0, is the input to the next decoding stage.

Zero set is used in the final decoder stages in a manner similar to that for the coder. A known signal is used as input to the last two stages. Although the decoder does not make decisions, the equivalent digit output point, which is the junction of the output of the operational amplifier and the steering diodes, is tested for polarity and the zero set correction currents are adjusted according to that result.

VII. SIGNALING

During signaling frames (every sixth frame of PCM words) only seven data digits contain information about the amplitude of the sample: The eighth data digit contains signaling information. Different values are produced by the decoder for 7-digit and 8-digit words in order to minimize quantizing error. This is illustrated in Fig. 16 which is

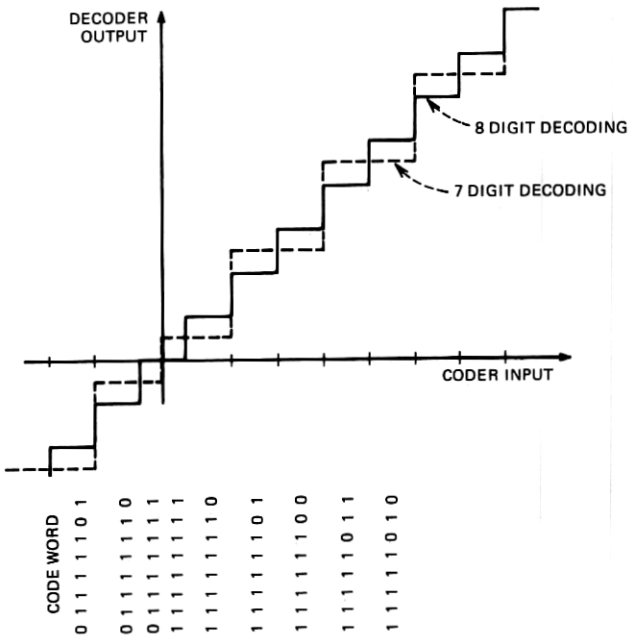

Fig. 16—7- and 8-digit decoding.

an overall CODEC transfer characteristic in the vicinity of zero input for 7-digit and 8-digit decoding.

VIII. PERFORMANCE

The measured performance of a production coder-decoder combination (CODEC) is shown in Fig. 17. Sine waves are generally used as input to measure the performance of a typical production CODEC rather than Gaussian noise which has a distribution that resembles speech more closely. Sine waves are not only easier to generate and measure but they also have the property that localized errors can be detected in the coding and decoding process with greater sensitivity and accuracy. A Gaussian-distributed signal would exhibit a smoother curve over the same defects. This difference is particularly evident in the theoretical signal-to-noise performance of an ideal CODEC when sine waves are used as inputs. This is illustrated in Fig. 18, where each step of the CODEC transfer characteristic manifests itself in a cyclic oscillation in the signal-to-distortion curve, and each segment of the piecewise linear approximation manifests itself in a cyclic oscillation

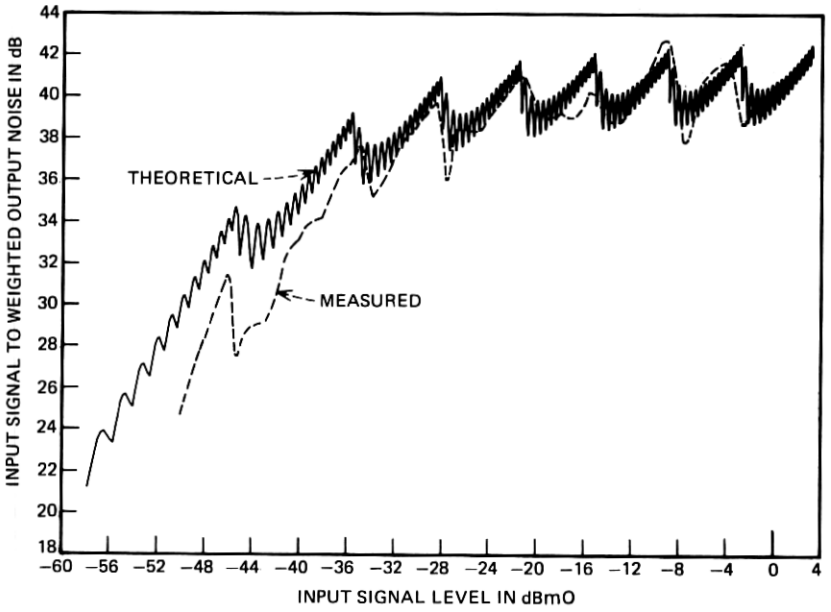

Fig. 17—8-digit, 15-segment, μ-law, non-uniform CODEC. Comparison of theoretical and measured signal-to-noise ratio for sine wave input.

of the envelope. With a Gaussian signal such fine structures are not evident. Furthermore, the Gaussian signal, because of its high peak factor, exhibits the overload characteristic early so that the accuracy of the outermost segment cannot be tested.

The theoretical signal-to-distortion curve is indicated in Fig. 17 for comparison with the measured performance. It can be seen that the typical performance of a production CODEC is very close to that of an ideal CODEC. Due to noise and crosstalk in the D2 bay the measured performance of the CODEC in the D2 Bank is not as good as that of the CODEC alone.

A photograph of the transfer characteristic of the CODEC is shown in Fig. 19. Only the transfer characteristic of the innermost segment is shown since this is the most critical area of the CODEC performance, where offsets will be most evident and errors in step size are most pronounced. If the entire transfer characteristic is plotted, only the step size for the outer segments will be obvious. The inner segments, being only one-128th the length of the outermost segment, will not exhibit visible steps at all.

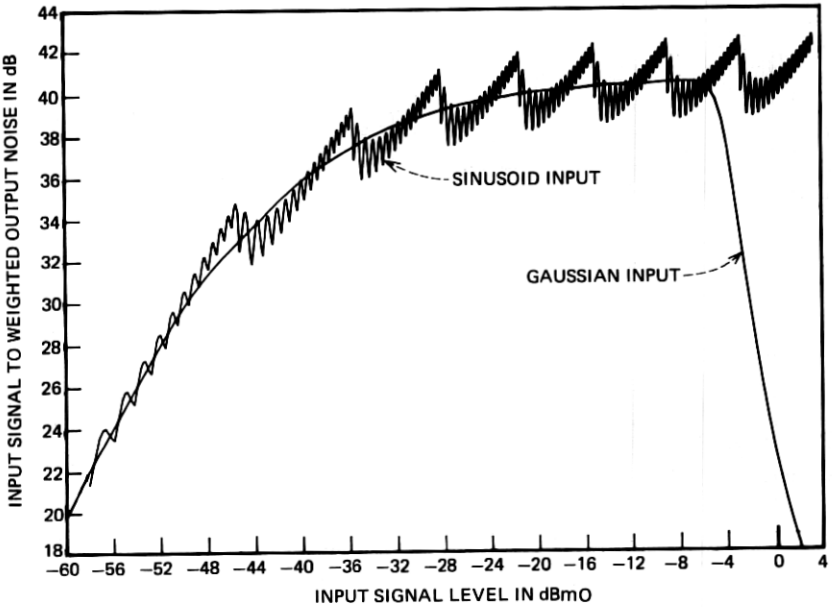

Fig. 18—8-digit, 15-segment, μ-law, non-uniform CODEC. Comparison of theoretical signal-to-noise ratios for sine wave and Gaussian inputs.

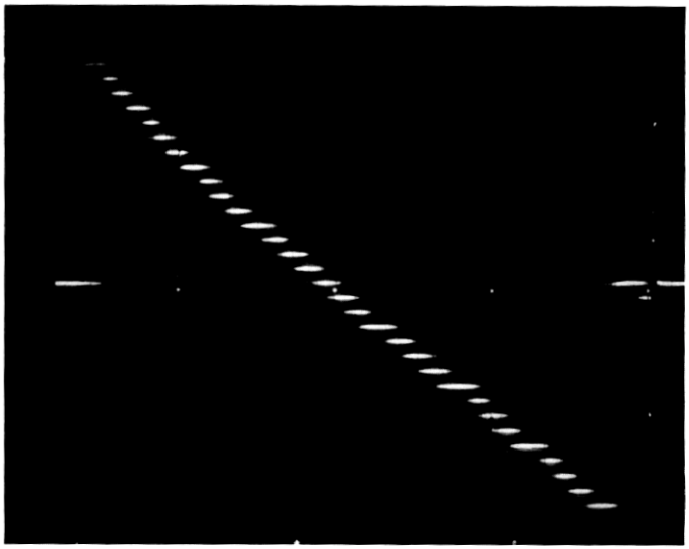

Fig. 19—CODEC transfer characteristic–only the inner two segments are shown representing 1/255 or 0.4 percent of the total range.

IX. SUMMARY

This article has discussed the analog multiplexing and coding aspects of the D2 Channel Bank. Multiplexing and demultiplexing are accomplished in two stages to ease the timing and crosstalk problems. Coding is accomplished by a digit at a time stage-by-stage coder. Its performance is very close to that expected of an ideal CODEC.

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