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# D2 Channel Bank:

# System Aspects

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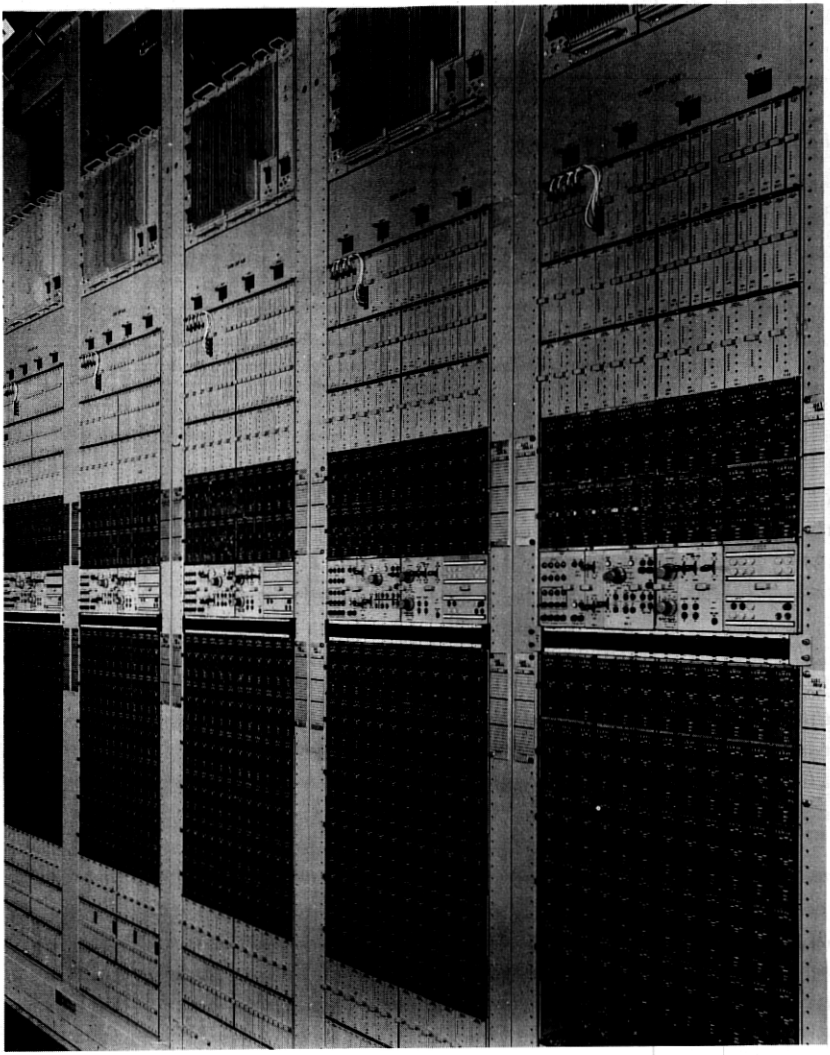
*This is the first of a series of articles describing the D2 Channel Bank–from initial conception, system design, circuit development, physical design, through manufacture, installation and service. Our objective is to provide a complete story of how one product progressed from identification of need through various phases leading from early planning to operating company application.*

*In this introductory article, the motivation for undertaking the development is pointed out, and the reasons for the choice of the various system parameters are discussed. The D1 Channel Bank, which was designed for exchange application, was the pioneer in digital channel banks. As a second generation channel bank developed for toll application, D2 could be expected to show significant advances over its predecessor. Of the many possible improvements, some would result in incompatibilities with portions of the existing plant. In such cases, engineering judgements were necessary to determine which of these were warranted by the performance improvements they allowed. This article documents the historical evolution of the D2 Channel Bank system parameters.*

## I. INTRODUCTION

The first digital transmission system used for commercial telephone service was introduced by the Bell System in 1962. This system consists



D2 Channel Bank

of the D1 Channel Bank and the T1 Repeatered Line.[1] The D1 Bank uses pulse code modulation to convert 24 voice-frequency signals and the associated signaling information into a 1.544 megabits per second digital stream for transmission over the T1 Repeatered Line. Because it has met its performance and cost expectations, the D1/T1 system, which is also known as "the T-Carrier," has been favorably received

by the telephone companies. Today it is the fastest growing carrier facility in the Bell System supplying nearly a million voice channels throughout the country. Its success is a direct result of one of the characteristics of digital systems–low terminal cost.

The success of D1/T1 has stimulated planning of a digital communications network. A fully digital network includes both digital switching and digital transmission. Most of the effort since 1962, however, has been directed towards the development of transmission systems for this network.[2,3] In this network there will be a hierarchy of digital transmission facilities that provide for long-haul transmission at high bit rates,[4] digital terminals that convert a variety of signals into a suitable digital form, and digital multiplexers that can derive several smaller capacity digital facilities from a large capacity facility. The existing T1 lines will become part of this hierarchy.

Since the D1 Channel Bank was designed primarily for short interoffice trunks, it does not have all the transmission performance and operating features required for toll service. As a result, there was appreciable motivation for the development of a new digital terminal, the D2 Channel Bank, which is designed to provide economical voice trunks for intertoll service, and which can also be used for exchange trunks. This article describes the system aspects of the D2 Channel Bank. Companion articles describe the various circuits of the D2 Bank, production, installation, and continued improvement after initial service.

## II. SYSTEM CHARACTERISTICS

Many objectives and constraints play a significant role in the system design of the D2 Channel Bank. First, a channel bank suitable for intertoll use must exhibit a performance level superior to that of the D1 Bank. This is because toll calls may include many digital trunks interconnected by switching machines which at present can handle signals only in voice-frequency form. In such situations, quantizing noise will accumulate because of repeated analog-digital and digital-analog conversions. Second, in the digital network envisioned for the future, the trunks may be switched in digital form. This means that a signal converted into digital form by one channel bank is expected to be reconstructed by any other channel bank. A high degree of standardization and uniformity is thus required of all such channel banks. Third, the D2 Channel Bank must be able to utilize the T1 line which is an existing transmission facility in the planned digital hierarchy.

Compatibility considerations with the D1 Bank and with other

domestic and foreign digital channel banks in existence or in development have also influenced the system design of D2. Incompatibility will affect the problem of digital interconnection between different telephone administrations in the future. It will also affect future channel bank designs. To be fully compatible, two channel banks must have these same attributes:

(*i*) number of voice channels
(*ii*) sampling rate
(*iii*) companding law
(*iv*) code format
(*v*) overload point
(*vi*) signaling format
(*vii*) framing format
(*viii*) output bit rate.

If any one of these attributes is different for two channel banks, then digital processing becomes necessary before they can be interconnected digitally. Each attribute requires varying degrees of digital processing to convert from one standard to another.

It was recognized in the system design of D2 that it would not be feasible to strive for complete compatibility with existing digital channel banks for performance reasons, or with future banks because international standards were not yet determined. The choices made in the design of the D2 Bank were such that complex digital processing could be avoided, but simple processing would be permissible for possible interconnection. The use of simple processing can readily provide changes in the code format, signaling format, and framing format. The number of voice channels and the output bit rate can be changed easily and efficiently if the numbers used by two channel banks form simple fractions. This allows an integral number of channel banks on either side to be interconnected. Both companding law and overload point can be changed by digital processing of low complexity. The most difficult parameter to convert is the sampling rate. To change this parameter, interpolation between samples is necessary. The complexity is equivalent to digital filtering.

As a result of these considerations, the number of channels, the sampling rate, and the output bit rate for D2 are chosen to match those of the D1 Channel Bank. This will allow the use of the existing T1 digital transmission line to interconnect D2 Banks and, with simple to moderate digital processing, allow digital interconnection between D2 and other channel banks with 8-kHz sampling.

All other attributes of D2 are not compatible with D1 primarily for reasons of improved performance. The most important differences are the number of digits used per coded sample and the companding law. These differences in turn cause other attributes, such as signaling format and framing format, to be different.

### 2.1 *Consequences of Eight Digits Per Coded Sample*

As mentioned earlier, in order to meet noise and distortion requirements for toll service, eight-digit PCM is used as compared to seven-digit PCM used in D1. But to increase the number of digits per coded sample and still maintain the same sampling rate and output rate, either the number of voice channels must be reduced or the portion of output bit rate devoted to signaling must be reduced. The latter approach is taken because a reduction in signaling rate to one-sixth of that in D1 could be tolerated without sacrificing the capability of the D2 Bank to operate with all the signaling systems that are presently handled by the D1 Bank. In this way, close to eight-digit PCM performance is achieved. The actual format used in D2 is to code each sample into eight-digit PCM in five out of six frames and into seven-digit PCM in the sixth frame when the eighth digit is used for signaling. The resultant quantization noise is about 2 dB above that of full eight-digit PCM.

The signaling capacity derived in this way is adequate for all signaling systems presently served by the D1 Channel Bank. This includes, for example, dial pulse and revertive pulse signaling. Switching systems in the future are likely to convert to Common Channel Interoffice Signaling (CCIS) where signaling information for a collection of voice channels are sent as a separate digital stream. With CCIS, the signaling circuit packs are simply removed, and the performance of full eight-digit coding can be realized.

### 2.2 *Frame Format*

The format of D2 allows for signaling in the present plant and future CCIS type signaling. This is accomplished as follows (see Fig. 1). At the frame rate of 8 kHz, there are 193 binary digits per frame as determined by the T1 transmission line. Each of the 24 voice channels occupies a time slot of eight digits. This totals 192 digits leaving the 193rd digit available for framing. Because in every sixth frame the "eight" digit in each time slot is devoted to signaling, and furthermore, for some switching systems two signaling paths are required, it is necessary to identify a super frame of 12 frames of which the sixth and twelfth frames contain the two signaling paths. To accomplish this identification and still allow

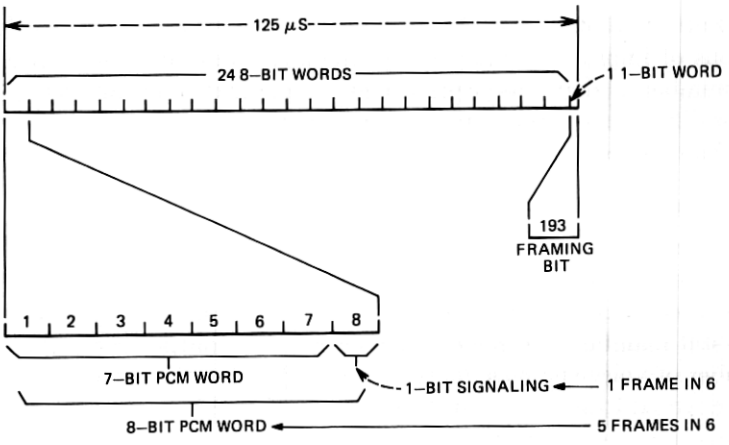



Fig. 1—D2 bit stream format.

rapid synchronization of the receiving framing circuitry, the frames are divided into odd and even frames. In the odd frames, the 193rd digit is made to alternate between 0 and 1. This allows the framing circuit to lock on and maintain synchronism. In the even frames, the 193rd digit is made to follow a 000111000111 ··· sequence. This identifies the sixth and twelfth frames as those that follow an 01 transition or 10 transition of this digit, respectively. When CCIS signaling is used, there is no need to identify the sixth and twelfth frames. The 193rd digits in even frames then become available for CCIS signaling.

### 2.3. *Companding Law and Code Format*

The companding law used in the original D1 Channel Bank is based on the nonlinear properties of diodes.* The biasing of the diodes is chosen to approximate a $\mu = 100$ companding law.[1] Careful selection of diodes and stringent temperature control of the diode environments are necessary to maintain matching of the compressor and expandor characteristics. To meet the requirement that any two D2 Banks may be interconnected at random under control of a digital switch, even more careful selection of diodes and tighter temperature control would be necessary if diode companding was used. For this reason, it is unlikely that the digital signals from D1 Banks that are based on diode companding can be switched to another similar bank with any assurance of

* Plug-in units will be available for D1 to make its companding law compatible with that of D2.

performance. At the time D2 was developed, techniques were available to achieve nonlinear coding directly. Among these were (*i*) the techniques of coding linearly and processing the result digitally to produce a nonlinear code, (*ii*) the technique of using a nonlinear feedback network in a digit-by-digit coding process, and (*iii*) the technique of stage-by-stage coding where each stage has one digit output and one nonlinear residue output. These techniques are capable of producing different classes of companding laws. In order to provide the greatest flexibility for future channel bank development, the choice was narrowed to two laws that can be implemented by any of the above techniques. The two laws are (*i*) the 13-segment approximation to the A-law that was actively being considered at that time as the standard for Western Europe, and (*ii*) the 15-segment approximation to the $\mu = 255$ law.[5] The $\mu = 255$ law (Table I) was chosen for D2 because it promised better idle circuit noise and crosstalk performance.[6] Conversion between the two laws is relatively simple.[7]

The most important property of either law is the digitally linearizable property. This allows simple digital processing to convert between companded PCM code words to linear PCM code words. In the linear

TABLE I—CODER THRESHOLD LEVELS AND STEP SIZES FOR 15-SEGMENT, $\mu = 255$ CODING LAW*

| Segment End Points | Step Size | Segment Number |
|---|---|---|
| $x_0 = 0$ | $\Delta x_0 = 1$ | 1 |
| $x_1 = 1$ | $\Delta x_1 = 2$ | |
| $x_{16} = 31$ | $\Delta x_2 = 4$ | 2 |
| $x_{32} = 95$ | $\Delta x_3 = 8$ | 3 |
| $x_{48} = 223$ | $\Delta x_4 = 16$ | 4 |
| $x_{64} = 479$ | $\Delta x_5 = 32$ | 5 |
| $x_{80} = 991$ | $\Delta x_6 = 64$ | 6 |
| $x_{96} = 2015$ | $\Delta x_7 = 128$ | 7 |
| $x_{112} = 4063$ | $\Delta x_8 = 256$ | 8 |
| $x_{128} = 8159$ | | |

* Points shown are for positive quadrant only; the negative quadrant is symmetrical. With the exception of the first, each segment contains 16 steps of equal step size $\Delta x_n$. The output levels are always midway between the threshold points. The table is normalized to 8159 so that all values are represented as integer numbers.

form, signal processing such as gain change, echo suppression, and signaling can be done digitally. Since some processing is expected on international connections or other long circuits, this processing point is then the logical interface between $\mu$-law and A-law regions.

To achieve the $\mu = 255$ companded coding, the stage-by-stage approach was chosen primarily because this approach had the greatest promise of achieving the necessary speed to code 96 voice channels on a time-shared basis.[8]

## III. SYSTEM OBJECTIVES

After the major system characteristics have been determined, a set of objectives can be formulated based on reasonable degradations from an ideal channel bank. In an ideal channel bank, the sources of degradations are (*i*) idle circuit noise, (*ii*) quantizing noise, and (*iii*) overload noise. These correspond to small signal, medium signal, and large signal characteristics of a PCM system. In a practical system, idle circuit noise and quantizing noise are expected to be worse than the ideal. Overload noise is not expected to differ from the theoretical value. In addition to the degradation attributed to the quantization process, there is also the degradation due to the sampling process. Some foldover noise (frequency aliasing) is expected due to incomplete removal of signal energy above the half sampling frequency of 4 kHz. Filter characteristics are designed with sufficient out-of-band attenuation so that this source of noise is negligible.

The voice-frequency transmission objectives set for D2 are listed in Table II.

The objectives on idle channel noise and signal-to-distortion can be interpreted as follows. For most of the talker volumes, the objective is

TABLE II—VOICE FREQUENCY TRANSMISSION OBJECTIVES FOR D2

| | |
|---|---|
| Overall Idle Channel Noise | <23 dBrnc0 |
| Interchannel Crosstalk Loss | >65 dB |
| Signal-to-Distortion Ratio | |
| C-Message Weighting | |
| Sine Wave Input | |
| +3 dBm0 to −30 dBm0 | 33 dB |
| −40 dBm0 | 27 dB |
| Overload Point | +3 dBm0 |
| Frequency Characteristics | |
| 300 Hz to 3,000 Hz | ±0.25 dB |

within 3 dB of the theoretically achievable performance. For very small signals such as those produced by noise and crosstalk, the objective is within 6 dB of theoretical. Overload point can be set arbitrarily, in the sense that every dB of overload results in a dB loss in low signal performance. As in D1, the desired overload point for D2 is near the peak of a +3-dBm0 sine wave.

The frequency characteristics of a channel bank is determined primarily by the filters. Toll transmission objectives for D2 require more complex channel filters than to D1.

## IV. SYSTEM DESCRIPTION

The overall block diagram of the D2 Channel Bank is shown in Fig. 2. Per channel equipment includes the channel unit, the transmitting and receiving filters and the multiplex and demultiplex gates. Common equipment performs analog-to-digital conversion at the transmitting terminal and the inverse operation of digital-to-analog conversion at the receiving terminal.

The total cost of a channel bank can be divided into per channel equipment and common equipment. Because of the additional operational and performance requirements necessary for toll operation, the per channel equipment is expected to be more elaborate and thus more expensive than that for D1. To offset this increased cost, the cost of common equipment can be reduced by sharing it over more channels. The most complex common circuits are the coder and decoder, which are shared by all 96 channels. Some common equipment is shared by fewer channels. Engineering judgment was exercised to decide between economy of operation, vulnerability to failure, and effect on working channels during repair whenever it was decided to share common equipment.

The equipment configuration of the D2 Bank also entered into the considerations concerning the maximum number of channels that can be processed on a timeshared basis by common equipment. A major portion of the bay space is taken up by the toll trunk channel units which contain a considerable amount of bulky components such as jacks and relays. Since it was decided to house all the equipment associated with the D2 Bank (including power converter and carrier group alarm) in a factory-assembled bay, 96 channels was the maximum number that could be accommodated on an 11-foot, 6-inch bay. Channel banks for exchange applications with less voluminous channel units could be designed to accommodate a larger number of channels in the same space.

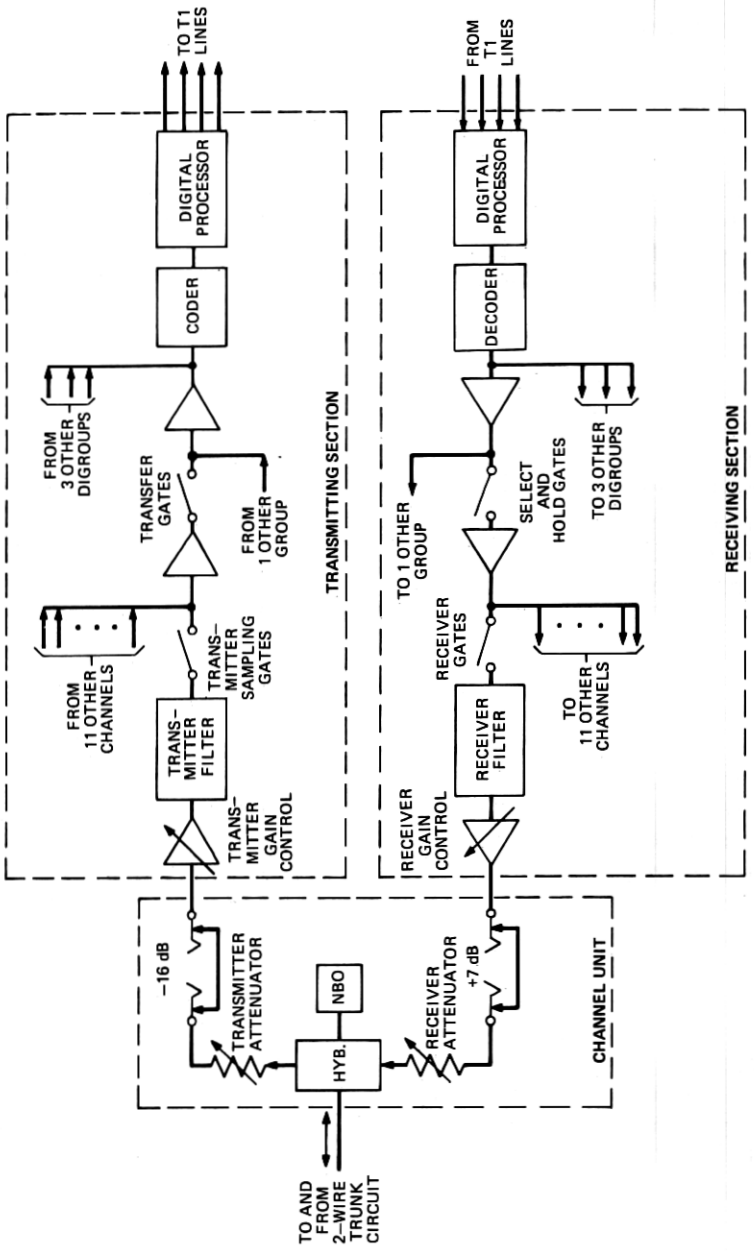



Fig. 2—Block diagram of D2 bank, showing the stages of time-division multiplexing into groups (12 channels), digroups (24 channels), and 96-channel signals.

### 4.1 *Channel Unit*

The interface equipment between trunk circuits, which are the terminations in a switching machine, and the channel bank, which terminates transmission systems, is contained in the channel unit. The basic functions performed are: (*i*) converting a 2-wire voice circuit into standard level 4-wire circuit, and (*ii*) converting the signaling states to digital form. These functions enable the switching machine to treat the voice channels that are derived by PCM techniques as if they were wire pairs. Each channel unit serves one channel, hence a fully equipped D2 Bank contains 96 channel units.

### 4.2 *Transmitting Terminal*

The transmitting terminal performs analog-to-digital conversion. This includes sampling, multiplexing, coding and digital processing. First, the signal from each channel unit is amplified and bandlimited by a lowpass filter to reject all signal frequencies above 4 kHz. The gain of the amplifier is adjusted to establish the correct level for coding for each channel. The bandlimited signal is then sampled 8,000 times a second by the sampling gate associated with this channel.

Since a single coder is time-shared to code the signals from 96 channels, it is necessary to time multiplex samples from these 96 channels. To achieve this in one step places severe crosstalk and noise limits on the sampling gates. A two-stage multiplexing scheme eases these problems and results in only moderate increase in complexity, since each gate in the second stage of multiplexing is shared by many channels. The number of channels for the first stage of multiplexing is chosen as 12. This number agrees with that of the D1 Bank and most frequency division systems. The eight PAM buses, each containing a *group* of 12 channels, are multiplexed together in the second stage. The resultant multiplex of 96 channels each occupying a time slot of 1.3 microseconds is converted sequentially to digital form by the coder.

The result of coding is a series of pulse-code-modulated digital signals called PCM words. These code words are processed by a coder output processor prior to its application to a digital transmission line. The purpose of digital processing is threefold: (*i*) the parallel digital output must be converted to serial form, (*ii*) signaling digits must be inserted at the appropriate times, and (*iii*) the digital signal must be split into four streams of 1.544 Mb/s each in bipolar format suitable for transmission over T1 lines.

### 4.3 *Receiving Terminal*

The receiving terminal performs the inverse operation of the transmitting terminal. It has a decoder input processor to bring the incoming digits into a parallel form for decoding by a single decoder, and it uses a two-stage demultiplexing process to distribute the decoded samples to the 96 low-pass filters which reconstruct the original signals.

Whereas it is relatively simple to split the output of the coder into four bit streams, combining four incoming bit streams for decoding by a single decoder is not as simple. The reason is that the four signals can originate from four different channel banks, each with a slightly different clock rate. Thus timing and framing signals are recovered from the four signals individually. Whereas the use of four separate decoders will result in the same apparent complexity as the use of a single decoder which requires digital circuits to combine four asynchronous signals, the single decoder approach results in less analog circuitry. Digital circuits necessary for single decoder operation are simple to build and are more amenable to integrated electronics technology.

The decoded samples undergo two demultiplexing steps to redistribute the signals to the 96 channels. The procedure is the inverse of the one used in the transmitting terminal. The first step demultiplexes the output of the decoder into eight groups of 12 channels each, and the second step demultiplexes each of the eight signals into individual channels for reconstruction by the receiving lowpass filters. In addition to demultiplexing, the first step also removes the timing jitter imparted to the signal by the process of sharing a single decoder. Since the decoder is shared, a digital code word arriving on one of the four lines must queue up for decoding; the waiting time can be as long as 5 microseconds (one word time slot on the line). This waiting time is absorbed by the select and hold circuit, which acts as an analog store as well as a demultiplexer.

## V. FEATURES

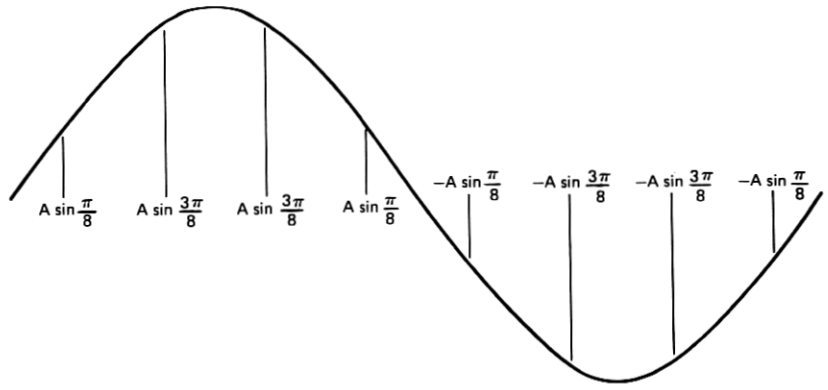
One important factor in the system design of the D2 Channel Bank is the provision for simplifying the installation and maintenance procedures including gain adjustments and noise measurements. For these purposes, a test panel is built into the D2 bay. This test panel contains standard signal sources, signal and noise test set interface equipment, and signaling test sets. The test panel provides convenient access to standard, permanently installed central office equipment.

Flexible jacking arrangements are also provided so that measurement of transmission, noise, distortion and crosstalk on all voice channels can be accomplished by one man with no portable test equipment.

### 5.1 *Digital Signal Generator*

To allow D2 to achieve a consistent correspondence between analog signals and their digital representation, a digital signal generator (DSG) is provided as a unique feature of the test panel. This circuit provides an invariant digital reference level for calibration purposes. The digitally derived signal consists of a repetitive sequence of eight PCM words. This signal is defined to be identical to a PCM signal that would be produced if a 0-dBm sinusoidal test tone of 1 kHz, synchronized with the sampling frequency, were encoded by a perfectly gain-adjusted transmitting terminal. The eight binary words that define the signal are listed in Fig. 3. The signal from the DSG can be inserted into any one of the four incoming PCM lines.

The DSG greatly simplifies the installation and maintenance procedures, including gain adjustments and distortion measurements. Prior to D2, the line-up of transmission systems required at least one man at each of the end terminals. One man would connect a calibrated signal at the transmitting end, while another man would perform




| DIGIT | CODE WORD SEQUENCE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 6 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 8 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

Fig. 3—The digital 1-kHz reference signal.

measurements and adjustments at the receiving end. The D2 Channel Bank takes advantage of the fact that the transmission line is digital. The digital line does not introduce loss or distortion to the coded analog signals. Only the analog circuits of the transmitting terminal and the receiving terminal each require adjustment. A terminal adjusted with the transmitting section looped to its own receiving section has the same transmission performance as that adjusted with distant terminals. This permits independent line-up of each terminal without requiring the assistance of personnel at the remote terminal location.

The first step in this procedure is to insert the digital 0 dBm0 signal into the input line of the receiving terminal. The gains of the voice-frequency amplifiers are adjusted so that the voice-frequency output for each channel is exactly 0 dBm0. Next, the transmitting terminal is looped* to the local receiving terminal in order to line up the transmitting section. A 0-dBm sinusoidal signal is applied to the voice-frequency inputs of the transmitting section and the gains of the transmitting voice-frequency amplifiers are adjusted until 0 dBm0 is detected at the receiving section voice frequency output.

An important result of this method of line-up is that once the gains are aligned with respect to this well-defined digital signal, any one D2 Bank can be digitally switched to any other D2 Bank, or any other bank so adjusted, without changes in signal levels and without variation in gain. This is a significant step towards the possibility of switching the voice signals in their digital form.

When the terminal is adjusted in this manner, the overload point of the D2 Bank is consistently 3.17 dBm0. This is a fraction of a quantizing step from the objective of 3 dBm0.

### 5.2 *Performance*

All of the performance objectives for the D2 Channel Bank have been met in the laboratory model during the development of the D2 Channel Bank. Difficulty was encountered for the production models with regards to the idle channel noise performance. All other performance objectives are met by the production models. The original idle channel noise objective was based on the fact that, according to the smallest step size of the coder near the origin, the theoretical noise floor should

* Since the transmitting terminal output line is looped to the receiving terminal input line, looping can only be accomplished on a 24-channel basis. At initial installation procedures, this presents no problem. However, when the bank is in service and a single channel is to be lined up, it would be necessary to busy out the other trunks on that line prior to looping. In such situations, it may be advantageous to use line-up procedures which may involve personnel at both terminals.

be about 18 dBrnC0. The original objective of 23 dBrnC0 allows 5 dB greater noise to account for imperfections in multiplexing and coding. It turns out, however, that although the mean of the idle circuit noise is fairly close to the theoretical noise floor, the standard deviation is much larger than anticipated.

A histogram of idle channel noise of approximately 100 production D2 Channel Banks, is shown in Fig. 4. The mean is 18.6 dBrnC0 which is very close to the theoretical noise floor. The standard deviation is 1.9 dB. For production testing it was found that a 23 dBrnC0 requirement is not realistic in view of this large standard deviation. The average noise contributed by the D2 Bank remains well below the original objective. Because of its large variation, idle channel noise on a few channels of a particular D2 Bank can be as high as 26 dBrnC0. Since the grade of service[9] is based on probability of an unacceptable circuit consisting of several channel banks in tandem, isolated above-average noise in one channel of one link will not increase this probability.

Signal-to-quantizing noise performance of the D2 Channel Bank is shown in Fig. 5. This figure illustrates the performance of two typical channels; one with very low idle channel noise, and another with relatively high idle channel noise. It is seen that, for medium-to-high signal levels, the quantizing noise performance is very close to the theoretical ideal performance. For a low-level signal, the idle channel noise of the D2 Bank dominates. The small signal performance of the coder by itself tested in its own test set exhibits almost ideal signal-to-noise performance even for small signals.[8]

Because the companding characteristics of the coder and decoder

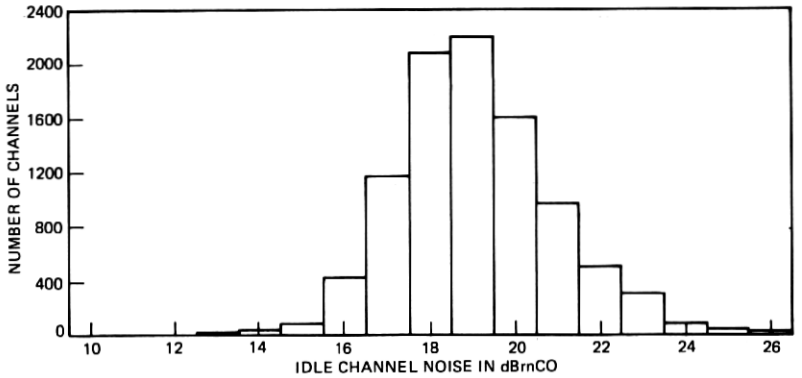



Fig. 4—A histogram of idle channel noise of approximately 100 production D2 Channel Banks.

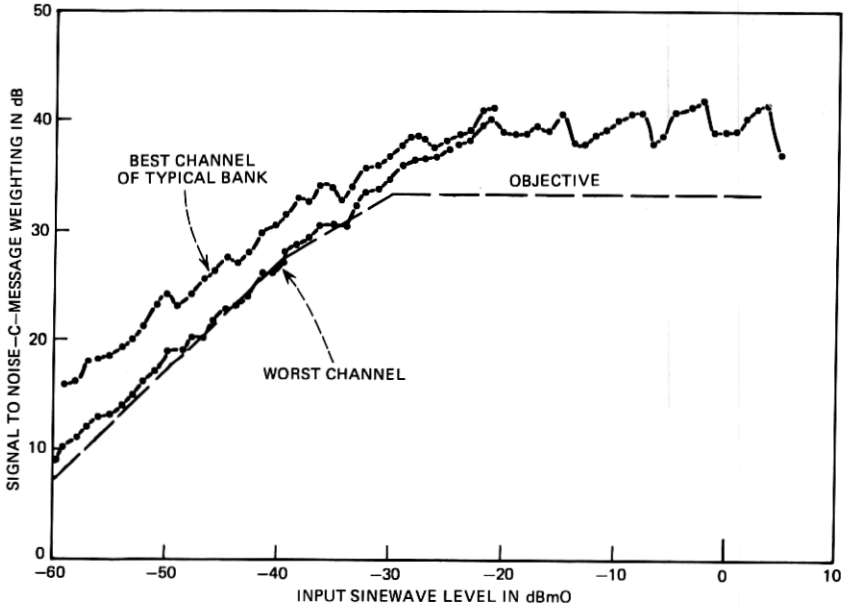



Fig. 5—Signal-to-noise performance of the D2 Channel Bank.

are controlled by highly precise thin-film tantalum resistors, they are expected to be very stable so that field adjustments in any of the common equipment were not necessary. Experience with the gain stability of the voice-frequency amplifiers indicates that analog transmission paths (voice-frequency amplifiers, filters, and gates) have long-term stability to within 0.1 dB after initial alignment.

## VI. SUMMARY

This article has summarized the system design considerations of the D2 Channel Bank. The next four articles will cover more detailed circuit aspects of (*i*) the trunk interfaces which includes channel units and filters, (*ii*) multiplexing and coding, (*iii*) digital processing, and (*iv*) power conversion. The last two articles cover aspects of bringing a product into fruition that are often neglected in the literature. These are physical design, development for manufacture, testing, and continued surveillance and product improvement.

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