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A Fast Bipolar-IGFET Buffer-Driver

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This paper discusses the performance and interface advantages of a self-isolating bipolar-IGFET (BIGFET) integrated structure as an output buffer-driver for IGFET integrated circuits. The low-capacitance, high-impedance input and low-impedance, high-current output characteristics make the BIGFET ideally suited to drive large output capacitances and to interface with bipolar logic circuits. It is shown that in a shift register application the operating speed is increased substantially when the BIGFET is used as output buffer and is essentially independent of output capacitance up to 100 pF. The application of BIGFET output circuits to 5-volt T^2L and 3-volt collector-diffusion-isolation (CDI) T^2L is also discussed.

I. INTRODUCTION

Due to the high output impedance normally associated with Insulated-Gate Field-Effect Transistors (IGFET) two problems often arise in digital IGFET integrated circuits: (*i*) Charging and discharging times for capacitances external to the integrated circuit are long compared to the corresponding times for internal circuit nodes. (*ii*) Interfacing with bipolar logic requires IGFETs to provide and/or sink currents which are larger than those normally available from IGFETs with typical integrated circuit geometries. Attempts to solve these problems usually involve large IGFET inverters or push-pull drivers as output stages. Since these types of output interface circuits employ large-geometry IGFETs and have higher input capacitances than those capacitances typically found at the nodes of the internal IGFET circuitry, the overall result is that circuit speed is degraded at the output interface.

This paper discusses the use of a self-isolating bipolar-IGFET (BIGFET) integrated structure in an output buffer-driver. Although this structure has been previously proposed,[1-3] there have been no reported experimental studies of improved circuit performance when the BIGFET is incorporated directly on a monolithic p-channel IGFET

integrated circuit. Since the BIGFET is capable of providing a low-capacitance, high-impedance input and a low-impedance, high-current output, it provides an almost ideal solution to the interface problems discussed above.

II. DEVICE STRUCTURE AND CHARACTERISTICS

A schematic and device cross section of a BIGFET are shown in Fig. 1. The structure is basically an IGFET and a vertical npn bipolar transistor in cascade. The collector of the npn transistor is common to the Silicon Integrated Circuit (SIC) substrate. A p-type diffusion performs the dual role of bipolar transistor base and p-channel IGFET drain. The emitter is formed by the same phosphorus diffusion that is used to make ohmic contact to the 6–9 Ω-cm n-type substrate.

The current-voltage characteristics for a typical BIGFET with $V_T = -1.0$ volt and $h_{FE} = 140$ at $I_c = 10$ mA are shown in Fig. 2. It may be seen in the figure that the output current is in the range of tens of milliamperes, although the IGFET gain factor, $\beta[(\mu\kappa\epsilon_o/t_{ox})W/L]$, for this structure is only 100 μmhos/volt. The overall effective gain factor is just the product of β and h_{FE} or, in this case, 14,000 μmhos/volt. Therefore, when using this structure for high-current output circuit applications, one may employ a small gain factor IGFET with correspondingly low input capacitance. Since this input capacitance need be no greater than that found at a typical internal node of an IGFET SIC, the delay through the BIGFET output-buffer, in turn, need be no greater than the intrinsic delays associated with the internal IGFET circuitry.

BIGFETs with the structure discussed above have been routinely

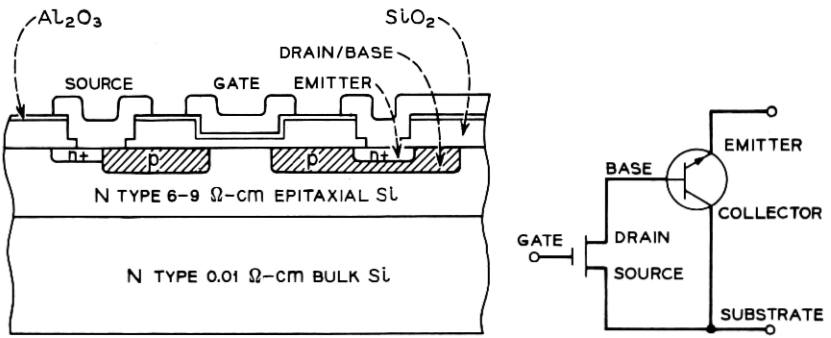

Fig. 1—BIGFET device schematic and structure.

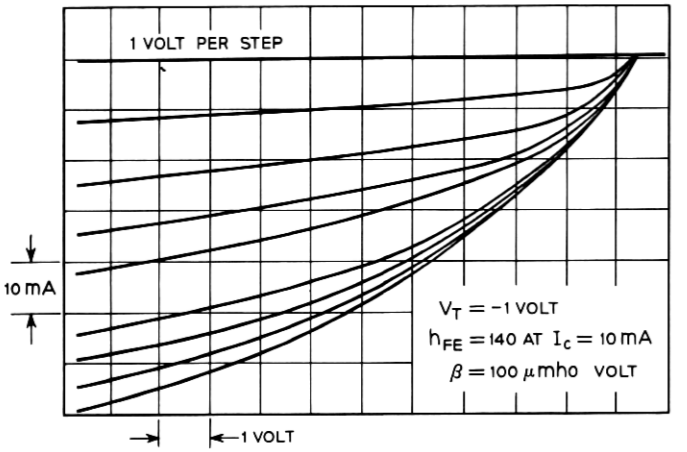

Fig. 2—BIGFET current-voltage characteristics.

fabricated with a minimum h_{FE} of 60 at $I_c = 1$ mA. Preliminary life-test data indicate that an end-of-life limit for h_{FE} of 50 is feasible for high-reliability applications. The temperature dependence of h_{FE} is $(dh_{FE}/dT)/h_{FE} \sim 1$ percent per degree from 0° to 80°C.

III. CIRCUIT PERFORMANCE

In order to assess empirically the circuit performance improvements achievable through the use of a BIGFET output driver, two four-bit static shift registers were designed, fabricated, and tested. One version of the shift register (SR1) has a large IGFET inverter ($\beta_{\text{driver}} = 60$ μmhos/volt) as the output stage. The βs of the IGFETs in the third and fourth bits are appropriately increased to achieve optimum design for maximum circuit speed. The second version (SR2) uses a BIGFET output driver which consists of a normal IGFET inverter ($\beta_{\text{driver}} = 20$ μmhos/volt) in cascade with a bipolar emitter follower. For the case of SR2, there was no increase in the gain factors of the IGFETs in the shift register bits just preceding the BIGFET buffer-driver. The two shift registers are shown schematically in Fig. 3.

To measure the maximum clocking frequency ($f_{\max}$) of the two shift registers, a 7-inverter cascade with a BIGFET output stage was used as signal discriminator. Signals from the shift register were acceptable only if they were capable of propagating through the seven-stage inverter cascade. Two voltage bias conditions were studied. In one case $V_{GG} = -3.0$ V and $V_{DD} = +5.0$ V while for the other $V_{GG} = 0$ V and $V_{DD} = +5.0$ V.

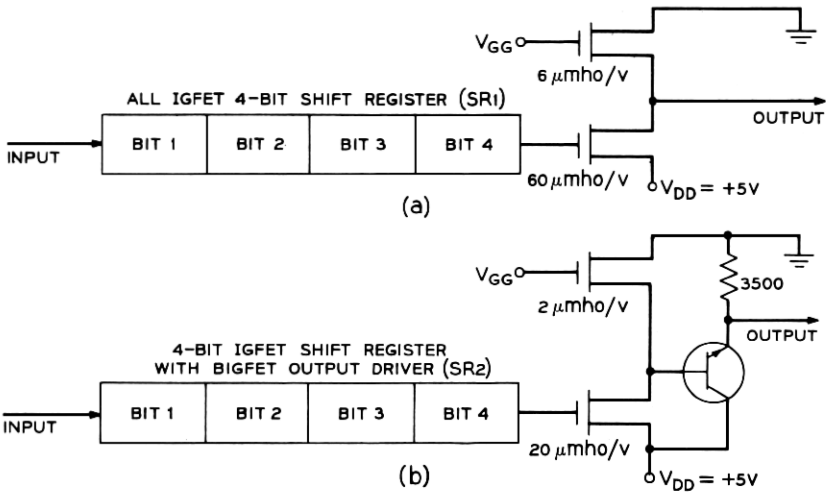

Fig. 3—Experimental circuits for comparative speed performance measurements.

The experimentally measured results for the two types of shift registers are summarized in Fig. 4. The maximum operating frequency is plotted as a function of the output capacitive load (C_o) for the two stated supply conditions. For SR1, f_{max} is twice as high at low values of C_o when two supplies are employed as when a single 5-volt supply is used. However, f_{max} decreases with increasing C_o at essentially the same rate regardless of the supplies used. On the other hand, SR2 is

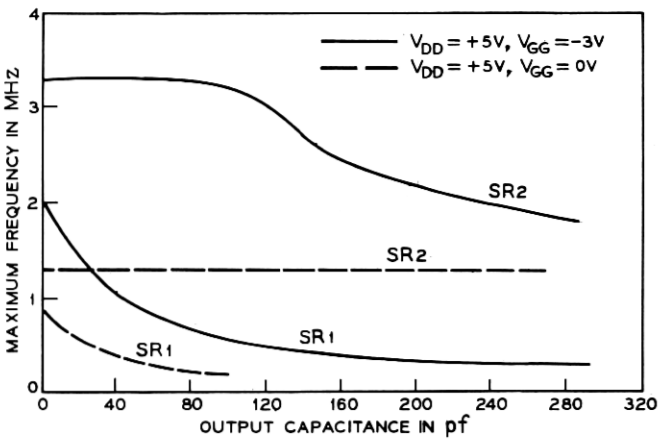

Fig. 4—Experimental performance results for all-IGFET (SR1) and BIGFET-output (SR2) shift registers.

capable of operating at 3.3 MHz for small values of C_o when two supplies are used and remains independent of C_o up to 100 pF. Beyond 100 pF the maximum operating frequency falls off in the same manner as SR1. In the single-supply case, f_{max} for SR2 is independent of C_o over the range investigated. Further comparison of the integrity of output waveforms with and without the BIGFET output buffer is demonstrated in Fig. 5. It can be seen that the output waveforms of SR1 with an IGFET output circuit are grossly degraded by the loading of 100 pF. The output of SR2 with the BIGFET is almost unaffected.

IV. CIRCUIT INTERFACE

In addition to its usefulness as an output driver, the BIGFET is also extremely versatile as a buffer to interface IGFET integrated circuits with bipolar logic. To interface with any bipolar logic, the primary design consideration is that the driver gate must furnish as well as sink currents required by the loading bipolar gate. The net result is that the value of the BIGFET emitter resistor R_E must be carefully chosen to reflect this requirement.

As an example, the choice of 1500 Ω for R_E allows a straightforward interface from BIGFET to low-power 5-volt T^2L logic. The circuit

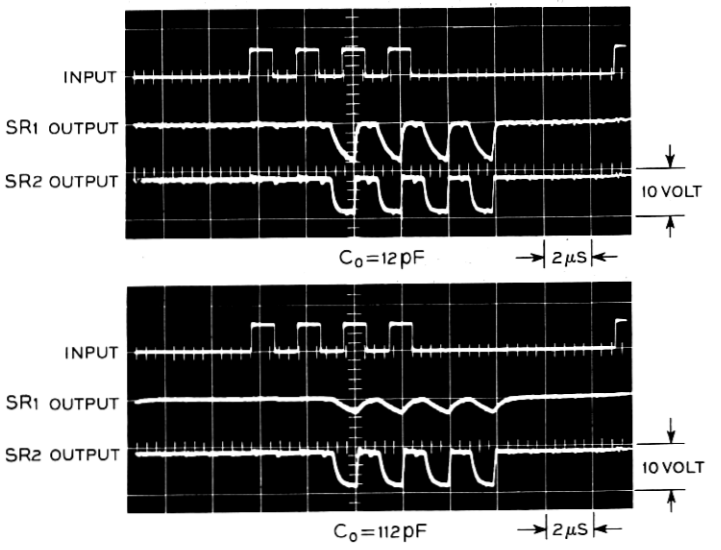

Fig. 5—Effects of capacitive loading on output waveforms for all-IGFET (SR1) and BIGFET-output (SR2) shift registers.

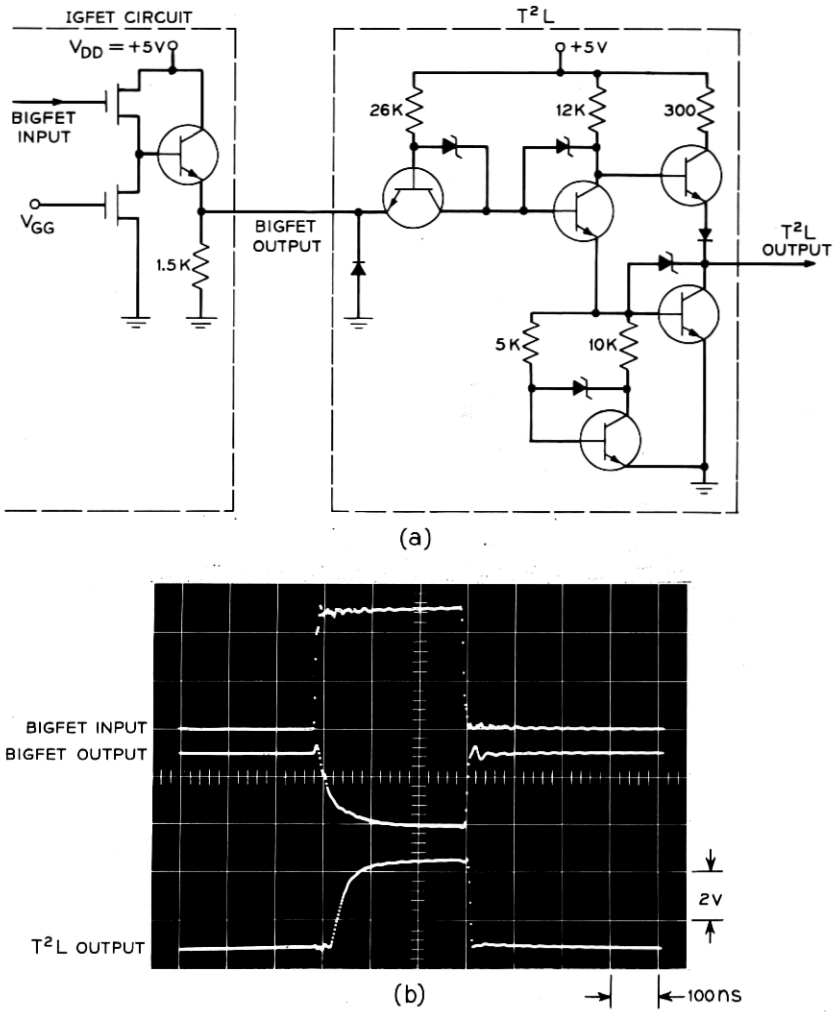

Fig. 6—(a) Circuit schematic of BIGFET-T²L interface. (b) Typical waveforms for BIGFET-T²L interface.

schematic is shown in Fig. 6a and the input and output waveforms of the circuit interface are shown in Fig. 6b. In like manner, a suitable choice of R_E allows the BIGFET to interface with RTL and DTL.

Interfacing with the 3-volt collector-diffusion-isolation (CDI)[4] T²L logic is less straightforward. If the same voltage biasing condition, i.e., R_E grounded, is used one finds that an R_E ladder of 900 Ω and 300 Ω

is needed to meet the current and voltage requirements of CDI-T²L. This is shown in Fig. 7a. The circuit shown requires a ±10-percent tolerance on the 300-Ω resistor which is not desirable for a high-yield, low-cost integrated circuit technology. Since a −3-volt supply is often available in low-threshold (V_T = −1 V) IGFET SIC applications, a higher-value and relaxed-tolerance R_E (~ 1500 Ω ± 20 percent) may be used if the emitter resistor is connected to the −3-volt supply. A schematic of this circuit configuration is shown in Fig. 7b.

Due to the voltage drop across the driver IGFET and the V_{BE} of the bipolar portion of the BIGFET, the output voltage level from the emitter follower may not be sufficient to provide adequate dc noise margin for low V_T IGFET SICs. However, this problem may be overcome by the introduction of a "pull-up" IGFET in parallel with the BIGFET output and using an IGFET as the active emitter load. This is shown in Fig. 8. The only requirement is that a gating signal

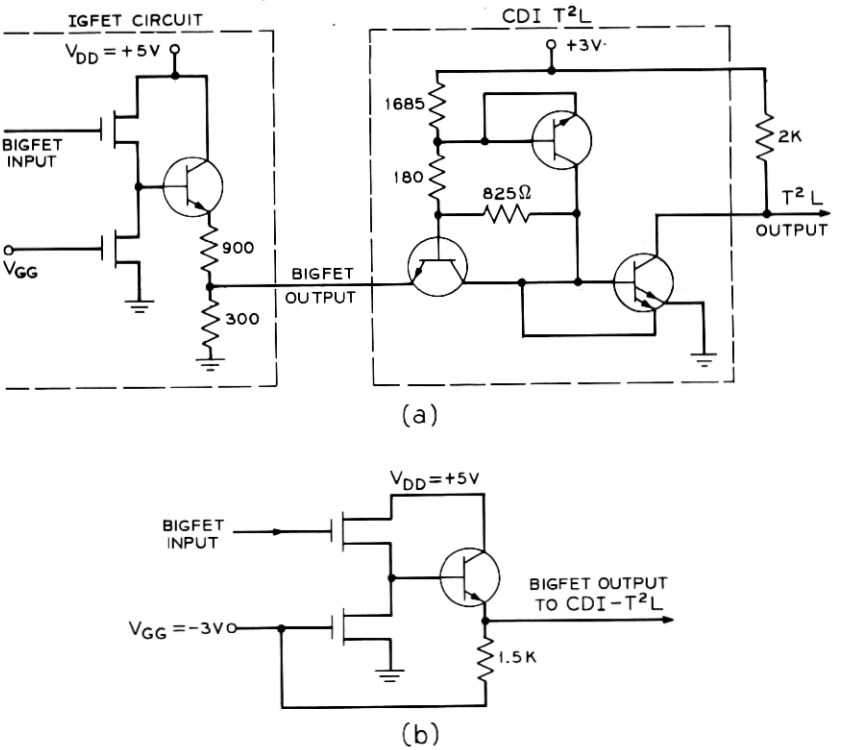

Fig. 7—Circuit schematic for BIGFET-T²L (CDI) interface: (a) resistor ladder output. (b) single emitter resistor.

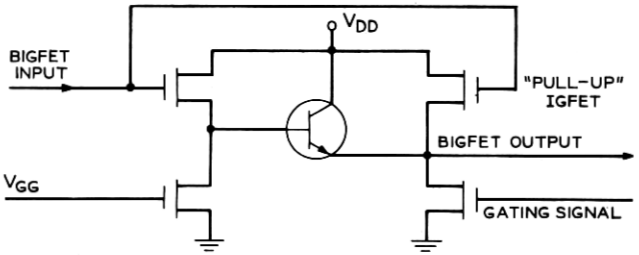

Fig. 8—IGFET "pull-up" circuit for BIGFET-IGFET interface.

must be applied to turn off the IGFET emitter load when the bipolar transistor and the associated "pull-up" IGFET are on. Such a gating signal is often conveniently available on circuits with timing signals, e.g., IGFET shift registers. An alternate solution is to provide a voltage level shifting buffer such as an IGFET source-follower at the input of the IGFET circuit to which the BIGFET interfaces.

V. CONCLUSION

This work demonstrates that there are significant advantages in using an integral bipolar-IGFET functional element as a fast interface buffer-driver. Specifically, the BIGFET driver

(*i*) requires no additional processing for isolation since the bipolar collector is common to the IGFET substrate,
(*ii*) significantly increases overall speed in multi-integrated circuit applications by reducing circuit-to-circuit propagation delays, and
(*iii*) allows direct interface with most forms of bipolar logic.

VI. ACKNOWLEDGMENTS

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