An Experimental 224 Mb/s Digital Multiplexer-Demultiplexer Using Pulse Stuffing Synchronization

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Solid-state device and circuit technology has advanced to the point where processing of digital signals with bit rates as high as 224 Mb/s may be accomplished. As a specific demonstration of this fact, an experimental multiplexer-demultiplexer has been developed which combines the following signals into a 224 Mb/s binary pulse train for transmission over a digital transmission network and which furnishes the necessary processing to reconstitute the original signal components:

i) A PCM-coded commercial color video signal (111.2 Mb/s)

ii) A PCM-coded FDM mastergroup signal (55.6 Mb/s)

iii) Two T1 carrier (24 voice channel TDM) signals (1.544 Mb/s each)

iv) Word generator signals to occupy the remaining time slots.

The line bit rate is derived from and is therefore synchronous with the coded video signal; however, the coded mastergroup and T1 carrier signals are derived from independent clocks. Synchronization of the latter two signal types has been achieved through the use of pulse stuffing synchronization with added-bit synchronization signaling.

The ability of a 224 Mb/s buffer memory coupled with a phase-locked loop to attenuate adequately the timing jitter which accumulates in a long digital transmission network has also been demonstrated.

All of the experimental results have indicated that the realization of a commercial high-speed digital multiplexer-demultiplexer is feasible.

I. INTRODUCTION

Elsewhere in this issue is a description of an experimental digital transmission terminal which has been used to demonstrate, among other things, the feasibility of multiplexing a variety of asynchronous* digital

* The term asynchronous as used here means a lack of synchronism both among the various signals being multiplexed and with the multiplexing clock. The individual digital signals taken separately are synchronous following the normal usage of the word in data transmission in that pulses occur at regular clock intervals.

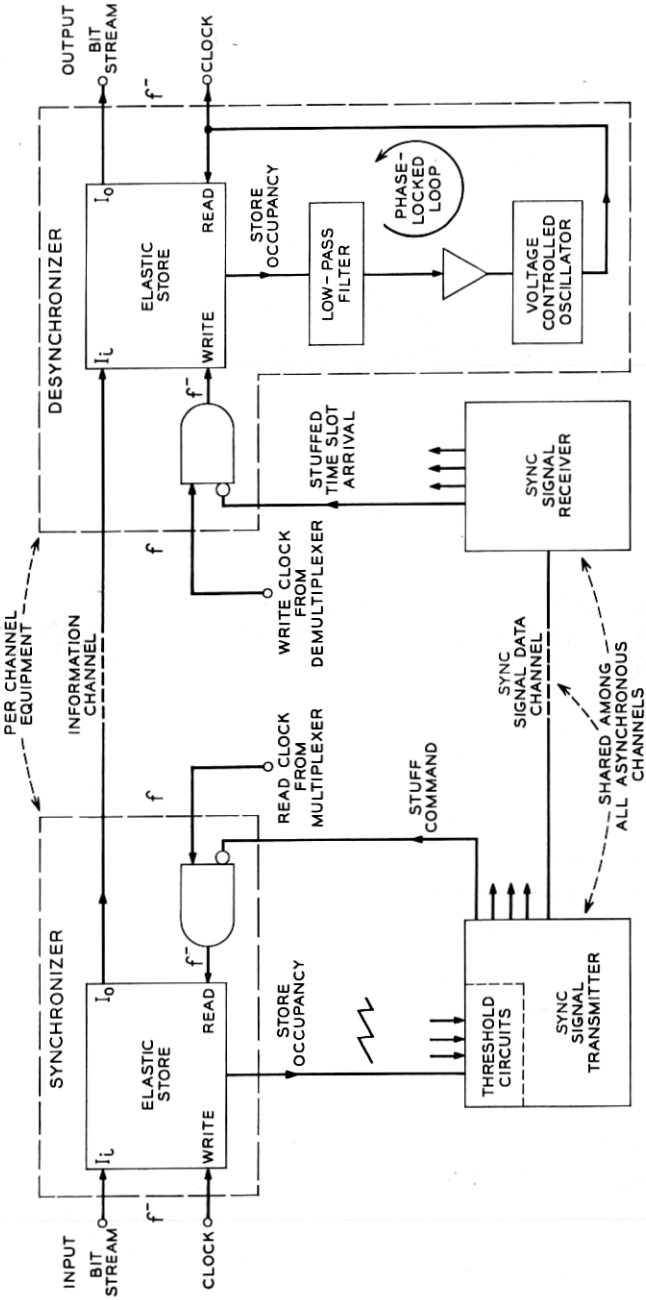


Fig. 1 — Pulse stuffing synchronization.

signals (PCM-video, PCM-SSB-FDM, data, coded *PICTUREPHONE** signals, and lower bit-rate PCM) into a 224 Mb/s binary pulse train.[1] This paper gives a more detailed description of the techniques used for multiplexing and demultiplexing, synchronization and timing jitter reduction. Also, a number of the high-speed digital circuit techniques which were employed are disccused.

II. PULSE STUFFING SYNCHRONIZATION

A variety of solutions have been proposed for the problem of synchronizing a large digital transmission network.[1] The method used in this system is that of pulse stuffing.[2,3] In concept, the technique is simply to constrain the bit rates of all multiplexed asynchronous signals to be slightly less than the bit rates needed at the multiplexer. These asynchronous signals are each passed through processing circuits, called "synchronizers," which sense the amount by which the bit rates must be increased to be synchronous with the transmitted clock. A buffer memory in each synchronizer, called an elastic store,[4,5,6] allows time slots to be added at a rate equal to the difference between the synchronous and asynchronous bit rates;† this difference is referred to as the stuff rate. The position of the stuffed time slots is signaled to the demultiplexer over a data channel which contains the synchronization information for all asynchronous channels. At the receiving terminal, the data channel is decoded, and the stuffed time slots are removed from the various signals which had been synchronized by "desynchronizers." This synchronization by digital signal processing is independent of the format of the signals which are multiplexed, and it achieves complete integrity of the information pulse streams. The only change which a digital signal undergoes is the addition of some timing jitter, and it will be shown that this jitter can be held to a sufficiently small amplitude so that the performance is quite suitable for application to a commercial system.

A simplified block diagram showing synchronization by pulse stuffing is shown in Fig. 1. The incoming pulse train at bit rate f^- is written into the synchronizer elastic store using the associated timing for a "write" clock. The store is read with a "read" clock of frequency f which is slightly higher than f^- and synchronized with the transmitting clock. By means of a phase detector, the elastic store furnishes an output which is

* A service mark of the American Telephone and Telegraph Company.

† Asynchronous bit rate and synchronous bit rate are terms defined here to describe the bit rates of the signal before and after it has been processed by the synchronizer.

proportional to the occupancy of the store. Since f is greater than f^- the store would become depleted, but before this happens a threshold circuit in the "sync signal transmitter" causes an inhibition of the read clock for one time slot. This action enables the elastic store to "recover" and results in an output time slot which corresponds to none of the input time slots, i.e., contains no message information. The sync signal transmitter also transmits over a data channel the position of the "stuffed" time slot.

At the receiving end of the system, the sync signal receiver decodes the signal from the data channel and inhibits the writing of the stuffed time slots into the desynchronizer elastic store. After inhibition, the bit rate of the signal is f^-, the asynchronous bit rate, but the timing contains abrupt phase discontinuities one time slot in amplitude. These phase discontinuities are reduced in amplitude by using a phase-locked loop to provide a read clock which is a smoothed version of the write clock.

III. FORMAT SELECTION*

Selection of the digital line bit rate was based on the bit rate of the digital signal components and the economic and technical aspects of regenerative repeater design. The signals which played a dominant role in the format selection were the PCM mastergroup (600 SSB-FDM voice channels) (~3 mc bandwidth × 2 samples/cycle × 9 bits/sample = 54 Mb/s), the PCM color video signal (~6 mc bandwidth × 2 samples/cycle × 9 bits/sample = 108 Mb/s)[2] and the T1 carrier 24-channel PCM signal (1.544 Mb/s).[7] A composite bit rate was chosen which would allow the multiplexing of four PCM mastergroups or two PCM color video signals or combinations of these and other signals. A bit rate slightly in excess of 216 Mb/s, but a multiple of 1.544 Mb/s, would seem appropriate. There are, however, other factors, including multiplex framing and synchronization signal signaling, which influence the bit rate selection.

3.1 *Multiplex Framing*

Of the several ways in which the various line signal components can be identified at the demultiplexer, the method of added-bit framing was used because it places very few restrictions on line format and it is relatively simple to implement. This technique, similar to the one used in the T1 system, allocates one time slot every 145 high-speed time slots to

* For a more detailed description of the line format selection, see Ref. 1.

an alternating ONE-ZERO pattern.* Thus, a "multiplex frame" is 145 high-speed time slots long. This selection yields a further system simplification: The multiplex frame rate is chosen to be the synchronous T1 carrier bit rate [(1.544 Mb/s) + δ ppm†]. The quantity δ is added to allow for the frequency offset required for pulse stuffing of T1 carrier signals.‡ The synchronous coded mastergroup and coded video bit rates are [(1.544 × 36 = 55.584) Mb/s + δ ppm] and [(1.544 × 72 = 111.168) Mb/s + δ ppm], respectively. The line bit rate becomes [(1.544 × 145 = 223.880) mc + δ ppm]. Fig. 2 shows several ways in which the 224 Mb/s line can be loaded. Bit interleaving is used because it simplifies the processing circuitry and allows the use of relatively small buffer memories.

The time slots for all signals to be multiplexed are uniformly spaced. Therefore, a phase discontinuity must be introduced into any signal which is not arriving at the frame rate (or some submultiple of it) in order to accommodate the framing pattern. This discontinuity will be referred to as the framing gap and, expressed in time, it must be precisely one high speed time slot in amplitude. To generate the framing gap in the information pulse stream, some form of memory is required.

The basic technique for accomplishing framing gap insertion and, at the same time, synchronizing the line frequency to a separate clock, is shown in Fig. 3. In the case shown, the line bit rate is synchronized to the incoming bit rate of a video pulse train which is to be multiplexed onto the line. Basically, three distinct functions are accomplished by the circuit shown. First, the framing gap is formed in the multiplexer clock circuits by means of the divide-by-145 counter containing an inhibit gate. Secondly, the multiplexer clock is synchronized to the video coder clock by means of a phase-locked loop. Lastly, in order to establish the phase discontinuity without errors in the information pulse train, a two-bit elastic store is used. Write and read clock signals for the store have a frequency of one-half the video signal bit rate since an n-bit store requires clock signals at $1/n$th of the bit rate. The reason for use of this frequency will become more apparent in Section 5.2.1 where the elastic store is described in more detail.

An explanation of the gap generation follows: Assume that the output

* A more complicated pattern could have been used at some expense in circuit complexity, but the reframe time performance with the simple scheme described above is adequate.

† ppm = parts per million.

‡ In the experimental terminal, the nominal offset δ for T1 carrier signals was chosen to be 60 ppm. Note that the offset need not be the same for other services; in fact, for the coded mastergroup, it was chosen to be 24 ppm, i.e., the nominal bit rate for the incoming coded mastergroup is [(1.544 × 36) Mb/s + (60 − 24)ppm] = [55.584 Mb/s + 36 ppm].

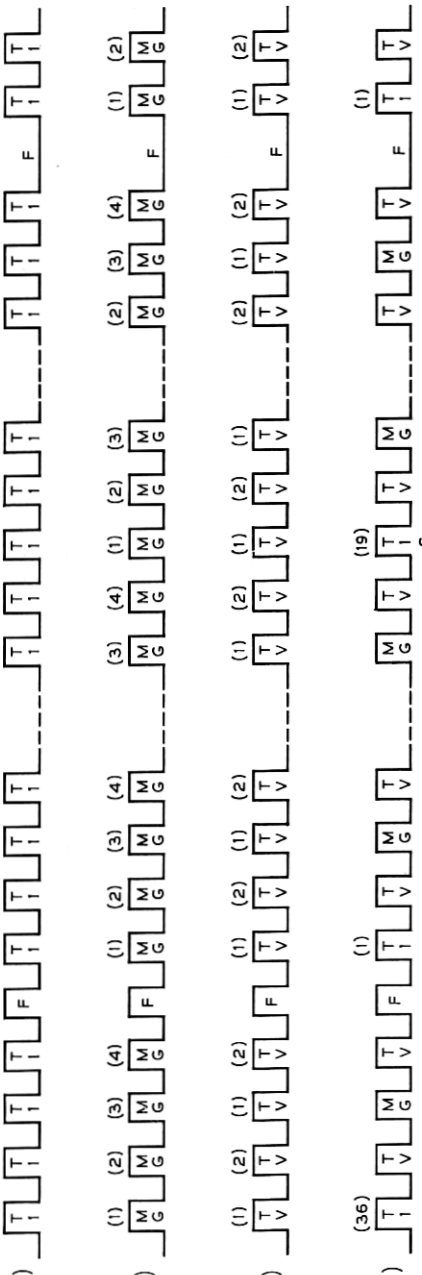


Fig. 2 — Some high-speed digital line loading possibilities.

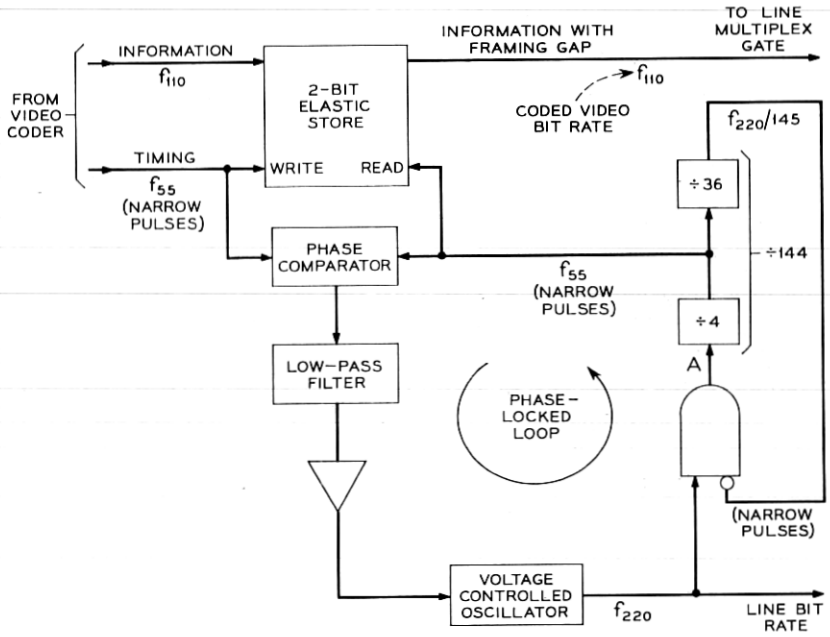


Fig. 3 — Framing gap insertion.

signal of the VCO is at the desired line bit rate. Entry of every 145th pulse into the divide-by-144 circuit is prevented by the inhibit gate. The net result is that at point A in Fig. 3 a pulse train exists which occurs at the line bit rate, but has every 145th pulse missing — thus, the framing gap. Part way through the counter (after division by four) the desired read clock rate is available with the framing gap. The phase-locked loop forces the average pulse repetition rate of the write and read clocks to be the same, and it synchronizes the line bit rate to the video bit rate.

The alternating ONE-ZERO pattern, which is placed in the framing gaps, yields a maximum average reframe time of 188 μs. This theoretical result is based on an assumption that the 144 information time slots contain a random pattern and that, in the search mode, the time slots are examined on a one-per-frame basis. To the above figure must be added a "flywheel effect" which results from the fact that, in order to control the misframe rate, the "frame detector" has been designed so that it does not begin searching until several framing pattern errors have been observed. The flywheel effect, adjusted for moderate line error situations (error rate $<10^{-6}$), adds a negligible amount to the reframe time.

3.2 *Synchronization Signaling*[8]

As mentioned in Section II, the signaling which identifies the inserted synchronizing time slots is sent over a data channel. A variety of methods exists for establishing the synchronization signaling data channel. To achieve independence of the format of the signals which are being synchronized, however, a separate time slot per frame is devoted to sync signaling. It will be seen that the information handling capability of this channel (1.544 Mb/s) is more than adequate to handle the synchronization of a full complement of asynchronous channels on the high-speed line. Because this channel contains data which is needed by all synchronized signal channels, certain steps were taken to make it relatively immune to line errors and to provide rapid recovery in the event multiplex framing, and thus the sync signaling channel, is lost. To these ends, within the sync signaling channel, stuff occurrence is redundantly coded and a code highly immune to errors is used for sync signal frame identification. Another feature of the format chosen is the one-for-one correspondence between stuff signal organization and line organization; hence, this organization lends itself to convenient dropping and adding of channels at points along a route.

In an operational system patterned after the experimental system described herein, the signaling pulses might occupy a single time slot per frame located midway between multiplex framing time slots and would be called "added-bit signaling." Thus, the sync signaling bit rate would be 1.544 Mb/s + δ ppm. For simplicity, however, the sync signaling for the experimental system was transmitted over the 73rd time slot of the frame and appears as a single T1 carrier channel. This time slot is identified by an "S" in Fig. 2(*d*), and the sync signal will be referred to as the "S bit" in what follows.

Fig. 4 shows the S-bit format. The C words (000 when no stuffing has occurred and 111 when it has) redundantly signal the presence of inserted time slots. At the demultiplex point, two out of three ONES are interpreted as a stuff indication. When an all-T1 carrier loading is used,

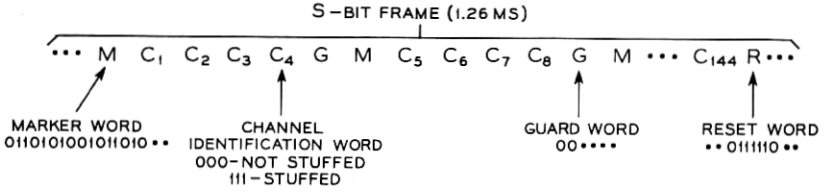


Fig. 4 — S-bit format (simplified).

each C word of an S-bit frame is allocated to a corresponding T1 carrier channel; for each mastergroup, 36 C words per S-bit frame are used, and for video, 72.

A key part of the sync signaling is the M word which is used to frame the S bit. It is the 16-bit word shown in Fig. 4 which has the characteristic that it can be identified exactly in an S-bit pulse train even though two errors exist anywhere within it. In many cases, more than two errors can exist and identification is still unique. An M word is inserted every fourth C word to allow for rapid reframing of the S bit for the higher bit rate synchronized channels. Reframing of the S bit for T1 carrier synchronization can take as long as a complete S-bit frame since the reset code, R, must be decoded to allow proper C-word association. The guard words, G, are strings of ZEROS which allow a simplification of the M word.

The format for the S bit as described above is inefficient in bandwidth usage because the statistical variations of the stuff rates used cause the C words to be 000 much of the time. A more efficient queuing system which signals stuffing by means of a channel address could have been used, but such a system would not yield the easy drop-add capability of the cyclic system described. The sync signaling for each digital channel is readily identifiable, and replacement would be a simple operation at drop-add points.

A disadvantage of the cyclic system is the waiting period between the time stuffing is demanded and the time it occurs. Since stuff signaling for a T1 carrier channel occurs once per S-bit frame (which is 1944 T1 carrier time slots long), the waiting period for T1 carrier can be as long as 1.26 msec, and hence, the maximum allowable T1 carrier stuff rate equals 794 c/s. Since one C word is allotted per line frame bit, the waiting time for higher bit rate constituents is proportionately less. For example, the maximum waiting interval for a video channel is 17.5 μs (1260/72 μs). The effect of this waiting interval is illustrated in Fig. 5. The phase of the signal at the output of the synchronizer (relative to the phase of the input signal) for the case where the stuff interval is large with respect to the waiting time is shown in Fig. 5(a). Note that it is approximately a sawtooth waveform of amplitude 2π (one time slot) and fundamental frequency equal to the stuff rate. Figs. 5(b) and 5(c) illustrate the nature of the output phase as the stuff rate increases: another component is added to that which would occur if demand stuffing could take place. This "waiting time effect" can include frequency components between dc and the stuff rate, and, as the stuff interval approaches the waiting time interval, the total jitter amplitude can be as great as 4π

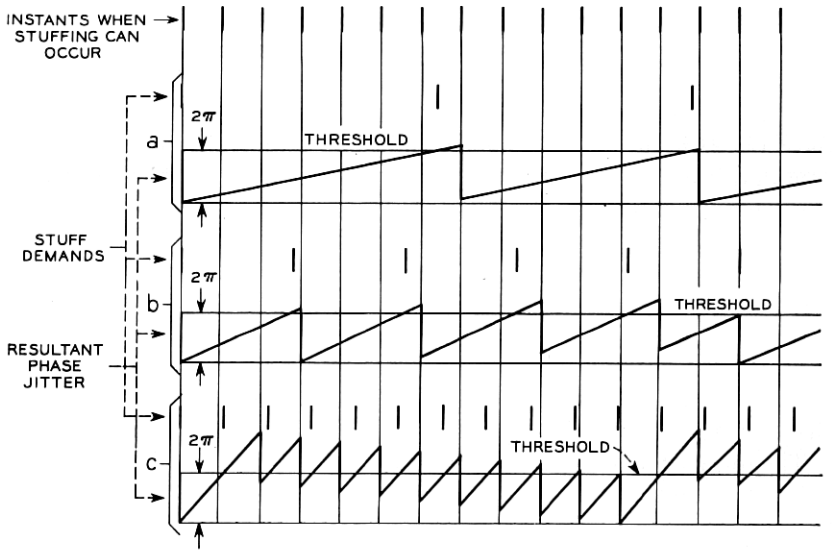


Fig. 5 — Pulse stuffing synchronization — waiting time effect.

(two time slots). Since the desynchronizer has a low-pass jitter attenuation characteristic, care must be exercised in the selection of the nominal stuff rate relative to the maximum stuff rate to assure that the residual output jitter after the desynchronizer is within tolerable limits.

Since the location of the inserted time slots is carried by the data channel, this method of synchronization is vulnerable to line errors. Analysis reveals, however, that misframes of an information channel due to sync signaling channel errors would never occur more frequently than several times per year for a line error rate of 10^{-6}. This performance could be improved, if necessary, through modification of the S-bit format; however, the format described is convenient to realize economically and is adequate in performance.

IV. PHASE JITTER REMOVAL

In a long digital transmission system there is an accumulation of phase jitter which arises from the dependence of the phase of the timing signal at each regenerative repeater on pulse pattern.[9] The contribution of each repeater is small, but the over-all effect can cause a significant transmission impairment.* Consequently, in a long system circuits

* See Ref. 1, this issue, p. 1827.

would be installed at intervals along the transmission route to reduce the accumulated jitter.

Fig. 6 is the block diagram of such a circuit, called a "dejitterizer," which consists of two closely associated parts: a phase-locked loop, which is driven by the jittered timing signal providing a timing signal with greatly reduced jitter, and an elastic store. After regeneration, the jittered line pulse train is sequentially written into the store using the jittered timing signal as a write clock. The smoothed timing is used as a read clock to produce a pulse train whose timing jitter has been substantially attenuated.

For the experimental system an eight-bit elastic store was developed. Tunnel diodes biased in a bistable mode proved to be highly satisfactory as storage elements. The effective store size is seven bits because the smallest spacing between write and read operations is about one-half bit at the line bit rate. Commutation was achieved by forming pulse trains at one-eighth the write and read clock rates and launching them down tapped delay lines. A ring counter could have been used to perform the function of the frequency divider and the delay lines, but it is a more expensive solution. It should be noted that application of delay line commutation is limited by the fact that misalignment of pulses at the AND gates occurs if phase jitter is present. This limitation may be expressed as follows for sinusoidal jitter with frequency $f_j \ll 1/(N-1)\tau$:

$$mf_j < \frac{M}{(N-1)\tau} \tag{1}$$

where

m = peak deviation of the phase jitter [radians]
f_j = jitter frequency [c/s]
M = allowable misalignment at the gates [time slots]
N = number of storage cells
τ = delay between taps [seconds].

For example, if $M = 0.1$ time slots for an eight-bit store operating at 224 Mb/s, then the maximum allowable phase jitter amplitude would be one radian at a jitter frequency of 3.2 Mc/s or ten radians at a jitter frequency of 320 kc/s. In the applications for which delay line commutation is used in the experimental system, the constraint expressed in inequality (1) is never limiting.

Since absolute phase information is not available at a repeater, the jitter attenuation characteristic must be a low-pass function, and very low frequency jitter will not be affected by the dejitterizer. Fortunately,

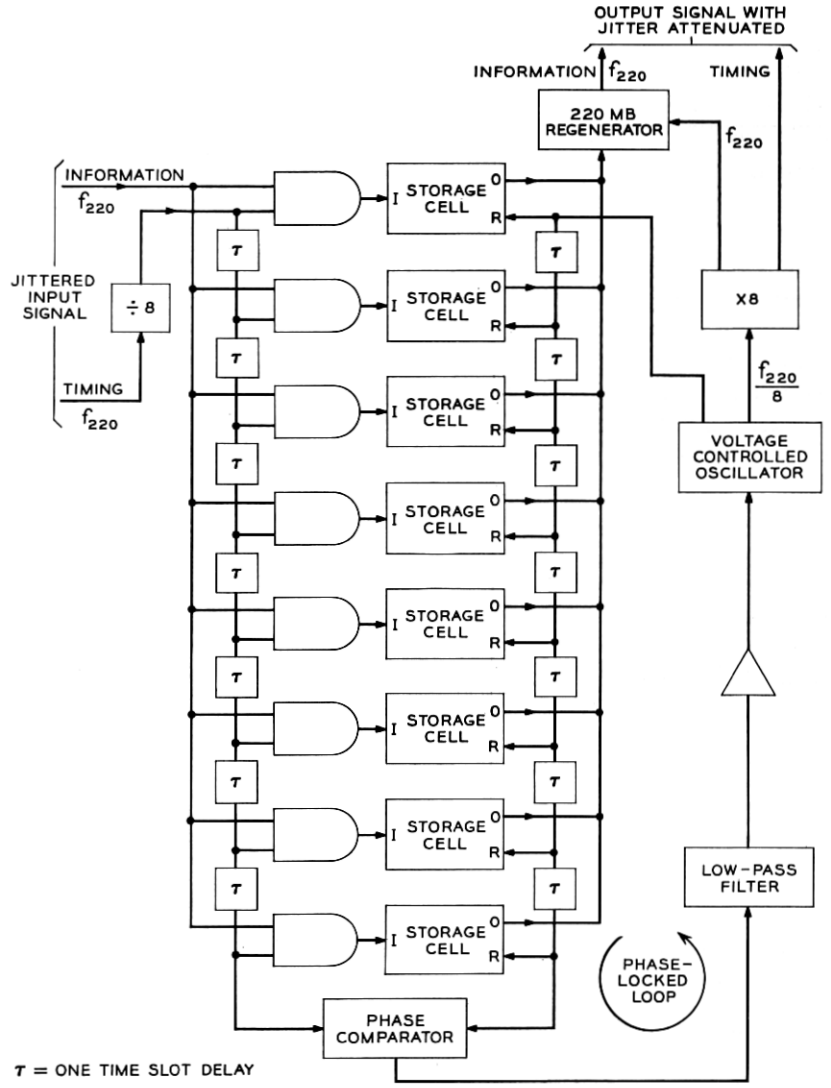


Fig. 6 — 224 Mb/s dejitterizer.

large amounts of low frequency jitter can be tolerated. Considerable flexibility exists for shaping the jitter attentuation characteristic through design parameters in the loop transmission function.[10] For all cases there is a tradeoff between the tolerable net oscillator instability (instability of line clock plus instability of the voltage controlled oscillator)

and the amount of store capacity allotted to frequency drift for a fixed jitter bandwidth of the dejitterizer. For the simplest case where there is no shaping network in the phase-locked loop (so-called no filter case), it may be shown that

$$(\delta_{VCO} + \delta_B) = \frac{B_j \cdot \pi n \cdot 10^6}{2\omega_B} = \frac{\pi n \cdot 10^6}{2Q} \tag{2}$$

where

δ_{VCO} = peak VCO frequency drift [ppm]
δ_B = peak line frequency drift [ppm]
B_j = jitter bandwidth [radians/sec]*
n = number of storage cells allocated to frequency drift
ω_B = line bit rate [radians/sec]
Q = quality factor of phase-locked loop considered as a bandpass filter.

As an example, for a net oscillator instability of 4 ppm and a Q of 10^6 (parameters used in the experimental system), a total of 2.5 storage cells would be allocated to frequency drift. If, however, the net oscillator instability were doubled, about five storage cells would be taken up by frequency drift alone.

The phase-locked loop is adjusted so that the elastic store is half full on the average, and the elastic store is made large enough so that overflow does not occur often enough to be a problem.

In order to examine the feasibility of a dejitterizer operating at a bit rate of 224 Mb/s, the eight-bit elastic store and associated phase-locked loop were designed to function as the last dejitterizer in a simulated long system. If it is assumed that the Chapman model† can be used for the regenerative repeaters,‡ and if the following assumptions are made:

Number of repeaters in system = 3600
Q of each repeater timing tank = 80
rms phase jitter per repeater = 11.2°§
One dejitterizer every 360 repeaters
No filter case with $Q = 10^6$ for each dejitterizer

then the spectrum of the jitter into the last dejitterizer would be that shown in Fig. 7.[11] This spectrum, approximated by the dashed curve,

* $B_j = 2\alpha_o$, where α_o = the loop gain [radians/sec/radian].
† Ref. 9, p. 2681.
‡ Insufficient experimental data exist to establish the validity of this model for a 224 Mb/s repeater, but experimental evidence has demonstrated its usefulness for estimating the jitter performance of strings of T1 carrier repeaters.[9]
§ Experimental models of regenerative repeaters have exhibited slightly better jitter performance than the 11.2° rms used here.

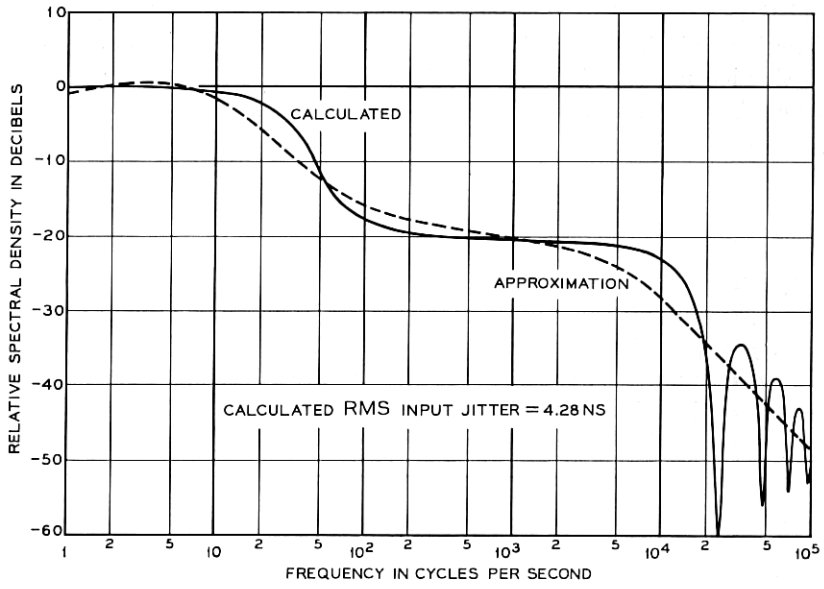


Fig. 7 — Spectrum of dejitterizer; input jitter.

was used to phase modulate the input signal of a dejitterizer having a $Q = 10^6$. The calculated and experimental results are shown in Fig. 8. No digital errors occurred during this experiment because the input phase deviation was limited (by clipping) to a level which prevented store overflow. An analysis has shown[11] that for a net oscillator instability of 4 ppm (used in the experimental system) and for the case described above, the effective size of store required for one overflow per minute, week and century would be 13, 15 and 17, respectively. Note how rapidly the overflow rate varies with store size. Since it has been determined that the required store size is not decreased rapidly as the number of dejitterizers is increased, it is expected that more than the eight cells used in the experimental dejitterizer would be needed in a commercial system. The store size required is still quite reasonable, however.

An indication of the effectiveness of the dejitterizer is provided by Fig. 9, where 1 kc/s sinusoidal jitter has been applied. That the effective store size is at least seven time slots is seen from the waveforms shown.

V. MULTIPLEXER-DEMULTIPLEXER DESCRIPTION

In order to demonstrate the feasibility of performing the variety of digital processing steps necessary to multiplex and demultiplex the

digital signals described earlier, the system shown in Fig. 10 was developed. The arrangement shown was chosen to allow the transmission of the following signal types over the 224 Mb/s digital line:

(1.) Synchronous PCM video.
(2.) Synchronous or asynchronous PCM mastergroup.
(3.) Two T1 carrier channels, synchronous with each other, but asynchronous with the line clock, which can be used separately or can be combined to handle a 3 Mb/s coded *PICTUREPHONE* signal. The individual T1 carrier channels also carried data-on-T1 carrier signals as one experiment.[12]
(4.) Pulses from a synchronous word generator to fill the unused time slots with a restricted set of pulse patterns which includes all-ZEROS and all-ONES.
(5.) The synchronous sync signaling signal (S bit).

One feature which was not demonstrated was the processing of an asynchronous PCM video signal; i.e., a 111 Mb/s synchronizer and desynchronizer was not developed. It is clear that development of these

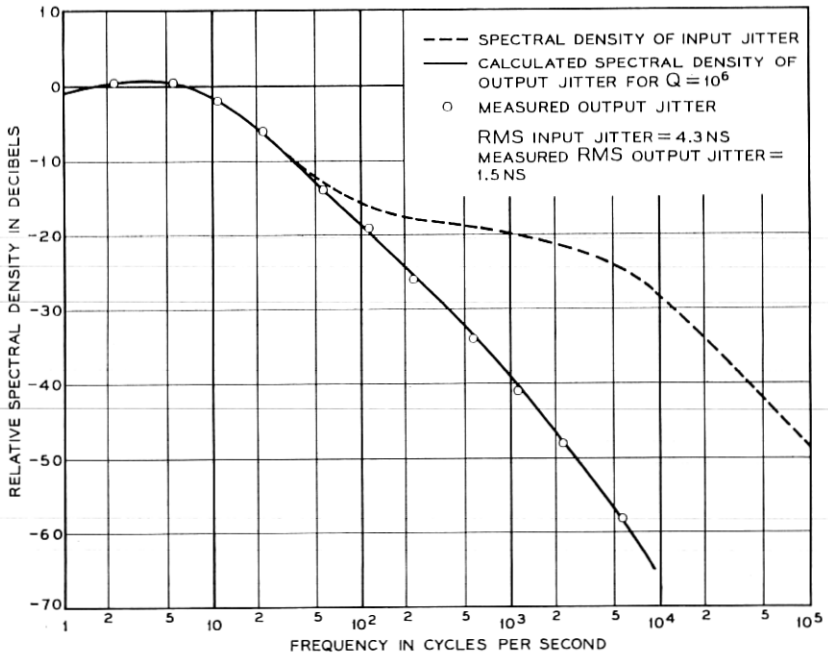


Fig. 8 — Spectrum of dejitterizer; output jitter.

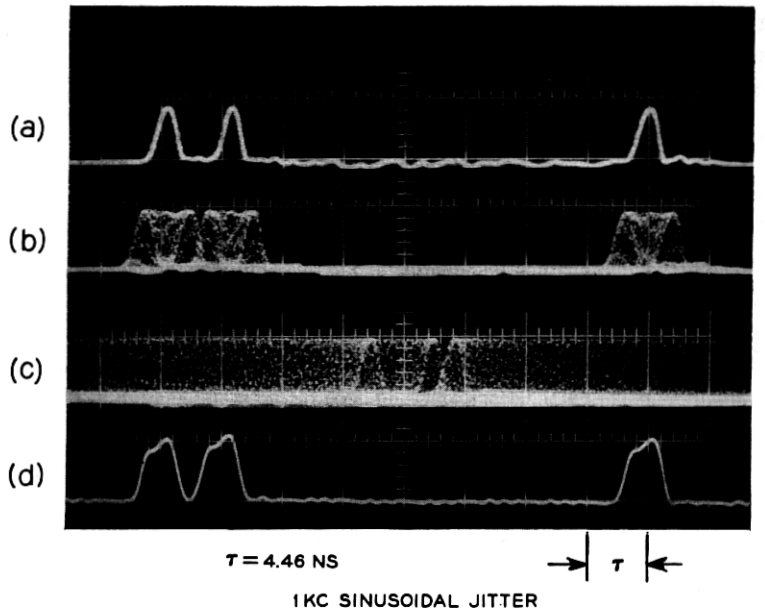


Fig. 9 — Performance of dejitterizer.

system blocks can be accomplished through the use of circuit design techniques which have been applied elsewhere in the experimental terminal. Also, the two T1 carrier channels were synchronized with each other. This was a requirement for processing a 3 Mb/s coded *PICTUREPHONE* signal,* and it was apparent that this simplification would not cause the omission of the development of a crucial circuit function. The format chosen highlights all of the significant developments needed for this study.

The line format is shown in Fig. 11 along with a timing diagram which defines all of the signals depicted in Fig. 10 and in the figures which follow. Table I defines the frequencies shown in Fig. 10. In the experi-

* Coding and decoding of the *PICTUREPHONE* signal into a 3 Mb/s digital signal was accomplished through the use of equipment developed within Bell Telephone Laboratories.

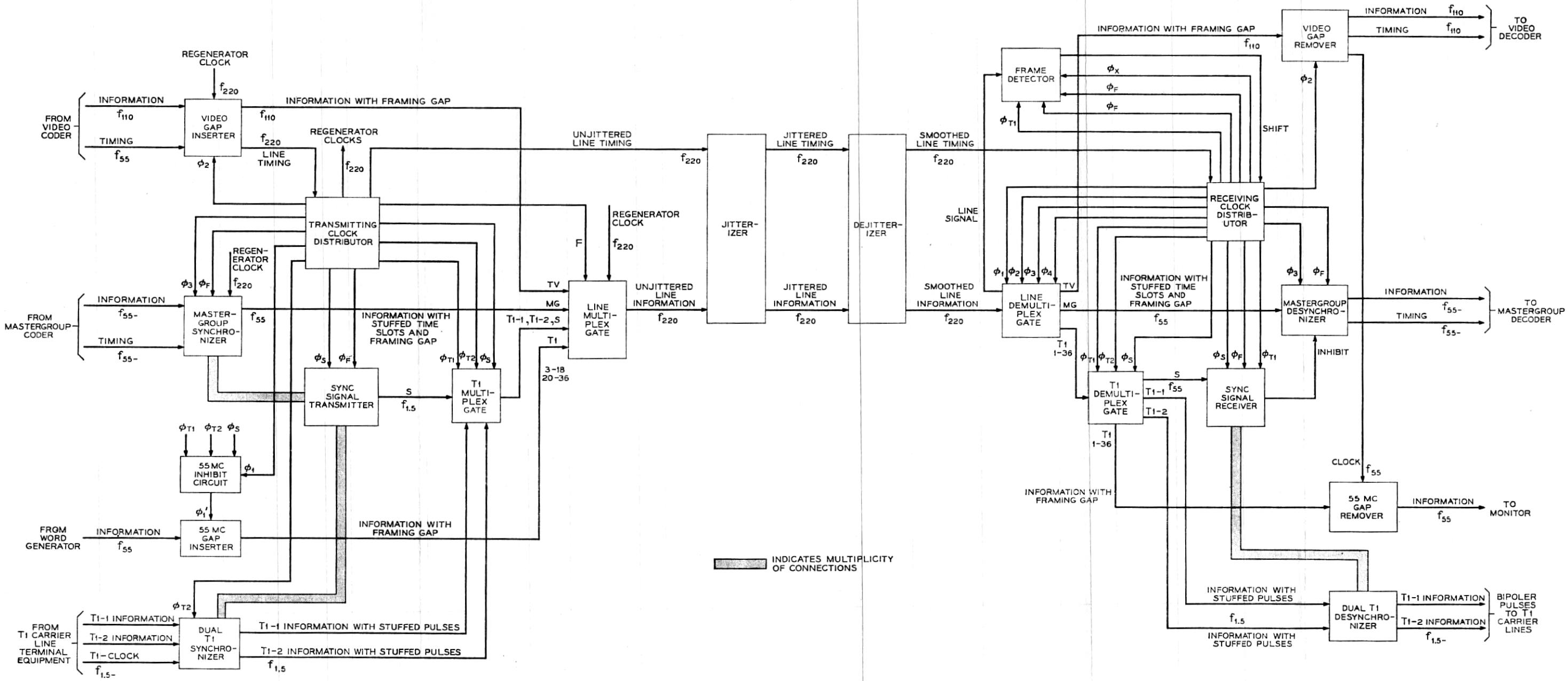


Fig. 10 — Block diagram of multiplexing and jitter portions of experimental terminals.

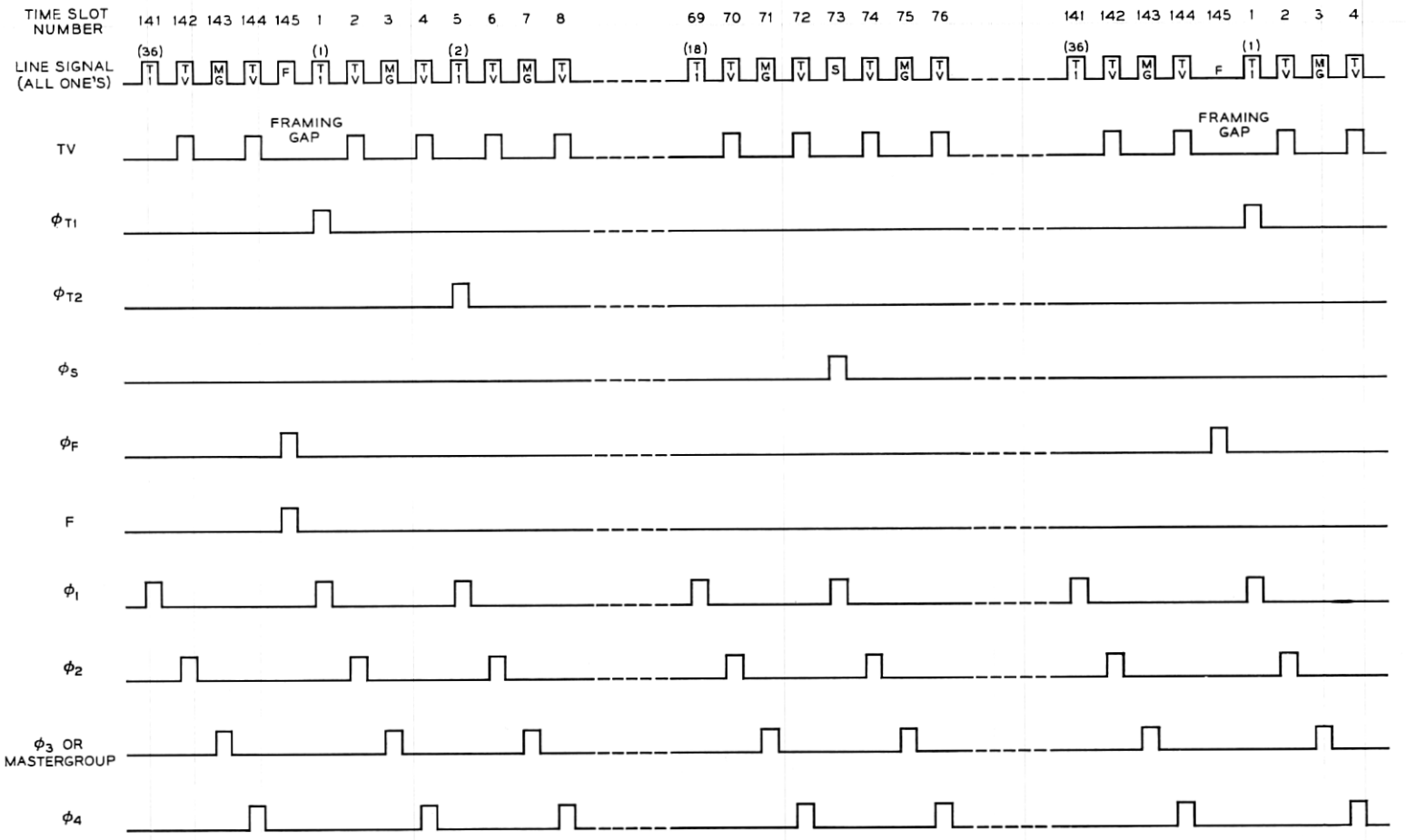


Fig. 11 — Time organization of the experimental terminal.

TABLE I — FREQUENCIES USED IN THE EXPERIMENTAL DIGITAL TRANSMISSION TERMINAL

$f_{1.5-}$ = Asynchronous T1 carrier bit rate	= 1.544 Mb/s ± 50 ppm
$f_{1.5}$ = Synchronous T1 carrier bit rate	= 1.544 Mb/s + (60 ± 2) ppm
f_{55-} = Asynchronous coded mastergroup bit rate	= (1.544 × 36 = 55.584) Mb/s + (36 ± 2) ppm
f_{55} = Synchronous coded mastergroup bit rate	= 55.584 Mb/s + (60 ± 2) ppm
f_{110} = Synchronous coded video bit rate	= (1.554 × 72 = 111.168) Mb/s + (60 ± 2) ppm
f_{220} = Line bit rate	= (1.544 × 145 = 223.880) Mb/s + (60 ± 2) ppm

mental terminal, the clock stabilities were taken to be ±2 ppm (readily attainable with a crystal in a simple oven) except for the T1 carrier clock which was assumed to be ±50 ppm.

Processing of the pulse trains from the various sources is required either to form the framing gap or to achieve a pulse train in synchronism with the line rate, or both. This processing is accomplished by the "video gap inserter," the "mastergroup synchronizer," the "55-Mc/s gap inserter," and the "dual T1 synchronizer."

The various sine wave and pulse clocks for the multiplex circuits are furnished by the "transmitting clock distributor." Synchronism between the line signal and the video bit rate is achieved by means of a phase-locked loop whose elements are portions of the video gap inserter and the transmitting clock distributor.

The sync signal transmitter monitors the mastergroup and dual T1 synchronizers for stuff-demand indications, clocks the stuffing operation, and signals with the S bit where and when stuffing has occurred.

Multiplexing of the S bit and each of the T1 carrier signals is accomplished in the "T1 multiplex gate." All signals are combined to form a binary line signal in the "line multiplex gate." *

The output of the line multiplex gate drives the "jitterizer" which is essentially the same circuit as the dejitterizer described in Section IV except that the phase-locked loop parameters are modified. The loop gain is increased substantially and the desired phase modulating signal is introduced at the output of the phase comparator.†

At the receiving end of the system the jittered signal is smoothed by the action of the dejitterizer. Frame synchronization of the "receiving clock distributor" is forced by the frame detector. The receiving clock distributor furnishes the variety of clocks required by the demultiplex

* Simultaneous use of signals from the 55-Mc/s gap inserter and the T1 multiplex gate is permitted even though their signals may coincide. The "55-Mc/s inhibit circuit" eliminates the pulses from ϕ_1 which fall in the time slots occupied by the T1 carrier signals and the S bit.

† Ref. 10, p. 571.

circuits. The "line demultiplex gate" separates the individual components of the line signal; as at the transmitting end, the S bit and the T1 carrier signals pass through another level of multiplex — the "T1 demultiplex gate." Framing gap and/or stuffed pulse removal is accomplished in the "video gap remover," the "mastergroup desynchronizer," the "55-Mc/s gap remover" and the "dual T1 desynchronizer." Decoding of the S bit is done by the sync signal receiver which signals the mastergroup and dual T1 desynchronizers exactly which time slots are to be dropped.

5.1 *Clock Distribution*

5.1.1 *Transmitting Clock Distributor*

A block diagram of this circuit is shown in Fig. 12. Its function is to derive from a sinusoidal line clock signal all of the clock pulse patterns

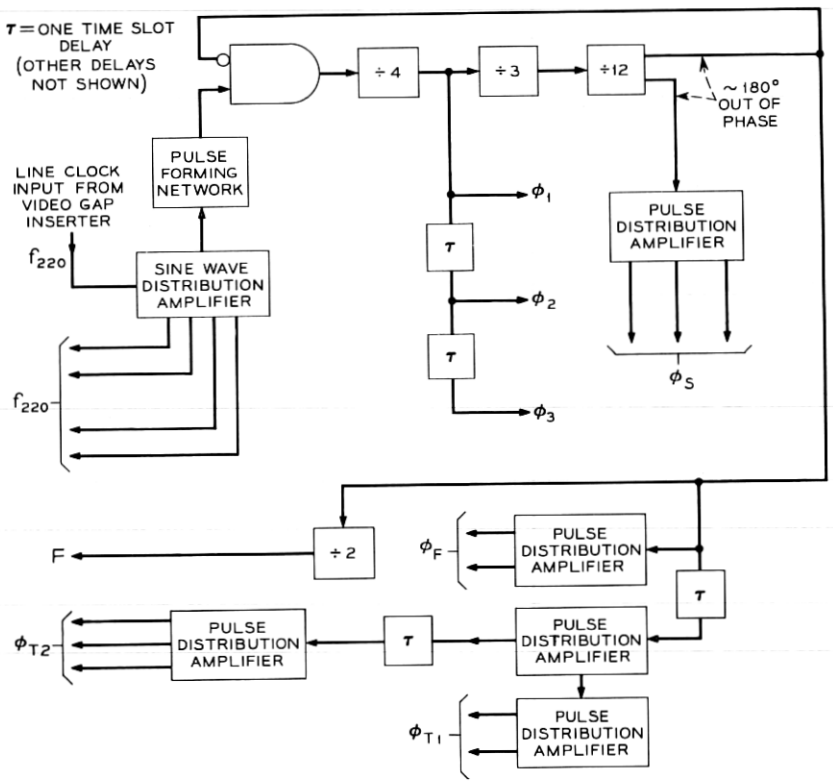


Fig. 12 — Transmitting clock distributor.

(ϕ's) shown in Fig. 11 and to distribute sinusoidal line clock signals. The framing gap, which is 4.47 ns wide and occurs once for every 145 line time slots, is created with a divide-by-144 counter preceded by an inhibit gate. The output of the counter inhibits the line rate input to the counter; hence, the framing gap exists on signals at each stage of the counter. Furthermore, the output of the counter occurs at the frame rate. Note that the S bit clock pulses, which are located midframe, are derived by selecting the "negative" phase at the output of the divide-by-12 counter, thereby avoiding the use of one-half frame of delay.

5.1.2 *Receiving Clock Distributor*

Note from Fig. 13 that this circuit is almost identical to the transmitting clock distributor, the main exceptions being the provision for inhibition by a signal from the frame detector and the furnishing of a special clock signal to the frame detector.

5.1.3 *Clock Distributor Performance*

The most difficult problems associated with the realization of the clock distributors were the counting function (because of the speed of the input signal and the delay stability dicated by the fact that such precise inhibition (one out of 145) was required), and the nature of the required output pulse trains. The circuit used for counting is discussed in Section 6.2.3. The nature of the pulse clock signals is shown in Fig. 14 where ϕ_1, ϕ_2, ϕ_3, and ϕ_4 are shown around the framing gap.

5.2 *Framing Gap Insertion and Removal*

5.2.1 *Video Gap Inserter*

The block diagram of Fig. 15 shows the components of the video gap inserter. The need for write and read clocks at one-half the video bit rate becomes apparent from this diagram. Pulses at that rate are launched down delay lines to accomplish sequential accessing of the storage cells. Complete regeneration of the 50 mV pulses at the output of the storage cells is performed by a 220 Mb/s regenerator. Use of the high speed regenerator at this point permits the use of a simple untimed line multiplex gate.

To allow for crystal control of the VCO, $f_{220}/18$ was generated and applied to a frequency multiplier, which is considered as an integral part of the VCO in Fig. 15.

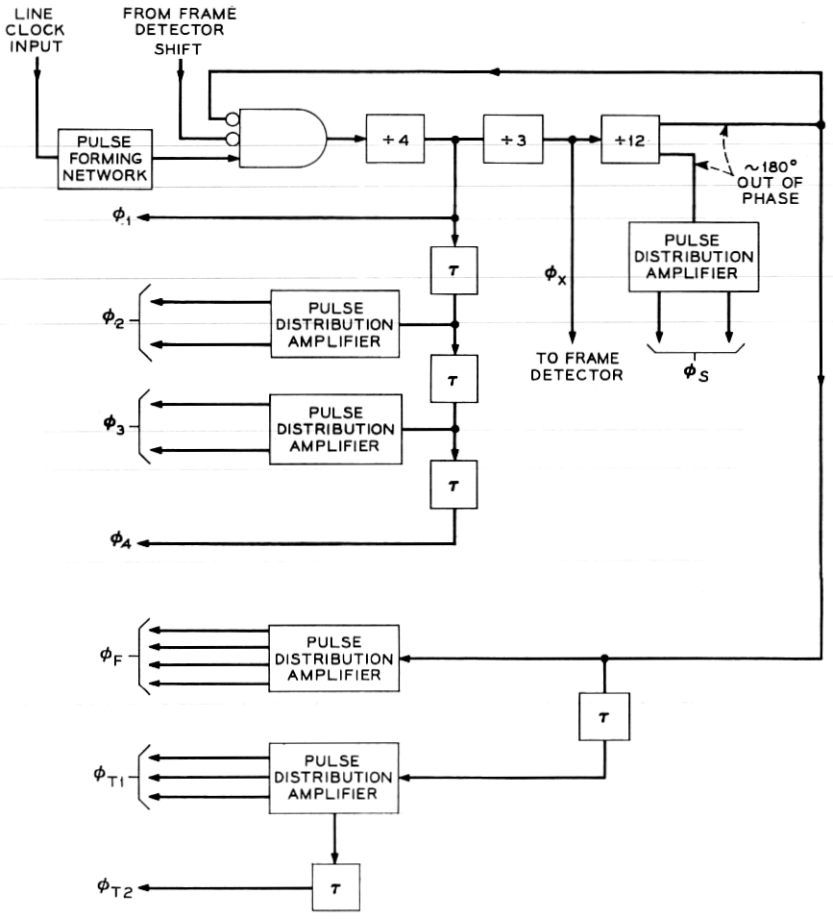


Fig. 13 — Receiving clock distributor.

5.2.2 *Video Gap Remover*

The phase discontinuity due to the framing gap can be thought of as phase jitter. Attenuation of this jitter is accomplished by the video gap remover shown in Fig. 16, which operates on the same principle as that used in the dejitterizer. The information containing the framing gap is written into the store under the control of ϕ_2, the write clock. The jitter on this clock is smoothed by the action of a phase-locked loop. The resultant smoothed timing signal is used as the read clock for the store. Note the similarity with the video gap inserter of Fig. 15. Many of the

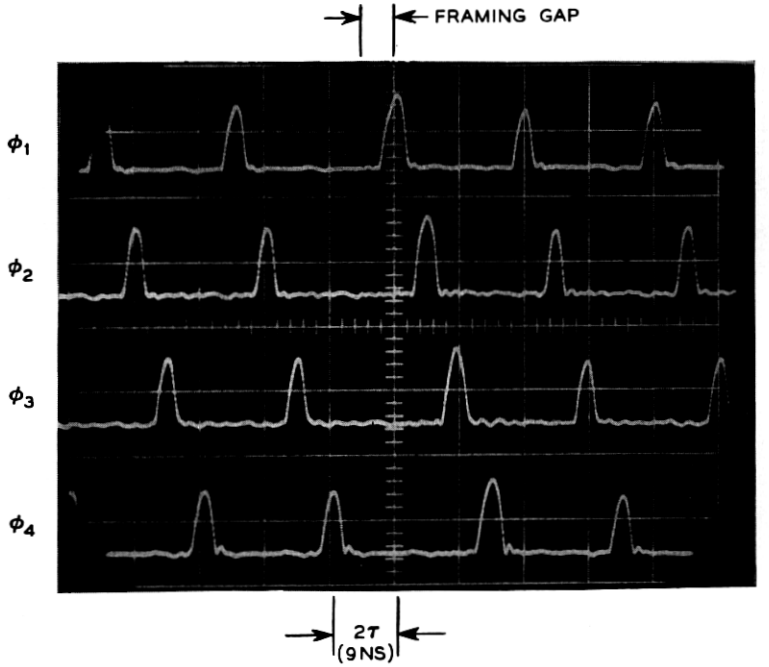


Fig. 14 — Oscilloscope trace showing ϕ_1, ϕ_2, ϕ_3, and ϕ_4.

circuit blocks are duplicated in the two equipment blocks. Also notice that a one-shot multibrator is used to widen the video information pulses from the line demultiplex gate to improve the operating margin of the store.

5.2.3 *55-Mc/s Gap Inserter*

This circuit, shown diagrammatically in Fig. 17, enables pules from a 55-Mb/s word generator (synchronized with the video coder clock) to be multiplexed onto the high-speed line. These pulses can be used to fill the time slots not occupied by video, mastergroup, T1 carrier, synchronization signaling (S) or framing pulses. This function could be performed by an elastic store as in the video gap inserter, but the lower bit rate being processed (f_{55}) allows the use of a simple stretching-sampling technique. The 55-Mb/s pulses are stretched to occupy three 224-Mb/s time slots. These are sampled by a modified ϕ_1 pulse train (called ϕ_1') to establish the framing gap. See Fig. 17. Pulse train ϕ_1' is ϕ_1 acted upon the 55-Mc/s inhibit circuit of Fig. 18 so that digits from the 55-Mc/s

word generator are not written into time slots occupied by the two T1 carrier channels and the S bit.

5.2.4 *55-Mc/s Gap Remover*

This circuit, shown in Fig. 19, applies the same stretch-sample technique employed in the 55-Mc/s gap inserter. The circuit is slightly more complicated since the narrow input pulses from the T1 demultiplex gate and the requirement for 50 per cent duty cycle output pulses dictate that pulse stretching take place at both input and output. The sampling clock is provided by the video gap remover. For the experimental system,

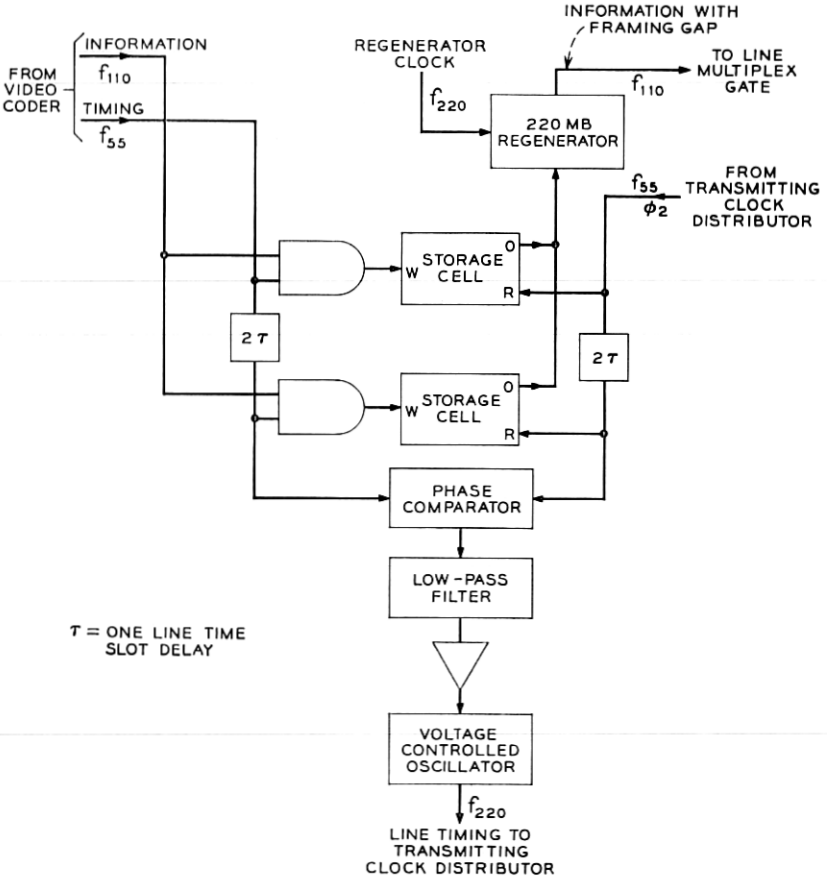


Fig. 15 — Video gap inserter.

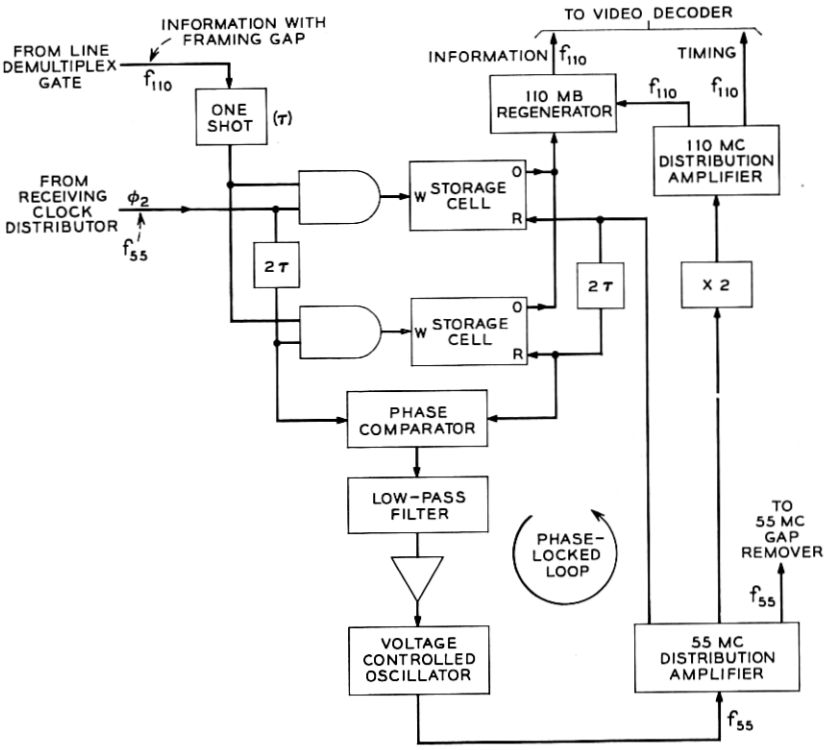


Fig. 16 — Video gap remover.

all 36 pulses per multiplex frame (T1 carrier, S bit, word generator) were processed as though they were from a synchronous coded master-group in order to establish the feasibility of this processing technique.

5.2.5 *Gap Insertion and Removal Performance*

Fig. 20 shows the performance of the video gap inserter and video gap remover. An all-ONES pattern was used to emphasize the phase discontinuity. The waveforms at the 55-Mc/s circuits are similar, but at one-half the bit rate.

5.3 *Pulse Stuffing Synchronization*

5.3.1 *Sync Signal Transmitter and Receiver*

These circuits provide a central control function for all synchronized channels. In addition to the coding and decoding of the sync signal (S

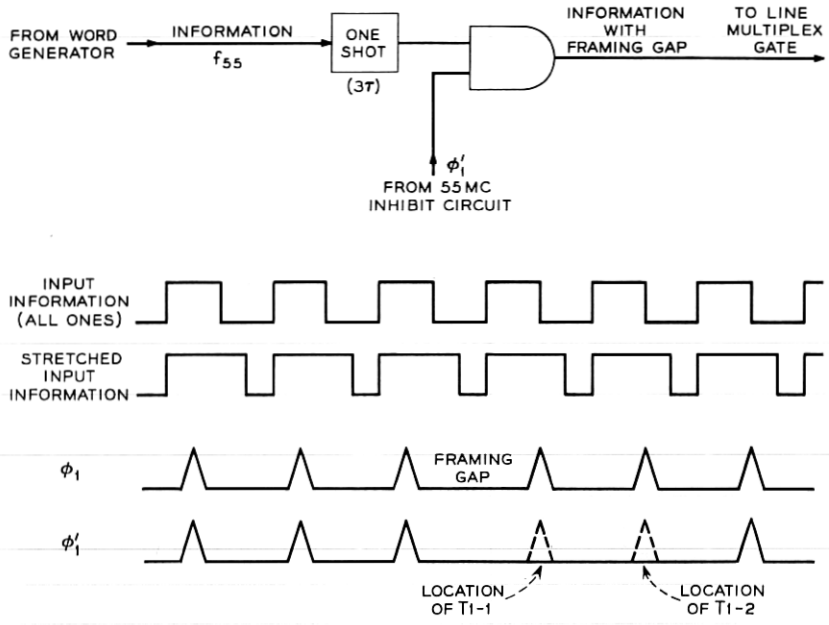


Fig. 17 — 55-Mc/s gap inserter.

bit), they control pulse stuffing and extraction at the synchronizers and desynchronizers. Each unit is a 1.5-Mc/s logic circuit which has been realized as a straightforward design using mostly ESS logic modules.[13] The S bit has been organized so that a single 18-stage shift register in each unit is used for generation and recognition of the M, R and C words.[8] In a commercial design, monolithic integrated circuits would probably be used for these circuits.

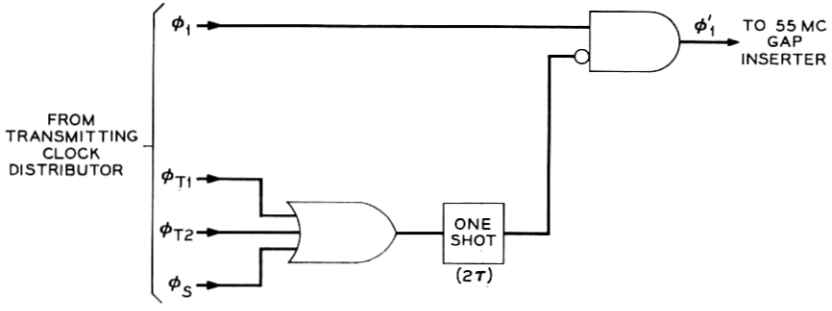


Fig. 18 — 55-Mc/s inhibit circuit.

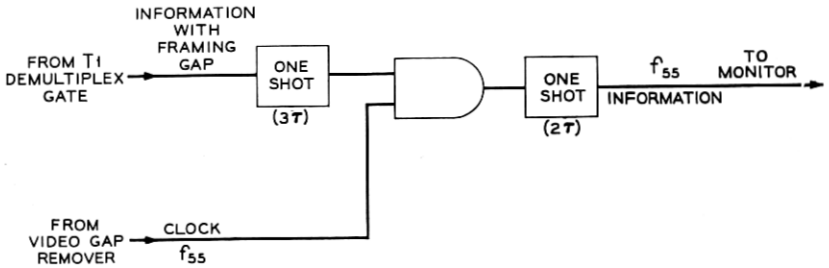
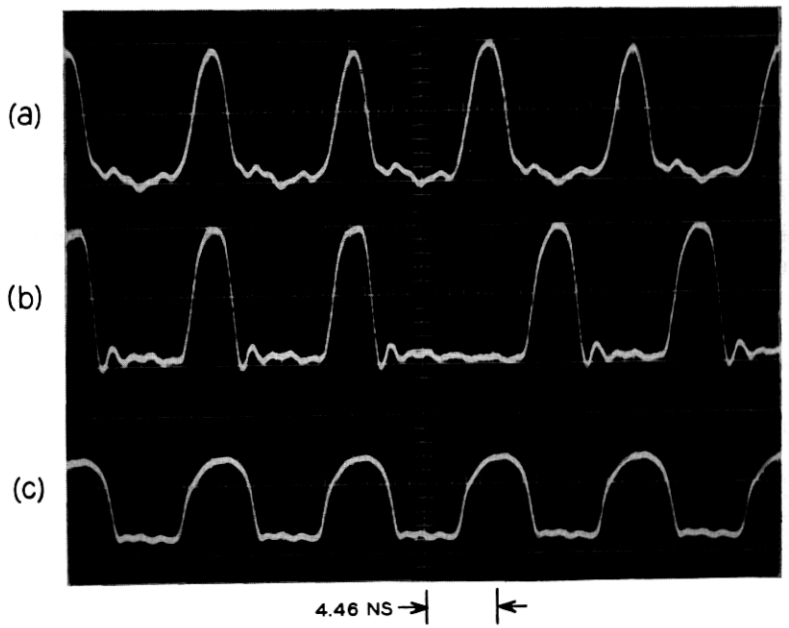


Fig. 19 — 55-Mc/s gap remover.



(a) VIDEO GAP INSERTER INPUT
(b) VIDEO GAP INSERTER OUTPUT
(c) VIDEO GAP REMOVER OUTPUT

Fig. 20 — Framing gap insertion and removal waveforms.

5.3.2 *Mastergroup Synchronizer*

This circuit, shown in block diagram form in Fig. 21, uses a three-cell elastic store with delay line commutation at the input and ring counter commutation at the output. Delay line commutation, which was used in the elastic stores of the dejitterizer, and video gap inserter and remover could not be used at the output because the stuff gap positioning was not synchronized with the multiplex clock. A three-cell store size is dictated by the following: one cell for the stuffed time slot, up to one more cell for waiting time when stuff rates near the maximum stuff rate are used, one-fourth cell for the framing gap (one 224 Mb/s time slot), one-fourth cell allowance for the fact the write and read operations cannot occur

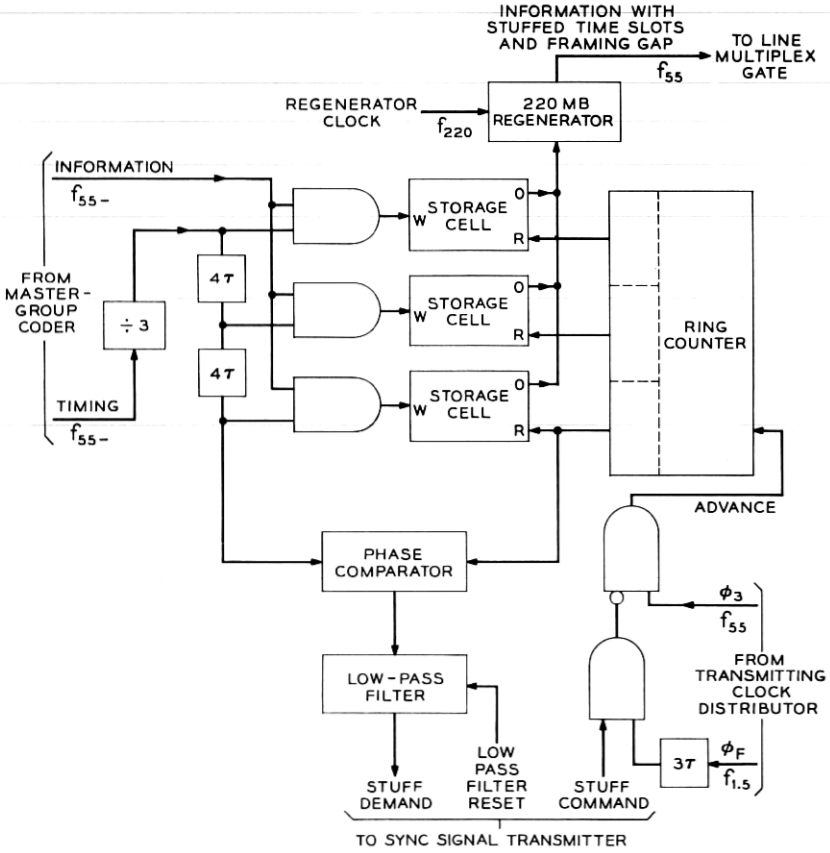


Fig. 21 — Mastergroup synchronizer.

simultaneously, and one-half cell for margin. Of course, lower stuff rates will increase this margin.

The low-pass filter reset signal is provided to assure that the need-to-stuff signal to the sync signal transmitter does not linger after stuffing has occurred.

5.3.3 *Mastergroup Desynchronizer*

It may be seen from Fig. 22 that the mastergroup desynchronizer is very similar to the mastergroup synchronizer except that ring counter commutation is required on the write side of the elastic store and that the read clock is obtained through the use of a phase-locked loop. Below

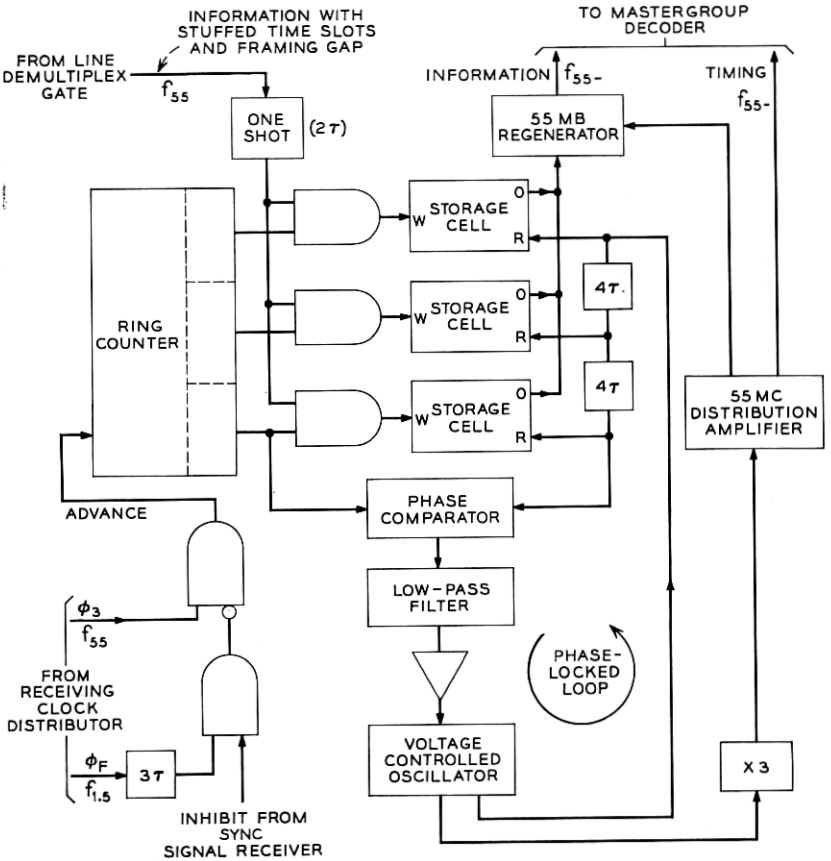


Fig. 22 — Mastergroup desynchronizer.

are calculations which show why the nominal offset of the synchronous and asynchronous 55-Mb/s rates was set at 24 ppm (see Table I).

It is apparent from the previous section that one-half cell is the maximum that is available for frequency drift if the maximum stuff rate is used. It was not anticipated that the maximum stuff rate be used during normal operation of the system, however, provision was made for operation at that rate to check out the circuits and to observe the effects of the resultant low-frequency phase jitter. Therefore, only one-half cell was allotted to frequency drift. The assumed ± 2 ppm clock stability (Table I) yields a low frequency mastergroup desynchronizer phase-locked loop gain, α_o, of

$$2\pi \cdot 142 \left(= \frac{(2 + 2)2\pi\ 55.}{\pi \cdot 1/2} \right)$$

radians/s/radian. (Equation (2) holds with α_o substituted for $B_j/2$.) With a simple one-pole RC filter with parameters set to yield critical damping, the jitter attenuation characteristic of Fig. 23 results. Note that if a 24 ppm offset (stuff rate = 1335 c/s) is used, the attenuation at the stuff rate is 27 dB, or the fundamental component of the residual phase jitter is 0.18 ns rms. This quantity of jitter can be seen from Fig. 7 of Ref. 1 to be acceptable. Furthermore, it may be demonstrated that since the stuff rate is about one-twentieth of the maximum stuff rate, the waiting time component of the jitter also meets the transmission requirements. The 24 ppm offset is by no means optimum, but the

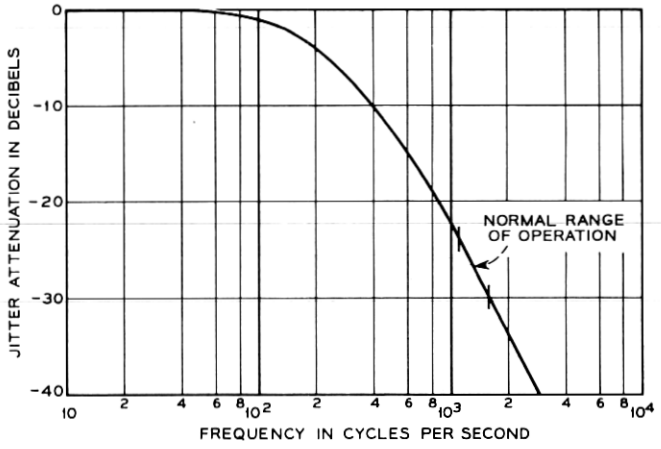


Fig. 23 — Jitter attenuation characteristic of mastergroup desynchronizer.

performance it yields indicates that pulse stuffing synchronization is indeed feasible. Note that almost a full cell of storage is available as margin for the stabilities indicated in Table I.

5.3.4 *Dual T1 Synchronizer*

This circuit, realized with monolithic integrated circuit modules, shares write and read circuits between two three-cell elastic stores. Whereas the tunnel diode is used elsewhere as the storage cell element, flip-flops are used for the T1 carrier processing circuits.

5.3.5 *Dual T1 Desynchronizer*

An interesting aspect of this circuit was that the phase-locked loop was made to have high-loop gain and the phase jitter was reduced only enough to prevent improper operation of a T1 carrier repeatered line. The motivation here was to reduce the amount of storage needed to accommodate the ±50 ppm T1 carrier clock variations and to allow the use of a noncrystal VCO. From Table I it may be seen that the maximum required stuff rate for a T1 carrier channel is 112 (=50 + 60 + 2) ppm or 173 c/s. The phase jitter due to pulse stuffing may be roughly represented by a sawtooth wave of frequency 173 c/s and amplitude 648 ns (one T1 carrier time slot) since the stuff rate is only about one-fifth of the maximum allowable stuff rate. Calculations revealed that the distortion in a T1 carrier system used for voice or data service which would result from this amount of phase modulation is entirely negligible. Measurements on the system bore this out. Since the distortion was even less for lower stuff rates, the full ±50 ppm variation of the T1 carrier clock could be tolerated.

Unfortunately this simplification of the dual T1 desynchronizer could not be tolerated for *PICTUREPHONE* transmission over two T1 lines. It was determined, however, that a three-bit store was adequate if the nominal offset were increased from 60 to 100 ppm and the phase-locked loop design were modified to provide some jitter attenuation. The sacrifice paid is a tighter stability requirement on the VCO; crystal control was necessary in order to make the T1 carrier clock the primary contributor to the net oscillator instability.

5.3.6 *Synchronizing Circuit Performance*

Clock frequencies were varied substantially more than those shown in Table I without any observable impairment of transmission of a coded mastergroup or T1 carrier signals through the system.

The mastergroup coder clock could be synchronized with the multi-

plex clock and with no circuit adjustment from the asynchronous arrangement, error-free performance was achieved. All of the circuits used to achieve synchronization operated over the full stuff frequency ranges, and the calculated quantities of phase jitter were observed.

5.4 *Multiplexing and Demultiplexing Circuits*

Two levels of multiplex are employed. The two T1 carrier channels and the S bit are first combined in the T1 multiplex gate. The output of this circuit and the other digital signals, now all synchronous, are combined in the line multiplex gate. At the demultiplexer, the two T1 carrier channels and the S bit are identified in the T1 demultiplex gate, but the entire "ϕ_3" digital channel is passed on to the 55-Mc/s gap remover to show the ability of the technique used therein to remove framing gap phase jitter.

5.4.1 *Line Multiplex Gate*

This circuit, shown diagrammatically in Fig. 24, is a simple five-input untimed combining gate followed by a regenerator. This simplicity is made possible by the shaping given to the pulses at the output of each processing circuit. Provision was made for clocking each input to the gate but it was not necessary.

5.4.2 *T1 Multiplex Gate*

This circuit is very similar to the line multiplex gate except that each input must be clocked because the T1 carrier and S-bit processing circuits furnish 50 per cent duty cycle pulses at 1.5 Mb/s. No regenerator is needed at the output of this gate.

5.4.3 *Line Demultiplex Gate*

Functions performed by this block, shown in Fig. 25, include the distribution of the incoming pulse train to the frame detector and the

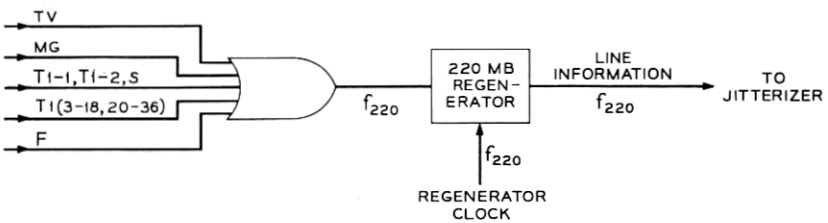


Fig. 24 — Line multiplex gate.

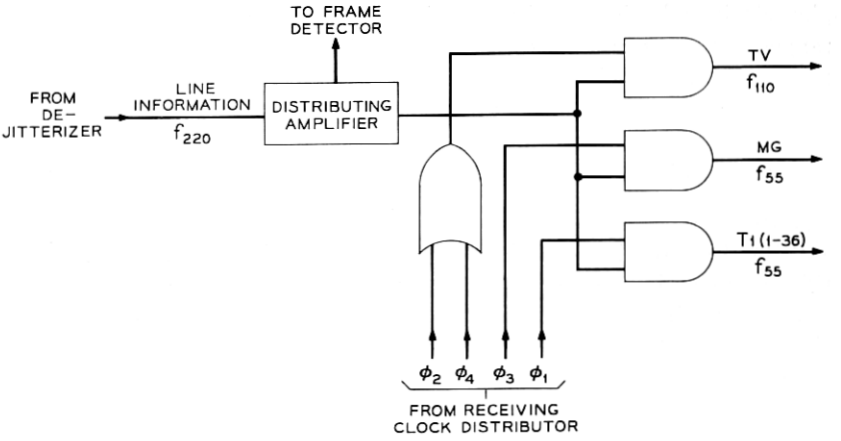


Fig. 25 — Line demultiplex gate.

separation of the coded video and the two 55-Mb/s pulse trains. Note that ϕ_2 and ϕ_4, the clock pulse trains for coded video, are first combined before entering the gate, thereby minimizing the fan-out of the gate driving amplifier to three, an important consideration for logic operating at this speed.

5.4.4 *T1 Demultiplex Gate*

As one sees in Fig. 10, the role played by this circuit is very similar to that of the line multiplex gate. The same basic circuit is used for both applications.

5.4.5 *Frame Detector*

The function performed by this circuit is similar to that performed by the frame detectors in the robbed bit coded video signal framing[14] and in the T1 carrier system.[7] However, a feature has been added which results in a circuit simplification.

In each system mentioned above and for the multiplex framing scheme, the framing pattern is alternating ONE's and ZERO's. During the reframe or search mode, the condition of a time slot is compared with the status of another exactly one frame away. If the comparison yields other than the alternation, the next later time slot is examined. To reduce the reframe time, not only is the time slot under consideration observed, but so is its neighbor. The previous methods mentioned above use the first half of a frame to make one comparison and the

second half to make the comparison for the neighboring time slot. This means that at least one-half frame of storage must be provided and that the comparator must be reset and must sense the condition of that neighboring time slot. A simpler comparator circuit, shown in Fig. 26 as a part of the frame detector, uses the neighboring time slot condition to route the error indicating pulse to either SET or RESET the flip-flop (whichever is appropriate), thereby readying the comparator for the next frame. Thus, one comparison per frame is made as with the other technique.

The gates and one shot multivibrators of Fig. 26 are required to provide pulse selection and to allow the use of slower logic circuits within the frame detector. The shift signal producing circuit contains an ad-

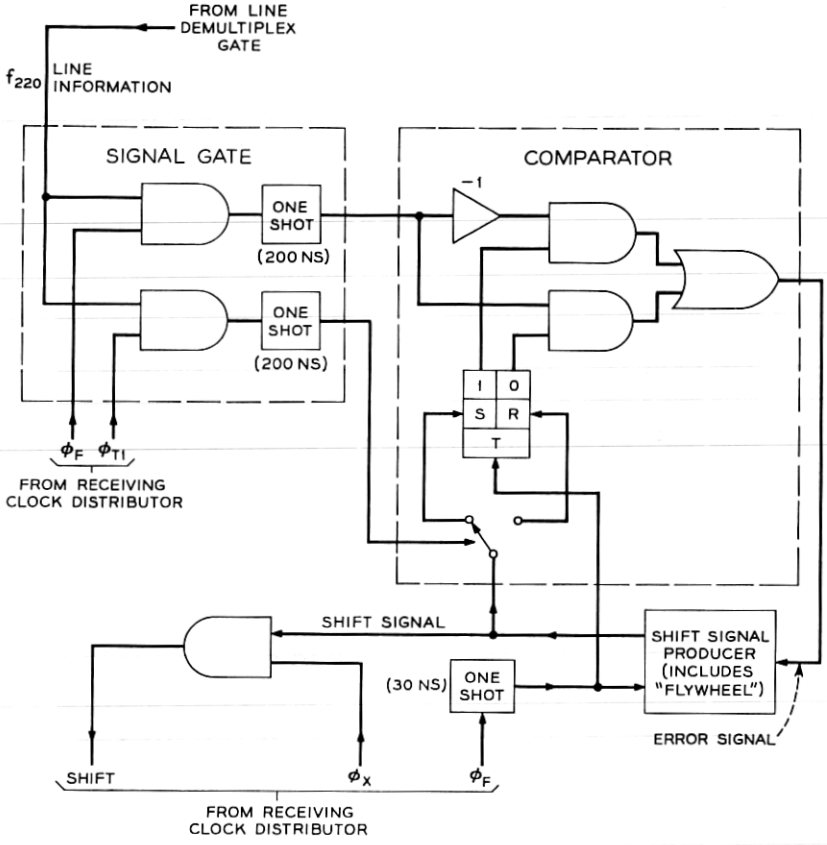


Fig. 26 — Frame detector.

justable flywheel which is realized with an integrator followed by a threshold circuit.

5.4.6 *Multiplexing and Demultiplexing Circuit Performance*

The multiplexing and demultiplexing functions provided complete isolation of the individual digital channels. These circuits performed satisfactorily for all signal formats which could be checked, which included fixed patterns ranging from all-ZEROS to all-ONES from word generators and typical continuously changing pulse patterns from the mastergroup, video and T1 carrier signal sources.

A photograph of an oscilloscope trace of a fully loaded line signal at the output of the line multiplex gate is shown in Fig. 27. Note the absence of intersymbol interference.

One test of the frame detector performance consists of forcing the out-of-frame condition to occur by forcing a single SHIFT output signal to be generated by the frame detector. Since searching takes place over an entire frame, the resulting reframe time is an upper bound on the

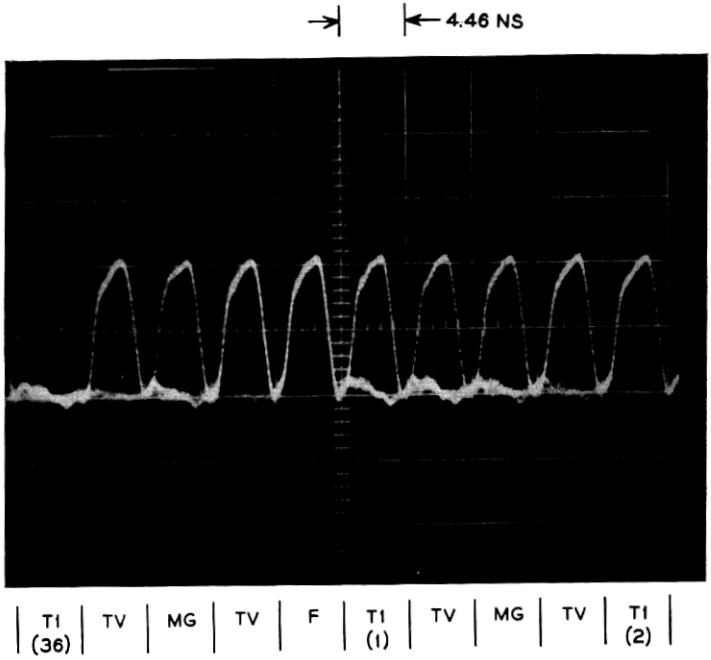


Fig. 27 — Line waveform.

actual reframe time for the particular line loading present at the time of the test. It was found that for an all-ZEROS line loading the reframe time was 93 μs. It was not convenient to make measurements with a random loading pattern, however with the loading shown in Fig. 27 the maximum average reframe time measured in 1000 trials was 134 μs. These numbers are consistent with the 188 μs calculated maximum average reframe time for a random pattern, after the flywheel effect was taken into account.

VI. CIRCUIT TECHNIQUES[15]

The intention of this section is to convey in general terms some of the more significant high speed circuit concepts which led to the realization of the multiplexer and demultiplexer in the 224 Mb/s digital transmission system.

6.1 *Solid-State Devices*

To achieve reliable logic circuits in a 224 Mb/s system, it was necessary to have available transistors which could switch in less than one nanosecond. Such a transistor was developed for this and other projects[16,17,18] which has a gain-bandwidth product in excess of 2.5 Gc/s, a dissipation rating of 50 mW at 25°C ambient and a maximum C_{ob} (direct collector-base capacitance with the emitter open circuited) of 0.8 pF. It is a pnp diffused base epitaxial mesa germanium transistor. All transistors shown in the diagrams which follow are this device.

In applications where higher power handling capability and/or lower speed requirements dictate, npn planar silicon devices are used. These units typically have a gain bandwidth product of 1.0 Gc/s, a 25°C ambient dissipation limit of 200 mW and a C_{ob} of 1.2 pF.

A number of tunnel and step-recovery diodes were used throughout the system. Many Schottky-barrier (metal-semiconductor) diodes were used because of their excellent low capacitance and small minority carrier storage characteristics. In the following figures, all diode locations not identified as tunnel or step-recovery diodes are applications for the Schottky-barrier diode.

6.2 *Specific Circuits*

6.2.1 *Current and Pulse Routing*

Fig. 28 illustrates how the current routing and pulse routing concepts[19] were utilized in the demultiplex gate. Of all the gating circuits realized,

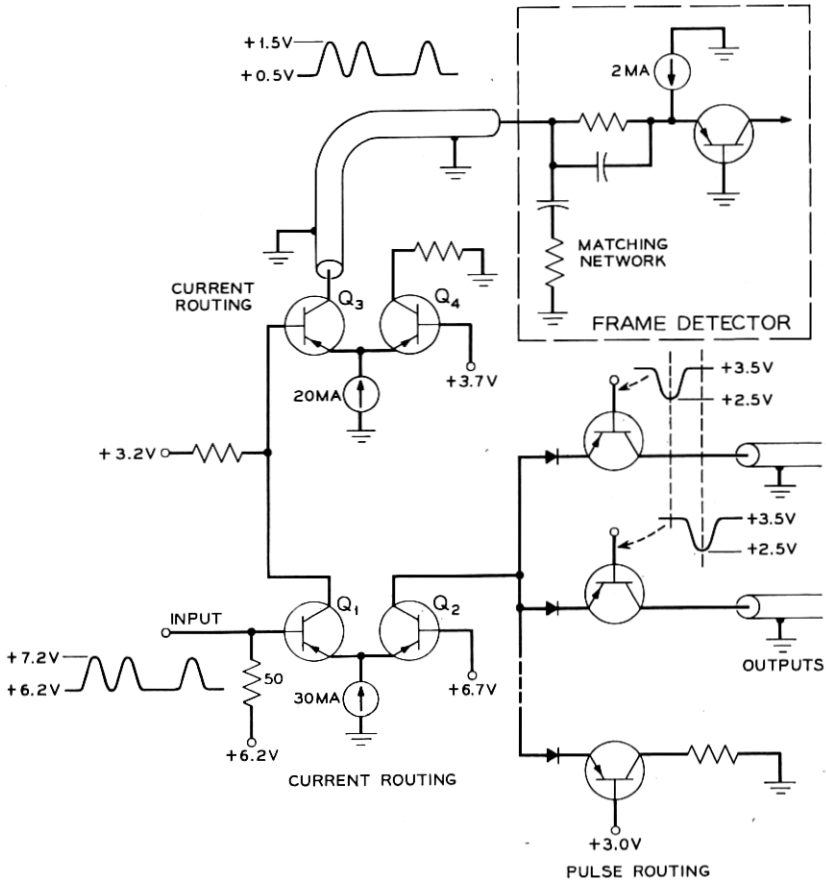


Fig. 28 — Current and pulse routing.

this one was found to be most demanding of the high speed characteristics of the available devices. The current routing stage with transistors Q_1 and Q_2 provides a good termination for the incoming pulse train, furnishes a noninverted signal for the gate transistors and drives another current routing stage (Q_3Q_4). Notice that the bias on the "cold" base is midway between the levels on the "signal" base.

The stage containing Q_3 and Q_4 is used as an inverter to send a replica of the input signal to the frame detector. One principle applied extensively throughout the system is the transmission of signals over moderate distances using coaxial cables with a far end termination only. The far end also provides the dc bias path for the line driving transistor.

The common-base stage shown, quiescently biased slightly ON and with a network to build out the input impedance, provides an excellent line termination with less than 10 per cent reflection and negligible memory.

The desired pulse trains are stripped off by applying the composite signal as a current drive to all emitters of the gate transistors and by clocking at each base (pulse routing).

Current routing and pulse routing are used extensively throughout the system, especially for circuits operating at the line bit rate.

6.2.2 *Tunnel Diode Storage Cell*

All elastic stores in the system except for those used to process the T1 signals use the storage cell and associated gates shown in Fig. 29.[6] The tunnel diode, biased in a bistable mode, furnishes a simple, fast memory element. As described earlier, write and read commutation comes from tapped delay lines except where ring counters are required. The write AND gate and read AND gate route current to the tunnel diode to change its state. The use of this type gate results in a controlled and predictable loading of the tapped write and read transmission lines. The "differentiator-clipper" is required to form the negative output pulse. Gating and clipping functions are performed by diodes rather than transistors for reasons of economy. However, the relatively small output level (50 mV across 50Ω) requires the use of regeneration; hence, in a

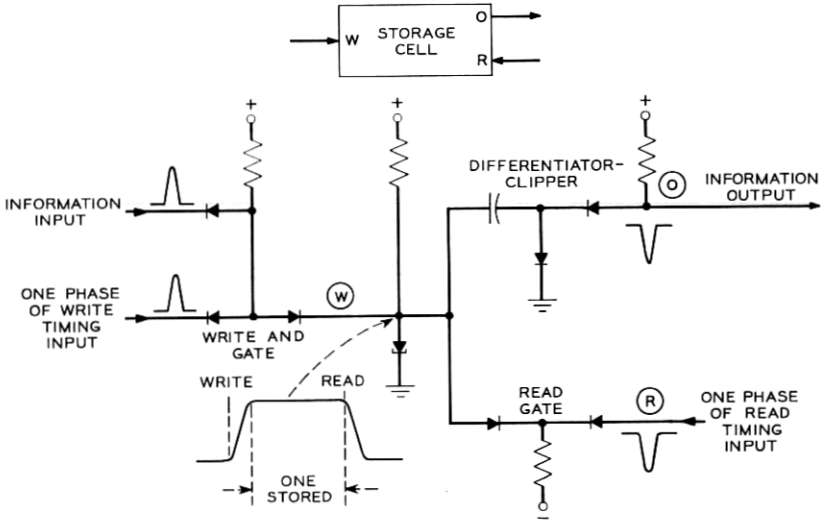


Fig. 29 — Tunnel diode storage cell.

commercial system, it is quite possible that for small stores a cost savings could result by using a transistor in each differentiator-clipper and thereby simplifying the regenerator design.

6.2.3 *Counter Stage*

Another use of the tunnel diode is in the binary counter stage shown in Fig. 30. The basic counting stage is that described by Chow.[20] Reliable cascading of these stages has been achieved by using a transistor with a small emitter bypass capacitor as a differentiator-clipper. In cases where feedback is applied to count by factors other than powers of two, the reset pulse is applied as a current drive to the point shown.

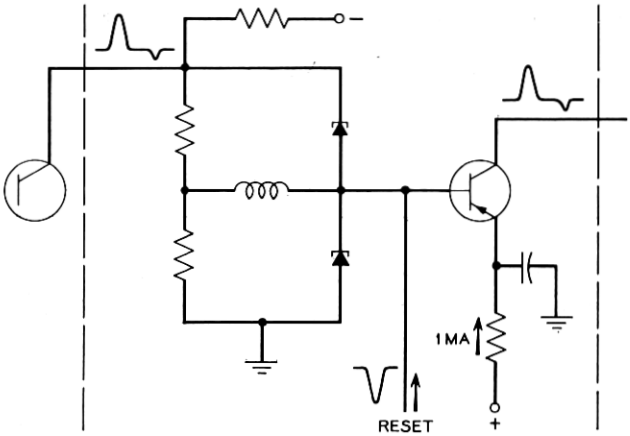


Fig. 30 — Basic counter stage.

A critical characteristic of the binary stage used in this system is its delay stability (see Section 5.1.3). A typical realization of the type indicated in Fig. 30 resulted in the performance shown in Table II for a single binary stage. For this circuit the tunnel diode bias voltage was obtained from the voltage drop of a forward biased diode. These data show that the delay stability performance of this circuit is quite adequate for use in this system.

6.2.4 *Tunnel Diode — Transistor Stage*

A circuit which has proven to be quite useful is the gallium arsenide tunnel diode - 2.5-Gc/s transistor circuit shown in Fig. 31.* The composite

* Ref. 20, pp. 275–277.

TABLE II — DELAY VARIATIONS FOR A SINGLE BINARY STAGE

±0.03 ns for ±20% power supply voltage variations
±0.04 ns for ±5 dB input pulse amplitude variations
0.08 ns over −10°C to +60°C temperature range

input I-V characteristic is very similar to that of a tunnel diode. A GaAs diode was chosen because it has the largest available valley voltage and is available with parameters which are good enough to make the transistor the speed limiting component. In earlier investigations, reliability problems were encountered with GaAs tunnel diodes when the valley voltage was exceeded. This circuit has the feature that the transistor input characteristic protects against this possibility, and furthermore, the tunnel diode, with its "backward diode" reverse characteristic, removes the strain from the transistor for a reversed polarity excitation.

As a bistable circuit, the combination is used to realize a sawtooth phase comparator (Fig. 32) and a pulse regenerator (Fig. 33). In the former application it can be seen that the dc value of the output waveform is proportional to the phase difference of the two input pulse trains. With moderately narrow trigger pulses (<3 ns at the base) this circuit

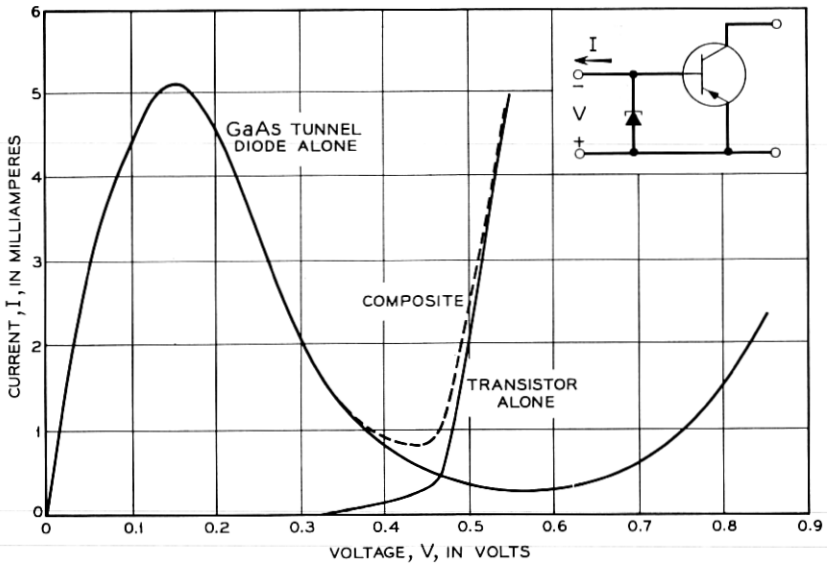


Fig. 31 — Tunnel diode transistor stage.

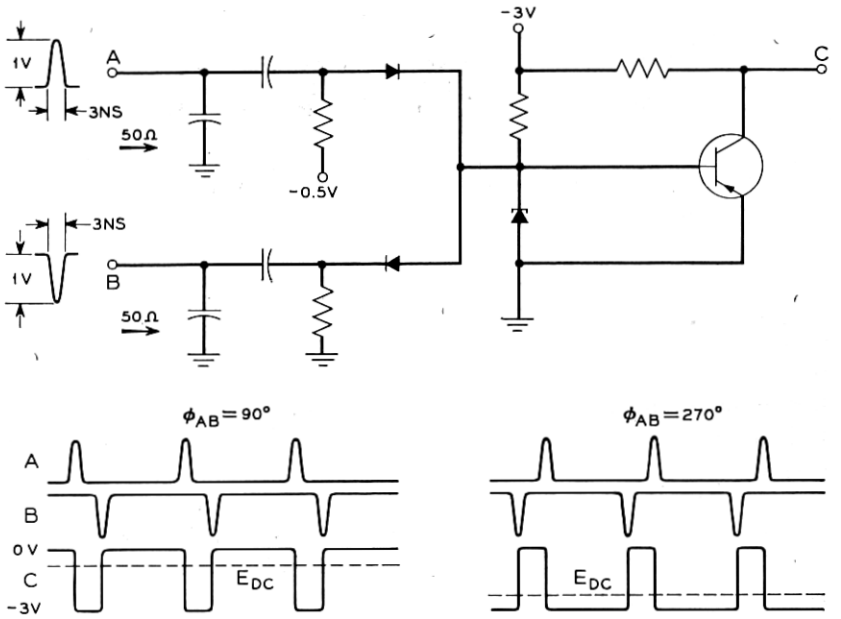


Fig. 32 — Sawtooth phase comparator.

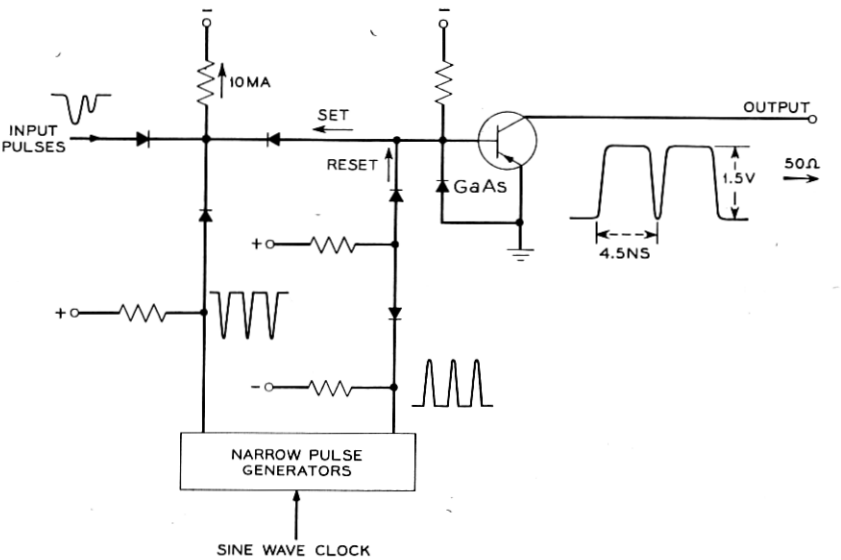


Fig. 33 — 224 Mb/s regenerator.

has been used up to 55 Mc/s (in the video gap inserter and remover) with excellent results.

In the pulse regenerator, the pulse to be regenerated is gated with a clock pulse generated from a sine wave in a step-recovery diode circuit. The resultant pulse turns the transistor ON. A second clock pulse of opposite polarity turns the stage OFF. This circuit is the one which produces the 224-Mb/s pulse train shown in Fig. 27.

Another application of the basic tunnel diode-transistor circuit is in the various one shot multivibrators in the system. Both kinds of R-L load lines with one stable point (quiescent ON and quiscent OFF) have been used with satisfactory results. Output pulse widths range from 4.5 to 300 ns.

VII. EQUIPMENT DESIGN

Since the primary goal of the investigation was to establish the feasibility of processing high-speed digital signals in the manner described, a conservative equipment design approach was used. For the most part, circuits shown as blocks in the preceding figures are constructed as separate units using point-to-point wiring boards mounted in an enclosure which provides good shielding and power supply decoupling. The construction technique for the elastic stores is described elsewhere.[6] Interconnection is accomplished by 50-ohm coaxial cable. Each functional block, such as the mastergroup synchronizer, is realized as a single 19-inch panel. All T1 and sync signaling circuitry is made from standard ESS plug-in modules and mounting hardware.[13] Standard relay racks house the equipment. The multiplexing and demultiplexing bays are shown in Fig. 34(a), and the bay containing the jitterizer and dejitterizer is shown in Fig. 34(b).

The equipment design approach used, although quite adequate from an electrical performance standpoint, would not be suitable for a commercial system. It is quite possible that a mother-board approach similar to that used in the coder[14] would yield suitable electrical performance. Also, integrated and thin-film circuit techniques would be applicable to some circuits.

VIII. SUMMARY

It has been demonstrated that solid-state device and circuit technology has advanced to the point where digital signals with bit rates up to 224 Mb/s can be readily processed. Through the use of the pulse stuffing synchronization technique, with added-bit sync signaling, a

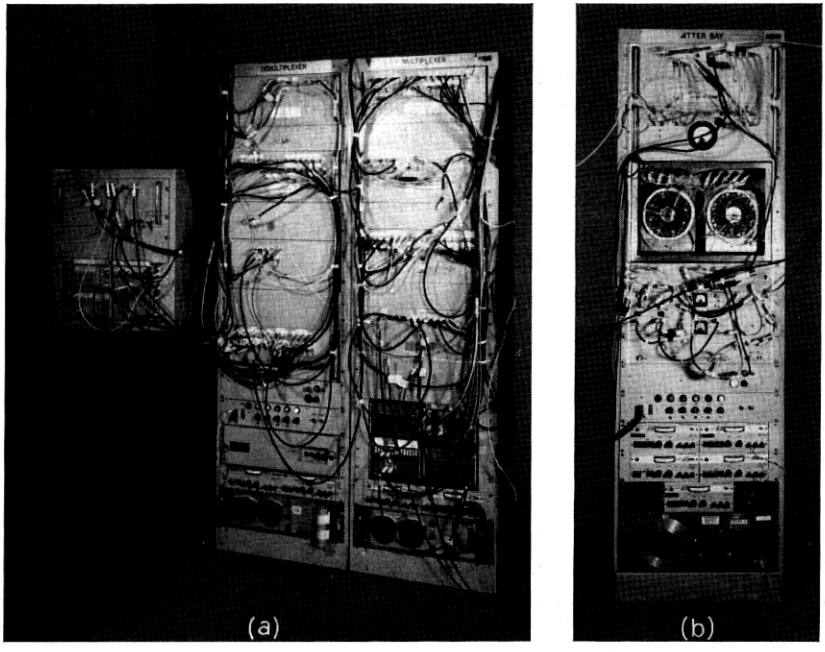


Fig. 34(a) — Multiplexer-demultiplexer bays.
(b) — Jitter bay.

multiplicity of asynchronous signals with a variety of bit rates can be combined into a 224-Mb/s pulse stream, and each signal can be recovered at the other end of the system. The techniques described also furnish the capability of dropping portions of the bit stream at an intermediate point and adding other signals in the vacated time slots. These latter signals can of course also be asynchronous. All of this can be accomplished without highly stable clocks and without large digital storage.

Also, it has been shown that accumulated phase jitter can be controlled sufficiently to avoid signal impairment.

A large number of presentations have been given where the features and performance reported herein were demonstrated. Experience during the course of these demonstrations has confirmed the conclusion that realization of an elaborate 224-Mb/s digital multiplexer-demultiplexer is feasible.

IX. ACKNOWLEDGMENTS

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