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Experimental 224 Mb/s PCM Terminals

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Experimental 224 Mb/s terminal equipment for a toll-grade, long-haul PCM transmission system has been designed, constructed, and successfully operated. Transmission of television and frequency-multiplexed mastergroups of voice channels is emphasized. Fundamental design considerations are explored. Detailed designs and performance levels are briefly mentioned, but are covered in detail in companion articles.

I. INTRODUCTION

During the late 1950's, the feasibility of pulse code modulation for the transmission of voice over cable pairs was established,[1] and since 1962 there have been substantial installations of such equipment. More recently, attention has been focused on extending PCM to much higher bit rates and to long-haul, toll quality systems. This effort has produced experimental 224 Mb/s PCM terminals capable of transmitting broadband signals such as television and mastergroups of voice channels with a signal quality that meets Bell System transmission objectives.

High-performance, high-speed terminals having provision for all major functions required in a commercial system were constructed in order to demonstrate the applicability of PCM to the broadband, long-haul network. Satisfactory solutions to all the major technical problems associated with high-speed PCM terminals have been demonstrated. Two important results of the studies are: the feasibility of precise encoding of broadband signals such as television and mastergroups by means of all solid-state circuits, and the feasibility of adding and dropping channels by digital means without locking the coder sampling frequencies to the line transmission frequency. Thus, a satisfactory solution to the PCM network synchronization problem has been demonstrated. Thorough analysis and experimental demonstration of satisfactory operation of jitter removal equipment indicates confidence that high-speed PCM systems can operate in the presence of time jitter on the received pulse train.

The experimental terminal has been an invaluable asset in obtaining experimental verification of analytical work done over the years on impairments introduced into broadband signals as a result of quantization, overload, time jitter, and digital transmission errors. The analysis was verified without significant discrepancies.[2] The experimental terminal has also been a valuable vehicle for high-speed circuit studies. At the inception of this work there was considerable question as to the technical feasibility of operating thousands of transistors in a circuit environment that required switching times as low as a fraction of a nanosecond. Although isolated circuits had been previously operated at these speeds, there was considerable uncertainty regarding the feasibility of interconnecting and reliably operating large amounts of circuitry at nanosecond speeds.

II. PROBLEM AREAS — PCM TERMINALS

2.1 *Coding and Decoding*

Rendering broadband signals such as color television and frequency division multiplex (FDM) mastergroups into pulse sequences with high precision is a difficult technical task. It is relatively easy to achieve sufficient coder precision so that moderately good picture and voice transmission (6 to 7 digit quality) may be demonstrated over a single codec (coder-decoder). It is a much larger task to build broadband codecs of sufficient precision that a very high-quality signal is delivered after passage through numerous codecs in tandem (9 digit quality). Tandem codecs will be required until digital transmission is available on all routes within the country, for the signal must be decoded each time it passes an interface between a PCM transmission link and an analog transmission link. Also, in the case of coded FDM mastergroups, the signal must be decoded to get access to channels within the mastergroup. With coded mastergroups, if 120 channels are to be dropped and added along a PCM route, the mastergroup must be decoded, the 120 channels (two supergroups) demultiplexed in the frequency domain, two new supergroups multiplexed back into the frequency slots previously occupied by the dropped supergroups, and then the new master group coded for transmission by PCM. It is apparent that the through channels experience an additional coding and decoding each time channels are added to the mastergroup.

2.1.1 *Television Signals*

A minimum bandwith of approximately 4.5 Mc/s is required for adequate transmission of black and white or color television. The PCM coder must, therefore, sample the television signal at at least a 9-Mc/s rate, and the sample must be coded with sufficient precision to avoid significant impairment of the pictures.[3] The number of levels or codes required in the coder depends on the signal-to-noise requirement, the number of codecs to be operated in tandem, and whether the full sync pulse is encoded along with the video component of the signal. Performance also depends on whether the video signal is dc clamped ahead of the coder or whether the signal may "drift" with dc content. Assuming the bottom of the sync pulse is clamped to the first code and the peak video excursion extends to the highest code, the quantization noise performance of Table I is achieved. It is seen that with a 1-db framing impairment (impairment resulting from a particular method of word framing), and recognizing that a 51-db peak-to-peak signal to rms noise ratio is required for a high-quality picture, seven binary digits per code will render a completely satisfactory signal. Allowing for reasonable departures from theoretical performance, up to nine digits per code are required when half a dozen codecs are operating in tandem. Although 8-digit coding may be satisfactory in the present television network, attention has been directed toward 9-digit coding in order to provide increased flexibility.

Assuming 9-digit encoding and a 12-Mc/s sampling rate (in order to

Table I — PCM-TV Performance Levels

Number Digits	$(S/N)_T$	$(S/N)_A$	n
7	52	51	1
8	58	56	3
9	64	59	6

$(S/N)_T$ = Theoretical peak-to-peak signal to rms noise ratio (including 1 db framing impairment).
$(S/N)_A$ = S/N ratio expected in codec at end of maintenance period.
n = number tandem codecs to give S/N = 51 db.

make the television bit rate twice that required for a coded mastergroup) leads to the time scale shown on Fig. 1, which is typical for a color television signal. The signal is sampled every 83 ns, and the signal in the vicinity of a sample changes at a maximum rate of about six steps per nanosecond. Analysis shows that for adequate performance (impairment small compared to quantizing noise) the mastergroup or television signal must be sampled in about 0.5 ns (gate switching time), and the value of the sample must be held constant during the coding interval to an accuracy of one part in several thousand.[4]

The television signal must be bandlimited to approximately half the sampling frequency. It is also important that the filters that accomplish this objective exhibit good transient response. The design of the bandlimiting filters at the input to the coder and the output of the decoder is established by balancing foldover distortion against transient response. Sharp cutoffs produce excessive ringing, while a gradual cutoff produces excessive foldover distortion. The filters may also employ pre-emphasis and de-emphasis.[5]

2.1.2 *Mastergroup Signals*

A mastergroup such as is transmitted in the Bell System's L3 carrier system is made up of 600 voice channels, frequency-division mul-

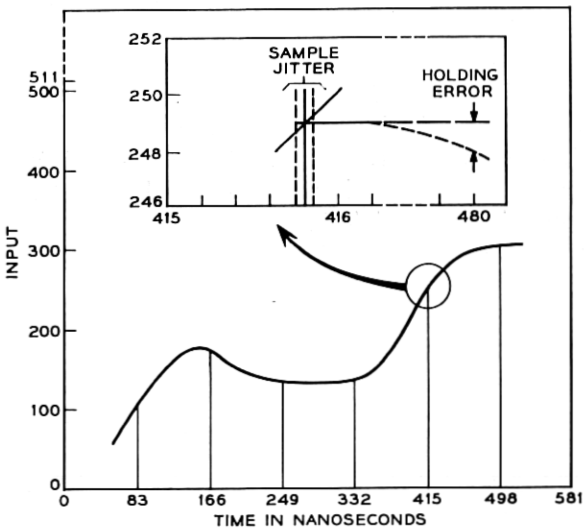

Fig. 1 — High-speed PCM sample and hold. (Expanded-scale insert shows sensitivity to sampling jitter and effect of "droop" on held sample waveform.)

tiplexed by single sideband techniques in a frequency band extending from 564 to 3084 kc/s.[6] It is well known that the mastergroup signal has a Gaussian amplitude distribution.

The mastergroup signal must be applied to a PCM coder in such a way that all code levels are exercised to the greatest extent possible, yet peak signal excursions beyond the range of available codes should occur very infrequently.[7] The theoretical noise performance of a mastergroup codec has been computed, experimentally verified, and is shown in Fig. 2. Minimum noise results when the amplitude of the mastergroup signal applied to the coder is set so that the rms signal

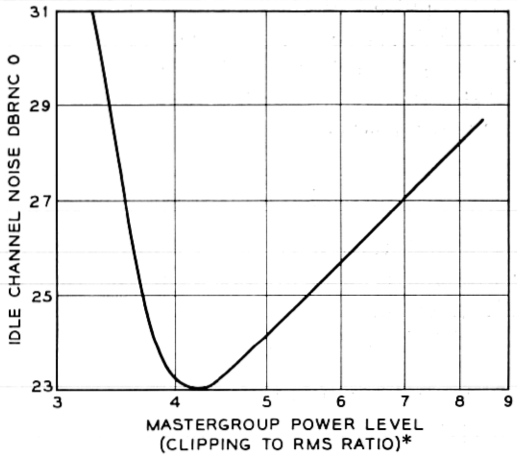

Fig. 2 — Theoretical noise performance of 9-digit mastergroup codec.

voltage is approximately one-eighth of the peak-to-peak voltage required to exercise all codes. For higher mastergroup power levels (small clipping to rms ratio), excessive noise is generated by frequent overloads, while for smaller mastergroup power levels the signal-to-noise ratio decreases because the quantization noise remains constant but signal amplitude drops. Under optimum signal amplitude conditions, 8-digit quantization results in approximately 29-dBrnc0 noise while 9-digit quantization yields a 23-dBrnc0 noise level. To obtain actual noise levels for a given telephone connection, allowance must be made for the operation of several codecs in tandem, imperfections in codec operation, and noise in the FDM equipment. It results that linear 9-digit coding is entirely satisfactory.

With the mastergroup in its normal frequency assignment of 564-

* Ratio of input amplitude at which coder clips to applied signal rms amplitude.

3084 kc/s, the minimum sampling rate is 6.168 Mc/s. This sampling rate may be lowered somewhat if the mastergroup is shifted down in the frequency domain prior to coding. When the mastergroup is coded directly the frequency band from dc to 564 kc/s is wasted. It is worth noting that the master group signal is severely bandlimited as a result of the frequency domain channel stacking, and only modest filters are required before and after the codec.

2.1.3 *Voice Channels*

The D1 channel bank of the T1 carrier system codes 24 voice channels into a 1.5-Mb/s pulse train.[8] The experimental terminal, therefore, does not provide for direct coding of voice. However, the design of the multiplex equipment allows the 224-Mb/s pulse train to be made up of various types of signal components, including 1.5-Mb/s streams of the type transmitted in T1 carrier.

2.1.4 *PICTUREPHONE* Signals*

A broadband signal that may be of considerable importance in future carrier systems is that produced by the Bell System's *PICTUREPHONE* set. The 0.5-Mc/s bandwidth signal has been coded into PCM and transmitted over the experimental equipment. The exact bit rate required for transmission of the *PICTUREPHONE* signal is still under study but is probably in the range of 3 to 6 Mb/s. Rather than develop special coding equipment for *PICTUREPHONE* signals, the sampling rate and the number of digits per code of the mastergroup codec were reduced in order to convert the *PICTUREPHONE* signal into PCM form. A coded *PICTUREPHONE* signal was also transmitted over the 224-Mb/s stream in the time slots normally allotted to two T1 line signals.

2.2 *Multiplexing and Demultiplexing*

The bit sequences from the various coders and bits from other sources such as data sets may be readily interleaved to form a high-speed pulse train provided the various input bit rates are exact submultiples of the high-speed line rate. Assume for the time being that the sampling rates for the various coders are locked to some master frequency, so judicious selection of sampling rates and number of digits per sample gives coder output rates that are harmonically related. A

* "*PICTUREPHONE*" is a service mark of American Telephone and Telegraph Company.

firm requirement is that the system be capable of accepting the T1 line signal (1.544 Mb/s). Also, a rather firm requirement for 9-digit encoding of mastergroups and a minimum sampling rate of 6.168 Mc/s for the unshifted mastergroup has been established. By selecting a sampling rate of 6.176 Mc/s (four times the T1 rate) for the mastergroup, the resulting codec output rate is precisely 36 times the T1 line rate. The multiplex equipment, therefore, sees a mastergroup as equivalent to 36 T1 line signals.

It is very desirable to have an integral relationship between the bit rate required for mastergroups and the bit rate required for television. It does not appear feasible to transmit high-quality television over the bit rate required for a coded mastergroup. It is, therefore, convenient to sample the television signal at twice the mastergroup sampling rate or 12.352 Mc/s, and it has been shown desirable to code television to nine digits also. The multiplex, therefore, sees the television signal as equivalent to two mastergroups or 72 T1 line signals.

There are various fundamental approaches to multiplexing lower speed bit streams into a high-speed stream. These differ primarily in the amount of digital storage provided in the multiplex. Since high-speed digital storage is very expensive, bit-at-a-time multiplexing is presently the most attractive approach for high-speed PCM.

The bit stream organization chosen for the experimental terminal is shown in Fig. 3 which gives the format when transmitting one television signal, one mastergroup signal, and one T1 line signal over the 224-Mb/s line. Ignore the synchronizing pulse for the time being and note that the multiplex circuit generates a basic frame of 145 pulse positions. The frame rate is 1.544 Mb/s, and the last time slot of each frame is devoted to a framing pulse which marks reference time. The

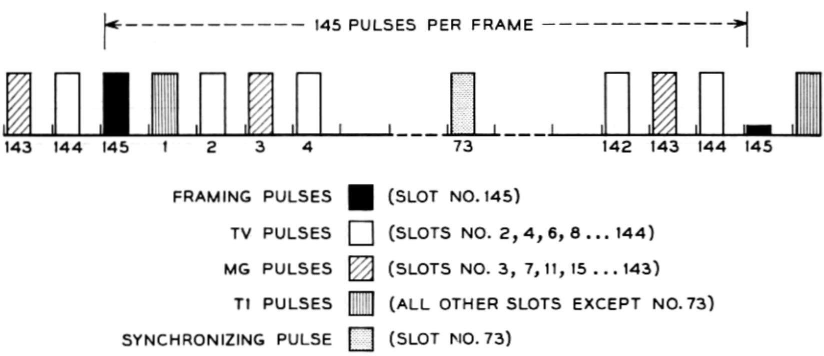

Fig. 3 — 224-Mb/s line organization.

framing pulse is given on ON-OFF statistic (alternating ONE-ZERO) which is very improbable for any other pulse, and the demultiplexer searches for a pulse which repeats at the frame rate and obeys the alternate ON-OFF statistic. A coded television signal is multiplexed into alternate time slots within the frame and a coded mastergroup multiplexed into every fourth time slot. The T1 line signal is transmitted on the 224-Mb/s line as a single pulse per frame, so the 224-Mb/s line may simultaneously transmit up to two television signals, or up to four mastergroups, or 144 T1 line signals. It can accommodate any combination of these signals totaling 144 units, where a television signal requires 72 units, a mastergroup 36 units and a T1 line signal requires one unit.

2.3 *Framing*

The need for an occasional framing pulse on the high-speed line in order to identify reference time at the demultiplexer is now obvious. Since bit multiplexing was chosen, additional framing is required at the various decoders to identify the most-significant digit of each code group. Had word multiplexing been chosen the 224-Mb/s line framing signal would also have identified the most-significant digit of each word. On the other hand, word-at-a-time multiplexing requires an excessive amount of high-speed storage, and leads to an inflexible multiplex based on a particular word length.

There are fundamentally two approaches to word framing of the various decoders. One approach makes use of known signal statistics and compares the statistics of the signal (either before or after decoding) to the known signal statistics.[9] When the decoder is operating on improperly grouped codes, the input-digit and output-signal statistics are altered, this fact is detected, and the phasing of the decoder is shifted until the output obeys the proper statistic. In the experimental terminal, this type of framing is used in the mastergroup codec. This coder operates in the reflected binary or Gray code, and it can readily be shown that such a coder operating on a Gaussian signal of the rms value previously shown to be optimum for coding of mastergroups produces output digits where the probability of a one in various digit positions is essentially 0.5 for all digits except the second, which has a 0.95 probability of being a one. Code groups are identified within the mastergroup decoder, therefore, by searching for the digit of each code that has high probability of being a one.[10] Many other approaches to statistical framing have been investigated.

A second approach to word framing a decoder is to add a distinguishable statistic to the signal being coded. This may be added in analog form before the coding process or in digital form after the coding process. The approach is demonstrated in the experimental system in the television codec. The least-significant digit of each ninth coded word from the television coder is forced to an alternate 1,0 sequence. The framing circuit for the television decoder, therefore, looks at every 81st received time slot and searches for a phase position where each 81st pulse follows an alternate 1,0 pattern. It can be shown that the quantizing noise impairment introduced by robbing the least-significant digit every m words is

$$10 \log \left(1 + \frac{3a}{m}\right) \text{dB},$$

where $a = 2$ if the decoder operates on the robbed bits just as if they were signal bits, and $a = 1$ if the decoder does not operate on the robbed bits. For $m = 9$, the increase in theoretical quantization noise is 2 dB if no special action is taken at the decoder or 1 dB if the robbed bits are not decoded.

Framing by means of occasional digits has been selected as preferable to utilizing clusters of framing bits in order to minimize the amount of high-speed digital storage required. Samples delivered by the decoder must be at a uniform rate, and clusters of framing digits generally interfere with the uniformity of receipt of codes unless sufficient digital storage is provided to bridge the time gaps introduced by the framing pattern. Also, it may be difficult to completely remove the time jitter introduced by large time gaps.

2.4 *Synchronization*

Multiplexing was stated to be a relatively simple operation if the bit streams entering the multiplexer are precise submultiples of some master frequency. This is readily accomplished if the sampling clocks for the various coders are locked to the same master frequency. In a nationwide network, however, coders are spread all about the country, and it is not a simple matter to frequency lock all coders to a master clock. If the various sampling clocks in a PCM network are not submultiples of the same frequency, multiplexing may still be readily accomplished provided techniques are developed for shifting a coder output from one rate to a slightly different rate. Both bit-rate shifting techniques and locked-frequency techniques have been examined.

2.4.1 *Master Clock*

The most obvious approach to frequency locking the sampling rates of coders at various geographic locations is to distribute a master clock to all coder locations. Sampling clocks for all coders are then derived from this master clock, so the outputs of the various coders are harmonically related in frequency. Then multiplexing and demultiplexing, including facility for digital adding and dropping, and the gating of certain portions of a high-speed bit stream from one line to another, are readily accomplished.

Such a system has numerous undesirable features. Since one clock serves the whole nation, the clock and its distribution system must be extremely reliable — protected by redundancy against technical failures as well as man-made or natural disasters. Since precise relative phasing must be maintained on all bit streams entering a high-speed multiplex, this approach requires that all transmissions delay variations be built out by variable delays located ahead of the multiplexer. The delay variation in the clock distribution system itself will amount to approximately 20 μs for a 1000-mile low-frequency radio link, approximately 2 μs for a coaxial link of the same length and approximately 0.2 μs for a 1000-mile microwave radio link. Even 1 μs of delay variation may necessitate the need of 100 bits of high-speed storage. Such a system, therefore, requires relatively large digital stores at each multiplex point. The storage time must be variable or of the "elastic delay" type, because the sum of transmission delay and delay through the store must be held constant to approximately 1 ns.[11,12] Two signals arriving at a point over separate 1000-mile links of cable must be phased to ± 0.5 ns. This is to be compared to the total delay of each 1000-mile circuit of approximately 8 ms.

The master clock plan has appreciable "start up" costs and is especially unattractive for the early days when there are relatively few PCM systems to share the relatively large costs of the master clock. Also, the technique is "brittle" in that delays must be precisely matched — precise length of cable interconnecting equipment is important, and there is appreciable equipment shared over otherwise independent transmission links. At the time of introduction of the master clock, existing PCM systems, such as T1, would also have to be modified in order to lock their clock rates to the master clock rate.

2.4.2 *Phase Averaging*

A technique has been studied which allows sampling clocks of all coders to be frequency locked, yet does not establish any individual clock as a master.[13] This technique is known as phase- or frequency-averaging. It makes use of the fact that an interconnected network of digital systems, especially two-way systems, has pulse streams entering and leaving every codec location. One may, therefore, establish a reference phase or frequency for each codec location which is the average of all phases or frequencies entering that location. If each location transmits the same phase or frequency to all other connected locations, it can be shown that the resulting reference frequencies established at the various locations are identical. For a particular implementation, where the reference phase at each location is established by an oscillator whose phase is locked to the average phase of all signals entering the location, it can be shown that the resulting sampling frequencies throughout the network are not only identical, but also bounded by the lowest and highest free-running frequencies of the various oscillators in the network. It can also be shown that the sampling frequency established by such a network responds to transients in a damped manner. If the network is disturbed (such as by addition or removal of equipment), the sampling frequency will settle in a well-controlled manner to the new frequency.

Networks synchronized by phase averaging do not have as serious a reliability problem as those synchronized by a master clock. On the other hand, much of the "brittleness" of the master clock system remains, i.e., precise control of phase, much equipment common to otherwise independent transmission links and necessary modification of existing systems. The scheme has been analyzed in considerable detail by Bell Telephone Laboratories' Systems Research Department, however, further analysis of specific embodiments of the phase averaging technique should be completed before committing a large system to this approach.

2.4.3 *Stable Clocks*

The use of very stable oscillators as sampling clocks allows asynchronous operation of a PCM network. If C bits of digital storage are provided at each multiplex interface, and a bit stream of frequency f_0 is multiplexed to a frequency $f_0 + \Delta f$, then the digital store will be exhausted (contents depleted or storage capacity exceeded) every $C/\Delta f$ seconds. Defining $s = \Delta f/f_0$ as the clock stability factor, the store is exhausted every C/sf_0 seconds. When operating at the highest pulse-rate of interest i.e., 100 Mb/s for television, store exhaustion period is approximately $C/s \times 10^{-13}$ days. Each time the store is exhausted, a group of pulses is either repeated or lost, and the system may have to reframe to re-establish proper timing sequence. If the store capacity and store resetting mechanism repeats or drops complete frames, then exhaustion of store capacity at the multiplex interface will result only in the loss of information bits and will not initiate a long reframing sequence. Nevertheless, if bits are to be lost or inserted into the pulse stream not more often than once per day, then the size of store required is $s \times 10^{+13}$ for the 100-Mb/s signal, as shown in Fig. 4. With the clock stability factor of 10^{-13} only one time slot of storage is required for once-a-day reframing. On the other hand, a clock stability factor of 10^{-10} dictates 10^3 bits of storage to produce once-a-day reframing.

There does not seem to be a question of technical feasibility of operating even high-speed PCM networks asynchronously. Use of a cesium beam clock with a long-term stability of 10^{-12} results in a very small storage requirement at all multiplex interfaces except at very high speeds and then only tens of bits (at 100 Mc/s). On the other hand, very stable clocks are expensive and, therefore, the stable clock must be shared over a number of systems — resulting in reliability problems. However, the most serious drawback of this approach to synchronization results from the fact that occasionally bits are lost or are repeated.

Although the long-term digital error rate due to store exhaustion is equal to the stability factor, s, the errors generally occur in bursts and/or produce reframing. The time of occurrence of these bursts may

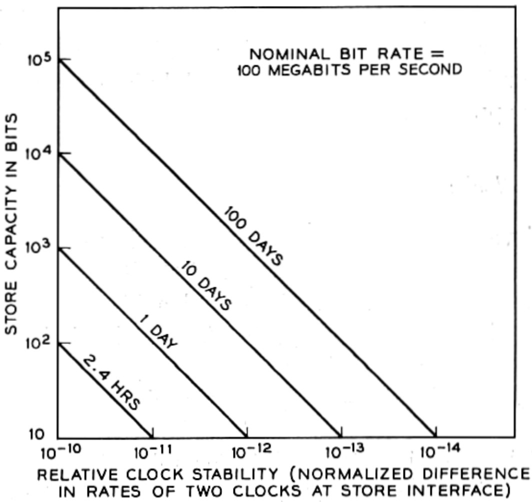

Fig. 4 — Contours of constant store exhaustion periods.

be controlled by command resetting of the store. This approach to synchronization may be entirely satisfactory from the point of view of analog signals, but may be disastrous for certain data signals. Although simple in concept, this approach is not as economical as might appear to be the case at first glance, unless frequent reframings are allowed.

2.4.4 *Pulse Stuffing*

A technique for asynchronous multiplexing has been developed which does not require that all coder clocks be synchronized, yet does not periodically lose bits. In this approach a coder does not provide as many pulses per second as the multiplexer needs, and the multiplexer is arranged to skip over occasional time slots so as to make up the frequency difference.[14,15] The multiplexer also communicates to the demultiplexer the precise locations of the "stuffed" time slots. The demultiplexer removes the stuffed slots from the pulse train, closes the time gaps occupied by the stuffed slots, and thus returns the pulse stream to its original form.

The basic operation is shown in Fig. 5. Pulses entering the multiplex point are written into a 3-bit digital store, and are read from store by

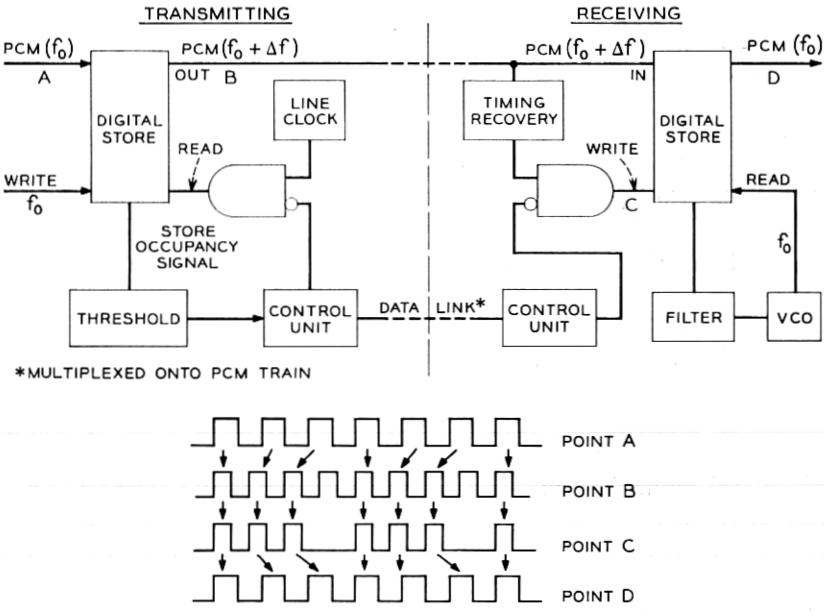

Fig. 5 — Pulse stuffing synchronization.

a submultiple of the line clock which is slightly faster than the input bit rate. There is a built-in tendency to exhaust stored bits, and the number of stored bits is monitored by a store occupancy signal. When this signal exceeds a critical value, the threshold circuit signals that a time slot should be stuffed into the output train. Prior to the actual stuffing operation, a control unit communicates to the receiving equipment the precise location of the stuffed time slot, then at the appropriate time provides the signal to inhibit reading of the store, allowing transmission of a stuffed time slot.

At the receiving end of the system the pulse train is written into a small store, but the stuffed time slots are not allowed to enter the store. Only the original coder output pulses flow through the store and these are read from the store at a smooth rate by using the store occupancy signal (after appropriate filtering) to drive a voltage controlled oscillator.

The store occupancy signal is a measure of the difference between phases of input and output pulses, and the closed loop around the oscillator is a rather conventional phase-locked loop.[16] This loop should have a cutoff frequency which is low compared to the average stuffing rate. In this way, time jitter on the output signal resulting from the removal of the stuffed pulses will be small and this jitter will not accumulate very rapidly on signals passing through tandem multiplexers.

The transmitting equipment must be capable of signaling the location of the stuffed pulse positions to the receiving equipment, and do this precisely, even in the presence of high transmission error rates. Error free signaling is most readily accomplished by utilizing redundant coding in the "data-link" of Fig. 5, but adequate signaling may also be accomplished by a predictive receiving circuit which operates on the basis that stuffing rates vary slowly with time and a future stuffed pulse position may be predicted on the basis of time occurrence of all past stuffed pulse positions.

Signaling the stuffed slot position information over the PCM line (multiplexing the "data-link" of Fig. 5 into the PCM stream) is attractive, and may be accomplished by devoting an occasional pulse on the PCM line entirely to this purpose. Another alternative is to multiplex the signaling information into the bit stream from the coder (without increasing bit speeds). J. W. Pan has proposed a "statistical subcarrier" approach based on this latter technique wherein certain codes are forbidden at the coder, and these forbidden codes are substituted for certain probable codes in order to transmit stuffed slot location information. At the receiving end receipt of the forbidden codes is noted, and the codes are changed back into the original probable code.

The most promising approach, however, appears to be the technique of adding occasional additional bits into the pulse stream as a "data-link" to communicate "stuffed" time slot positions. This approach was taken in the experimental terminals where a single pulse per frame was devoted to this task. This pulse was transmitted over a pulse position normally allotted to a T1 line signal, but normally a frame of 146 pulses would be required to transmit a frame of 144 information pulses. The last pulse per frame is used for framing, and the 73rd used for the synchronization data link, as shown in Fig. 3.

2.5 *Jitter Reduction*

The delay a PCM pulse train experiences in passing through a self-timed regenerative repeater is necessarily a function of pattern density being transmitted.[17] The amount of jitter introduced by each repeater is small, perhaps a few degrees of phase shift at the pulse repetition frequency.[18] For random pulse patterns, it is probable that the jitter introduced by a given repeater is random with an rms value of a few degrees. This jitter is introduced at each repeater and accumulates along a string of repeaters proportional to the square root of the number of repeaters.[19] A repeater design that results in an rms jitter of five degrees per repeater will result in the accumulation of 150° of rms jitter in a string of 1000 such repeaters.

The bandwidth of the jitter introduced into the pulse stream by a number of self-timed repeaters is determined by the effective Q of the timing extraction circuit of each repeater. Since the transmission pulse rate is usually very high compared to the bandwidth of a signal before coding, and since extremely high repeater Q's are difficult to achieve and result in uneconomical repeater designs, then it is quite likely that a long string of regenerative repeaters will introduce timing jitter of sufficient amplitude and broad enough frequency spectrum that it will impair the quality of any broadband signal being transmitted. Time jitter on the PCM pulse train results in pulse postition modulation of the decoder output, and this introduces noise components into the signal.[20]

Both television and mastergroup signals are quite vulnerable to pulse jitter. The amount of jitter that one might tolerate in a coded mastergroup has been computed, experimentally verified, and is shown in Fig. 6. Results are plotted for the most vulnerable channel (the one multiplexed to the highest FDM frequency slot), and two constraints have been placed on the resulting signal impairment. For large jitter bandwidths, the effect is to produce crosstalk between channels within the FDM package, and this has been constrained to equal theoretical 9-digit quantizing noise (if the jitter is random the crosstalk will be unintelligible, but if the jitter is sinusoidal, and a multiple of 4 kc/s, intelligible crosstalk would be produced). For jitter bandwidths much less than 4 kc/s, the effect of jitter is to shift frequency components within a given channel, which results in signal distortion. The curve of Fig. 6 constrains low-frequency jitter to a level which produces a signal-to-distortion ratio of 30 dB.

Jitter introduced into a PCM pulse train does not constitute an irremovable signal impairment. It is relatively easy to remove jitter from a pulse train, particularly bothersome high-frequency jitter. This is accomplished by writing the jittered pulse train into a digital memory and reading the pulses from memory at a smoothed rate. A circuit for accomplishing this, a dejitterizer, is shown in Fig. 7.[11] The input pulses are read sequentially into memory cells in a jittered fashion. However, the bits are read from memory by the controlled oscillator, which is locked to the fundamental pulse rate. The flip-flop phase comparator keeps the store "half full" on the average by supplying a control signal for the oscillator. By use of a suitable low-pass filter ahead of the controlled oscillator, the resulting phase-locked loop may be designed to have a high Q. Obviously, the pulse stream out of the dejitterizer will

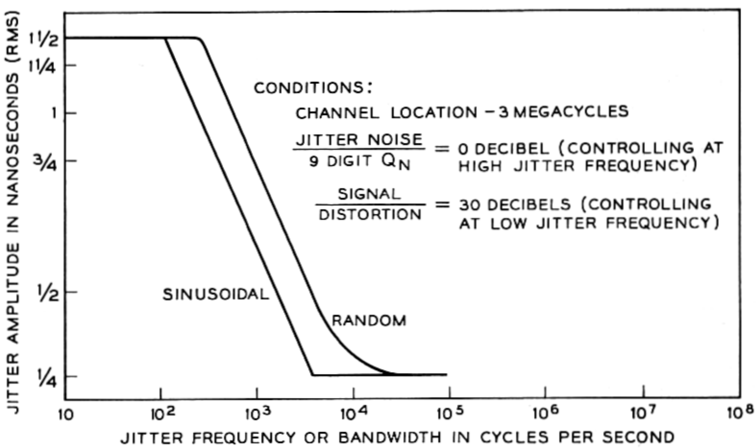

Fig. 6 — Jitter allowed in FDM-PCM system.

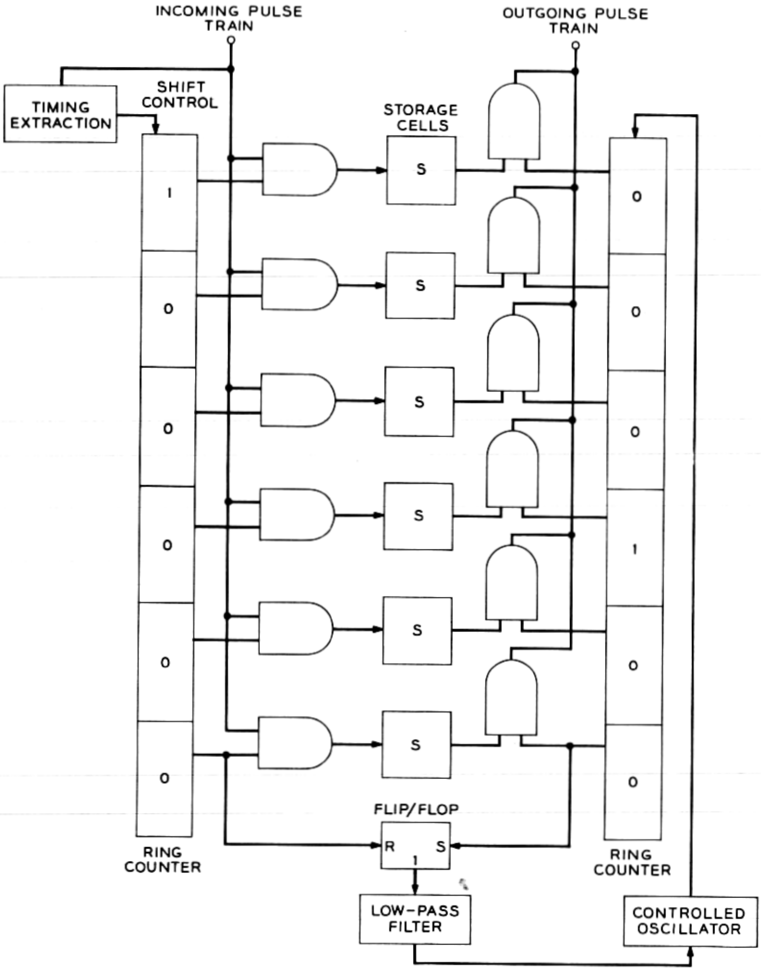

Fig. 7 — Jitter reducer circuit.

contain some low-frequency jitter components, as determined by the frequency response characteristic of the phase-locked loop. Very high effective Q's can be realized by reducing loop gain, but this results in large static phase shifts (a large correction signal must be supplied from the phase detector to overcome any drifts in natural frequency of the oscillator). Large static phase shift "wastes" storage capacity in the memory.

Although the dejitterizer does not remove very low-frequency jitter components, very low-frequency jitter components do not significantly impair the coded signals. For example, very low-frequency jitter is introduced by delay variations in the transmission media, especially as a function of temperature, and such slow variations could be removed only by the introduction of very large stores. The amount of very low-frequency jitter that one can tolerate depends on the types of signals being transmitted, and the jitter requirements shown in Fig. 6 were deliberately not shown in the frequency range below ten cycles. It is apparent that the curve of Fig. 6 can be extended from 1.5 ns at ten cycles to an infinite amount of jitter at zero frequency. For speech, the subjective impairment of large amounts of low-frequency jitter is small, so the low-frequency end of Fig. 6 is determined by certain narrowband special service signals that may be transmitted over a voice channel. Subjective tests of the effect of jitter on color television suggest the signal is not significantly impaired by Gaussian random jitter of up to 1 ns rms amplitude.

III. THE EXPERIMENTAL TERMINAL

The experimental terminal design focused attention on the important PCM problem areas to be overcome prior to the design of a commercial high-speed system. These areas include:

— Coding and decoding of black and white and color television

— Coding and decoding of mastergroups of voice channels

— Multiplexing of lower-speed digital signals into high-speed PCM

— Ability to organize the bit stream in such a way as to accommodate a wide range of input signal mixtures

— Ability to control information flow through the PCM network with adequate reframe times for each circuit

— Ability to operate the various coders with sampling rates independent of the line transmission rate

— Ability to reduce the expected amount of pattern jitter accumulation to levels that may be tolerated by the signal components.

An important overall objective was that the various signal components be processed with the precision required for a commercial system.

The resulting terminal block diagrams are shown in Figs. 8 and 9. A commercial television signal is sampled at 12 Mc/s and each sample coded with 9-digit precision. A mastergroup signal is sampled at 6 Mc/s and also coded with 9-digit precision. Capability for transmission of two 1.544-Mb/s PCM signals is also provided, and the additional unused time slots are filled with random pulses. The master-group coder and the 1.544-Mb/s line signals are not frequency locked to the 224-Mb/s

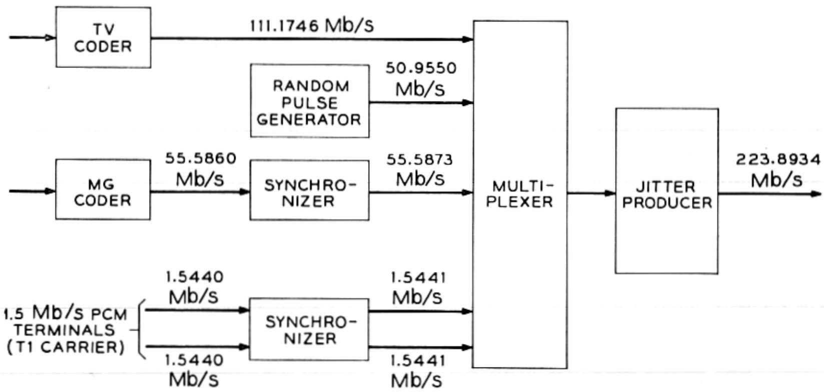

Fig. 8 — Transmitting terminal.

line, and the frequency difference is made up by pulse stuffing-type synchronizers. The multiplexer interleaves the various signal components and the jitter producer simulates transmission of up to 4000 miles of repeatered line. The received signal is dejitterized and demultiplexed. The television signal is decoded, and thereby restored to analog form. The mastergroup signal must have the stuffed time slots removed by the desynchronizer prior to decoding. The stuffed time slots are also removed from the 1.544-Mb/s signals, which may then be transmitted over T1 carrier lines to T1 carrier terminals. The T1 line signals have also been used to transmit high-speed data and coded *PICTUREPHONE* signals.

Although the experimental equipment appears to be a point-to-point system, all the features have been provided that are required

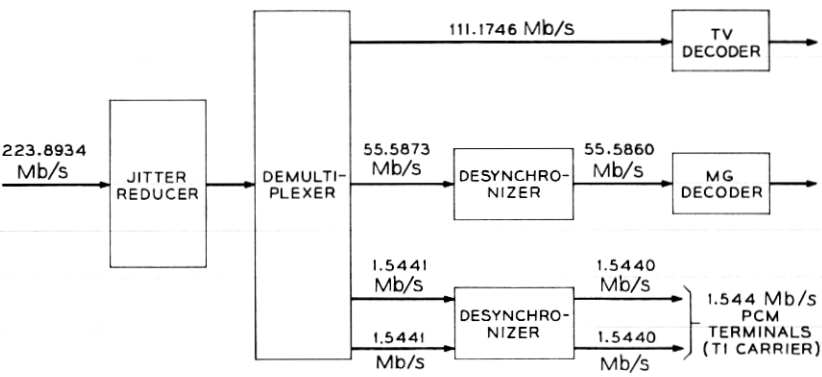

Fig. 9 — Receiving terminal.

for terminal equipment located along the PCM route to add and drop portions of the 224 Mb/s stream.

In addition to the terminals described above, a 224-Mb/s repeatered line (for use with coaxial cables) has been developed. This line will be the subject of a future paper by the group responsible for repeater development.

IV. PREFERRED CIRCUIT APPROACHES

4.1 *Coding*

Work on the broadband experimental PCM system was initiated at a time when the only sure road to success in video coding involved use of the beam encoding tube. This device was, therefore, further perfected and extended to 9-digit capability.[21] The basic device consists of cathode and lens structure for generating a ribbon beam which is focused onto a code plate. The signal sample to be coded is applied to the deflection plates. Beam deflection is proportional to the sample voltage, and apertures on the code plate allow current to be collected on output wires in an on-off pattern defining a binary number proportional to the sample. The major sources of signal impairment in such a coder are nonuniformity of current density across the beam, tilt of the beam relative to the code plate structure and an adverse ratio of smallest aperture width on the code plate to a standard deviation of the thickness of the electron beam. These parameters have been sufficiently controlled and sufficiently precise external solid-state circuits have been constructed so that the resulting coder performs with the quantizing noise level within a few dB of theoretical performance when operating at 12 Mc/s sampling rate and 9-digit coding.

An effort parallel to that devoted to the perfection of the tube coder was directed toward all solid-state encoding. A survey was made of possible coding approaches, and a "folding" encoder was selected for development. This coder consists of tandem operational amplifiers (one for each digit) where each operational amplifier has the input-output characteristic shown in Fig. 10. The transfer characteristic has a slope of precisely $+2$ for negative input signals and a slope of precisely -2 for positive input signals. The coder operates directly in the reflected binary or Gray code. The digits are obtained from each stage — a zero if the gain (slope) is in the $+2$ state and a one if the gain is in the -2 state. The performance of such a coder is limited by the fundamental accuracy (static and dynamic) with which the input-output characteristic can be established.

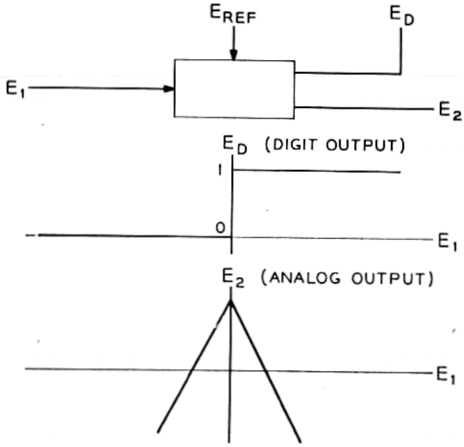

Fig. 10 — Characteristic of one stage of folding coder.

The basic technique for realizing the characteristics of Fig. 10 uses the operational amplifier with nonlinear feedback shown in Fig. 11. It is seen that positive input currents are routed to the E_B output and negative input currents are routed to the E_A output. The E_D output undergoes an abrupt transition as the input current goes through zero and provides a convenient point for extracting the coded digit. Various techniques may be applied to combining E_A, E_B, and a reference so as to produce the desired characteristic of Fig. 10.

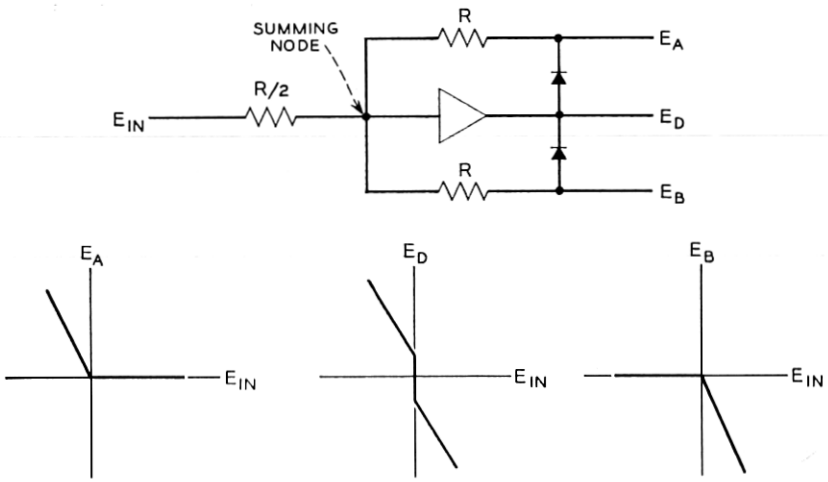

Fig. 11 — Realization of characteristic for solid-state coder.

Precise 9-digit encoding of television signals requires operational amplifiers that settle to an accuracy of one part in several thousand in a few nanoseconds. This level of performance is presently achievable, and the folding coder approach is a sufficiently satisfactory solution to the precise high-speed coding problem that further development of the coding tube does not appear warranted. The solid-state coder is more economical than the beam tube coder (for the production rates envisioned) and, in addition, is much smaller, and does not require high voltage power supplies. There are other potential advantages such as reliability, but it remains to be proven that these advantages exist in reality.

Both the beam tube coder and the solid-state coder have been used for coding mastergroup and television signals. The resulting coder assemblies are shown in Figs. 12 and 13. Both arrangements require precise sample-and-hold circuits and equipment to convert the parallel code available from the coder to a serial line code. The television coder also includes the framing pattern generator which forces the least-significant digit of each ninth code word to an ON-OFF pattern. The mastergroup coder transmits no special digits for identification of word framing.

4.2 *Decoder*

A standard resistor ladder network decoder is employed for decoding of broadband signals. Precise reference currents are gated into a resistive ladder network with 6-dB attenuation between current injection points. Extreme care must be exercised in designing the decoder, how-

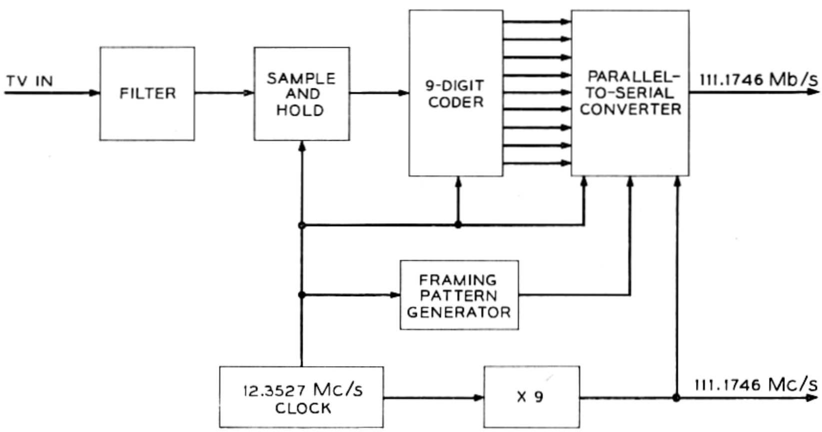

Fig. 12 — Television coder.

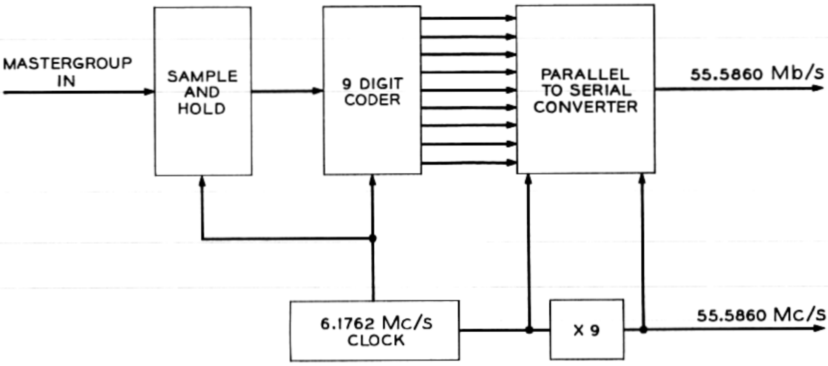

Fig. 13 — Coder for FDM mastergroups.

ever, to prevent the digital control signals from crosstalking into the analog output. Also, precise broadband resistors with end-of-life tolerance of better than 0.1 per cent are required for 9-digit decoders. Broadband precision resistors for the experimental terminals have been realized by the use of nitrided tantalum thin-film. Also, low-capacitance, negligible-storage-time diodes are required for gating of the reference currents. Both gallium arsenide and hot-carrier silicon diodes have served this purpose. Resulting decoder arrangements for television and mastergroups are shown in Figs. 14 and 15. Note that the transmitted code must be converted from Gray to binary, the serial train converted to parallel form, and the output of the decoder must be resampled to remove "spikes" generated during the time of change

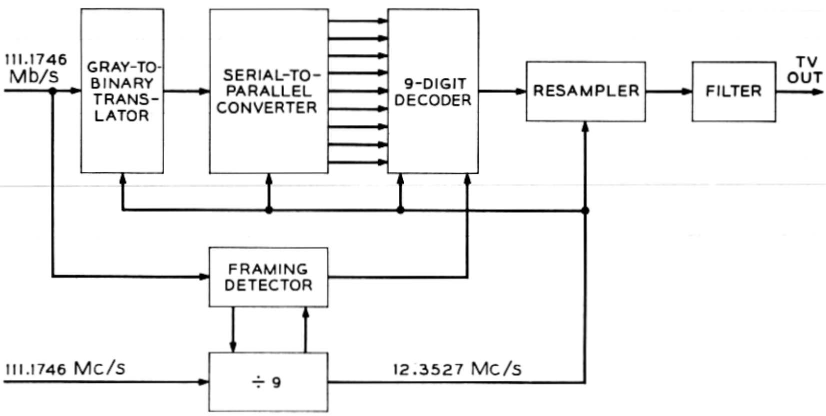

Fig. 14 — Television decoder.

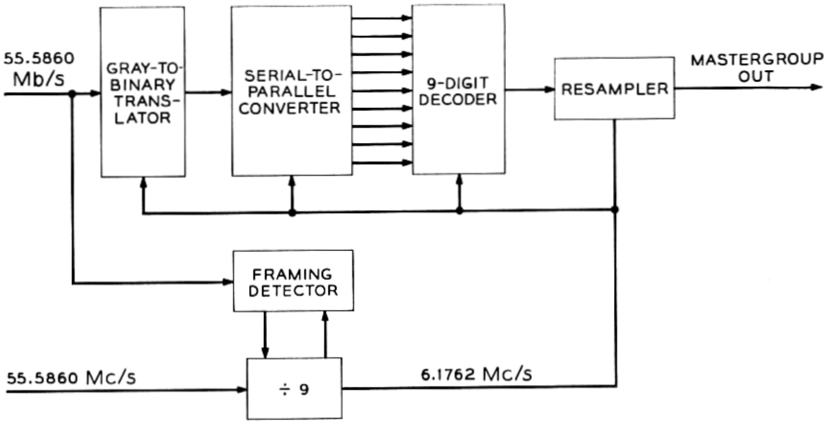

Fig. 15 — Decoder for FDM mastergroups.

of code. In the television decoder, the forced least-significant digit must be searched out to lock the decoder timing so as to properly group incoming words. In the case of the FDM decoder, word framing is accomplished by searching out the second digit in the Gray code, a digit which has a much higher probability of being a ONE than any of the other digits.

4.3 *High-Speed Multiplexer-Demultiplexer*

The multiplexer for combining the various low-speed trains into a 224-Mb/s pulse stream, and the associated demultiplexer are organized in such a way as to accommodate the various options required for a given signal package. Television equipment may be replaced by the equipment required for two mastergroups, and mastergroup equipment may be replaced by equipment to handle 36 T1 line signals.

In the experimental terminals the television signal is handled synchronously, and the repeatered line clock is derived from the video signal. This is accomplished by a two-bit elastic-store, phased-locked-loop arrangement shown in Fig. 16 as the video gap inserter. This unit not only derives the appropriate line frequency but also provides momentary storage for the video signal while the multiplex framing pulse is being transmitted.

Sampling clocks for the T1 line signals and the coded mastergroup operate independently of the 224-Mb/s line rate. The frequency difference is made up by the pulse stuffing technique previously described. The sync signal transmitter generates the basic pulse format for the data link interconnecting the multiplex and demultiplex. This data link is time shared among all asynchronous inputs. The output of the sync signal generator is a 1.544-Mb/s signal which is multiplexed into the transmitting bit stream. This 1.544-Mb/s data link signal is made up of repeating sequences, and each sequence begins with a redundantly coded marker code. The first three time slots after the marker code are devoted to the first signal component to be synchronized, the second three time slots to the second component, etc. When an input signal train is to be stuffed, three ones are transmitted in the appropriate time position. Receipt of two or more ones in the three time slots assigned to a given signal signifies stuffing has taken place, and the receiver drops out a time slot in a predetermined position, which has been arranged to be precisely the position of the stuffed slot.

The demultiplex equipment (Fig. 17) operates in the manner similar to the multiplexer. There is a frame detector that searches for the 224-Mb/s framing pulse and locks the receiving clock to the appropriate phase. The sync signal receiver detects the synchronizing marker code and demultiplexes the stuffing commands so as to provide the proper

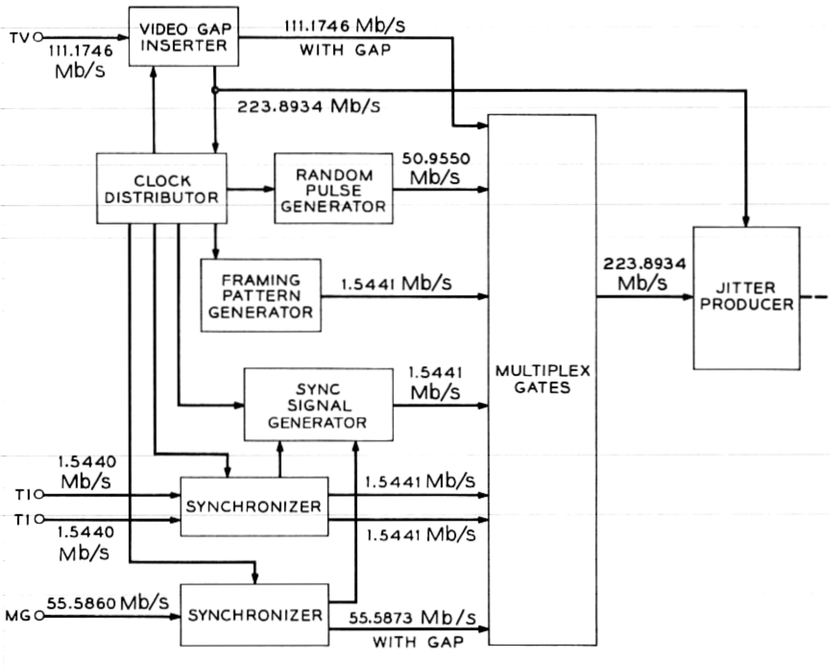

Fig. 16 — High-speed multiplex.

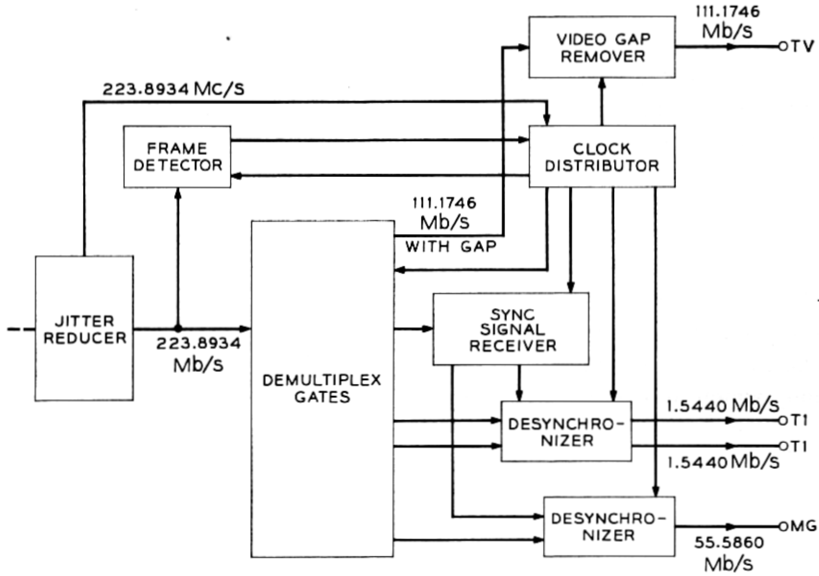

Fig. 17 — High-speed demultiplex.

write-inhibit signals to the elastic stores of the desynchronizers. The video gap remover closes the time gap introduced into the video signal by the multiplexer and thus delivers the same bit sequence to the television decoder as had been generated by the television coder.

A large portion of the multiplexer-demultiplexer circuits operate at high bit speeds. For rates up to about 120 Mb/s, logic is performed by high-frequency planar silicon transistors — often operating in the current routing or pulse routing mode.[22] The 224-Mb/s speeds have been achieved by using tunnel diodes and tunnel diodes in combination with a high-frequency germanium transistor ($f_t \approx 2.5$ Gc/s). Both silicon point-contact and hot-carrier diodes have been used with success in gates of fractional nanosecond rise time. Care has been exercised in the layout of circuit blocks and in construction techniques. All circuit functions have been realized by conventional construction techniques augmented by the use of a few integrated circuits and thin-film components. Of course, stripline and coaxial interconnections are frequently used.

4.4 *Jitterizer and Dejitterizer*

High-speed jitter reduction equipment of the type shown in Fig. 7 has been used to remove the effects of pattern jitter. Eight storage slots were provided in the elastic delay, and an effective Q as high as 10^7 has been realized in the design of the phase-locked loop, which also exhibits satisfactory lock-in, pull-out, and static phase shift performance.

A second dejitterizer was constructed and operated as a jitter producer. By introducing bandlimited noise in the phase-locked loop, it is possible to simulate the expected jitter performance of a repeatered line. This has been used as a vehicle for observing signal impairments resulting from jitter as well as demonstrating the ability of the dejitterizer to remove the expected amounts of pattern jitter.

V. SYSTEM PERFORMANCE

Companion papers give detailed design and performance information for the various parts of the experimental terminal.[23,24] It has been established that signals transmitted through the experimental terminals meet Bell System transmission objectives for long-haul systems, and in a signal deterioration sense, a commercial design need not perform at a significantly higher level than has been achieved in the experimental equipment. The beam-tube encoder has been used at both television and mastergroup speeds and more than meets the objectives that have been tentatively set for in-service performance of a broadband codec. The solid-state coder also meets expected performance level requirements when coding mastergroups. However, the quantizing noise falls 2 dB short of present objectives when coding television. Performance is currently being improved, but even at the present performance level one should be able to operate at least four codecs in tandem and yet meet transmission objectives for television.

It has been shown that the pulse stuffing technique (for synchronization) is an effective solution to the synchronization problem. Performance of the T1 carrier terminal and the mastergroup codec when transmitting over the 224-Mb/s line has been shown to be independent of the precise sampling frequency, and these frequencies may drift over a range which is quite adequate for run-of-the-mill crystal oscillators. This system is also capable of simulating the jitter expected in 4000 miles of repeatered coaxial line, and, as a result of the action of the dejitterizer, there is no noticeable signal impairment introduced by the expected amounts of jitter.

The experimental terminal utilizes approximately 1300 transistors, and many of these are operated at nanosecond speeds. In spite of the serious problems presented by high-speed, high-accuracy circuits, all these devices have been satisfactorily interconnected, and the resulting system has proven to be quite reliable. It has operated for approximately a year without major difficulties, and its operation has been satisfactorily demonstrated on numerous occasions.

VI. CONCLUSIONS

Experimental equipment has demonstrated the technical feasibility of the transmission of high-quality broadband signals by means of pulse code modulation. The experimental terminals demonstrate a satisfactory solution to all fundamental system problems. Signal impairment introduced by the experimental terminals does not differ significantly from analytical predictions, nor does the signal impairment differ significantly from that expected from a commercial system.

VII. ACKNOWLEDGMENTS

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