



**HEWLETT  
PACKARD**

**OPERATING AND PROGRAMMING MANUAL**

**8182A  
DATA ANALYZER  
(Including Option 001)**

This manual applies directly to all instruments.

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HERRENBERGER STR. 110, D-7030 BOBLINGEN  
FEDERAL REPUBLIC OF GERMANY

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15409A  
5 plug-on BNC adaptors



15410A  
5 plug-on SMB adaptors



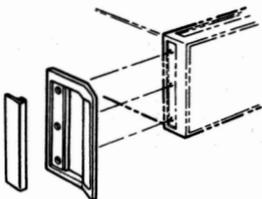
15411A  
5 plug-on coax open-end adaptors for fixed wiring or use of custom connector



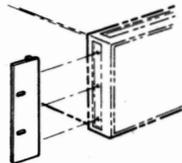
15415A  
5 plug-on miniprobes, which can be used in conjunction with the HP 10024A IC Test Clip for easy probing of dual in-line packages



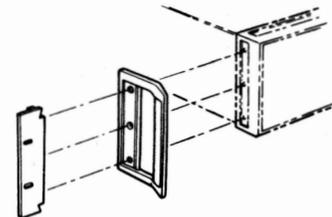
15416A  
Cable for parallel operation of 2 each 8182A.  
Ensures synchronous operation of setups with up to 64 channels



Front handle  
Order Option 907  
(H.P. Part No.  
5061-0090)



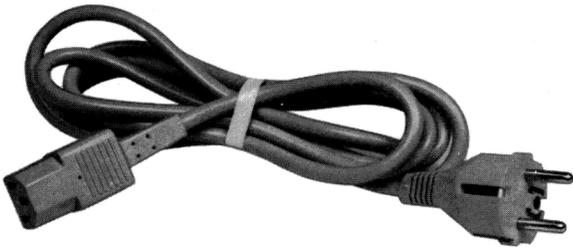
Rack flange  
Order Option 908  
(H.P. Part No.  
5061-0078)



Rack flange with front handle  
Order Option 909  
(H.P. Part No.  
5061-0084)

Figure 1-2. Available Connector and Rack Mount Accessories.

General Information



POWER CORD



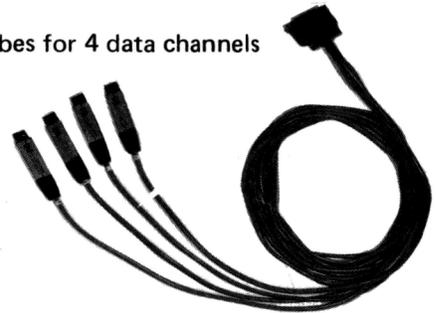
FUSE

- Accessories 1x 15406 A  
 2x 15407A  
 2x 15408A  
 1x 15412A

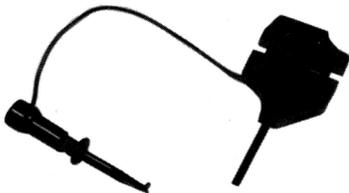
15406A  
 Clock Probe



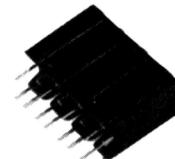
15407A  
 Cable-set with probes for 4 data channels



15408A  
 5 plug-on grabbers with ground leads



15412A  
 20 solder-in receptacles for the fastest connection of the data analyzer probes or the 8180A/8181A data generator cables to a circuit board



(x5)

Figure 1-1.8182A and Supplied Accessories.

## SECTION 1

### GENERAL INFORMATION

#### 1-1 INTRODUCTION

This Operating Manual contains information required to install, operate and test the Hewlett-Packard Model 8182A. Figures 1-1 and 1-2 show the mainframe, the accessories supplied and those available. This section covers instrument identification, description, options, accessories, specifications and other basic information.

#### 1-2 SPECIFICATIONS

Instrument specifications for the 8182A are listed in Table 1-2. These specifications are the performance standards or limits against which the instrument is tested.

#### 1-3 SAFETY CONSIDERATIONS

The Model 8182A is a Safety Class 1 instrument (instrument with an exposed metal chassis that is directly connected to earth via the power supply cable).

Before operation, the instrument and manual, including the red safety page, should be reviewed for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instrument in a safe condition.

#### 1-4 INSTRUMENTS COVERED BY THE MANUAL

Attached to the rear of each instrument is a serial number plate (Figure 1-3). The first four digits of the serial number only change when there is a significant change to the instrument. The last five digits are assigned to instruments sequentially. The contents of this manual apply directly to the instrument serial number quoted on the title page (or to all instruments if stated). For instruments with higher serial numbers, refer to the Manual Change sheets at end of this manual. In addition to change information, the Manual Change sheets may contain information for correcting the errors in the manual. To keep this manual as up-to-date and accurate as possible, Hewlett-Packard recommends that you

periodically request the latest Manual Change supplement. The supplement for this manual is identified by a print date and part number, both of which appear on the title page. Complimentary copies are available from Hewlett-Packard.

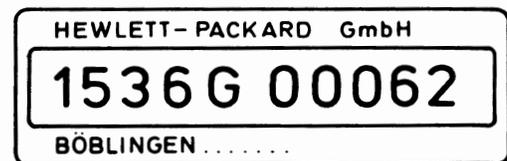


Figure 1-3 Serial Number Plate

#### 1-5 DESCRIPTION

The 8182A is a modular, high-speed data analyzer for the analysis of multichannel digital circuits. It offers programmable timing and thresholds with high resolution. By combining the 8182A with the 8180A/8181A Data Generator/ Data Generator Extender, a complete stimulus/response system for ac-parametric hardware analysis of digital IC's, boards and modules is realised. The 8182A has an operating concept based around a CRT and softkeys which is designed to simplify operation. Programming over the HP-IB\* is straightforward since every parameter can be directly accessed.

\*Hewlett-Packard Interface Bus, Hewlett-Packard's implementation of IEEE Standard 488 "Standard Digital Interface for Programmable Instrumentation".

A summary of the 8182A features is as follows:

- 1Hz->50MHz data rate (synchronous and asynchronous)
- 8->32 channels with 1kbit memory per channel

- delayable sampling point with respect to the active clock slope with 100ps resolution
- real time window compare with 100ps resolution for window width and placement
- real glitch detection and storage
- single or dual threshold measurements
- comfortable compare pattern editing
- convenient softkey operation
- full HP-IB programmability

The 8182A can contain up to 32 data channels with one or more additions of Option 001 (each addition 8 channels). Two 8182A's can be synchronized, allowing the configuration to be expanded up to 64 channels.

**1-6 OPTIONS**

The standard 8182A contains 8 data channels and 1 clock input channel. The Option 001 features 8 additional data channels. Possible configurations for the 8182A Data Analyzer are:

- 8182A standard (8 channels)
- 8182A + 1 x Option 001 (16 channels)
- 8182A + 2 x Option 001 (24 channels)
- 8182A + 3 x Option 001 (32 channels)

A list of the 8182A Options is given as follows:

**OPTION**

- 001** Additional 8 data channels—includes 2 x 15407A, 2 x 15408A and 15412A
- 907** Front Handle Kit (Part No.5061-0090)
- 908** Rack Flange Kit (Part No.5061-0078)
- 909** Rack Flange and Front Handle Combination (Part No.5061-0084)
- 910** Additional Complete Manual Set (Part No.08182-90000)
- 916** Additional Operating Manual (Part No.08182-90006; sub-set of Opt.910)

**RETROFIT OPTION**

81821A Eight data channels (includes installation at HP service office; 2 x 15407A, 2 x 15408A and 15412A)

**1-7 ACCESSORIES SUPPLIED**

The 8182A is supplied complete with the following accessories (see Figure 1-1):

ITEM	HP PART NO.
5A fuse for 230V operation	2110-0010
\	
one fitted and one supplied	
/	
10A fuse for 115 V operation	2110-0051
1A fuse for 250 V operation	2110-0007

Power Cable (see Figure 2-2)

1 x Clock Probe	15406A
2 x Cable-set,each with probes for 4 data channels	15407A
2 x set of 5 plug-on grabbers with ground leads	15408A
1 x set of 20 solder-in receptacles (see following diagram)	15412A

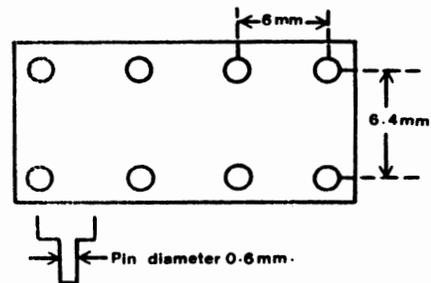


Figure 1-4 15412A Dimensions

**1-8 ACCESSORIES AVAILABLE**

a) Electrical Accessories  
In addition to the cable sets supplied with the instrument, various other connector and probe accessories are available.

These are illustrated in Figure 1-2 and are as follows:

ITEM	HP PART NO.
Set of 5 plug-on BNC adapters	15409A
Set of 5 plug-on SMC adapters	15410A
Set of 5 plug-on coax open-end adapters for fixed wiring or use of custom connector	15411A
Set of 5 plug-on miniprobes for use in conjunction with the HP10024A IC Test Clip to enable easy probing of dual in-line packages.	15415A
Cable for parallel operation of 2 8182A's	15416A

## b) Mechanical Accessories (see Figure 1-2)

ITEM	HP PART NO.
Rack Flange Kit	5061-0078
Rack Flange and Front Handle Kit	5061-0084
Front Handle Kit	5061-0090

**1-9 RECOMMENDED TEST EQUIPMENT**

Equipment required to maintain the 8182A is given in Table 1-1. Alternative equipment may be substituted, provided that it meets or exceeds the critical specifications listed in the table.

Table 1-1. Recommended Test Equipment.

INSTRUMENT TYPE	RECOMMENDED MODEL	REQUIRED CHARACTERISTICS	REQUIRED FOR
Data Generator	HP 8018A	Data Rate 50 MHz	P T
Universal Counter	HP 5335A	Time Interval; A to B; > 50 MHz	A P
Oscilloscope	HP 1725A	275 MHz Bandwidth; 1 ns/Div	A P T
Pulse Generator	HP 8007B	100 MHz/10 Hz Variable Transition times	A P T
Digital Voltmeter	HP 3456A	1mV Resolution	A P T

DC Power Supply	HP 6002A	30V Fine tuning	P
Plug-on BNC Adapter	HP 15409A		A P T
Clock Probe Assy	HP 15406A		A P T
Data Probe Assy	HP 15407A		A P T
Feedthrough Termination	HP 11048C	50 Ohm	A P T
BNC Cable Assy	HP 11170C		A P T
Cable Assy	HP 11035A	Dual Banana- BNC (m) 30 cm	A P
BNC Tee	1250-0781		A P T
Adapter	1250-2277	BNC (+) to dual banana plug	A P T
2 x Attenuator		20 dB,20W	P T
Capacitor		.22 uF	P
Delay Line		3 ns (50 Ohm)	A P T
Delay Line	34.0 ns		A T
Time Mark Generator	Time Mark	2ns	A P

## Table 1-2. Specifications

**8182A DATA ANALYZER SPECIFICATIONS**

Specifications are valid at the front-end of the active probes and for the operating temperature range from 0°C to 50°C.

**Memory Size**

The memory depth is 1024 bit per channel. The memory width is 8 channels for the 8182A standard. It can be increased up to 32 channels by adding channel expansion options.

**Inputs**

The instrument has 8 to 32 data inputs (depending on options), 1 clock input, 1 clock qualifier input, 1 trigger arm input, 1 trigger qualifier input, and 1 external stop input.

**Clock and Data Inputs**

The clock and data inputs are active probe inputs at the end of 1.5 m long cables.

**Input resistance:** 1 MOhm  $\pm$  5 %

**Input capacitance:**  $\leq$  7 pF

**Overvoltage protection:**  $\pm$  100 V continuous

**Clock Input**

The clock input threshold voltage is individually programmable. The active clock slope is selectable to be positive, negative or both.

**Max input amplitude:** 10 Vpp

(For amplitudes up to 16 Vpp refer to Section 3

**Threshold range:** -10 V to +10 V — Timing Considerations

**Threshold resolution:** 10 mV

**Threshold accuracy:**  $\pm$  2 % of programmed value  $\pm$  10 mV

**Hysteresis symmetrical to threshold:** 100 mV max.

**Threshold overdrive:**  $\geq$  10 % of amplitude or  $\geq$  100 mV, whatever is greater

**Min clock pulse width at threshold:** 5 ns

**Min clock slew rate:** 10 V/ $\mu$ s

**Data Inputs**

6 single and 6 dual threshold voltages can be programmed. Any threshold can be assigned to any data input.

**Max input amplitude:** 10 Vpp

(For amplitudes up to 16 Vpp refer to Section 3

**Threshold range:** -10 V to +10 V — Timing Considerations

**Threshold resolution:** 10 mV

**Single threshold accuracy:**  $\pm$  2 % of progr. value  $\pm$  10 mV

**Dual threshold**

**Lower threshold accuracy:**  $\pm$  2 % of progr. value  $\pm$  10 mV

**Upper threshold accuracy:**  $\pm$  1 % of progr. upper threshold  
 $\pm$  1 % of progr. lower threshold  
 $\pm$  1 % of progr. upper minus lower threshold  $\pm$  10 mV

**Min difference between upper and lower threshold:** 100 mV

**Max input signal deviation from any threshold:** 10 V

**Threshold overdrive:**  $\geq$  10 % of amplitude or  $\geq$  50 mV, whatever is greater

**Level detection accuracy 50 ms after input signal transition:** actual threshold  $\pm$  15 mV

**Timing of Clock and Data Inputs**

Timing specifications apply for equal amplitudes of clock and data inputs,  $\geq$  0.5 Vpp, with threshold progr. to the middle between high and low level of input signal.

For different conditions see Section 3 — Timing Considerations

**Logic analyzer mode, external clock operation (synchronous)**

**Max clock frequency:** 50 MHz

**Progr. clock delay range:** 0.0 ns to 1.0 s

**Clock delay resolution:** 3 digits, best case 100 ps

**Sampling point accuracy:**  $\pm$  5 % of progr. clock delay  $\pm$  1 ns  
 (Clock input to data channels, including channel skew; this specification replaces setup and hold time specifications)

**Sampling point repeatability:** Factor 4 better than accuracy

**Max clock delay:** 95 % of period -1 ns

**Min detectable pulse and glitch width at threshold:** 5 ns

**Channel skew:**  $\leq$  2 ns

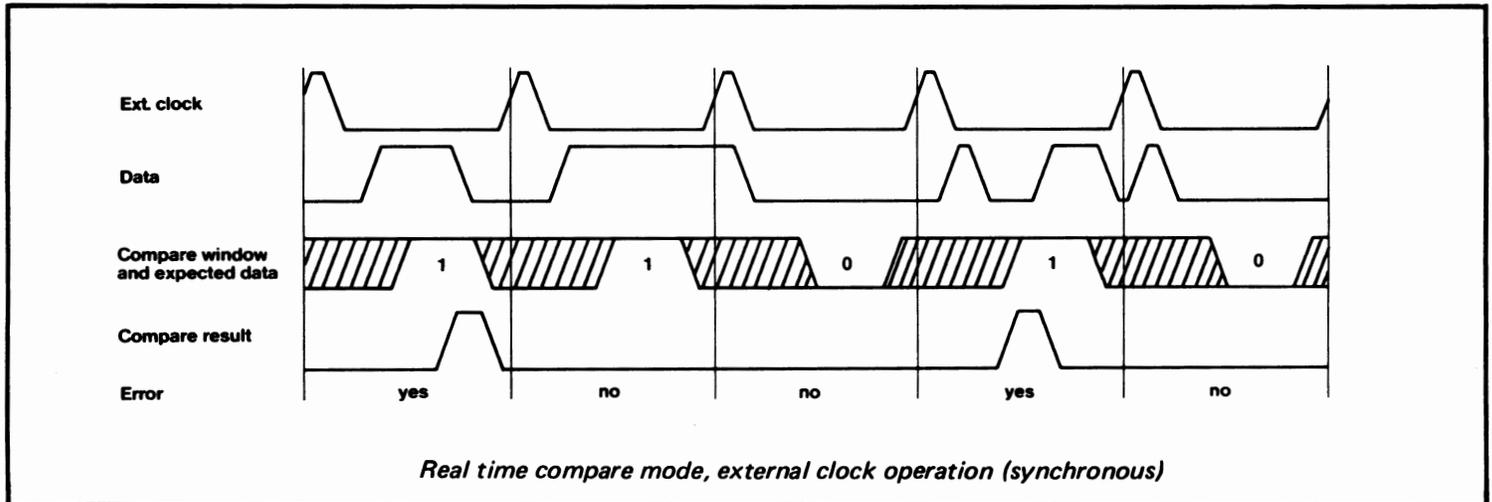
*Logic analyzer mode, internal clock operation (asynchronous)*

- Progr. clock period range:** 20 ns to 1.0 s (1 Hz to 50 MHz)
- Clock period steps:** 1 – 2 – 5 sequence
- Clock period accuracy:** 0.01 % of progr. period
- Min detectable pulse and glitch width at threshold:** 5 ns
- Channel skew:**  $\leq 2$  ns

*Real time compare mode, external clock operation (synchronous)*

- Max clock frequency:** 50 MHz
- Progr. compare window delay range:** 0.0 ns to 1.0 s
- Compare window delay resolution:** 3 digits, best case 100 ps
- Max compare window delay:** 95 % of period – 1 ns
- Compare window delay accuracy:**  $\pm 5$  % of progr. value  $\pm 2$  ns
- Compare window delay repeatability:** Factor 4 better than accuracy

- Progr. compare window width range:** 10.0 ns to 1.0 s
- Compare window width resolution:** 3 digits, best case 100 ps
- Max compare window width:** 95 % of period – 9 ns
- Compare window width accuracy:**  $\pm 5$  % of progr. value  $\pm 1$  ns
- Compare window width repeatability:** Factor 4 better than accuracy
- Min detectable pulse width at threshold:** 5 ns
- Channel skew:**  $\leq 2$  ns



**Control Inputs**

(Clock Qualifier, Trigger Arm, Trigger Qualifier, and External Stop Input)

For each input an individual threshold can be set up. The trigger arm and the external stop input are edge triggered. The active slope is selectable to be positive or negative. The clock qualifier and the trigger qualifier are level triggered. The active level is selectable to be high, low or don't care. All these inputs are BNC inputs on the rear panel of the instrument.

**Input impedance:** selectable 50 Ohm or 100 kOhm independently for each input

**Threshold range:** –10 V to +10 V

**Threshold resolution:** 10 mV

**Threshold accuracy:**  $\pm 3$  % of progr. value  $\pm 50$  mV

**Threshold overdrive:**  $\geq 100$  mV

**Max input voltage:**  $\pm 10$  V into 50 Ohm,  $\pm 20$  V into 100 kOhm

**Min amplitude:** 250 mVpp

**Min pulse width at threshold:** 8 ns

**Setup time:** 5 ns

**Hold time:** 0 ns

(Setup and hold time specified for typical application conditions, i.e. test generator connected via 1.2 m (48 in) BNC cable (HP 10503A or 11170C) to control input connectors. Specified times are relative to signal at input to clock probe).

## Outputs

The instrument has a real time error output, a latched error output, a trigger word match output, an active state indicator output, and a clock output.

In the real time compare mode, the real time error output delivers a pulse every time the comparison fails. The latched error output is set with the first compare failure and cleared when a new compare cycle starts. In the synchronous logic analyzer mode, the external clock is fed thru to the clock output. The time from clock input to clock output is determined by the programmed sampling point delay plus a fixed propagation delay.

In the real time compare mode, the clock output pulse width is equivalent to the programmed compare window width. In the asynchronous logic analyzer mode, the internal clock is delivered to the clock output.

**Levels apply when driving into 50 Ohm load**  
(voltages double, if no load connected)

**High level:** typically 2.5 V

**Low level:** typically 0 V

**Transition times:**  $\leq 4$  ns

**Propagation delay for pulsed and latched error output signal with respect to data probe input:** typically 60 ns

## HP-IB CAPABILITY

All data, parameters and modes are programmable via HP-IB. Interface functions implemented are:

SH1, AH1, L4, SR1, RL1, T6, PP0, DC1, C0, E2

By means of a specific command, the display of the 8182A may be used as a format free, general purpose alphanumeric display.

Times are measured by programming with the HP 9826A computer and remote message page of 8182A active.

## PARALLEL OPERATION

Synchronous parallel operation of two 8182A Data Analyzers is possible with the 15416A cable.

The trigger word detection is extended across both instruments, to a maximum of 64 channels.

Asynchronous analysis is not possible in parallel option.

For further limitations, please refer to Section 3  
– Parallel Operation

## Programming Times

(time for 8182A to receive, verify and execute message, typical)

**Int. clock period:** 7 ms

**Delay, Width:** 24 ms

**Threshold:** 70 ms

**Run:** 6 ms

(except first Run command in Real Time Compare Mode: 550 ms).

## Transfer Times

(time for 8182A to receive message, typical)

**Character transfer time for  $\leq 255$  characters:**  $\leq 75 \mu\text{s}$ /character

**Number of characters per command:** 4 – 6 for modes, 6 – 11 for thresholds and timing

## Expected Data Memory Load Time

(time for 8182A to receive, verify and execute message, typical)

a. formatted (HEX), 8 channels x 1024 bit: 21 s  
formatted (HEX), 32 channels x 1024 bit: 37 s

b. unformatted, 8 channels x 1024 bit: 90 ms  
unformatted, 32 channels x 1024 bit: 320 ms

## Captured Data Transmitting Time

(time for 8182A to send data, typical)

a. formatted (HEX) 8 channels x 1024 bit: 9 s  
formatted (HEX) 32 channels x 1024 bit: 18 s

b. unformatted, 8 channels x 1024 bit: 90 ms  
unformatted, 32 channels x 1024 bit: 320 ms

## Data, Parameters and Modes Storage Capability (non-volatile)

1 active operating data/parameter/mode set

3 programmable parameter/mode sets

1 standard parameter/mode set

After eight hours of continuous operation, batteries maintain all stored data, parameters and modes up to 3 weeks with instrument switched off.

**GENERAL**

**Recalibration period:** 1 year

**Warm-up time:** 30 min.

**Environmental:**

**Storage temperature:**  $-40^{\circ}\text{C}$  to  $75^{\circ}\text{C}$

**Operating temperature:**  $0^{\circ}\text{C}$  to  $50^{\circ}\text{C}$

**Max operating humidity at  $40^{\circ}\text{C}$ :** 95 % R.H.

**Video output:** Composite video signal, negative SYNC

1.0 Vpp into 75 Ohm

(Recommended monitor HP 82913A)

**Power:** 115/230 V rms +10 %, -22 %;

48-66 Hz; 900 VA max, 510 W max

**Weight:** Net 20.0 kg (44 lbs)

Shipping 27.0 kg (60 lbs)

**Dimensions:** 178 mm high, 426 mm wide, 500 mm deep

(7 x 16.8 x 19.7 in)

## SECTION 2

### INSTALLATION

#### WARNING

The instrument weighs 20.0 kg (44 lb). Care must be exercised when lifting to avoid personal injury.

#### 2-1 INTRODUCTION

This section provides installation instructions for the 8182A and its accessories. It also includes information about initial inspection and damage claims, preparation for use, packaging, storage and shipment.

#### 2-2 INITIAL INSPECTION

Inspect the shipping container for damage. If the container or cushioning is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been verified both mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1 plus any accessories that were ordered with the instrument.

Procedures for checking the electrical operation are given in Section 4. If the contents are incomplete, mechanical damage or defect is apparent, or if an instrument does not pass the operator's checks, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for settlement.

#### 2-3 PREPARATION FOR USE

#### WARNING

*To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers, panels, etc.).*

#### 2-4 Power Requirements

The instrument requires a power source of 115/230 V rms (+10%, -22%) at a frequency of 48-66 Hz single phase. The maximum power

consumption is 510 W (900 VA).

#### 2-5 Line Voltage Selection

#### CAUTION

*BEFORE SWITCHING ON THE INSTRUMENT, make sure that the instrument is set to the local line voltage.*

Figure 2-1 provides information for line voltage and fuse selection.

VOLTAGE	230 V	115 V
---------	-------	-------

FUSE	5 A	10 A
------	-----	------



Figure 2-1 Switch settings for line voltages

#### 2-6 Power Cable

In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate a.c. power receptacle, this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure 2-2 for the part number of the power cable available.

#### WARNING

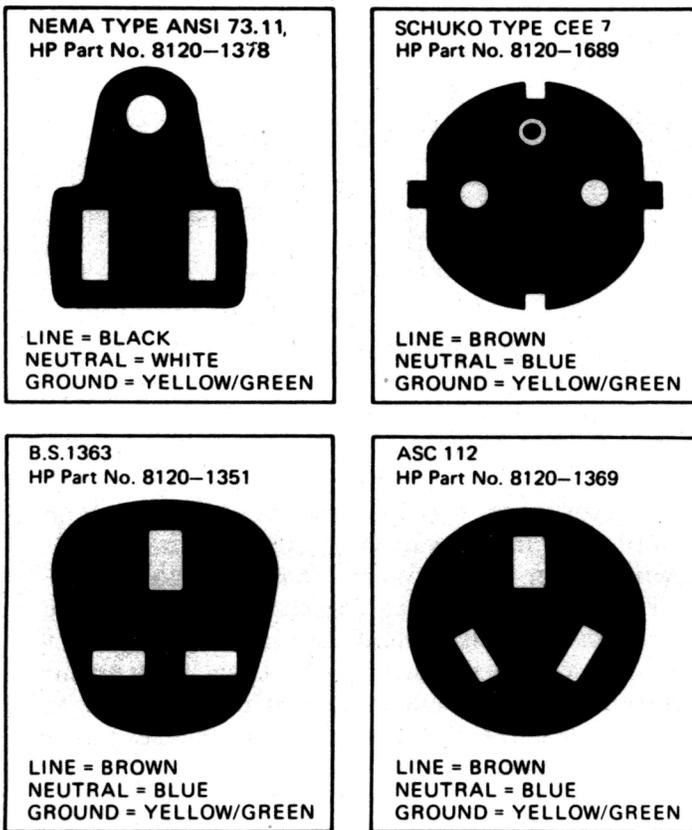
*To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on.*

- a. *If this instrument is to be energized via an auto-transformer for voltage reduction, make sure that the common terminal is connected to the grounded pole of the power source.*

b. The power cable shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

c. Before switching on the instrument, the protective ground terminal of the instrument must be connected to a protective conductor of the power cable. This is verified by checking that the resistance between the instrument chassis and the front panel and the ground pin of the power cable is zero ohms.

Figure 2-2 Available power cables - plug identification



The following work should be carried out by qualified electrician - all local electrical codes being strictly observed. If the plug on the cable does not fit the power outlet, or the cable is to be attached to a terminal block, cut the cable at the plug end and re-wire it. The colour coding used in the cable will depend on the cable supplied (see Figure 2-2). If a new plug is to be connected, it should meet local safety requirements and

include the following features:

Adequate load-carrying capacity (see table of specifications in Section 1).

Ground connection.

Cable clamp.

**2-7 HP-IB Connector**

The rear panel HP-IB connector (Fig 2-3), is compatible with the connector on Cable Assemblies 10833A, B, C and D. If a cable is to be locally manufactured, use connector male, HP part number 1251-0293.

**2-8 HP-IB Logic Levels**

The 8182A HP-IB lines use standard TTL logic, the levels being as follows:

True = Low = digital ground or 0 V to 0.4 V dc.

False = High = open or 2.5 V dc to 5 V dc.

All HP-IB lines have LOW assertion states. High states are held at 3.0 V d.c. by pull-ups within the instrument. When a line functions as an input, approximately 3.2 mA of current is required to pull it low through a closure to digital ground. When a line functions as an output, it will sink up to 48 mA in the low state and approximately 0.6 mA in the high state.

**CAUTION**

**ISOLATION:** The HP-IB line screens are not isolated from ground.

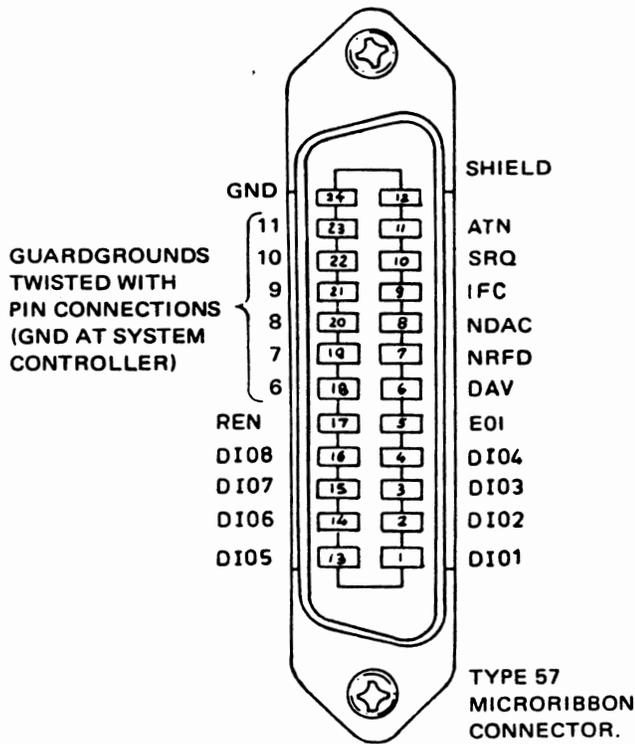


Figure 2-3 HP-IB Connector

### 2-9 Operating Environment

The operating temperature limits are 0 degrees C to 55 degrees C. The specifications also apply over this range.

### 2-10 FRONT HANDLE/RACK MOUNTING

Figure 1-2 illustrates the possible handle/rack mounting configurations. If handles are fitted and subsequently need to be removed, the plastic trim must first be taken off as shown in Figure 2-4.

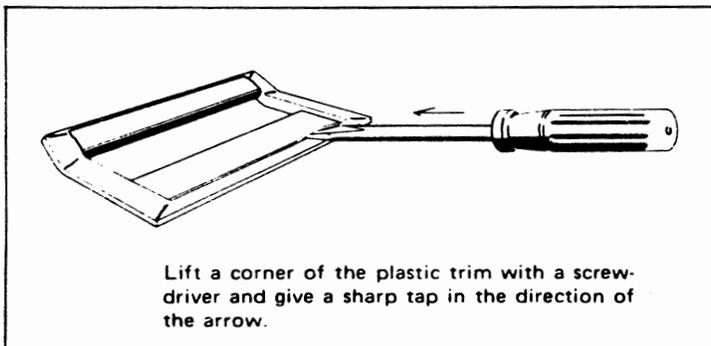


Figure 2-4 Removing Plastic Trim

### 2-11 CLAIMS AND REPACKAGING

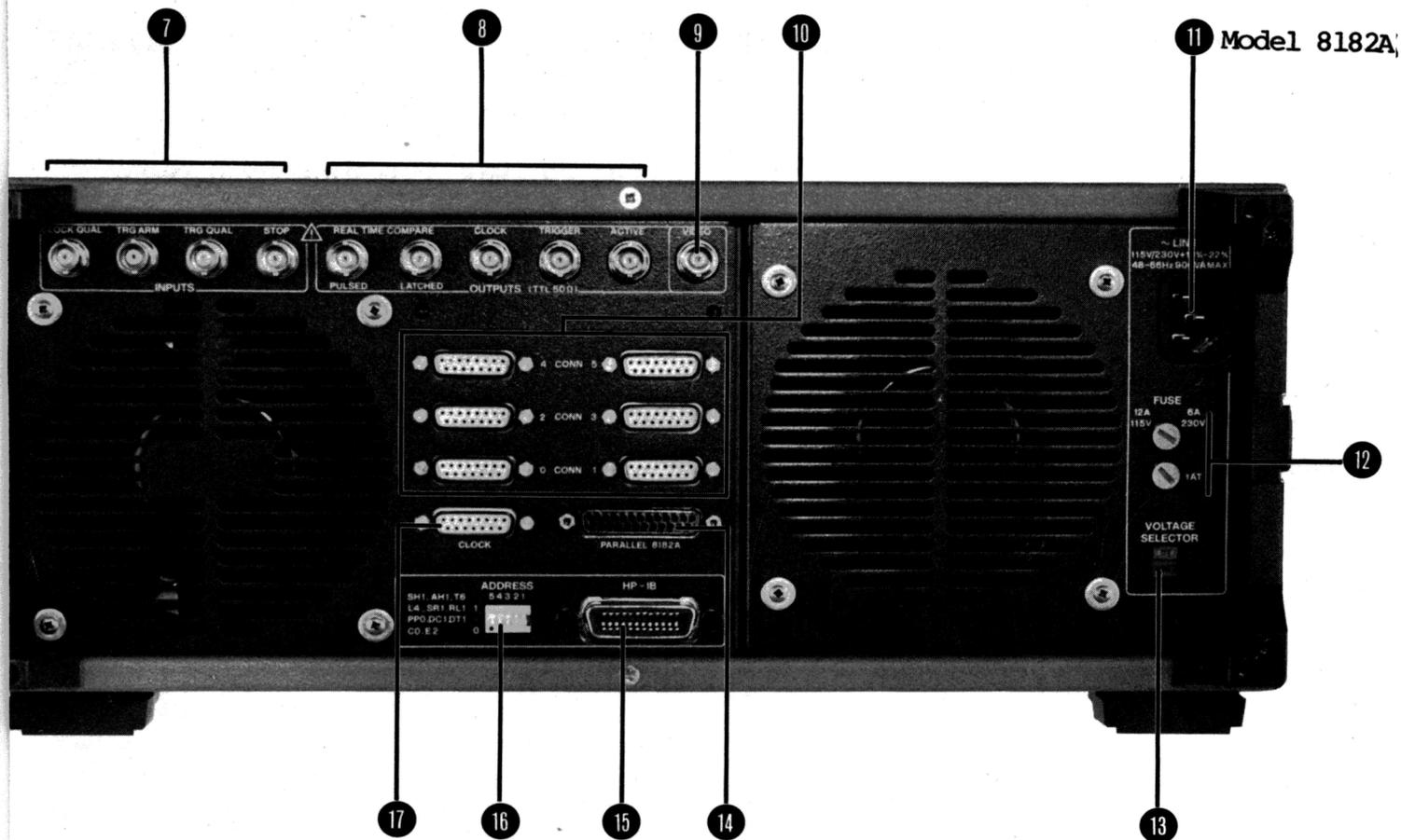
If physical damage is evident or if the instrument does not meet specification when received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

### 2-12 Storage and Shipment

The instrument can be stored or shipped at temperatures between minus 40 degrees C and plus 75 degrees C. The instrument should be protected from temperature extremes which may cause condensation within it.

If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required. The original shipping carton and packing material may be reusable, but the Hewlett-Packard Sales/Service Office will also provide information and recommendations on materials to be used if the original packing is no longer available or reusable. General instructions for repacking are as follows:

1. Wrap instrument in heavy paper or plastic.
2. Use strong shipping container. A double wall carton made of 350-pound test material is adequate.
3. Use enough shock-absorbing material (3 to 4 inch layer) around all sides of the instrument to provide a firm cushion and prevent movement inside container. Protect control panel with cardboard.
4. Seal shipping container securely.
5. Mark shipping container **FRAGILE** to encourage careful handling.
6. In any correspondence, refer to instrument by model number and serial number.



4 input BNC connectors for connecting external control signals. (Clock Qualifier, Trigger Arm, Trigger Qualifier and External Stop Input). Input impedance and input threshold can be set for each input using front panel softkeys.

5 BNC connectors provide various timing signals for synchronizing external devices. Signals include: a real time error output, a latched error output, a clock output, a trigger output and an active state indicator output. Output levels and impedance are fixed for all outputs.

BNC connector for providing a video output signal of the current display information.

8 connectors providing a total of 32 data input channels. CONNectors 0 and 1 are standard installations; CONNectors 2 through 7 are optional installations.

Power line voltage receptacle.

Fuses; one for current overload protection (6 Amp/12 Amp) and one for excessive line voltage protection (1 Amp).

Line voltage selector sliding switch to be set to local line voltage.

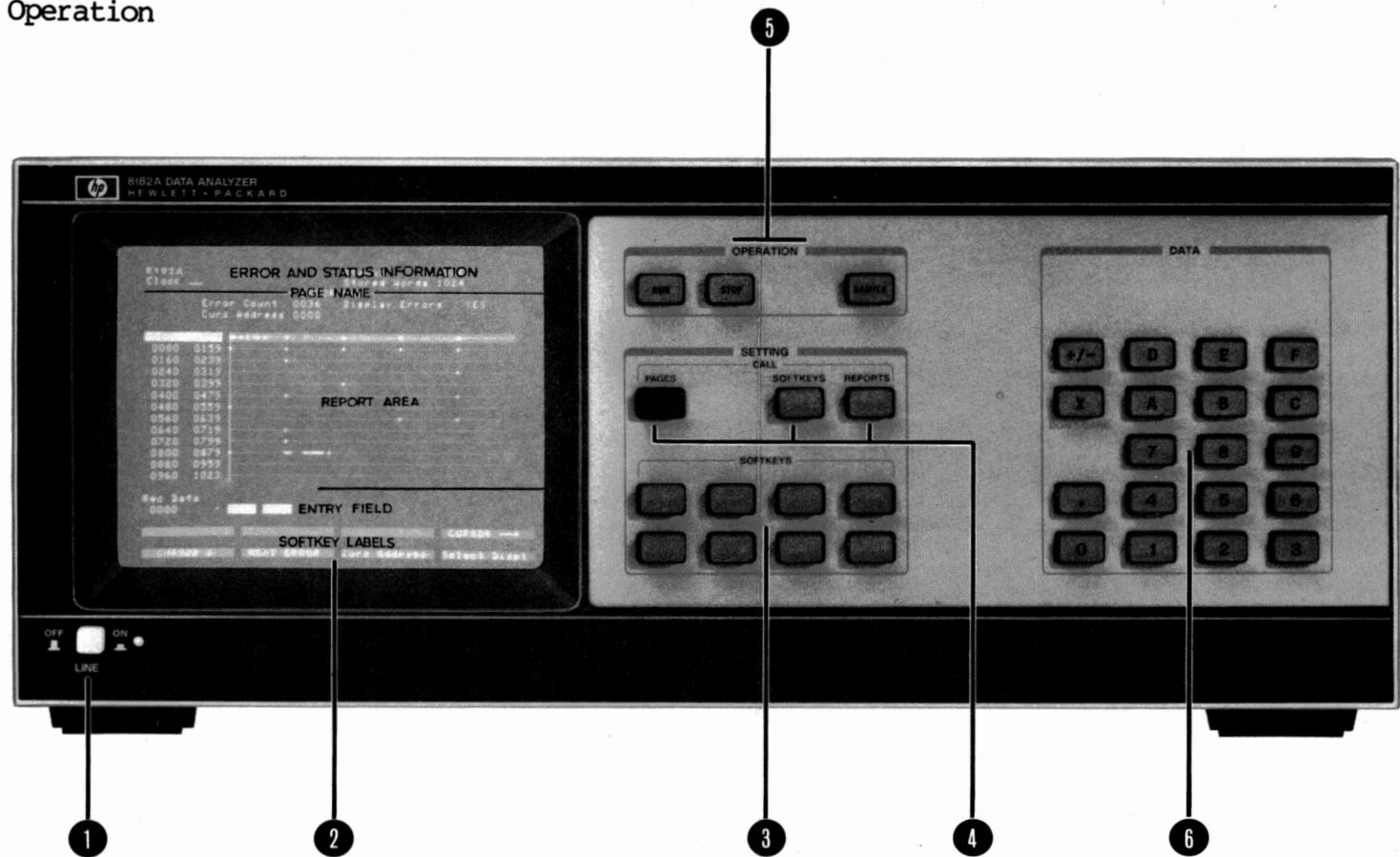
Connector for synchronous parallel operation of two HP8182A Data Analyzers.

HP-IB interface connector

Switch for setting the HP-IB address.

Connector for connecting external clock source.

## Operation



1 LINE power on/off pushbutton switch with ON indicator lamp.

2 7 inch CRT screen with two permanently defined display sectors:

Upper sector for clock indicator, clock error messages and status information.

Lower sector for PAGE display. Further details of the PAGE display are given in the PAGE CONTROL section.

An overview of a typical display format is shown above in the front panel illustration.

3 **SOFTKEYS** - eight keys with variable functions which are used to access PAGES and all instrument settings. They can also be used for new value entry depending on the type of setting. Their current function is shown by the **SOFTKEY LABELS** displayed in the bottom portion of the screen.

4 "**CALL**" keys - enable recall of PAGES menu via (**CALL**) PAGES key and mixing of PAGE REPORTS and SOFTKEYS via (**CALL**) SOFTKEYS and (**CALL**) REPORT keys.

5 Instrument **OPERATING** keys for controlling the 3 instrument operating states:

**RUN** - ARMS the instrument.

**STOP** - returns the instrument to IDLE state.

**SAMPLE** - ACTIVATES the instrument and generates a single clock pulse for sampling the current data word on the input channels.

6 **DATA** keys - these enable new parameter values and data to be entered and include: hexadecimal, octal and binary input as well as decimal entry capability. Only those keys currently appropriate for the entry type are enabled.

Figure 3-1 HP8182A Controls, Connectors and Display

## SECTION III OPERATING

### 3-1 INTRODUCTION

This section explains the functions of the controls, connectors, and display of the HP8182A and provides operating and programming information. The information is provided under the following main headings:

- a) **Operating Instructions.** This includes a general overview, basic description of PAGES, PAGE control, entering of values, modes of operation, triggering, timing considerations, "on the fly" parameter changes, memory features, error messages and parallel operation.
- b) **Programming Information.** This includes address assignment, listener and talker modes, ASCII and binary data transfers and simple programming examples for individual PAGES.
- c) **Quick Reference Section.** This includes a quick locator index for parameters and operating modes (front panel operation) and a list of HP-IB commands and mnemonics for programming the instrument.

### 3-2 SPECIAL OPERATING POINTS

#### CAUTION

The following steps must be taken before applying power to the HP8182A:

- a) *Read the red safety summary at the front of this manual.*
- b) *To avoid instrument damage, ensure that the VOLTAGE SELECTOR switch is set for the local line voltage. Before making any necessary change to the setting, switch the instrument off and disconnect the power cord.*

#### WARNING

If any change is made to setting of the VOLTAGE SELECTOR switch, the line fuse must also be changed. Before changing either of the rear-panel fuses, switch the instrument off and disconnect the power cord.

 Maximum allowable external voltage at input connectors -> see Table 1-2.

Maximum allowable external voltage at output connectors -> +5V to -1V

### 3-3 CONTROLS, CONNECTORS AND DISPLAY

Front and rear panel controls, connectors and display are identified and briefly described in Figure 3-1. This should be read prior to continuing with the following paragraphs, and referred to as necessary when reading the operating instructions.

**NOTE:** Input Cables - Probe Identification Using cable-set 15407A, four data channels can be connected to a rear panel data input connector. The four cables comprising the cable-set are numbered 0, 1, 2 and 3 respectively to identify the corresponding channel.

### 3-4 OPERATING INSTRUCTIONS

#### 3-5 Operating Concept

The HP8182A operates on a layered menu concept for instrument setup and data analysis as illustrated in Figure 3-2. The menu is itemized in 7 displays referred to as "PAGES", each page assigned to a specific area of instrument operation e.g. parameter setting, data entry data analysis etc. Every page is divided by a horizontal line into two distinct areas:

**REPORT** containing operating conditions, data, or data analysis, depending on the page.

**SOFTKEYS** comprising an entry field for entering new values, and a label set indicating current softkey functions.

The PAGES and settings are accessed via front panel "SOFTKEYS", which are a group of eight variable-function keys (non-permanently defined). Following access of the required setting, the entry of the parameter value, operating condition or data is made via either the SOFTKEYS or DATA keys depending on the type of setting.

Another important feature of the operating concept for front panel operation is the "keyboard stack". This ensures continued keyboard operation during the time required for the 8182A to process a setting and refresh the current REPORT. Up to 8 keystrokes (including all front panel keys) can be stored, and will be executed in the same sequence that they are made.

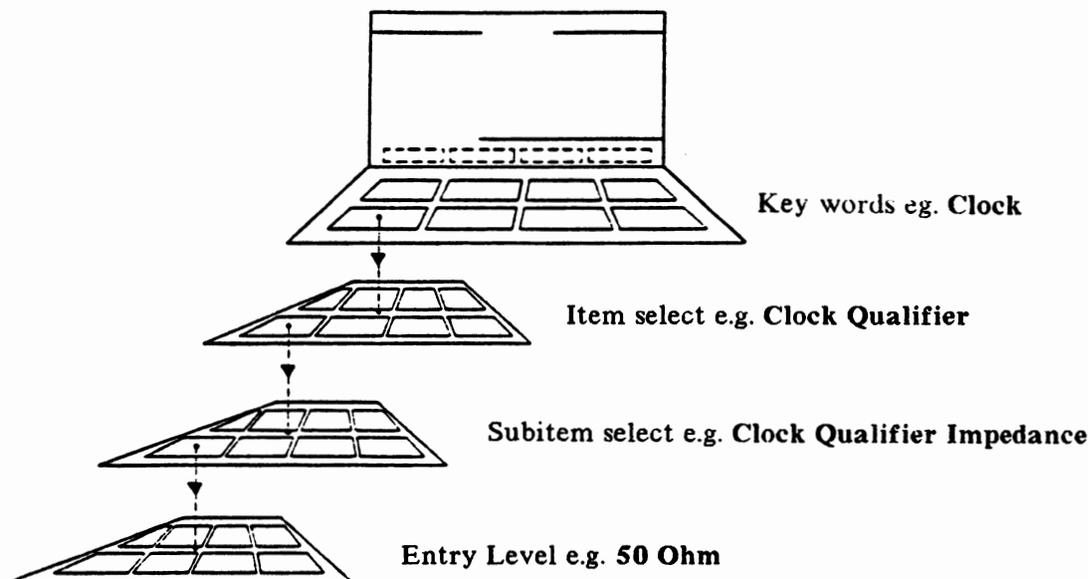


Figure 3-2 HP8182A Operating Concept.

#### 3-6 OPERATOR'S CHECKS

Press the LINE switch. Do not operate any other front panel key until a screen message appears. During this wait interval, the cooling fans start up after a few seconds and the ON indicator illuminates. The screen then indicates one of the following:

- a) SELECT PAGE prompt and the page menu indicated by softkeys.
- b) An error message and a softkey labelled CONTINUE.

Any error message is the result of the self-test routine performed at power-on. The 6 error messages in order of importance are as follows:

- 1) RAM/STACK-TEST FAILED
- 2) ROM-TEST FAILED
- 3) KEYBOARD TEST FAILED
- 4) CLOCK-TEST FAILED
- 5) ECL COUNTER-TEST FAILED
- 6) DATA BOARD TEST FAILED

If any of the above error messages appear, it is recommended that the user contact the nearest Hewlett Packard Office.

Errors 1) and 2) cause the self-test routine to be interrupted; pressing the CONTINUE softkey then enables the self-test to continue.

Error messages (3) to (6) are displayed when the self test is completed. Should the user decide to continue operating the instrument, pressing the CONTINUE softkey brings the SELECT PAGE prompt and page menu into the display.

**NOTE:** Under certain circumstances, the warning PARAMETERS DESTROYED-STANDARD SET CALLED may flash above the SELECT PAGE prompt. A detailed explanation of this warning is given later in this manual under "Memory Features".

### 3-7 PAGE CONTROL

**PAGE MENU:** At power-on, or after pressing the "PAGES" key, the page menu is indicated by softkey labels. 4 pages are allocated to instrument setting prior to data capture; 3 pages are allocated to data analysis during or after data capture. A brief description of the contents of each page is given as follows:



### 3-8 GETTING STARTED

If you are unfamiliar with the instrument, the easiest way to get started is to recall the standard settings. To do this, use the following keystroke sequence:

**MISCELLANEOUS, Recall, Standard Set, EXECUTE.**

A complete set of known values has now been activated for all mode and parameter settings. (A list of these standard settings is given on the MISCELLANEOUS page in the Quick Reference Information at the end of this Section.)

**CONTROL** - Holds general control and start/stop settings.

**INPUT** - Holds channel configuration, threshold voltages and display format.

**EXPECTED DATA** - Allows input and editing of expected data.

**STATE LIST** - Only functional in Logic Analyzer mode (described later), it displays received data, glitches and compare results in state format.

**TIMING DIAGRAM** - Only functional in Logic Analyzer mode, it displays data and glitches as time diagrams (Horizontal + Vertical zoom provided).

**ERROR MAP** - For the complete memory content, displays a summarized version of the compare result.

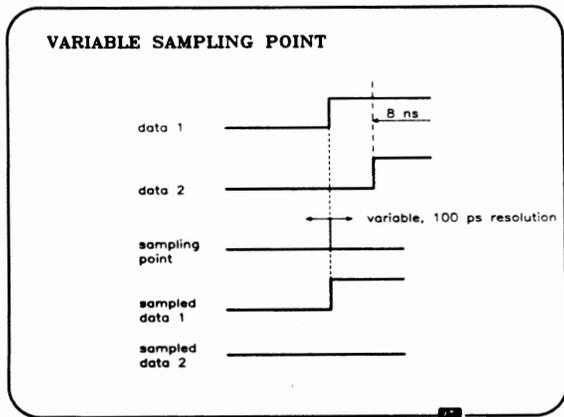
**MISCELLANEOUS** - Holds information not directly related to other pages.

Also 3 sets of complete user-defined parameter settings / operating conditions and a fixed standard set.

The next step should be to select the CONTROL page. You do this by pressing the front panel PAGES key, then pressing the CONTROL softkey.

The CONTROL page defines exactly what the analyzer will do when started. It is therefore highly recommended to thoroughly go through all the parameters when setting up the instrument. Wrong settings on this page are the main reason that the analyzer does not measure what the operator expects. A complete list of the settings on this page (and other pages), together with their meanings, is given in the Quick Reference Information at the end of this Section.

As you can see from the standard settings activated for this page, the **Clock Source** setting is **EXTERNAL**. The analyzer is therefore set for synchronous sampling. This means that the point at which the analyzer samples data is referenced to an external clock. This point can be varied via the **Clock Delay** setting as illustrated in the following diagram.



To change the standard setting for the **Clock Delay** (00.0 ns), use the following keystroke sequence:

**Clock, Clock Delay, INCREMENT**

When you have set the desired value, press **EXIT** to return to the other clock settings on this page.

It is now recommended that you either read the following paragraphs, or go to the **Quick Reference Information**. The following describes how various settings can be used to capture different segments of a continuous datastream. The **Quick Reference Information** provides a description of all analyzer settings.

### 3-9 OPERATING MODES

The HP8182A operating modes are located on the **CONTROL** page menu. Basically, there are 2 modes of operation:

a) **Logic Analyzer Mode**. Two softkeys are assigned to this mode to enable analysis of post- and pre-trigger data. The softkeys are labelled:

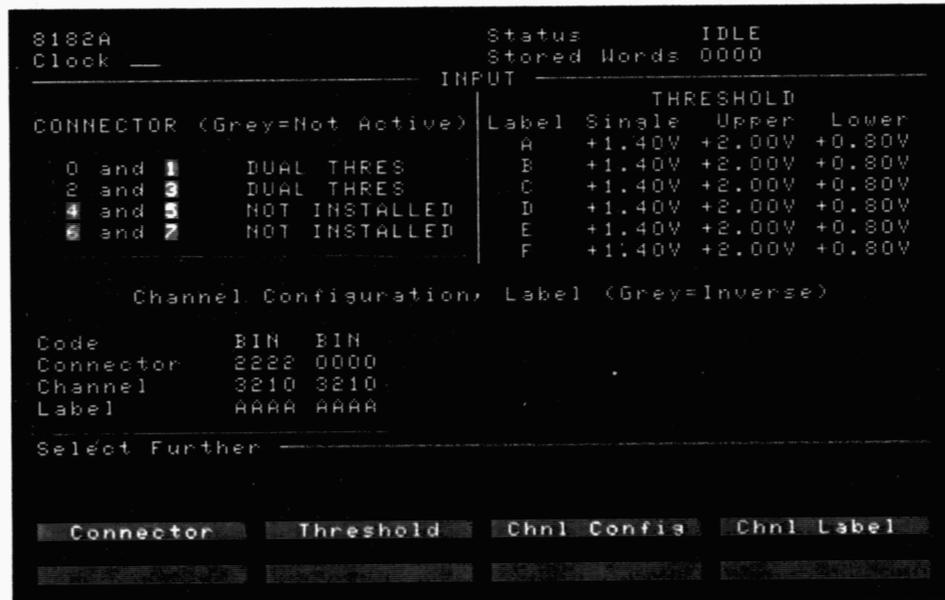
**TRG STRT ANAL** Selects Trigger Start Analysis for analyzing post-trigger data.

**TRG STP ANAL** Selects Trigger Stop Analysis for analyzing pre-trigger data. In this mode, 2 working memories are available: a high-speed memory for storing incoming data, and a low-speed memory for storing expected data. Both memories are equal in size (channel number x 1024 bits).

b) **Real Time Compare Mode**. This mode is selected via the **TRG STRT COMP** softkey. When selected, the HP8182A performs a real time comparison of the incoming data with the expected data. A comparison is executed during each clock period within the programmed time window. Words and channels failing the comparison are marked and displayed. In this mode, the expected data is stored in the high speed memory. (Incoming data is not stored).

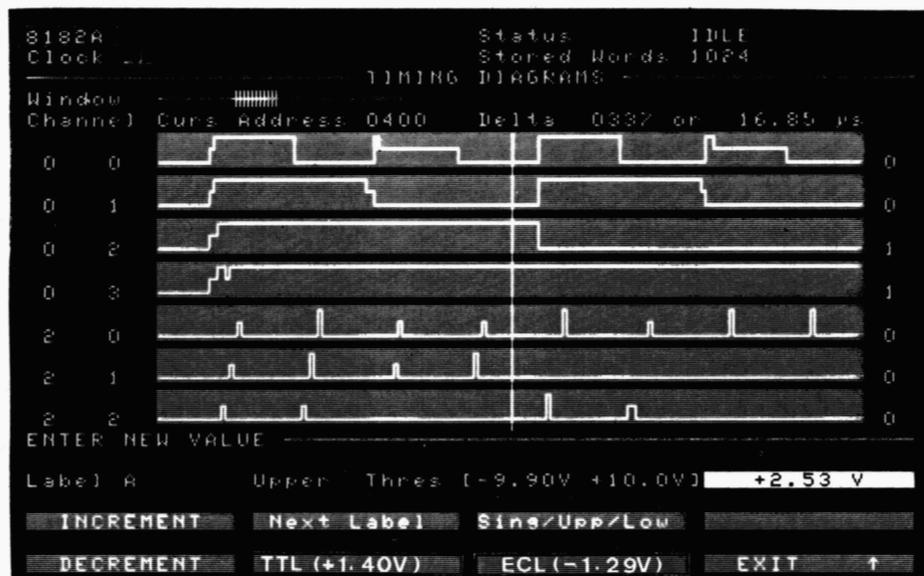
**SYNCHRONOUS/ASYNCHRONOUS OPERATION**: In both modes, the HP8182A can be operated synchronously (referenced to an external clock) or asynchronously (with internal clock). Clock selection is via **CONTROL** page softkeys.

**DUAL THRESHOLD COMPARISON**: Again in both modes, the HP8182A provides dual threshold compare capability for testing the logic levels of incoming data. As can be seen from the following video print of the **INPUT** page, dual threshold must be assigned to 8-channel groups (connectors 0 and 1; 2 and 3; etc). The active channel count is then reduced to 4 channels per group, with only even numbered connectors remaining active. Within each group, any of 6 freely programmable high/low threshold pairs (Labels) can be assigned to each channel.



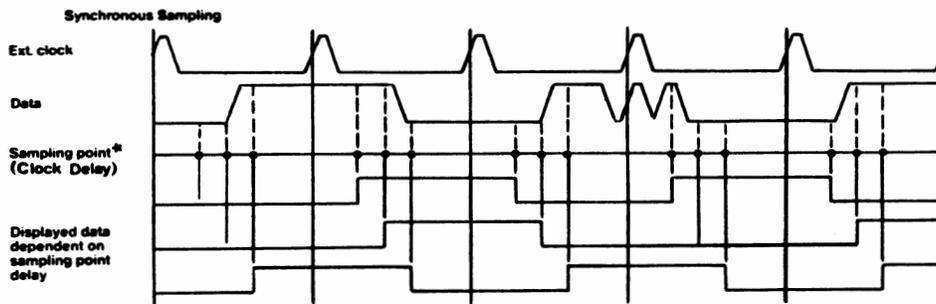
The following video print of a typical page-mix (TIMING DIAGRAMS page REPORT and INPUT page SOFTKEYS) illustrates how the "live keys" feature of the HP8182A can be used to test incoming data levels. As can be seen from

the print, the upper threshold is varied while observing the incoming data. The intermediate levels shown indicate that the signal transition has passed the lower threshold but not the upper threshold.



### 3-10 LOGIC ANALYZER MODE

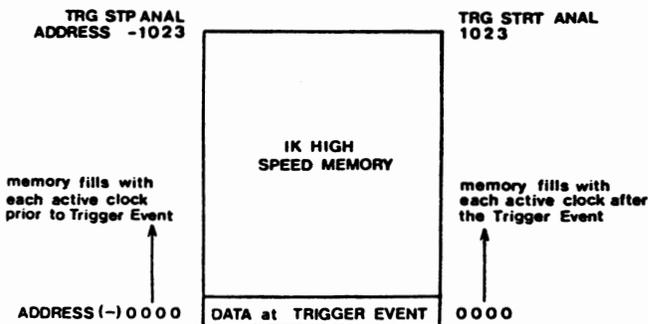
In synchronous logic analyzer mode all data input lines are simultaneously sampled at a time determined by the active slope of the clock input and the programmed "Clock Delay". Both clock slope and clock delay are set via CONTROL page softkeys, the following diagram illustrating the effect of varying the clock delay on the displayed data. In asynchronous operation, the data is sampled at a rate determined by the internal crystal clock generator. Internal clock period is set via the Clock Period softkey on the CONTROL page.



\*Sampling point delayable relative to external clock with 100 ps resolution.

The facility to analyze either post-trigger or pre-trigger data is provided by the Trigger Start Analysis TRG STRT ANAL and Trigger Stop Analysis TRG STP ANAL softkeys respectively. In either case, memory addressing is arranged to suit the data capture requirements as can be seen from the following diagram. A real addressing system is used in Trigger Start Analysis, with the data word at the trigger event being stored in

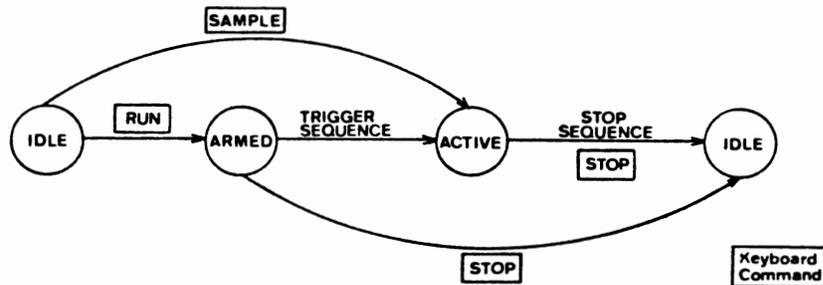
address 0000 and each successive data sample being stored in ascending address sequence (up to a maximum 1023). In Trigger Stop Analysis, a relative addressing system is used whereby the data word stored at the trigger event (the last stored word) is allocated address -0000, and each word stored prior to the trigger word allocated an address accordingly. e.g.the 10th word prior to the trigger word is located in address -0010. When selecting STATE LIST or ERROR MAP pages in either mode, therefore, the displayed address corresponds to that word's relative position to the trigger event.



**NOTE:** Editing of the EXPECTED DATA page is simplified as the displayed address range changes automatically according to the selected analysis mode. e.g.in TRG STP ANAL, the expected data word immediately prior to the trigger event is entered in address -0001.

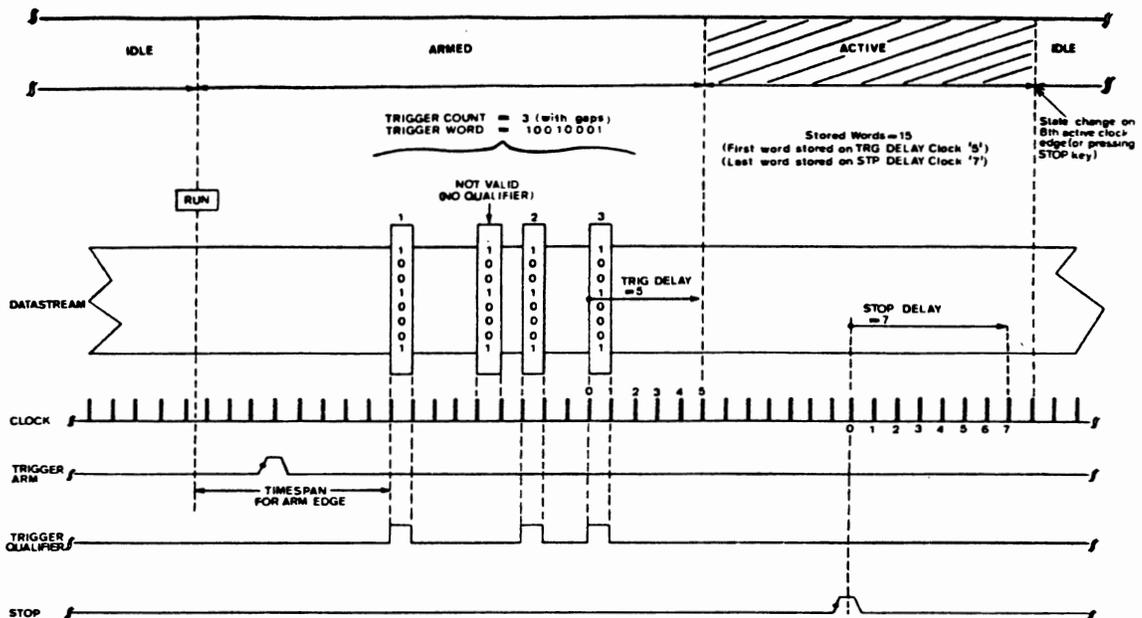
**TRIGGER START ANALYSIS:** After pressing the frontpanel RUN key, sampling is started by the trigger sequence and terminated by the stop sequence. A maximum of 1024 words (address 0000 to 1023) can be stored in the analyzer memory. The following state diagram illustrates instrument operation in Trigger Start Analysis.

**IDLE** : the instrument is waiting for the arming condition (RUN command)  
**ARMED**: the instrument is searching for trigger conditions  
**ACTIVE**: input data is sampled



As a further aid to understanding data capture when Trigger Start Analysis is selected, a simplified timing diagram (together with relevant settings) is given as follows. The diagram illustrates the accumulative effect of the various trigger and stop conditions in determining the data capture window.

In Trigger Start Analysis, because data is stored in predetermined addresses (first word in address 0000, etc.), memory readout for comparison and display (e.g. STATE LIST page) can commence for lower addresses as data is still being written into the higher addresses. This interactive readout is especially useful at low clock frequencies in laboratory applications, where stored data can be inspected for errors before the data capture cycle is completed.



Clock Source : EXTERNAL  
 Clock Slope : POS SLOPE  
 Clock Qualifier : DON'T CARE

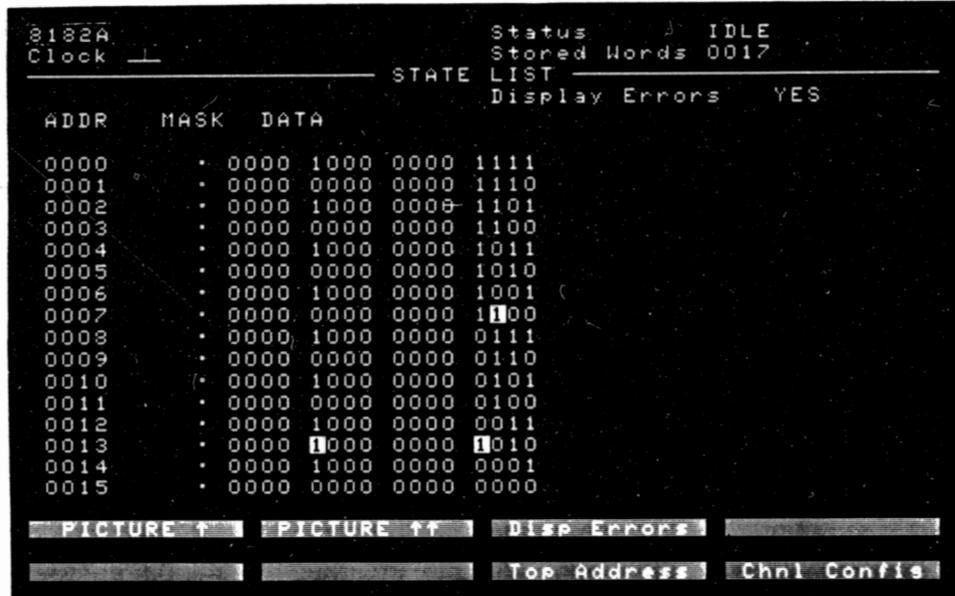
Trigger Arm (Slope) : POS SLOPE  
 Trigger Word : 10010001  
 Trigger Qual (Level) : HIGH LEVEL  
 Trigger Count : 03  
 Trigger Delay : 00005

Stop Slope : POS SLOPE  
 Stop Delay : 0007



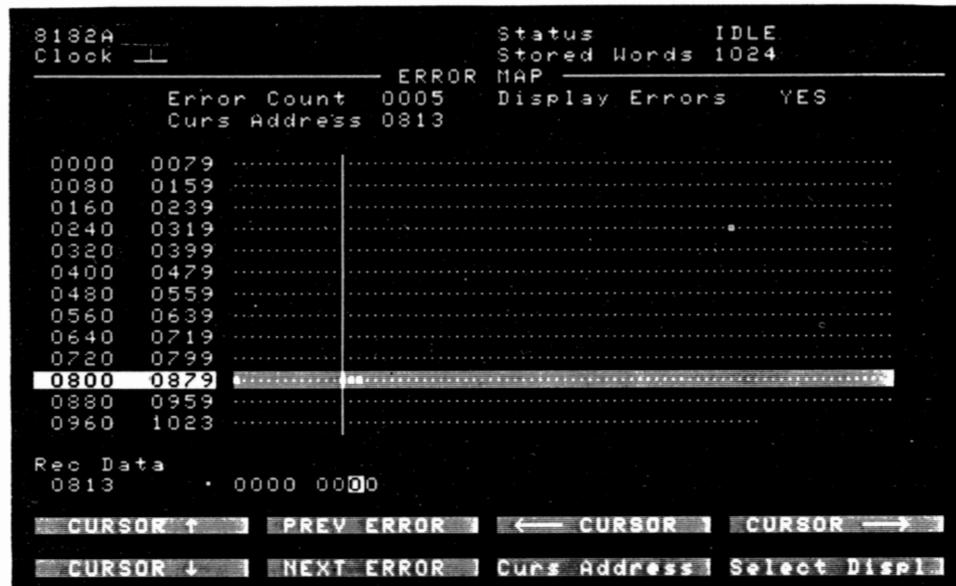
### 3-11 Error Display

In Logic Analyzer Mode, captured data can be compared with previously stored expected data for the purpose of displaying any detected errors. This feature is selected via the **Disp Errors** softkey on the **STATE LIST** page and is illustrated by the following video print of the **STATE LIST** page.



As can be seen from the print, errors are displayed in inverse video. The expected data memory is the same size as the high speed memory used for data capture (channel number x 1024 bits). When editing the **EXPECTED DATA** page, bits, channels or words not required for comparison can be masked. Whereas the

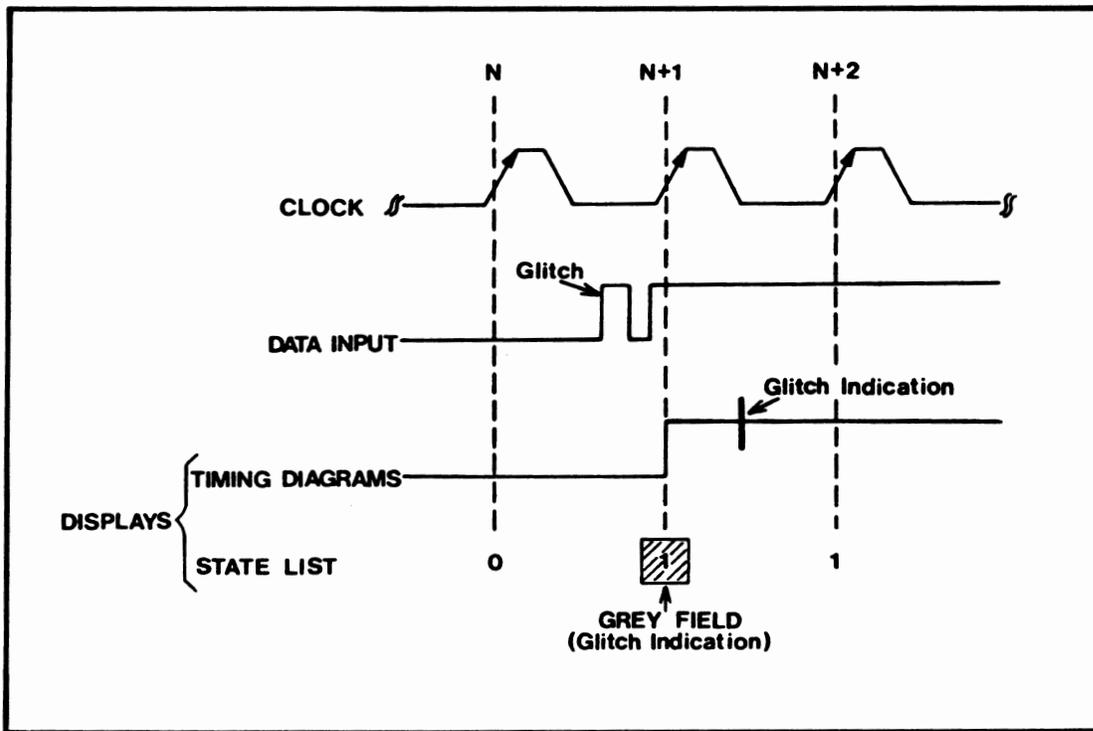
**STATE LIST** and **TIMING DIAGRAMS** pages provide partial memory displays for locating erroneous bits, the **ERROR MAP** page provides an overview of the entire memory in one display. Any error in the captured data is thus quickly located as shown in the following "ERROR MAP" video print.



### 3-12 Glitch Detection

In Logic Analyzer Mode, glitch detection capability is provided for all channels. The maximum usable memory depth is then reduced to 512 words. This feature is selected on the CONTROL page via the Glitch Detect softkey. When selected, two or more transitions between 2 sampling points (=1 clock period) are treated as a glitch. A detected glitch is indicated on each of the 3 analysis pages (TIMING DIAGRAMS, STATE LIST, ERROR MAP) as follows:

TIMING DIAGRAMS	by a short vertical line superimposed on the data signal (see following illustration).
STATE LIST	by a grey field (see following illustration).
ERROR MAP	as an error (a small square). Display of glitch related errors can be switched off.



**NOTE:** The ERROR MAP uses the same marker (a small square) to indicate errors and glitches. If both the error and glitch displays are ON, the user cannot determine if the error is a compare result or a glitch. For this reason, one of the displays should be switched off, and only errors

associated with the remaining display will be shown. This also explains why the NEXT ERROR and PREV ERROR softkeys remain active when the Disp Errors is set to OFF i.e. cursor moves from glitch to glitch.

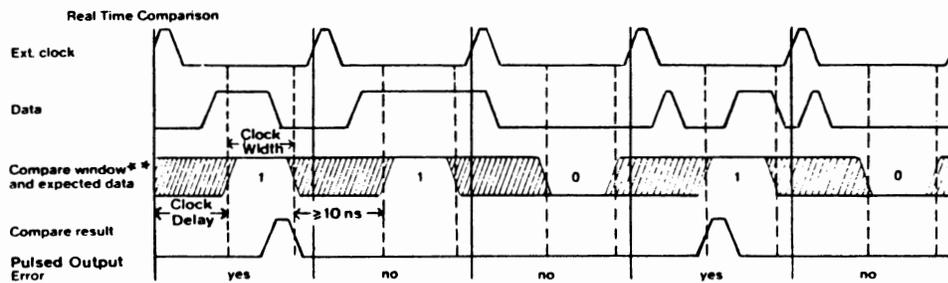
### 3-13 REAL TIME COMPARE MODE

#### 3-14 General

This mode is selected via the TRIGGER START COMPARE TRG STRT COMP softkey on the CONTROL page menu.

In synchronous Real Time Compare Mode, the active slope of the external clock signal is used to generate a "time window", within each clock

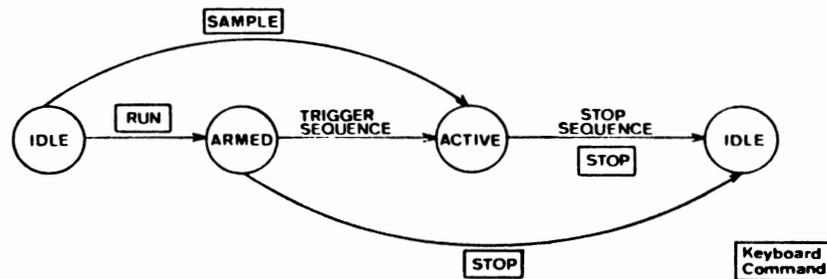
period, for comparing incoming data with an expected data pattern. The positioning and width of this time window are set via the Clock Delay and Clock Width softkeys, respectively, as shown in the following timing diagram. (Both softkeys are located on the CONTROL page menu)



\*\*Compare window delay and width programmable with 100 ps resolution.

After pressing the RUN key, comparison is started by the trigger sequence and terminated by the selected stop conditions (e.g. Stop on Error, external stop signal, pressing STOP key etc.) The

following state diagram illustrates HP8182A operation in this mode:



- IDLE** :Waiting for the arm condition (RUN command)
- ARMED** :Searching for the trigger conditions
- ACTIVE** :Comparing incoming data with expected data.

In the ARMED state, the HP8182A searches for the selected trigger word by momentary sampling of incoming data as in Logic Analyzer mode, the sampling point being determined by the active clock edge and Clock Delay setting. For valid trigger word recognition, therefore, the trigger word must be true when sampling occurs. (The Clock Width setting has no effect on data sampling in ARMED state.) In the ACTIVE state, the HP8182A compares incoming data with the expected data for the duration of the "time window", as determined by the Clock Width setting. At the end of each compare window, the next word of expected data is made available for comparison. To accomplish this, the HP8182A requires a gap between successive "time windows" of at least 10 ns.

To aid analysis of the compare results, the HP8182A provides the following:

- 1) ERROR MAP Page. For each compared word, the compare result is indicated by a dot or square. A dot indicates error-free comparison; a square indicates an error is detected. (See following video print).
- 2) ERROR MAP Page. The channel(s) in which the error(s) occurred are indicated by the "Channel Marking" field. An erroneous channel is marked by a dot in inverse video. (See following video print).

3) ERROR MAP Page. The message "Compare PASSED" or "Compare FAILED" at the top of the report area indicates the signal status of the rear panel LATCHED output.

4) Rear Panel LATCHED Output. This output signal goes high with the first error and remains high until the HP8182A is re-armed.

5) Rear Panel PULSED Output. Delivers a real time compare result. A high-going pulse indicates error within the current "time window".

**NOTE:** Outputs (4) and (5) also function in Logic Analyzer mode to indicate comparison errors. In this case, comparison takes place after the data has first been stored.

At the end of a compare cycle, any change to the word mask settings on the EXPECTED DATA page will not affect error indications 1) to 5), above, until the next compare cycle begins.



### 3-15 Memory Loading

Before selecting Real Time Compare Mode, the expected data pattern must be prepared in the EXPECTED DATA page memory. This is done by:

a) entering and editing manually via front panel DATA keys,

or

b) executing a memory dump of data recorded in Trigger Start Analysis (Logic Analyzer Mode).

Before executing a memory dump, it is recommended that data is recorded under identical triggering conditions to those required for Real Time Compare mode. It should be remembered, therefore, to set the Trigger Delay setting to a minimum of 1 (maximum 65.535) when recording data in preparation for real time comparison [In Real Time Compare mode, comparison starts a minimum 1 clock period after the Trigger Word, hence the minimum Trigger Delay setting.]

If the Trigger conditions have not been observed, the Roll Up Memory/Roll Down Memory feature of the EXPECTED DATA page line editing enables cyclic rolling of the memory content. This is illustrated in the following video print.

With the display as shown, pressing the EXECUTE softkey will roll the data content of addresses 0002 through 0012 up into addresses 0000 through 0010. (The content of addresses 0001, 0000 will be rolled into addresses 1023 and 1022 respectively.)

The following provides a general memory dump procedure prior to real time comparison:

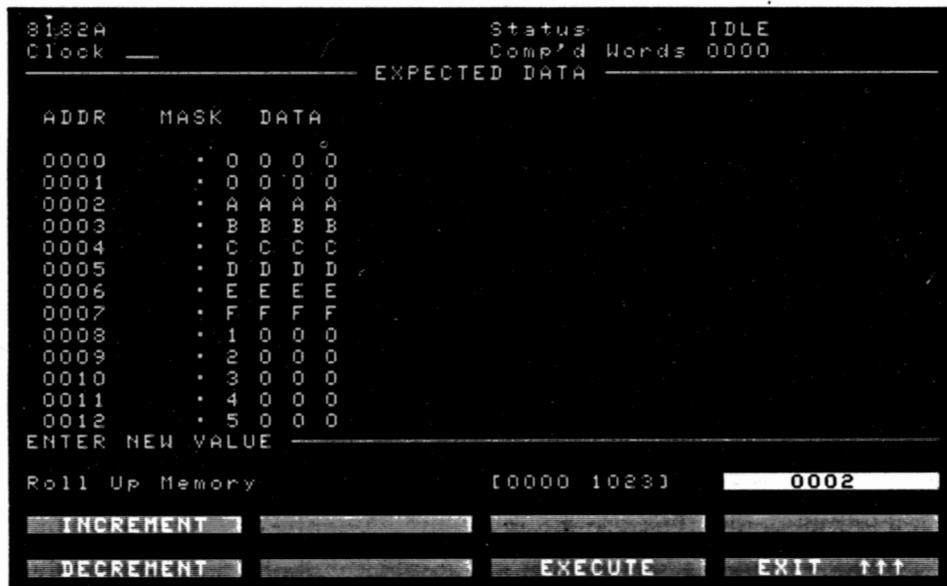
1) With synchronous Trigger Start Analysis selected, define the data capture window using the "Trigger" and "Stop" softkeys on the CONTROL page [see TRIGGER START ANALYSIS description]. Ensure the Trigger Delay setting is  $\geq 1$ .

2) Press the front panel RUN key to record data.

3) Press the front panel "PAGES" key and select the EXPECTED DATA page.

4) Dump recorded data from the high speed memory into the low speed expected data memory using the following keystroke sequence: Edit, Dump Rec Data, EXECUTE.

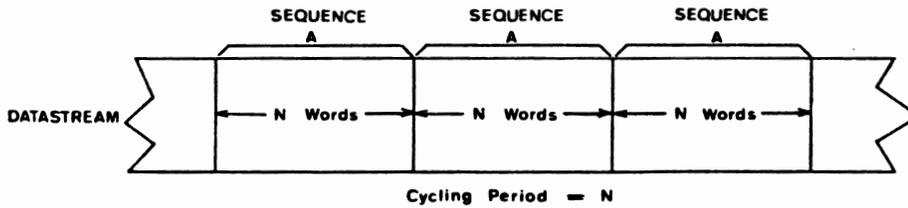
The user can now return to the CONTROL page and select Real Time Compare mode. The content of the EXPECTED DATA page memory is automatically transferred back to the high speed memory the first time the RUN key is pressed.



### 3-16 Autocycling

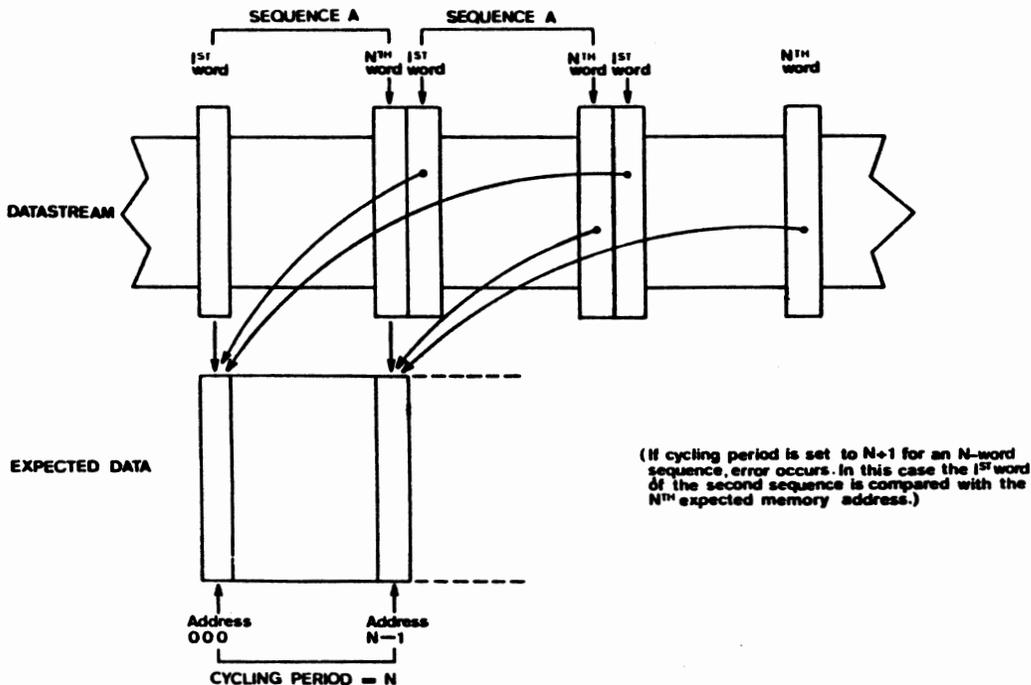
For data streams comprising long repetitive data sequences, the autocycling feature of Real Time Compare mode can be used to provide continuous monitoring of the datastream until an error occurs. Autocycling is selected via the **Cycling Per** softkey on the **CONTROL** page menu. When set to "ON", the entered value must correspond exactly to the repeated sequence length.

e.g.



For Cycling Period = N, therefore, the HP8182A compares each consecutive sequence of N words with the first N words of expected data, starting with memory address 0000.

**NOTE:** If expected data has been loaded using the "Dump Recorded Data" feature described under "Memory Loading", the content of memory address 0000 is determined by the "Trigger Delay" setting. e.g. If **Trigger Delay** = 6, memory address 0000 contains the sixth word following the Trigger Word.



During autocycle operation, the user can select either of the following error-related stop conditions:

- a) Set "Stop on Error" to ON via the Stop on Error softkey. (CONTROL page). Real time comparison then stops one clock period after an error occurrence. The ERROR MAP will display the compare result for all words up to and including the word immediately following the error word. [No display during error-free cycling]
- b) Connect the REAL TIME COMPARE LATCHED output to the STOP input, and make the following CONTROLS page settings via softkeys:

Stop on Error -> OFF  
 Stop Slope -> POS  
 Stop Delay -> e.g. 15

(Set other parameters as required)

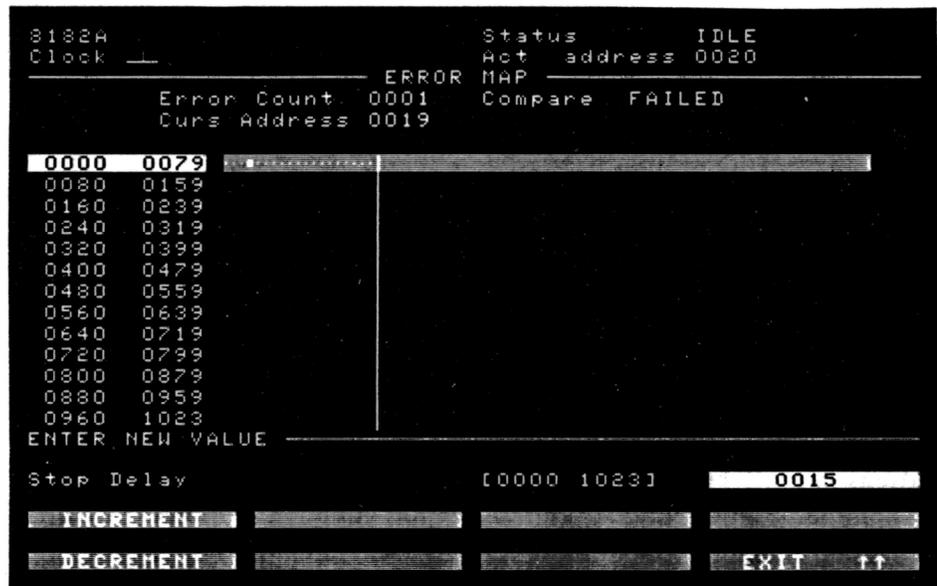
Real time comparison is then stopped after the 16th clock period (could be 17th or 18th, depending on frequency and propagation delay) following the error occurrence. The ERROR MAP will display the compare result for at least 16 words following the error word as shown in the following video print. This is a useful method for determining if the error is sporadic or if a sequence of errors has occurred. [No display during error-free cycling]

### 3-17 TRIGGERING

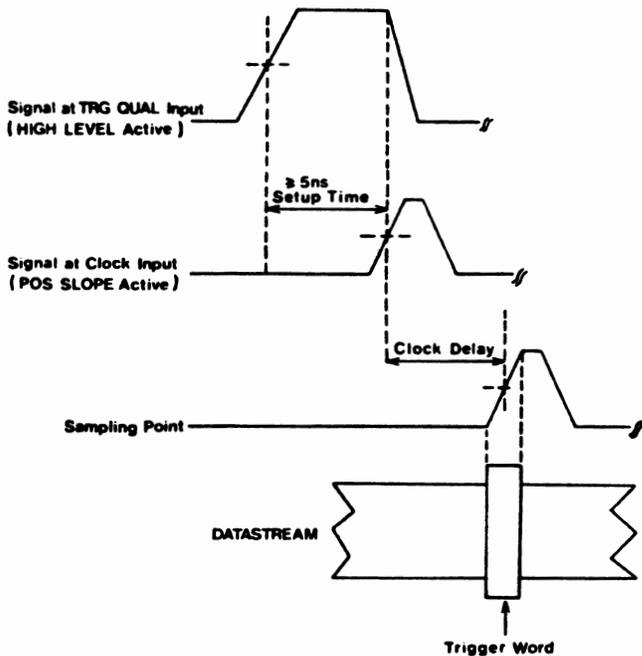
In both modes of the 8182A, data sampling is started (or stopped) by the trigger sequence. This sequence is a combination of various conditions which together define the "trigger event" i.e. the point at which the 8182A changes state - from ARMED to ACTIVE (or ACTIVE to IDLE). The various conditions are as follows:

- a) Trigger Arm - edge active
- b) Trigger Qualifier - state active
- c) Trigger Word - pattern recognition
- d) Trigger Count - trigger word count
- e) Trigger Delay - clock count

The signal applied to the rear panel TRG ARM input determines the start of the trigger sequence, the active edge of this signal being defined by Trigger Arm setting on the CONTROL page. (All trigger conditions are set on the CONTROL page) When the active edge occurs, the 8182A begins to search for qualified



trigger words, the number of words being defined by the **Trigger Count** setting. To decrement the trigger word counter, the trigger qualifier and trigger word must be true with respect to the clock input and sampling point, as illustrated in the following timing diagram.



During countdown, there are 2 count modes as determined by the "Allow Gaps" setting on the CONTROL page:

1) **Allow Gaps YES.** The counter is decremented for each qualified trigger word, even if they don't occur on consecutive clock pulses. After the pre-programmed number of qualified trigger words, the Trigger Delay counter is activated.

2) **Allow Gaps NO.** Only qualified trigger words occurring on consecutive clock pulses are counted. During countdown, any clock pulse occurring without trigger word recognition causes the counter to be reset to the start number.

An important feature of the 8182A trigger sequence is that the arm, qualifier, word and count conditions can all be true relative to the same clock edge. In this case, the 8182A goes into ACTIVE state if the **Trigger Delay** is set to 00000. For any other **Trigger Delay** setting, the trigger delay counter is activated.

### 3-18 TIMING CONSIDERATIONS

The sampling accuracy of the HP8182A is expressed by the following specifications (1) to (3) as given in Table 1-2:

#### Logic Analyzer Mode (External clock)

(1) Sampling Point Accuracy:  
+/- 5% of progr. clock delay +/- 1 ns

#### Real Time Compare Mode (External clock)

(2) Compare Window Delay Accuracy:  
+/- 5% of progr. value +/- 2 ns

(3) Compare Window Width Accuracy:  
+/- 5% of progr. value +/- 1 ns

Instruments are adjusted to fulfill these specifications by applying clock and data signals with predetermined signal characteristics. These characteristics are listed as follows:

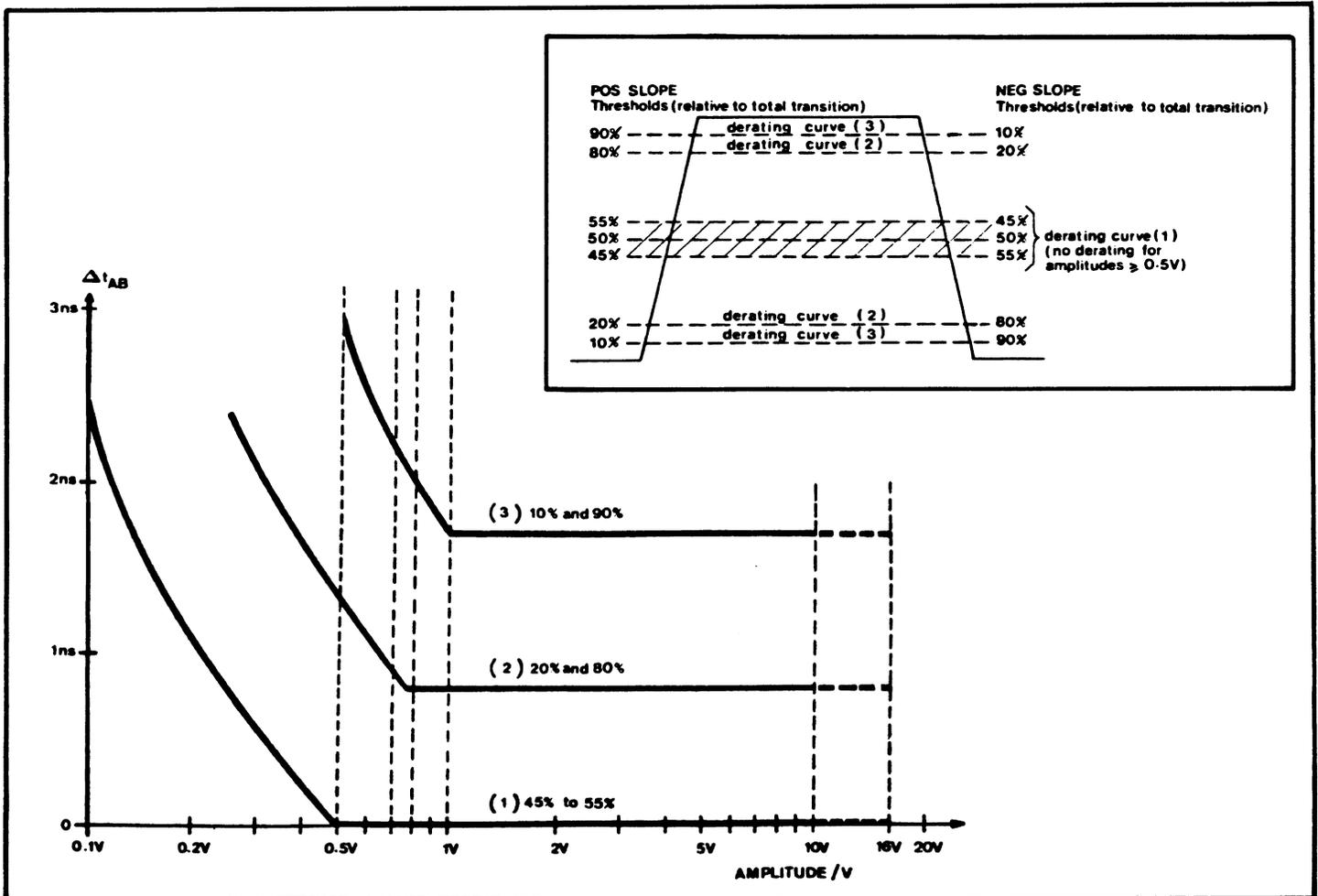
- a) Threshold level set to a point between 45% and 55% of total swing.
- b) Amplitudes  $\geq 0.5V$ .
- c) Slew rate around threshold level  $\geq 1 V/ns$ .
- d) Transition times  $\geq 2ns$  (10% to 90% points)

Because the above requirements apply to both clock and data signals, any deviation for either signal has an incremental derating effect ( dt clock or dt data ) on specifications (1) to (3). The derating factors are calculated as follows:

$$\begin{array}{rcc}
 dt \text{ clock} = +/- dt AB & +/- dt C & + dt D \\
 \uparrow & \uparrow & \uparrow \\
 \text{if (a) or (b) not true} & \text{if (c) not true} & \text{if (d) not true} \\
 \downarrow & \downarrow & \downarrow \\
 dt \text{ data} = +/- dt AB & +/- dt C & - dt D
 \end{array}$$

where:

dt AB is given an absolute value for clock and data according to the following derating curves for various thresholds and amplitudes.



dt C is calculated from the following formulae:

$\frac{2\% \text{ of progr. clock thresh.} + 35\text{mV}}{\text{clock input slew rate around thresh.}}$  for dt clock

$\frac{\text{data threshold accuracy}}{\text{data input slew rate around thresh.}}$  for dt data

# dt D is calculated from the following formula for clock and data:

$$0.4 * [2 \text{ ns} - \text{transition time}(10\%-90\%)]$$

# Note that if both clock and data signals exhibit fast transition times, e.g. 1 ns, the net derating effect from dt D is zero (+0.4 ns for dt clock; -0.4 ns for dt data).

Having determined the absolute values for dt clock and dt data, whichever is relevant, they should be applied to specifications (1) to (3) as follows:

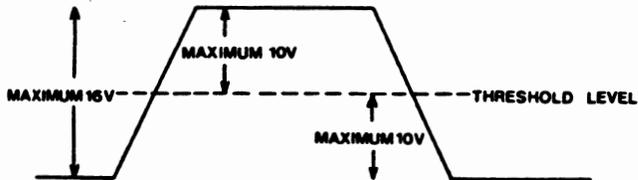
- (1) = as specified + dt clock + dt data
- (2) = as specified + dt clock + dt data
- (3) = as specified + dt data

### 3-19 Amplitudes between 10V and 16V

As indicated in Table 1-2, a maximum of 10V amplitude is specified for clock and data signals, although amplitudes from 10V to 16V may be applied with further derating of the sampling accuracy specifications. [(1) to (3) above]. For this higher amplitude range, +/- 2ns must be added

to dt clock and/or dt data (as calculated for different thresholds above) providing the following signal characteristics are fulfilled:

- a) Absolute voltage difference between any point on the input signal and the threshold level  $\leq 10V$  as shown in the following



- b) Width at threshold level  $> 20ns$   
 c) Frequency  $\leq 5MHz$   
 d) Transition times  $\geq 10ns$

For frequencies  $> 5MHz$  and  $< 15MHz$ , or transition times  $< 10ns$ , a further  $\pm 3ns$  derating factor (total  $\pm 5ns$ ) must be added to dt clock and/or dt data.

### 3-20 "ON THE FLY" PARAMETER CHANGES

Any change to a parameter setting is executed immediately, independent of the current 8182A state (IDLE, ARMED or ACTIVE). However, only certain parameter values can be changed without any interruption of the current data capture cycle i.e. "on the fly". These parameters are listed as follows:

- 1) The thresholds for each Label on the INPUT page.
- 2) The threshold of each of the auxiliary rear panel BNC inputs (all set on the CONTROL page).
- 3) The active levels (HIGH,LOW,DON'T CARE) of the Clock Qualifier and Trigger Qualifier inputs. (CONTROL page).

- 4) In Logic Analyzer mode, data and data masking on the EXPECTED DATA page. (These, together with the channel configuration and normal/inverse settings, can be changed at the end of a capture cycle. The ERROR MAP will change accordingly).

For any other parameter, a change will either interrupt the current capture cycle by disabling the clock for the duration of the change execution, or abort the capture cycle completely, depending on the parameter e.g. changing the Clock Delay or Clock Width setting disables the clock for approximately 15 ms.

### 3-21 MEMORY FEATURES

These include the capability to store and recall the following via the Store/Recall softkeys on the MISCELLANEOUS page:

- a) 1 standard mode/parameter set
- b) 3 programmable mode/parameter sets

In addition to the above, the HP8182A auto stores the following at switch-off:

- a) 1 complete data set
- b) the current mode/parameter set.

...and auto recalls them at switch on [see Battery Storage Specifications].

**NOTE:** After changing a mode/parameter setting during current operation, allow 2.5 seconds before switching the instrument off. An internal software routine compacts the current mode/parameter set into a "check signature". This routine is repeated every 2.5 seconds, the result being used for determining valid auto recall. If the instrument is switched off less than 2.5 seconds after the last change, the warning **PARAMETERS DESTROYED-STANDARD SET CALLED** will be displayed at instrument switch-on. This warning is also displayed if the instrument was switched off longer than 3 weeks.

### 3-22 ERROR MESSAGES

During instrument operation, any of three error messages can be displayed due to incorrect operator settings. The error messages and their meanings are described as follows:

**CLOCK IS TOO FAST** - the clock timing parameters are incompatible e.g. clock delay setting incompatible with clock period.

**CLOCK WAS TOO FAST** - indicates that at some point in current operation the clock parameter settings were incompatible, but the clock timing is now error-free.

**VALUE OUT OF RANGE** - the user attempted to enter a parameter value which is out of instrument specification.

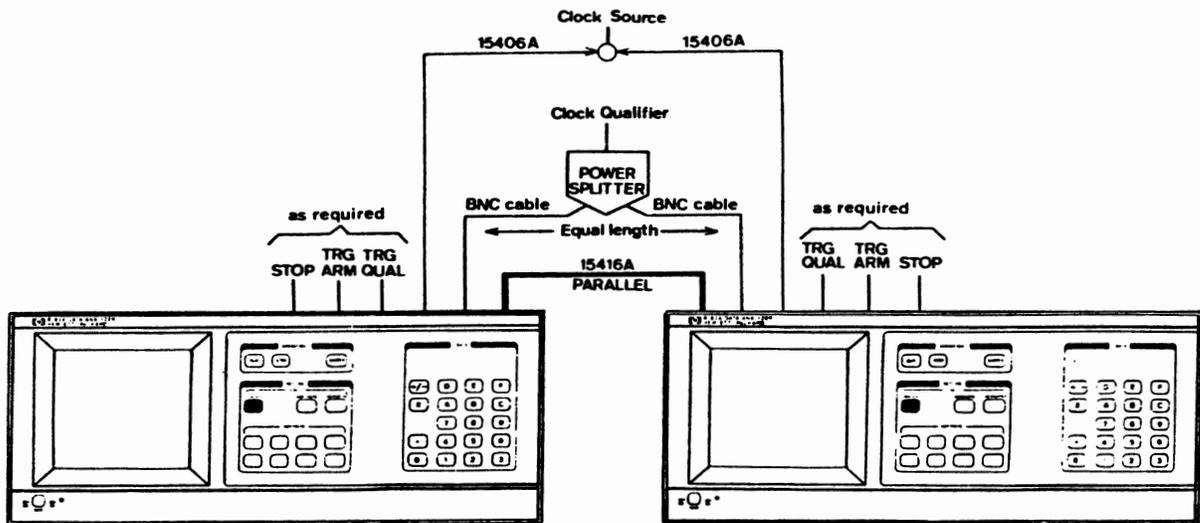
### 3-23 PARALLEL OPERATION

#### 3-24 General

Using the HP15416A cable accessory, the trigger conditions of two HP8182A's are synchronized thus increasing the number of data channels to a maximum of 64. The following provides information on setup requirements as well as functional and parametric restrictions in parallel operation. A summary of the restrictions is given at the end of this description.

#### 3-24 Setup Requirements

The following setup diagram illustrates the basic connections and settings for parallel operation. Briefly, both instruments must be set to the same operating mode, connected to a common external



#### SETTINGS

<b>Operating mode</b>	(1)	(2)
<b>Clock Source</b>	same as (2)	same as (1)
<b>Clock Slope</b>	<b>EXTERNAL</b>	<b>EXTERNAL</b>
<b>Clock Thres</b>	same as (2)	same as (1)
<b>Clock</b>		
<b>Qualifier</b>		
<b>Level</b>	same as (2)	same as (1)
<b>Threshold</b>	same as (2)	same as (1)
<b>Impedance</b>	50 Ohm	50 Ohm

clock(only synchronous data sampling possible), and have identical clock slope and threshold settings. If a clock qualifier signal is applied for selective sampling purposes, then it must be connected as shown, although this signal is not mandatory to parallel operation. (Otherwise, set the Clock Qualifier Level to `DON'T CARE` on both CONTROL pages).

Although both instruments are connected to the same clock source, the clock delay (and clock width in Real Time Compare mode) settings are independently programmable within the following range specifications:

**Maximum Clock Delay:**

95% of Period - 11ns

**Maximum Delta Delay between (1) and (2):**

95% of Period - 19ns

Note that in the event of different clock delays, the channel skew time is equal to the delay difference.

### 3-26 Data Capture

The data capture cycle is determined by the front panel OPERATION keys (RUN, SAMPLE, STOP) and the following CONTROL page settings:

- trigger conditions
- stop conditions
- autoarming

With reference to the OPERATION keys, a brief description of their role in parallel operation is given as follows:

**RUN** - pressing either RUN key arms both instruments.

**STOP** - if the autoarming function is switched off for both instruments, pressing either STOP key stops both instruments. With autoarming switched on for one instrument (only one instrument should have autoarming enabled) then only the STOP key for this instrument can abort autoarming. Pressing this key stops both instruments.

**SAMPLE** - function independently and their use is not recommended in parallel operation.

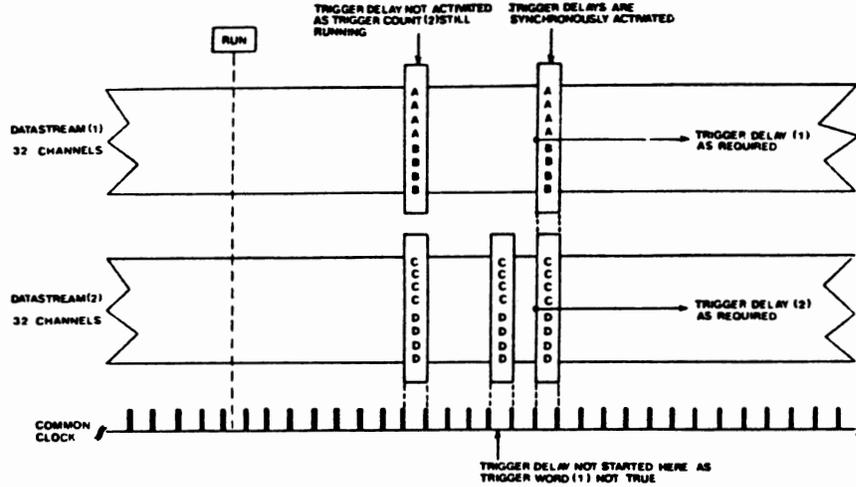
Regarding the CONTROL page settings, special operator considerations in parallel operation are dependent on the selected operating mode. For this reason, these considerations are detailed according to mode in the following.

**LOGIC ANALYZER MODE:** Whereas in single operation the trigger delay is immediately active at the end of the trigger count, in parallel operation the trigger delay counters of both instruments are synchronously started only when

both trigger count conditions are satisfied, and the combined trigger word is true. This is illustrated in the following simplified timing diagram.

For termination of the data capture cycle, all stop parameters on the CONTROL page of each instrument are independently programmable.

Also, for repetitive data capture cycles, the auto-arming feature should only be set on one instrument. Both instruments are then re-armed at the end of a capture cycle. Regarding the 'Abort on Compare Error' feature of autoarming, neither instrument is re-armed if the error occurs in the instrument set to autoarming.

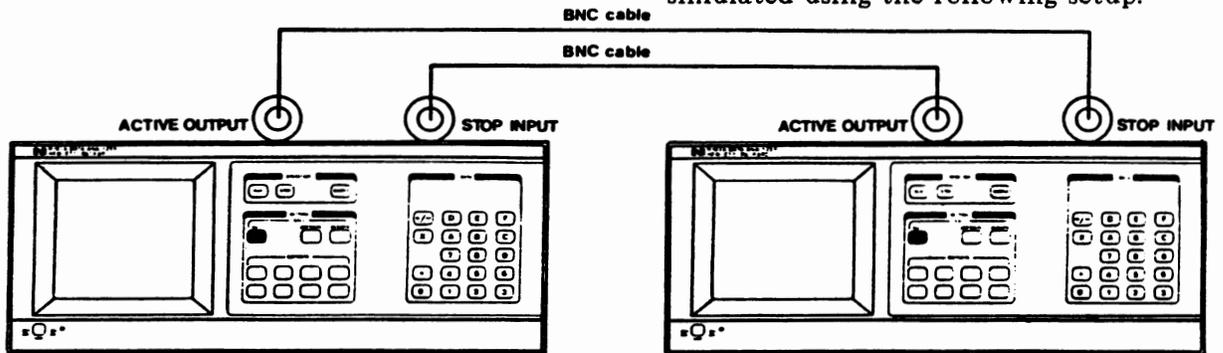


SETTINGS

	(1)	(2)
Trigger Arm Slope	DON'T CARE	DON'T CARE
Trigger Word	AAAABBBB(hex)	CCCCDDDD(hex)
Trigger Qualifier	DON'T CARE	DON'T CARE
Trigger count	01	02
Allow Gaps	YES	YES
Trigger Delay	as required	as required

**REAL TIME COMPARE MODE:**The trigger sequence in this mode functions as already described for Logic Analyzer mode, with the additional consideration that the Trigger Delay

of both instruments must be set to a minimum of 2. The 'Stop on Error' feature of this mode functions independently for both instruments, although a combined 'Stop on Error' can be simulated using the following setup.



SETTINGS

	(1)	(2)
Stop Slope	NEG SLOPE	NEG SLOPE
Stop Thres	TTL	TTL
Stop Imp	50 Ohm	50 Ohm

If the above setup is used, there may be a stop difference of a few words depending on the clock period and internal propagation delays. During data comparison, both ERROR MAPS must be inspected to ensure error-free compare results (i.e. no combined error display). The rear panel error outputs (PULSED and LATCHED) of both instruments are also independent of each other. In the event of a combined output being required, the output signals can be added via a power splitter.

### 3-27 Summary

The following provides a summary of restrictions, parametric and operating, which apply to parallel operation.

**PARAMETRIC.** The only parametric restrictions refer to the Clock Delay settings and are listed as follows

Maximum Clock Delay:

95% of Period - 11ns

Max. Delta (Clock) Delay between both 8182A's:

95% of Period - 19ns

**OPERATING.** The operating restrictions are:

- 1) Only synchronous data analysis possible.
- 2) The minimum Trigger Delay in Real Time Compare mode is 2.
- 3) In Real Time Compare mode, there is no combined 'Stop on Error'.
- 4) All displays are instrument specific and cannot be combined on one screen.
- 5) The error outputs are instrument specific, but can be added via a power splitter.

## QUICK LOCATOR GUIDE

The Quick Locator Guide is intended to aid the user locate various instrument settings relevant to current measurement requirements. The guide is arranged in a sequence typical to user considerations when setting up the instrument. For each consideration, the user is directed to the relevant PAGE and associated Keyword (in the softkey label set upon PAGE selection) which accesses the required setting. e.g. if synchronous data sampling is required, the user is directed to the CONTROL PAGE, Keyword Clock, in the following guide.

	PAGE Select	Keyword
Data Analysis:	CONTROL	Operating Mode Glitch Detect
Data Sampling:	CONTROL	Clock
Data Recognition:	INPUT	Connector Labels Chnl Label
Data Capture:	CONTROL	Trigger Stop Autoarming Cycling Period(Real Time only)
Data Comparison:	EXPECTED DATA	Edit
Data Display:	INPUT	Chnl config

**NOTE:** This setting is accessible on various PAGES. Any change to the setting on one PAGE changes the other PAGES accordingly. The other PAGES are: EXPECTED DATA (under Edit Keyword) STATE LIST TIMING DIAGRAM (under Select Displ) ERROR MAP (under Select Displ).

STATE LIST	Disp Errors Also available on ERROR MAP (under Select Displ)
	Top Address This setting affects the same setting on EXPECTED DATA PAGE, and vice-versa.
TIMING DIAGRAMS	Select Displ Reset Delta
ERROR MAP	Select Displ
MISCELLANEOUS	Cur Top Addr

### PAGES - HOW TO USE THEM

The following gives a short description of each PAGE'S main features - how to access them and what they mean. The term "value entry" in the following descriptions can mean a numerical value, specific condition or mode.

**NOTE:** (Applicable to several PAGES) If DATA keys are used for integer values, entry can be with or without all leading zeroes. Without all leading zeroes ENTER NUMBER must be pressed, e.g. 0012 or 12 and ENTER NUMBER.

Also, softkey labels comprising all capitals, e.g. INSERT CHNL, indicates immediate execution on softkey operation. Labels with initial capitals, e.g. Stop, indicate that further softkey operation is required before a setting is complete

For each page in the following, a softkey illustration is provided to show how items within the page can be selected. Upon selection, the type of entry is indicated by one of the following mnemonics:

- DS - means a direct select entry
- NI - means a numeric integer entry
- NR - means a numeric real entry
- ND - means a numeric data entry

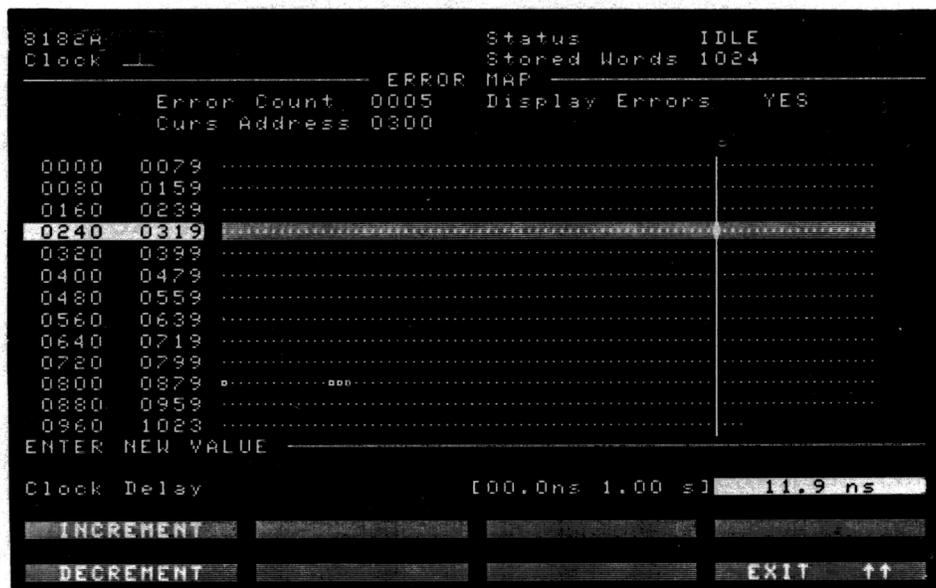
Each of these entry types are described in more detail in the following.

**PAGE SELECT:** Press the appropriate softkey to select a page.

**PAGE EXIT:** The user exits a page at any time by pressing the "PAGES" key. The page menu is then displayed by softkey labels, together with the "SELECT PAGE" prompt.

**PAGE MIXING:** Using the "CALL SOFTKEYS" and "CALL REPORTS" keys, the operator can combine the report of one page with the softkeys of another. An example to illustrate this feature would be to combine the "ERROR MAP" report with the "CONTROL" softkeys. This way, parameters such as "clock delay" can be varied to determine the value at which an error occurs. The following screen print illustrates this example.

**NOTE:** Clock Delay cannot be changed "on the fly". Data capture will be interrupted.



can be selected by pressing "CALL REPORT" key and pressing softkey labelled "ERROR MAP"

can be selected by pressing "CALL SOFTKEYS" key and pressing softkey labelled "CONTROL"

## REPORT ENTRIES

The HP8182A front panel operating menu is itemized in the 7 page reports. Upon page selection, the report displays only those items under the current operating conditions which can be assigned new values.

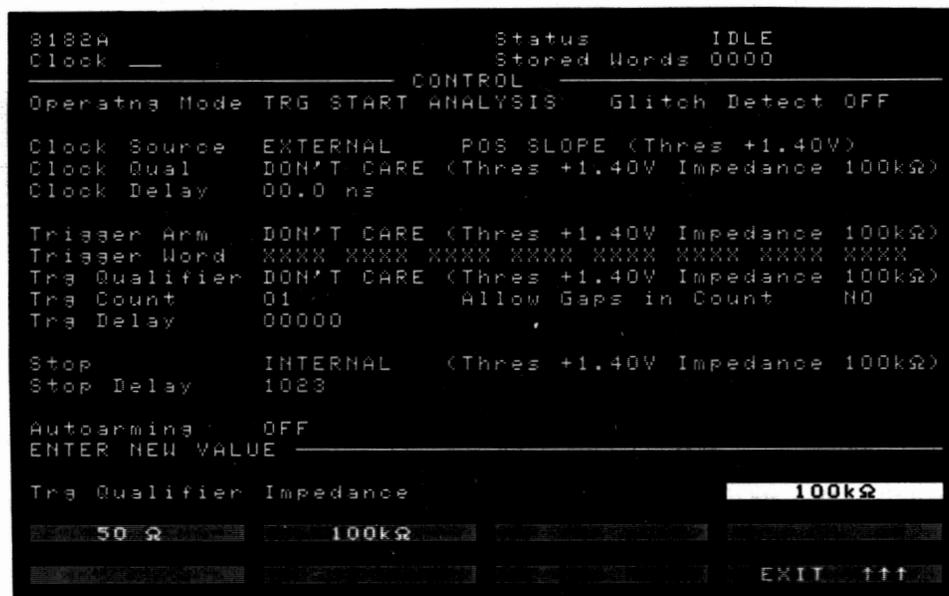
### Item Selection

Using the frontpanel softkeys, any item in the report can be re-called into the (SOFTKEYS) entry field for entering a new value. As can be seen from the following CONTROLS page example, related items are grouped together. On page selection, the softkey labels identify each group with a keyword e.g. Trigger. Selecting a group containing more than one item changes the softkey function to item select. For items with subitem choice (e.g. Trigger Qualifier: Level, Threshold, Impedance) the softkey function changes once again, on item selection, to subitem select. Any menu item, therefore, requires a maximum of 3 keystrokes depending on its location in the level hierarchy. The following CONTROLS page example shows how the entry field aids key operation by displaying level selections in group, item, subitem sequence.

## Types of Entry

Depending on the selected item, entries are either direct select or numerical, as explained in the following:

**DIRECT SELECT ENTRIES:** The user must press a softkey to directly select one of a fixed choice of settings e.g. ON/OFF, INTERNAL/EXTERNAL etc. DATA keys are disabled for these entries.



**NUMERICAL ENTRIES:** For numerical entries, either softkeys or DATA keys can be used, depending on whether the entry is integer, real, or data code. The entry conditions for each are described in the following:

**Integer**

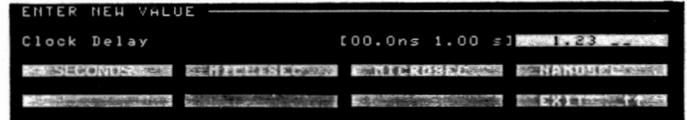
Entry is either by incrementing/decrementing the current value using the softkeys, or entering a new integer using the DATA keys "0" through "9". The minimum/maximum limits for an integer value are displayed alongside the inverse video field for the current setting. Incrementing/decrementing ceases automatically when these limits are reached. Attempting to use the DATA keys to enter a value outside the displayed limits causes the "VALUE OUT OF RANGE" error message to blink in inverse video; in this case the last valid entry remains active.



**Real**

Entry is either by incrementing/decrementing the current value using the softkeys, or entering a real number using the DATA keys. When using the DATA keys, entry is completed on unit selection via the softkeys. Parameter limits and the "VALUE OUT OF RANGE" error message are as already explained for Integer values. In addition, the current entry may be incompatible with the previous entry for another parameter e.g. user attempt to set the high threshold lower than the previously set low threshold of a channel label. The HP8182A automatically changes

the previous setting to meet the minimum compatibility requirements and a message is displayed in the entry field to inform the user of the change.



**Data Code**

Individual bits/bytes can only be entered using the DATA keys. Quick loading of the complete memory can be done via softkeys e.g. dump received data on the EXPECTED DATA page. DATA keys not relevant to the currently selected code (binary, octal, hex) are inactive. Note that the "DON'T CARE" key is only active for data code entries, and for codes other than binary, sets all bits corresponding to the selected digit to don't care. On the EXPECTED DATA page, this key is also used for masking bits, words or channels.



**Use of the EXIT Softkey (↑, ↑↑, ↑↑↑)**

As already mentioned in the previous paragraphs, item entries and item selection require softkey operations to step through the level hierarchy. The operator returns from the current level to the preceding level in the hierarchy by pressing the EXIT softkey. The vertical arrows on the EXIT label indicate how many levels the user has descended in current softkey operation.

**CONTROL PAGE**

**KEYWORD** GIVES ACCESS TO: xxxx, DETAILS ARE:

**Operatg Mode****TRG STRT ANAL**

for recording post-trigger data [Logic Analyzer Mode]

**TRG STOP ANAL**

for recording pre- or post-trigger data [Logic Analyzer Mode]

**TRG STRT COMP**

for real time comparison of incoming data and previously stored expected data [Real Time Compare Mode]

**Glitch Detect**

ON or OFF. When set to ON, the available memory for data recording is reduced to Channel number x 512 bits.

**Clock****Clock Source**

Can be set to EXTERNAL for synchronous operation, or INTERNAL for asynchronous operation.

**Clock Qual**

for qualifying (or gating) the clock signal, the qualifier signal is applied to the rear panel CLOCK QUALIFIER input BNC connector. Active signal level, input threshold and input impedance can all be set via softkeys.

NOTE: The following clock parameters available if EXTERNAL clock selected:

**Clock Slope**

POS SLOPE, NEG SLOPE, or BOTH SLPS. Note that selecting BOTH SLPS doubles the frequency, so ensure the time between slopes is  $\geq 20$ ns.

**Clock Threshold**

Continuously variable via INCREMENT/DECREMENT softkeys, or entry via front panel DATA keys. (Fixed TTL or ECL value also selectable via softkeys).

**Clock Delay**

Continuously variable via INCREMENT/DECREMENT softkeys, or entry via front panel DATA keys. The delayed clock signal is available at the rear panel CLOCK output BNC connector.

NOTE: The following clock parameter only available if INTERNAL clock selected:

**Clock Period**

Use INCREASE/DECREASE softkeys for 1,2,5 sequence (e.g. 100 ns, 200 ns, 500 ns) or use FAST INCREASE/FAST DECREASE softkeys for x 10 sequence (e.g. 1 ms, 10 ms)

**NOTE:** The following clock parameters only available if EXTERNAL clock selected in TRG STRT COMP MODE:

**Clock Width**

Continuously variable via INCREMENT/DECREMENT softkeys or entry via front panel softkeys.

**Trigger****Trigger Arm**

Provides edge-active trigger condition using a signal applied to the rear panel TRG ARM input BNC connector. Active slope, input threshold and input impedance can be set.

**Trigger Word**

Provides pattern recognition trigger condition. Data pattern can be entered in hexadecimal, octal or binary depending on the code setting on the INPUT page. Entry is via front panel DATA keys; cursor control is via softkeys.

**NOTE:** If the logic polarity is changed via the NORMAL/INVERSE setting on the INPUT page (also on TIMING DIAGRAMS, STATE LIST and ERROR MAP), then this word is automatically changed to correspond to the new polarity.

**Trg Qualifier**

Provides level-active trigger condition using a signal applied to the rear panel TRG QUAL input BNC connector. Signal qualifies the Trigger Word as valid or invalid (unless level is set to DON'T CARE). Active level, input threshold and input impedance can be set.

**Trg Count**

Determines how many times the (qualified) Trigger Word must occur prior to triggering. Set via incrementing/decrementing current value using softkeys, or entering integer value using front panel DATA keys.

**Allow Gaps (YES, NO)**

When set to NO, the (qualified) Trigger Word must occur on consecutive clock pulses, the number of pulses being defined by the Trg Count setting.

**Trg Delay**

Determine how many clock periods downstream from the trigger event, that triggering occurs.

**Stop****Stop Slope**

Set to POS or NEG determines the active slope of a signal applied to the rear panel STOP input BNC connector. Set to INTERNAL, stop occurs a selected number ( Stop Delay setting) of clock periods after triggering. Set to NOT ACTIVE, the "stop" function is switched off. For the external stop signal, input threshold and impedance are also selectable.

**Stop Delay**

When INTERNAL stop selected, determines how many clock periods after transition to ACTIVE state that data capture is stopped. Using external stop signal, this setting determines how many clock periods after the active edge of the stop signal that data capture is stopped. No function if "Stop Slope" set to INACTIVE.

**Stop on Error Only**

Available in Real Time Compare mode. When set to ON, comparison stops 1 clock period after an error occurs.

**Autoarming**

**value entry**

Used to replace RUN key operations. At the end of a data capture cycle, the instrument is automatically re-armed for the next capture cycle. If set to an (\*) value, re-arming is disabled on error detect.

**Cycling Period**

**value entry**

Only available in Real Time Compare mode for enabling autocycling. The integer setting determines the cycle length.

```

8182A                               Status      IDLE
Clock _____                     Stored Words 0000
                                CONTROL
Operatg Mode TRG START ANALYSIS      Glitch Detect OFF

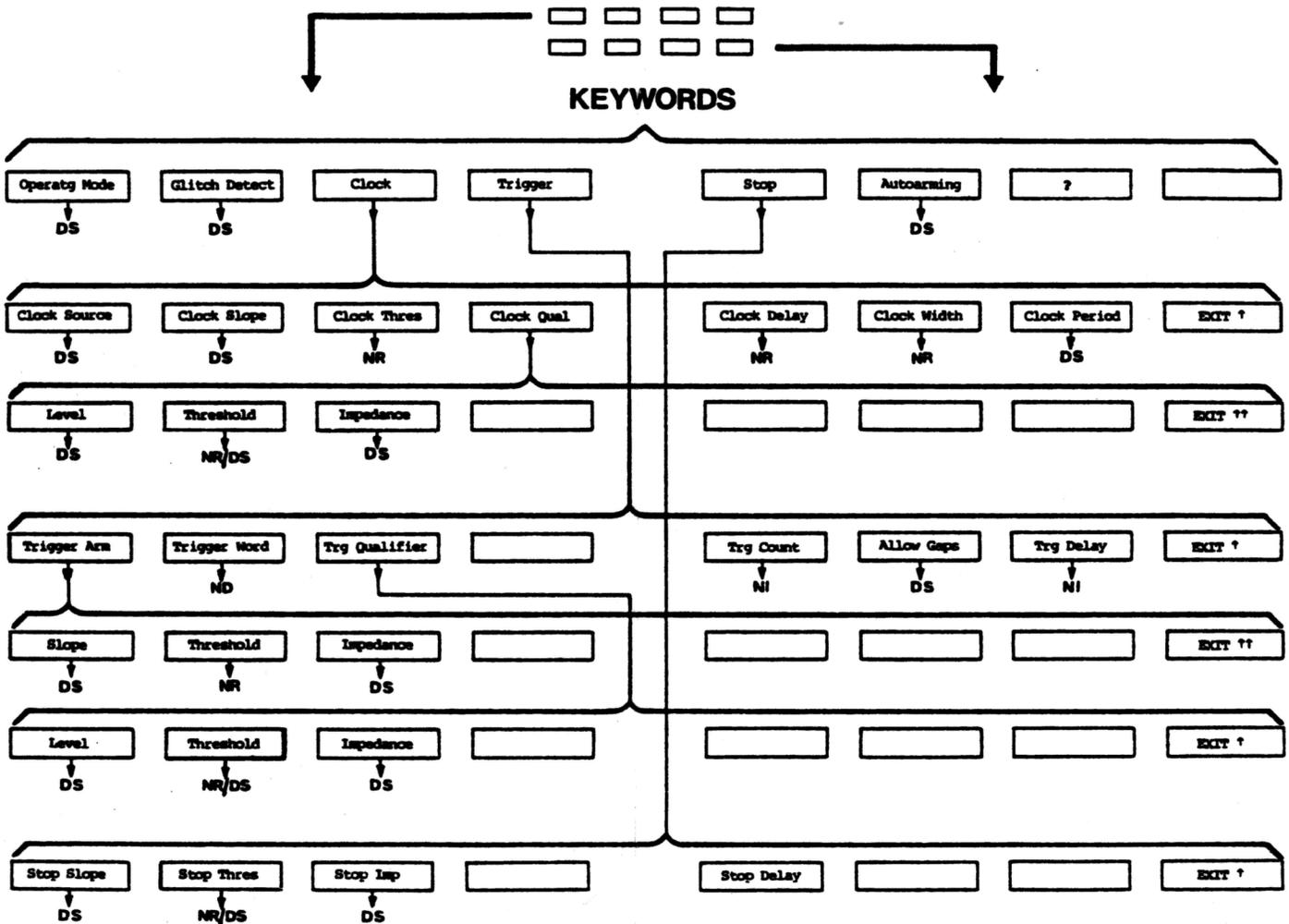
Clock Source EXTERNAL      POS SLOPE (Thres +1.40V)
Clock Qual   DON'T CARE (Thres +1.40V Impedance 100kΩ)
Clock Delay  00.0 ns

Trigger Arm  DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trigger Word XXXX XXXX XXXX XXXX
Trg Qualifier DON'T CARE (Thres +1.40V Impedance 100kΩ)
Trg Count    01          Allow Gaps in Count NO
Trg Delay    000000

Stop         INTERNAL      (Thres +1.40V Impedance 100kΩ)
Stop Delay   1023

Autoarming   OFF
Select Further _____

Operats Mode  Glitch Detect  Clock  Trigger
Stop         Autoarming
    
```



**INPUT**

**KEY WORD**           **GIVES ACCESS TO: xxxx, DETAILS ARE:**

**Connector**

**0 and 1, 2 and 3, etc.**

Selecting a connector pair enables single threshold or dual threshold to be set, the levels being determined by the currently assigned label.

**Labels**

**value entry**

Each label comprises 3 values for determining input threshold levels. The SINGLE value is active when SINGLE THRES has been set for the connectors to which the label is assigned; the UPPER and LOWER values are active when DUAL THRES has been set for the connectors to which the label has been assigned.

**Chnl Config**

**INSERT CHNL, DELETE CHNL, INSRT SEGMENT**

Used for configuring the channels as required for data display. DATA keys can be used to change channel number at current cursor position.

**Std Configuration**

Activates the channel configuration stored in the standard set on the MISCELLANEOUS page.

**Code/Polarity**

Hexadecimal, octal, binary code can be selected for data entry/display. Data can also be displayed according to positive or negative logic convention (NORMAL and INVERSE respectively).

**Chnl Labeling**

**value entry**

Use to assign a threshold label to each channel. Softkeys provide cursor control. Label is defined using DATA keys (A, B, C, D, E, or F).

```

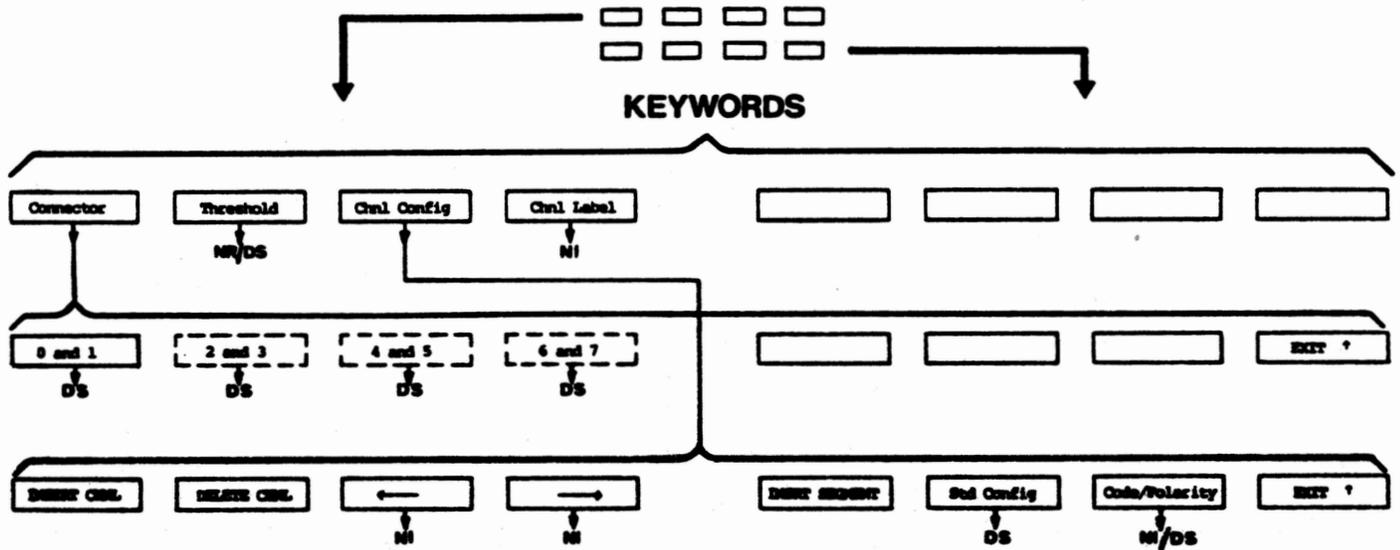
8182A                               Status      IDLE
Clock _____                     Stored Words 0000
                                     INPUT
CONNECTOR (Grey=Not Active)         THRESHOLD
Label Single Upper Lower
0 and 1    SINGLE THRES             A   +1.40V +2.00V +0.80V
2 and 3    SINGLE THRES             B   +1.40V +2.00V +0.80V
4 and 5    NOT INSTALLED            C   +1.40V +2.00V +0.80V
6 and 7    NOT INSTALLED            D   +1.40V +2.00V +0.80V
                                         E   +1.40V +2.00V +0.80V
                                         F   +1.40V +2.00V +0.80V

Channel Configuration, Label (Grey=Inverse)
Code      BIN  BIN  BIN  BIN
Connector 3333 2222 1111 0000
Channel   3210 3210 3210 3210
Label     AAAA AAAA AAAA AAAA

Select Further _____

Connector Threshold Chnl Confis Chnl Label

```



## EXPECTED DATA

### KEYWORD

GIVES ACCESS TO: xxxx, DETAILS ARE:

**CURSOR ↑**  
**CURSOR ↓**  
**CURSOR →**  
**CURSOR ←**

**value entry**  
These cursor keys enable cursor positioning prior to code entry via the front panel DATA keys. Upon entry, auto cursor movement is determined by the Entry Mode setting.

**PICTURE ↑↑**  
**PICTURE ↓↓**

Operating either of these keys brings the content of the next (^) or previous (v) 16 memory addresses into the display.

**Top Address**

**value entry**  
Upon entry, the data content of 16 consecutive memory addresses, starting with the entered address, is displayed.

**Edit**

#### **Clear & Set**

Enables the user to set the memory content of the displayed channels "all 0's". Via this key, the user can also mask all bits or all words for comparison. Masking can be removed for individual words or bits by moving the cursor to the required word/bit and pressing the "." DATA key.

**NOTE:**Bit masking is not available in Real Time Compare mode.

#### **Dump Rec Data**

[Logic Analyzer mode only] Enables the user to dump the recorded data in the high speed memory into the expected data memory.

#### **Channel Edit**

Edit facility on an entire channel basis. Edit features include: set all channel bits to 0; set all channel bits to 1; copy entire channel data into another channel; exchange the data content of two channels; mask a complete channel.

#### **Line Edit**

Allows a line of data to be inserted or deleted. Also, the entire memory content can be re-addressed using the "Roll Down Memory" and "Roll Up Memory" features.

#### **CHECKSUM**

Enables the user to check for any change in the content of expected data memory. Each time new data is entered, a new checksum is generated.

#### **Entry Mode**

Controls auto movement of the cursor after code entry.

#### **Chnl Config**

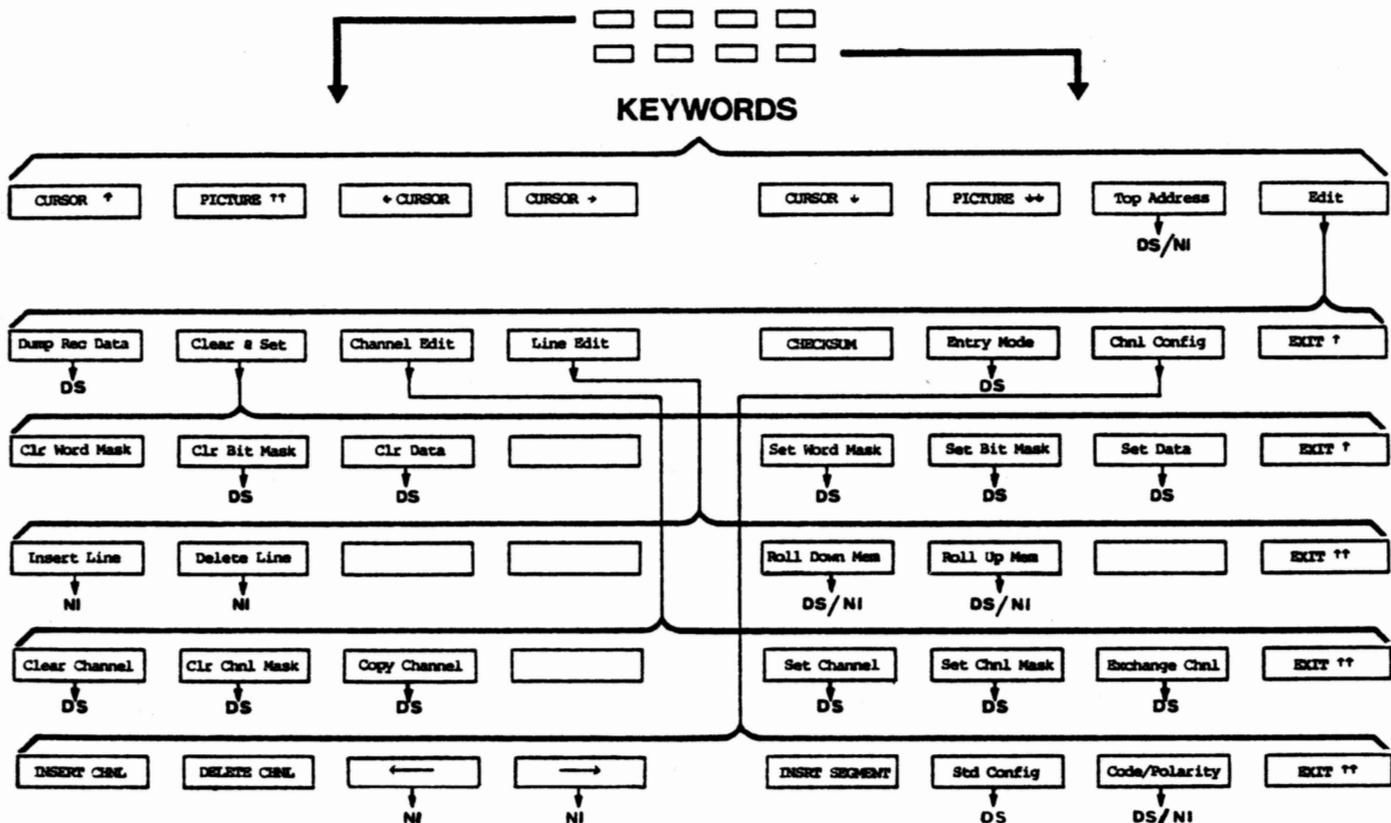
As already described for the INPUT page.

Any change here automatically changes the display configuration of the INPUT, ERROR MAP, TIMING DIAGRAMS and STATE LIST pages.

8182A	Status	IDLE
Clock	Stored Words	0000
EXPECTED DATA		
ADDR	MASK	DATA
0000	. 0000	0000 0000 0000 0000
0001	. 0000	0000 0000 0000 0000
0002	. 0000	0000 0000 0000 0000
0003	. 0000	0000 0000 0000 0000
0004	. 0000	0000 0000 0000 0000
0005	. 0000	0000 0000 0000 0000
0006	. 0000	0000 0000 0000 0000
0007	. 0000	0000 0000 0000 0000
0008	. 0000	0000 0000 0000 0000
0009	. 0000	0000 0000 0000 0000
0010	. 0000	0000 0000 0000 0000
0011	. 0000	0000 0000 0000 0000
0012	. 0000	0000 0000 0000 0000
0013	. 0000	0000 0000 0000 0000
0014	. 0000	0000 0000 0000 0000
0015	. 0000	0000 0000 0000 0000

PICTURE ↑↑	← CURSOR	CURSOR →
CURSOR ↓	Top Address	Edit



NOTE: If Cur & Top Addr on the MISCELLANEOUS page is set to LOOSED, two address markers, SET and CUR, appear in the report of this page to monitor cursor movement on the TIMING DIAGRAMS page.

SET - marks the address at which the cursor on the TIMING DIAGRAMS page was positioned when the RESET DELTA key was pressed.

CUR - marks the current cursor position on the TIMING DIAGRAMS page.

**MISCELLANEOUS****KEYWORD** GIVES ACCESS TO: xxxx, DETAILS ARE:**Auto Exit****value entry**

When set to ON, entering an item value returns the user automatically to the previous softkey menu level.

**Brightness****value entry**

sets the display brightness.

**Cur & Top Addr****value entry**

Set to LINKED, current position of the cursor on the TIMING DIAGRAMS (and ERROR MAP) page determines the top address of the displayed data when selecting STATE LIST or EXPECTED DATA page. Set to LOOSED, the top address of the displayed data, when STATE LIST (or EXPECTED DATA) page selected, is that which was active on previous page exit.

**Store****value entry**

Storage of any of 3 user-defined instrument settings.

**Recall****value entry**

Recall of any 3 user-defined instrument settings, or the standard instrument setting.

**NOTE:** When pressing the Recall softkey, only those "set" locations which have been used to store an instrument setting can be accessed. e.g. if 2 user-defined settings have been stored in Set 1 and Set 2, then only Set 1 and Set 2 will appear as softkey labels when Recall is pressed.

**STANDARD SET**

The following settings apply when the standard set is recalled. The settings are located on various pages, and are therefore listed under their respective pages as follows:

## CONTROL PAGE

Item	Standard setting
Operating Mode	TRIGGER START ANALYSIS
Glitch Detect	OFF
Clock:	
Source	EXTERNAL
Slope	POSITIVE
Threshold	1.4V
Clock Qualifier:	
Level	DON'T CARE
Threshold	1.4V
Impedance	100 k Ohm
Clock Delay	0.00 ns
Clock Width (not active)	10.0 ns
Trigger Arm:	
Slope	DON'T CARE
Threshold	1.4V
Impedance	100 k Ohm
Trigger Word	
	XXX... etc. (all channels DON'T CARE. Each "X" masks a "O")
Trigger Qualifier:	
Level	DON'T CARE
Threshold	1.4V
Impedance	100 k Ohm
Trigger Count	01
Allow Gaps in Count	NO
Trigger Delay	00000
Stop:	
Slope	INTERNAL
Threshold	1.4V
Impedance	100 k Ohm
Stop Delay	1023
Stop On Error	OFF
Autoarming	OFF
Cycling Period	OFF

**INPUT PAGE**

<b>Item</b>	<b>Standard Setting</b>
All installed Connectors  (8182A software interrogates hardware to determine how many connectors are installed, and sets the installed connectors accordingly)	<b>SINGLE THRESHOLD</b>
All Labels:	
Lower Threshold	0.8 V
Upper Threshold	2.00 V
Single Threshold	1.40 V
Channel Labelling	All channels labelled A.
Channel Configuration	4 channels for every installed connector
	1111 0000 ->... 3210 3210

**EXPECTED DATA PAGE**

<b>Item</b>	<b>Standard Setting</b>
Top Address	0000

**STATE LIST PAGE**

<b>Item</b>	<b>Standard Setting</b>
Display Errors	YES
Display Glitches (disabled as Glitch Detect OFF)	(if user switches Glitch Detect On)

**TIMING DIAGRAMS PAGE**

<b>Item</b>	<b>Standard Setting</b>
Cursor Address	0000
Entry Mode (Cursor Automove)	HORIZONTAL
Display Errors	YES
Display Glitches (disabled as Glitch Detect OFF)	YES(if user sets Glitch Detect ON)
Horizontal Zoom	1
Vertical Zoom	1

**ERROR MAP PAGE**

<b>Item</b>	<b>Standard Setting</b>
Error Count	OFF
Display Errors	YES
Display Glitches (disabled as Detect ON)	YES(if user switches Glitch Detect OFF)    Glitch

**MISCELLANEOUS PAGE**

<b>Item</b>	<b>Standard Setting</b>
Cursor & Top Address	LINKED
Display Brightness	Middle
Autoexit	OFF

Model 8182A

```

8182A                               Status      IDLE
Clock _____                     Stored Words 0000
_____ MISCELLANEOUS _____

Autoexit                            OFF
Cursor & Top Addr                    LINKED
Display Brightness                   #####

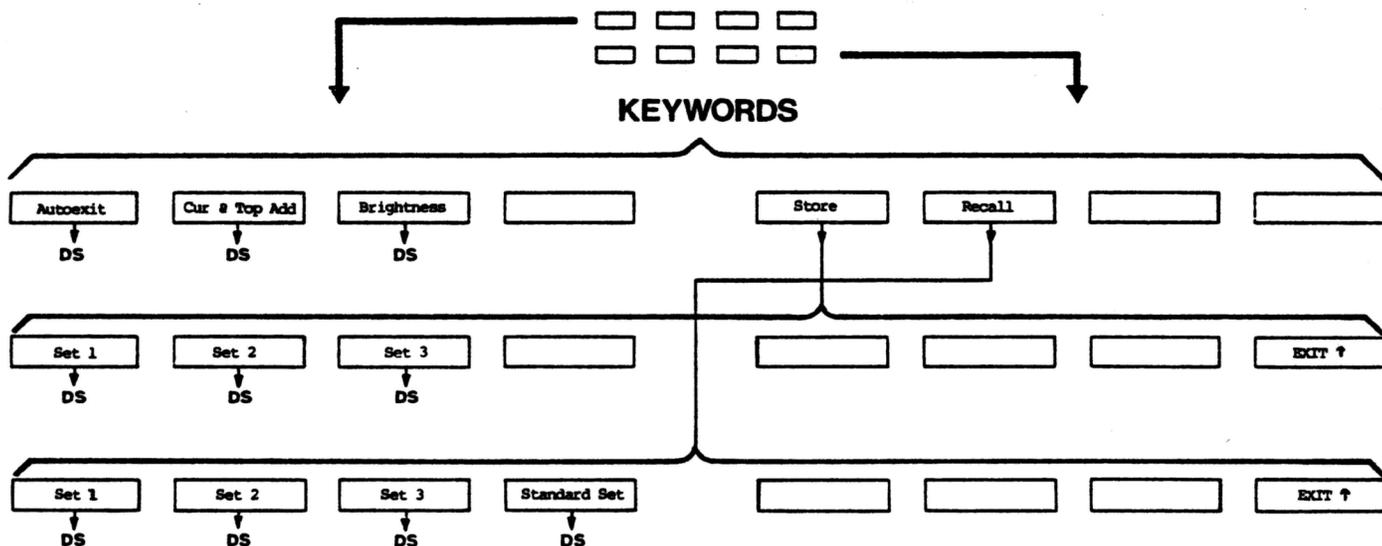
_____ FOR INFORMATION ONLY _____

HP-IB ASCII Address                  02
HP-IB Binary Address                 03

Total Channels                       16
Installed Connectors                 0123

Select Further _____

Autoexit+ Cur & Top Addr Brightness+
Store Recall
  
```



STATE LIST PAGE

KEY WORD           GIVES ACCESS TO: xxxx, DETAILS ARE:

PICTURE ↑  
PICTURE ↓  
PICTURE ↑↑  
PICTURE ↓↓

Used for controlling which 16 consecutive memory addresses provide the current data display. Arrows indicate whether higher or lower addresses are displayed on key operation.

**Disp Errors**

**value entry**  
Detected errors are only displayed when set to ON.

**Top Address**

**value entry**  
Upon entry, the data content of 16 consecutive memory addresses, starting with the entered address, is displayed.

**Chnl Config**

As explained for INPUT page. Any change here automatically changes the displayed configuration in the INPUT, EXPECTED DATA, ERROR MAP and TIMING DIAGRAMS pages accordingly.

**NOTE:** If Cur & Top Addr on the MISCELLANEOUS page is set to LOOSED, two address markers, SET and CUR, appear in the report of this page to monitor cursor movement on the TIMING DIAGRAMS page.

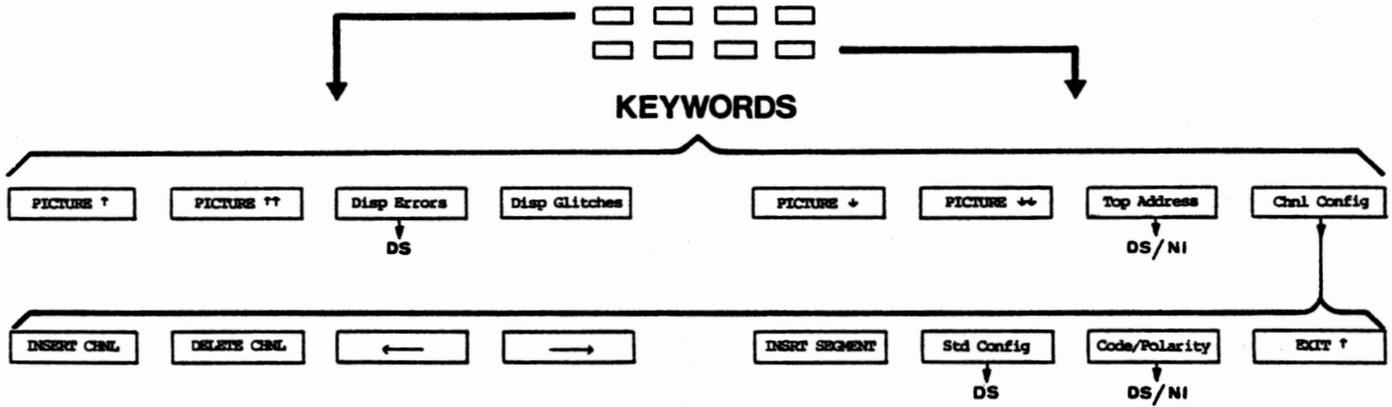
**SET** - marks the address at which the cursor on the TIMING DIAGRAMS page was positioned when the RESET DELTA key was pressed.

**CUR** - marks the current cursor position on the TIMING DIGRAMS page.

8182A			Status	IDLE
Clock			Stored Words	0000
		STATE	LIST	
			Display	Errors YES
ADDR	MASK	DATA		
0000	.			
0001	.			
0002	.			
0003	.			
0004	.			
0005	.			
0006	.			
0007	.			
0008	.			
0009	.			
0010	.			
0011	.			
0012	.			
0013	.			
0014	.			
0015	.			

PICTURE ↑	PICTURE ↑↑	Disp Errors	
		Top Address	Chnl Config



## TIMING DIAGRAMS

**KEYWORD** GIVES ACCESS TO: xxxx, DETAILS ARE:

**<- PICTURE  
PICTURE ->**

Position the display "window" over channel data.

**<- CURSOR  
CURSOR ->**

Cursor positioning keys.

**RESET DELTA**

Used in conjunction with cursor keys for "delta-time" measurements. Current cursor position when key is pressed in the start reference for time measurement.

**Select Displ**

**Curs Address**  
Provides fast cursor positioning.

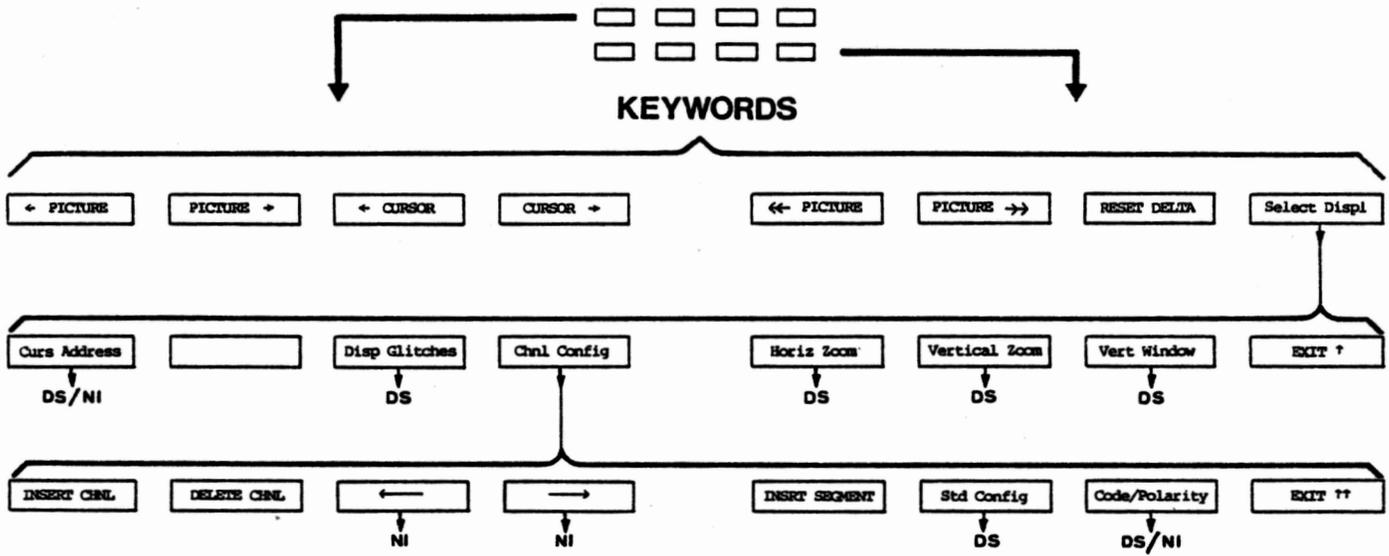
**Disp Glitches (with Glitch Detect on the CONTROL page)**  
Glitches only displayed when set to ON.

**Chnl Config**  
As already described on the INPUT page. Any change here automatically changes the displayed configuration on the INPUT, EXPECTED DATA, ERROR MAP and TIMING DIAGRAMS pages accordingly.

**Horizontal Zoom**  
For expanded time display.

**Vertical Zoom**  
For increased channel count in display.

**Vert Window**  
For determining which channels are displayed.



## ERROR MAP PAGE

KEY WORD

GIVES ACCESS TO: xxxx, DETAILS ARE:

CURSOR ↑  
CURSOR ↓  
CURSOR ->  
CURSOR <-

Provides cursor movement over the entire memory.

PREV ERROR  
NEXT ERROR

Provides error-related cursor movement

Curs Address

Provides fast cursor positioning

Select Displ

### Error Count

Provides quick overview of total error-count in current data capture cycles.

#### \*Disp Errors Detected

errors are only displayed when set to ON

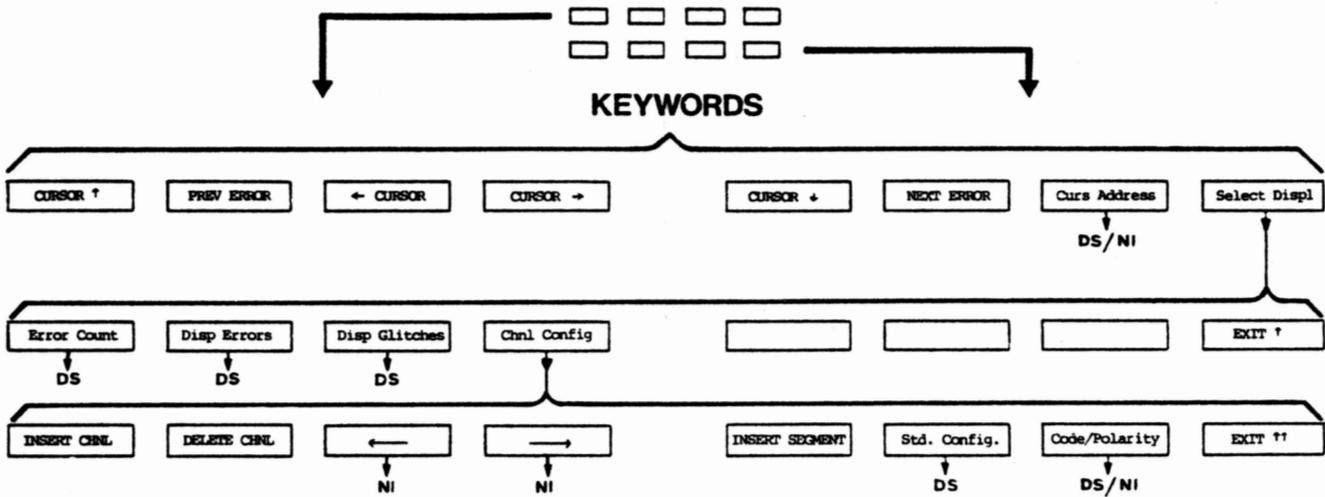
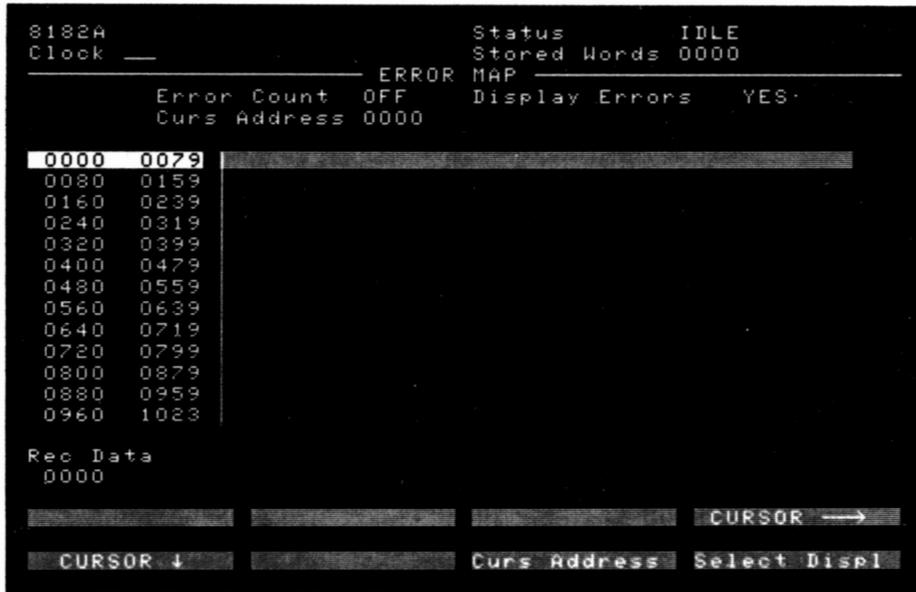
#### \*Disp Glitches

(with Glitch Detect set ON at the CONTROL page) Detected glitches are only displayed when set to ON

**\*NOTE:**The ERROR MAP uses the same marker (a small square) to indicate errors and glitches.If both displays are ON,the user cannot determine if the error is a compare result or a glitch For this reason,one of the displays should be switched off, and only errors associated with the remaining display will be shown.This also explains why the NEXT ERROR and PREV ERROR softkeys remain active when the Disp Errors is set to OFF. i.e.cursor moves from glitch to glitch.

### Chnl Config

As already described for INPUT page. Any change in this page automatically changes the displayed configuration on the INPUT, EXPECTED DATA, STATE LIST and TIMING DIAGRAMS pages accordingly.



## PROGRAMMING INFORMATION

### P-1 General

The following provides useful information and examples on programming of the 8182A. A complete list of HP-IB commands is given at the end of the quick reference section in this manual.

Basically, the 8182A has 2 remote modes of operation:

**ASCII Mode** - in which data, parameter and mode settings are transferred over the HP-IB as serial ASCII bytes. The ASCII message is then interpreted by the 8182A and executed accordingly.

**Binary Mode** - for fast transfer of binary data to/from the "expected data" and "captured data" memory sections.

A description of the listener and talker functions, in each of these modes, is given in the following. This information is generally restricted to 8182A specifics, and for detailed bus information, the user should refer to the following publications:

IEEE Interface Standard 488-1975  
ANSI Interface Standard MC1.1  
HP Publication 59401-90030  
HP Publication 5952-0058

### P-2 Address Assignment

When operating on the HP-IB, 2 addresses must be reserved for 8182A use; the first address for ASCII-byte transfer, and the second for binary data transfer. Both addresses are determined as follows by the setting of the rear panel HP-IB ADDRESS switch:

**ASCII address** = HP-IB ADDRESS switch setting (factory preset to decimal 00)

**Binary address** = ASCII address + 1 (decimal 01 for factory setting above )

At power-on, the 8182A checks address bits A1 through A5 of the rear panel switch to determine its current addresses, and displays both addresses in decimal on the MISCELLANEOUS page.

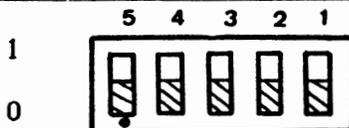
To change the addresses, first ensure that the 8182A is in local mode and not currently addressed, then change the bit settings on the rear panel switch. The new addresses will be activated within 2 seconds, or after switching power off and on. No address change will be accepted by the 8182A if the front panel display (top left corner) indicates that the 8182A is currently addressed to talk or listen.

Table 3-1 lists all possible addresses on the HP-IB. Note that if the rear panel address switch is set to decimal 30, no binary transfer can take place as address 31 is not allowed. The message "HP-IB Binary Address ILLEGAL" will then be displayed on the MISCELLANEOUS page.

Table 3-1. Available Addresses (ATN true)

Available Addresses (ATN true)										
Data bus (D IO lines)					Address in ASCII					
Fixed			Selectable		Talk	Listen				
8	7	6	5	4			3	2	1	DEC
O	T	L	0	0	0	0	0	0	@	SPACE <--- 8182A set for these
O	T	L	0	0	0	0	1	1	A	! <--- addresses at factory
O	T	L	0	0	0	1	0	2	B	"
O	T	L	0	0	0	1	1	3	C	#
O	T	L	0	0	1	0	0	4	D	\$
O	T	L	0	0	1	0	1	5	E	%
O	T	L	0	0	1	1	0	6	F	&
O	T	L	0	0	1	1	1	7	G	'
O	T	L	0	1	0	0	0	8	H	(
O	T	L	0	1	0	0	1	9	I	)
O	T	L	0	1	0	1	0	10	J	*
O	T	L	0	1	0	1	1	11	K	+
O	T	L	0	1	1	0	0	12	L	,
O	T	L	0	1	1	0	1	13	M	-
O	T	L	0	1	1	1	0	14	N	.
O	T	L	0	1	1	1	1	15	O	/
O	T	L	1	0	0	0	0	16	P	0
O	T	L	1	0	0	0	1	17	Q	1
O	T	L	1	0	0	1	0	18	R	2
O	T	L	1	0	0	1	1	19	S	3
O	T	L	1	0	1	0	0	20	T	4
O	T	L	1	0	1	0	1	21	U	5 <--- Usually controller address
O	T	L	1	0	1	1	0	22	V	6
O	T	L	1	0	1	1	1	23	W	7
O	T	L	1	1	0	0	0	24	X	8
O	T	L	1	1	0	0	1	25	Y	9
O	T	L	1	1	0	1	0	26	Z	:
O	T	L	1	1	0	1	1	27	[	;
O	T	L	1	1	1	0	0	28	\	<
O	T	L	1	1	1	0	1	29	]	=
O	T	L	1	1	1	1	0	30	^	>
O	T	L	1	1	1	1	1	31	-	? <--- Forbidden settings.

UNT, UNL commands.



Selector on 8182A rear panel (factory setting)

L = 1 for listen address, 0 for talk address

T = 1 for talk address, 0 for listen address

### P-3 Notes on Programming Examples

Programming examples are sometimes used in the following to illustrate the explanation. These examples assume that an HP9836 Calculator is the controller, and that BASIC is the programming language. Also, the following address convention is used to clarify when a command relates to ASCII or Binary mode of operation:

Ana\_ascii = 700 (assuming the factory setting)

Ana\_binary = 701

e.g. OUTPUT Ana\_ascii replaces the usual command OUTPUT 700

The examples are also valid for an HP9826 Calculator, but note that the HP9826 screen width is 50 characters whereas a line of information from the 8182A screen is 55 characters.

### P-4 ASCII MODE OF OPERATION

### P-5 Syntax Convention

The following syntax (Backus-Naur form) is used for HP-IB command definition in this manual:

	::=	means "is defined as"
	::=	or
< >	::=	non terminal symbol. The first time the symbol appears in the following descriptions, a further definition is provided.
{ }	::=	optional (zero, one, or more).
< Letter >	::=	A B C D ... Z   a b c ...z Alpha upper and lower case have the same effect
< Digit >	::=	1 2 3 4 5 6 7 8 9 0
< Hexadecimal >	::=	<Digit> A B C D E F a b c d e f
< Address >	::=	<hexadecimal><hexadecimal><hexadecimal><hexadecimal>
< SP >	::=	Blank
< Separator >	::=	<CR> <LF>  ,   ;   <SP>
< CR >	::=	Carriage return.
< LF >	::=	Line feed.
< Delimiter >	::=	<CR> <LF>  ,   ;
< Sign >	::=	+   -
< DP >	::=	Decimal point = .
< Empty >	::=	Nothing
< HEX >	::=	H <BIN                    >::= B <OCTAL                    >::= O
<Standard Number>	::=	{<SP>}<Sign> <Empty><Number 1> <Number 2> <Number 3> {<SP>}<Exponent> <Empty>
< Number 1 >	::=	<Digit>{<Digit>}
< Number 2 >	::=	<Digit>{<Digit>}<DP> <Empty>{<Digit>}
< Number 3 >	::=	<DP><Digit>{<Digit>}
< Exponent >	::=	E   e <sign> <empty><Digit>{<Digit>}

The number of digits in number 1, 2 or 3 must be smaller than 100. The result of the digits in the exponent must be smaller than 100.

< Integer Number >	::=	<Standard Number> the result of which is an integer number.
< Real Number >	::=	<Standard Number>, the result of which can be real. The number will be truncated after 3 significant digits (no rounding).
< Unit >	::=	<Volt>   <Time>
< Volt >	::=	V   v
< Time >	::=	<Millisec>   <Microsec>   <Nanosec>   <Seconds>
< Millisec >	::=	mS   MS   Ms   ms
< Microsec >	::=	uS   US   Us   us
< Nanosec >	::=	nS   NS   Ns   ns
< Second >	::=	S   s

### P-6 Listener Function

All modes, parameters and data can be programmed by HP-IB commands when the 8182A is addressed to listen in ASCII operation. A complete list of the commands is given in the Quick Reference Information at the end of this section. The commands are classified in types and described in the following:

1) **Type E.** These are 3-character commands which are executed immediately. The commands are listed as follows:

<Type E> ::= RUN | STP | SPL | CLD | SED | CBM | SBM | CWM | SWM  
DRD | SSC | NXE | PRE | RSS

e.g. OUTPUT Ana\_ascii;"RUN" (Comment: same as front panel RUN key)

**NOTE:** A complete set of mode/parameter settings is permanently stored in the 8182A memory. This set can be activated for quick setup purposes using the RSS command (Recall Standard Set) above.

e.g. OUTPUT Ana\_ascii;"RSS"

A complete list of these standard settings is given on the MISCELLANEOUS page in the Quick Reference Information.

2) **Type S.** Direct select commands defined as follows:

<Header S> {<SP>} <Digit>

<Header S> ::= OPR | GLD | TAS | TAI | TQL | TQI | AGC | SPS | SPI | SPE | CKL | CKS |  
CQL | CQI | AAD | C01 | C23 | C45 | C67 | DSE | HOZ | VEZ | CTE | DSG  
| STO | RCL | PAG | REP | KEY | TLK | BLI | BTK |

e.g. OUTPUT Ana\_ascii;"OPR1" (Comment: selects Trigger Start Analysis)

3) **Type I.** Integer commands defined as follows:

<Header I> {<SP>} <Integer Number>

<Header I> ::= TRC | TRD | SPD | CYP | MSK | SYN | TAD | CAD | DLI | ILI | RDO |  
RUP | LIN | BSA | TSA

e.g. OUTPUT Ana\_ascii;"TRC5" (Comment: sets trigger count to 5)

4)Type R. Real commands defined as follows:

<Header R> {<SP>} <Real Number> {<SP>} <Unit>

<Header R> ::= TAT | TQT | SPT | CKT | CKD | CKW | CQT | SIx | LOx | UPx  
(x=A|B|C|D|E|F)

e.g.OUTPUT Ana\_ascii;"SIA 2.3V" (Comment: sets single threshold of Label A to 2.3V)

5)Type F. Formatted data commands which are code dependent and subdivided into 3 categories. Each category is defined as follows:

**F1.1** ::= <Header F1.1> {<SP>} <one segment> {<SP>{<SP>} <one segment>}  
{<SP>} <Delimiter>

<Header F1.1> ::= TWD | DAT  
<one segment> ::= <Hexadecimal>|<DP>| X | - >{ <Hexadecimal> |<DP>| X | - }

NOTES. <DP> and X have the same effect as the front panel "." and "X" keys

i.e.clear and set mask respectively.The - sign skips a channel or channels depending on the code.

The complete <one segment> entry must correspond to the code and channel segmentation of the Channel Configuration setting (Type SP)

e.g. 10 OUTPUT Ana\_ascii;"CAS B 03 02 01 00 ;ADS B 13 12 11 10"  
20 OUTPUT Ana\_ascii;"TWD 10X0 0-- 1"

Comments: Line 10 clears all channels and adds 2 binary coded segments containing channels 3,2,1 and 0 of connectors 0 and 1.

Line 20 sets the trigger word.Channel 01 is masked and channels 12 and 11 are skipped. Delimiter CR LF is sent automatically at the end of the string with the HP9836's OUTPUT command, unless suppressed per user command.

**F1.2** ::= <Header F1.2> {<SP>} <Word Mask> {<SP>{<SP>}<one segment>}  
{<SP>}<Delimiter>

<Header F1.2> ::= DAM  
<Word Mask> ::= X | <DP>

NOTES. As above for F1.1.

e.g.OUTPUT Ana\_ascii;"TSA 43 DAM X 1111 0000"

Comments: TSA 43 sets the transfer start address to 0043. Using the DAM command, the binary word 1111 0000 is transferred to this address and X sets the word mask.

**F2.1** ::= <Header F2.1> {<SP>} <hole segment> {<SP>{<SP>}<hole segment>}  
{<SP>}<Delimiter>

<Header F2.1> ::= LBL | POL | CCD | SCD | CCM | SCM | COC | XCH  
<hole segment> ::= <A|B|C|D|E|F|N|I|1|2|> {A|B|C|D|E|F|N|I|1|2|>}

NOTES. For each header, a <hole segment> character must be entered for every channel as defined in the Channel Configuration setting. See the Quick Reference Information to determine which characters are valid for which header.

e.g. OUTPUT Ana\_ascii;"LBL ABBA DDDD"

Comments: Using the same Channel Configuration for F1.1 above, label A is assigned to channels 03 and 00; label B to 02 and 01; label D to 13,12,11 and 10.

6) Type SP. Special type commands, each of which is explained as follows:

**Channel Configuration.** 2 commands for setting the channel configuration.

1. **Clear all channels and add one segment.**

CAS {<SP>} <Code><SP> < <Connector><Channel> > {<SP>}<SP> < <Connector><Channel> >}{<SP>}<Delimiter>

<Code>	::=	<HEX>   <BIN>   <OCT>
<HEX>	::=	H
<BIN>	::=	B
<OCT>	::=	O
<Connector>	::=	0 1 2 3 4 5 6 7
<Channel>	::=	0 1 2 3

2. **Add segment.**

ADS...command definition as given above for CAS.

NOTES. For both commands, the entered connector must be active. If dual threshold is set for a connector pair, then the odd-numbered (1,3, 5 or 7) connector will not be a valid entry in the command string.

A maximum of 16 channels are allowed in one segment.

The maximum configuration, including channels and spaces between segments, is 41.

e.g. OUTPUT Ana\_ascii;"CAS B 03 02 01 00;ADS H 13 12 11 10"

Comments: The CAS command clears the current configuration and adds a binary coded segment containing channels 3, 2, 1 and 0 of connector 0. The ADS command adds a further hex-coded segment containing channels 3, 2, 1 and 0 of connector 1.

**Clock Period** ::= CKP {<SP>} <Standard Number> {<SP>} <Time>

NOTES. The result of the <Standard Number> and unit must be one of the following values:

20ns, 50ns, 100ns, 200ns, 500ns, 1us, 2us, 5us, 10us, 20us, 50us, 100us, 200us, 500us, 1ms, 2ms, 5ms, 10ms, 20ms, 50ms, 100ms, 200ms, 500ms, 1s.

e.g. OUTPUT Ana\_ascii;"CKP 500ns" (Comment: sets internal clock period to 500ns.)



**Display Text** in the Report Area of REMOTE Page 8. ::= DSP {<Any ASCII character>} <CR>|<LF>

{Any ASCII character} ::= any 7-bit ASCII character

NOTES: The DSP command is accepted only if the report area of page 8 is in the display (Command REP 8). The display line must also be defined using the LIN command (LIN 4 to LIN 23 can be defined).

e.g. OUTPUT Ana\_ascii;"REP8 LIN5 DISP Operator command"

Comment: The message "Operator command" will appear on line 5 of the REMOTE page.

### P-7 Talker Function

In ASCII operation, 8 blocks of information can be retrieved from the 8182A memory for transmission over the HP-IB. These blocks are selected by commands TLK1 through TLK8, which are sent to the 8182A in listener mode.

```
e.g.  10 DIM A${50}
      20 OUTPUT Ana_ascii;"TLK1"
      30 ENTER Ana_ascii;A$
```

Comments: Line 10 reserves memory space. Line 20 requests status information (TLK1—see following) from the 8182A. Line 30 enters the status bytes in string A\$.

The information selected by each of the TLK commands is as follows:

```
TLK1 - Status
TLK2 - Current parameter set
TLK3 - Display dump
TLK4 - Expected data
TLK5 - Captured data
TLK6 - Error and glitch information from the STATE LIST page
TLK7 - ERROR MAP lines
TLK8 - Channel marking
```

The default talk mode (forced at power on) is TLK1; otherwise the 8182A outputs the information as defined by the last given TLK command in response to an ENTER statement.



TLK 2 = CURRENT PARAMETER SET

6 ASCII strings,each 74 characters long.

```

330 DIM B$[76]
340 DIM C$[76]
350 DIM D$[76]
360 DIM E$[76]
370 DIM F$[76]
380 DIM G$[76]
390 OUTPUT Ana_ascii;"TLK 2"
400 ENTER Ana_ascii:B$.C$.D$.E$.F$.G$
410 !TLK 2:ENTERS ALL PARAMETER SETTINGS
420 !NOTE: THIS INFORMATION IS COMPRESSED
430 !AND NOT INTERPRETABLE BY THE USER. IT
440 !IS ONLY FOR STORAGE PURPOSES ON A MASS
450 !STORAGE DEVICE AND FOR FAST RESTORAGE
460 !INTO THE ANALYZER
    
```

TLK 3 = DISPLAY DUMP

```

LINE 1-          TALK          STATUS          IDLE          <CRLF>
          CLOCK I          ACT address 0328          <CRLF>
----- ERROR MAP -----<CRLF>
LINE 4-          Error Count 0002 Compare FAILED          <CRLF>
          Curs Address 0187          <CRLF>
          <CRLF>
          0000 0079 .....I.....<CRLF>
          0080 0159 .....I.....<CRLF>
          0160 0239 .....I.....<CRLF>
          0240 0319 .....I.....*.....<CRLF>
          0320 0399 .....I.....<CRLF>
          0400 0479 .....I.....<CRLF>
          0480 0559 .....I.....<CRLF>
          0560 0639 .....I.....<CRLF>
          0640 0719 .....I.....<CRLF>
          0720 0799 .....I.....<CRLF>
          0800 0879 .....I.....<CRLF>
          0880 0959 .....I.....<CRLF>
          0960 1023 .....I.....<CRLF>
          <CRLF>
          Channel          <CRLF>
          Marking          **** *.* **** *.* **** *.* .*** *.*<CRLF>
LINE 23-          <CRLF>
          CURSOR |          PREV ERROR          - CURSOR          CURSOR -          <CRLF>
          <CRLF>
LINE 26-          CURSOR |          NEXT ERROR          Curs Address          Select Displ<CRL<CRLF>
    
```



TLK 5 = CAPTURED DATA

One line in ASCII format

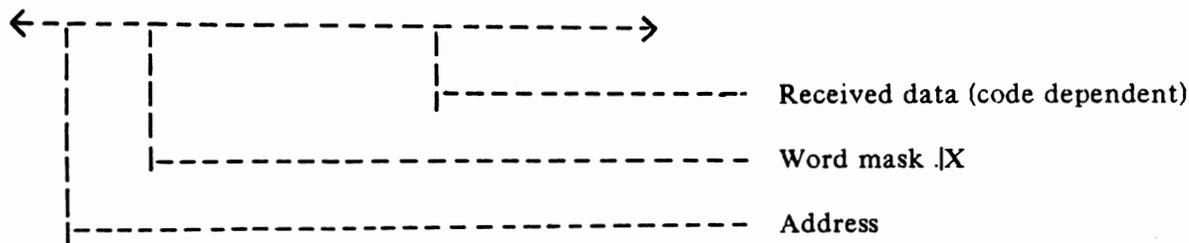
(refer to Transfer Start Address (TSA), SPECIAL COMMANDS in Quick Reference Info)

If TSA DISABLE or Real Time Compare mode: <CRLF>

If TSA ENABLE:

+0000,X 0000 12F2 311-A.....<CRLF>

8 to 49 bytes



If no data present - only address and word mask

Format is the same as channel grouping; groups separated by blanks.

```

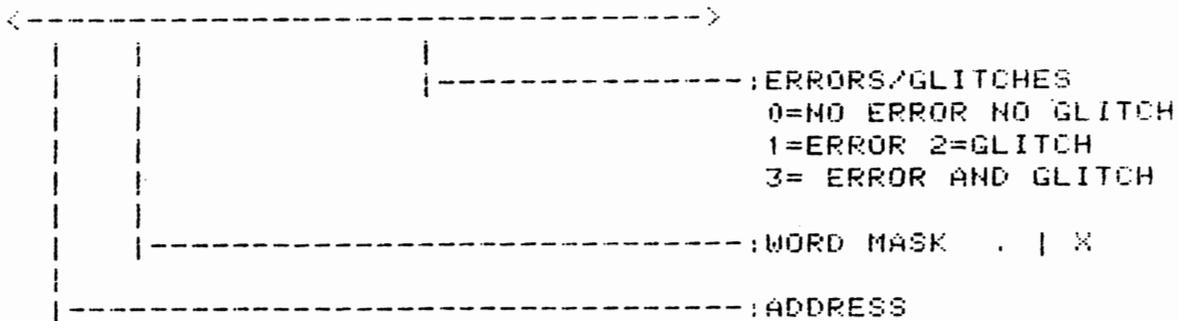
1010 DIM Q$(100)
1020 OUTPUT Ana_ascii;"TSA0 TLK5"
1030 FOR L=1 TO 5
1040 ENTER Ana_ascii:Q$
1050 PRINT Q$
1060 NEXT L
1070 !TLK 5: THIS IS TO READ RECEIVED DATA
1080 !FROM THE ANALYZER TO THE CONTROLER.
1090 !FORMAT IS THE SAME AS CHANNEL CONFIGURATION.
1100 !IN THIS CASE 5 WORDS ARE ENTERED STARTING
1110 !AT ADDRESS ZERO.
    
```

TLK 6 = ERRORS/GLITCHES from STATE LIST (CAPTURED DATA)

One line errors and glitches in ASCII format  
 (Refer to Transfer Start Address (TSA),SPECIAL COMMANDS in Quick Reference Info)

If TSA DISABLE or Real Time Compare mode: <CRLF>  
 If TSA ENABLE:

+0000, . 000 1231 2100 1111 320011 1<CRLF>  
 8 TO 49 BYTES



Format is the same as channel grouping; groups separated by blanks.

If no data and therefore no error|glitches present: only address and word mask

If the display errors or display glitches is set to OFF, no error or glitch message will be sent.  
 (refer to front panel operation)

```

1210 OUTPUT Ana_ascii;"TSA0 TLK6"
1220 DIM R$(100)
1230 ENTER Ana_ascii;R$
1240 PRINT R$
1250 !TLK 6: THIS IS TO ENTER ERRORS AND
1260 !GLITCHES. FORMAT IS THE SAME AS CHANNEL
1270 !CONFIGURATION
    
```

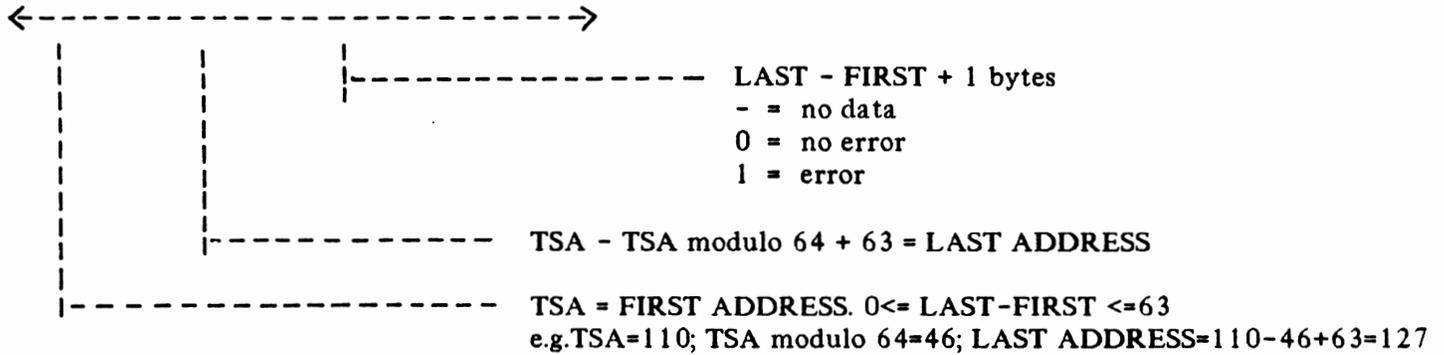
**TLK 7 = ERROR MAP**

One line; see Transfer Start Address, section SPECIAL COMMANDS in Quick Ref. Section.

If TSA DISABLE: <CR LF>

If TSA ENABLE :

+0000,+0063,0100001100-----<CRLF>  
 13 to 76 bytes



```

1350 DIM S$(100)
1360 OUTPUT Ana_ascii;"TLK 7 TSA 0130"
1370 ENTER Ana_ascii;S$
1380 PRINT S$
1390 !TLK 7: THIS IS TO TRANSFER THE ERROR MAP
1400 !LINES TO THE CONTROLLER. INDICATES ERRORS.
1410 !AND NO DATA.FIRST ADDRESS IS +0130;LAST
1420 !ADDRESS IS +0191(TSA MODULO 64=2;LAST
1430 !ADDRESS =TSA-2+63=191).
    
```

**TLK 8 = CHANNEL MARKING**

0011 0110 11110000 1 10 <CR LF>  
 <----->  
 0 to 41 bytes

- a) Length is 0 (empty string) if Real Time Compare mode or no data .
- b) Format is the same as channel grouping; groups separated with blanks.
- c) No errors coded as 0; errors coded as 1.

## P-8 Service Request Status Byte

During program execution, certain conditions can arise which cause the 8182A to make a service request (i.e.set SRQ line true). If the 8182A is then addressed as talker using the serial poll command (e.g.N=SPOLL(Ana\_ascii) in program sub-routine, or SPOLL(Ana\_ascii) as single statement), the 8182A responds by putting a single 8-bit status byte on the bus, the decimal equivalent of which can then be displayed or printed by the HP9836. From the decimal number, the user can determine which bits of the status byte have been set to '1', and hence the reason(s) for the service request. The following relates bit labelling to DIO lines, and continues by listing the bit allocation.

DIO 8	DIO 7	DIO 6	DIO 5	DIO 4	DIO 3	DIO 2	DIO 1
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

### STATUS BYTE

#### Bit 7 : POWER ON BIT

- 1 : Power on test failed
- 0 : Power on self test passed

#### Bit 6 : REQUEST BIT

- 1 : 0 to 1 transition of one of the bits 5 to 0. These bits are enabled by the bit mask (msk) command.
- 0 : SPOLL complete or RESET

#### Bit 5 : ERROR BIT

- 1 : Fast clock detected
- 0 : SPOLL complete or RESET

#### Bit 4 : READY BIT

- 1 : STOP routine executed
- 0 : SPOLL complete or RESET. This bit can be used to indicate to the controller that a measurement cycle is completed (IDLE state) and data transfer (e.g.of captured data) can commence.

#### Bit 3 : FRONT PANEL SRQ BIT

- 1 : "SRQ" key pressed
- 0 : SPOLL complete or RESET

#### Bit 2 : AUTOCORRECT

- 1 : autocorrection done
- 0 : SPOLL complete or RESET

For example, if Trigger Delay is set to 00000 and Real Time Compare mode (OPR3) is selected, Trigger Delay is automatically set to 00001 and this bit is set to 1.

**Bit 1: WRONG VALUE BIT**

1 : Attempt to program a wrong value  
 0 : SPOLL complete or RESET

**Bit 0: WRONG STATEMENT BIT**

1 : Statement not recognized by interpreter or not allowed  
 0 : SPOLL complete or RESET

Bit 7 set to 1 does not cause a service request, but disables remote operation of the 8182A until the front panel CONTINUE softkey is pressed (see para.3-6 OPERATOR'S CHECKS).

Bits 0 to 5 can be masked using the MSK command as illustrated in the following example:

e.g. OUTPUT Ana\_ascii;"MSK 27"

Comments. This masks bits 2 and 5 (binary 011011=dec.27).The value 63 is the default value forced at power-on and at an HP-IB address switch change.

**P-9 BINARY MODE OF OPERATION**

There are 3 listen commands and 2 talk commands for initiating a binary transfer to or from the 8182A. The commands and their functions are listed as follows:

BLI1 - transfers expected data from the controller to the 8182A.  
 BLI2 - transfers bit mask data from the controller to the 8182A.  
  
 BTK1 - transfers captured data from the 8182A to the controller.  
 BTK2 - transfers expected data from the 8182A to the controller.  
 BTK3 - transfers bit mask data from the 8182A to the controller.

Each of the above commands must be sent to the 8182A in ASCII listener mode prior to the binary transfer command.

e.g. 10 OUTPUT Ana\_ascii;"BSC 01 BSA 0 BTK2"  
 20 DIM A\$(100)  
 30 ENTER Ana\_binary USING "-K,%,#";A\$

Comments: **BSC 01** defines data bits of channels 00, 01, 02, 03, 10, 11, 12 and 13. **BSA 0** defines address 0000. **BTK2** requests expected data. (Channel 00 provides least significant bit).

# suppresses terminators.

% characters entered until EOI true or string full.

-K free entry field (CR LF is accepted in the event that the binary data = CR LF; otherwise transfer interrupted).

Another example to illustrate bit mask data transfer is given as follows:

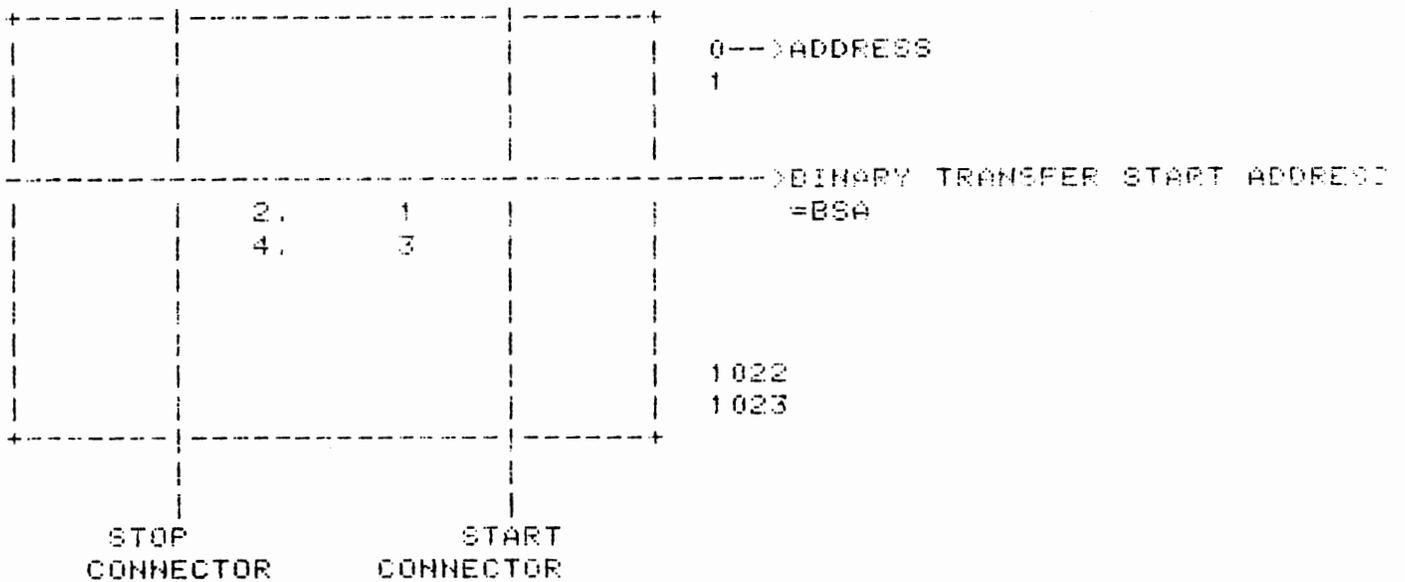
e.g. 10 OUTPUT Ana\_ascii;"BSC 01 BSA 0 BLI2"  
 20 OUTPUT Ana\_binary USING "#,A";CHR\$(32)

Comments: The binary equivalent of ASCII 32 (0010 0000) is transferred to address 0000. A "1" will result in masking of the respective bit position. In this case, the channel 11 bit is masked (2nd channel of connector 1).

The following memory map illustration aids the user in defining individual bit positions of the 8182A memory.

**MEMORY MAP of EXPECTED DATA and CAPTURED DATA (STATE LIST)**

```
77776666555544443333222211110000  -->CONNECTOR
32103210321032103210321032103210  -->CHANNEL
```



Data is always transferred as 8-bit bytes, the BSA and BSC commands being used to position these bytes as shown in the above illustration (if 4 bytes are transferred, their positions are indicated by digits 1, 2, 3 and 4). The following provides a brief description of these commands and an example of their use.

**Binary Transfer Start Address : BSA... (Type I)**

Range : 0 to 1023 not autoincremented.  
 Default 0, forced at power on or GPIB address switch change.

**Binary Select Start|Stop Connector : BSC... (Type SP)**

BSC{<SP>}<Start Connector>{<SP>}<Stop Connector>

<Start Connector> ::= 0 | 2 | 4 | 6  
 <Stop Connector > ::= 1 | 3 | 5 | 7

SRQ if Start Connector > Stop Connector or Stop Connector > Max. installed connectors .

Example: The following output sequence will set the expected data in the following order:

OUTPUT Ana\_ascii,"BSC 2 5 BSA 408 BLI 1"  
 OUTPUT Ana\_binary USING "#,4A","1234" Comment: # suppresses terminators.

5555444433332222 --> CONNECTOR  
 3210321032103210 --> CHANNEL

0011001000110001 --> ADDRESS 408  
 0011010000110011 --> ADDRESS 409

NOTES: ASCII 1 = 00110001 binary as shown in address 408, channels 2 0 to 3 3

The actual transfer address is reset to the BSA if:

- a) Last data bit of address 1023 reached.
- b) Address changed (Listen|Talk|Unlisten etc.).
- c) Serial poll complete.
- d) BSA or BSC changed.
- e) EO1 received (in Listener).
- f) BLI or BTK changed.

(In Talker mode, the last data bit of address 1023 is sent with EO1 true.)

The contents of the expected|captured data memories and the bit mask depend on the operating mode and the state of the Glitch Detector. The following memory maps indicate the memory content of the different BSA addresses (e.g. CAPTURED DATA: in OPR1, GLD1 the memory content of BSA address 1023 is the glitch information of front panel display address 511.)

**EXPECTED DATA**

		BSA	LOGICAL ADDRESS (SAME AS IN DISPLAY)	
			OPR1	OPR2
77776666555544443333222211110000				
32103210321032103210321032103210				
+-----+-----+				
	8 bits	8 bits		
		0000	+0000	-1023
		511	+511	-512
		512	+512	-511
		1023	+1023	-0000
+-----+-----+				



Example assuming TSA 512, OPR 1, GLD 1 and BSC 01.

	1	1	1	1	0	0	0	0	-->Connector
	3	2	1	0	3	2	1	0	-->Channel
			0				0		-->no glitch
connector 0			1				0		-->high level glitch on channel 1 of
			0				1		-->low level glitch on channel 1 of
connector 0			1				1		-->glitch on channel 1 of connector 0 which has passed through both levels.

COMMANDS OF THE CONTROL PAGE (1)  
 =====

TITLE	COMMAND
Operating Mode (Type S)	
-----	
TRIGGER START ANALYSIS.....	OPR 1
TRIGGER STOP ANALYSIS	OPR 2
TRIGGER START COMPARE	OPR 3
Glitch Detect (Type S)	
-----	
Glitch Detect ON.....	GLD 1
Glitch Detect OFF	GLD 2
Clock Source (Type S)	
-----	
Clock Source External.....	CLK 1
Clock Source Internal	CLK 2
Clock Slope (Type S)	
-----	
Active Slope: Positive.....	CKS 1
Active Slope: Negative	CKS 2
Active Slope: Both Slopes	CKS 3
Clock Threshold (Type R)	
-----	
Range: - 10 V to + 10 V.....	CKT.....
Clock Qualifier Level (Type S)	
-----	
Active Level: High.....	CQL 1
Active Level: Low	CQL 2
DON'T CARE	CQL 3
Clock Qualifier Threshold (Type R)	
-----	
Range: - 10 V to + 10 V.....	CQT...1.4V
Clock Qualifier Impedance (Type S)	
-----	
Impedance = 50 OHM.....	CQI 1
Impedance = 100 K OHM	CQI 2
Clock Delay (Type R)	
-----	
Range: 0.00 NS to 1.00 S.....	CKD.....

Clock Width (Type R)  
 -----  
 Range: 10.0 NS to 1.00 S.....CKW....

TITLE COMMAND

Clock Period (Type SP)  
 -----  
 (see Type SP).....CKP....

Trigger Arm Slope (Type S)  
 -----  
 Trigger Arm Active Slope : POSITIVE.....TAS 1  
 Trigger Arm Active Slope : NEGATIVE TAS 2  
 Trigger Arm Active Slope : DON'T CARE TAS 3

Trigger Arm Threshold (Type R)  
 -----  
 Range: - 10 V to + 10 V.....TAT....

Trigger Arm Impedance (Type S)  
 -----  
 Trigger Arm Impedance = 50 OHM.....TAI 1  
 Trigger Arm Impedance = 100 K OHM TAI 2

Trigger Word (Type F)  
 -----  
 Range and format depend on the channel.....TWD....  
 Configuration (see Type F)

Trigger Qualifier Level (Type S)  
 -----  
 Active Level: HIGH.....TQL 1  
 Active Level: LOW TQL 2  
 DON'T CARE TQL 3

Trigger Qualifier Threshold (Type R)  
 -----  
 Range: - 10 V to + 10 V.....TQT....

Trigger Qualifier Impedance (Type S)  
 -----  
 Impedance = 50 OHM.....TQI 1  
 Impedance = 100 K OHM TQI 2

Trigger Count (Type I)  
 -----  
 Range: 1 to 16.....TRC....

Allow Gaps in Count (Type S)  
 -----  
 YES.....AGC 1  
 NO AGC 2



## COMMANDS OF THE INPUT PAGE

TITLE	COMMAND
Connector (Type S)	
-----	
Connector 0 and 1 Single Threshold.....	C01 1
Connector 0 and 1 Dual Threshold	C01 2
Connector 2 and 3 Single Threshold	C23 1
Connector 2 and 3 Dual Threshold.....	C23 2
Connector 4 and 5 Single Threshold	C45 1
Connector 4 and 5 Dual Threshold	C45 2
Connector 6 and 7 Single Threshold	C67 1
Connector 6 and 7 Dual Threshold.....	C67 2
Define Labels (Type R)	
-----	
Label x Single.....	Six....
Range : - 10 V to + 10 V	
Label x Lower....	LOx....
Range: - 10 V to + 9.90 V	
Label x Upper.....	UPx....
Range: - 9.90 V to + 10.0 V	
x = Label A-F	
Upper minus Lower level force to 10 V	
Channel Configuration (Type SP)	
-----	
1. Clear all channels and add segment.....	CAS....
2. Add Segment	ADS....
(see type SP)	
Set Standard Configuration (Type E).....	SSC
-----	
Polarity (NORMAL/INVERSE) (Type F)	
-----	
Valid entries: N=NORMAL.....	POL....
I=INVERSE	
-=Skip Channel	
Channel Labeling (Type F 2.1)	
-----	
Valid Entries: A,B,C,D,E,F,-.....	LBL....
Example: LBL ADE BB-<CR LF>	

COMMANDS OF THE EXPECTED DATA PAGE

TITLE	COMMAND
Top Address (Type I) -----	
Range:.....	TAD....
+0000 to +1023 in OPR 1 & GLD 2 (OFF) or OPR 3	
+0000 to +0511 in OPR 1 & GLD 1 (ON)	
-1023 to -0000 in OPR 2 & GLD 2 (OFF)	
-0511 to -0000 in OPR 2 & GLD 1 (ON)	
Expected Data (Type F) -----	
See also tranfer start address (section: SPECIAL COMMANDS)	
1. Expected data without word mask (see Type F).....	DAT....
2. Expected data with word mask (see Type F)	DAM....
Clear and Set (Type E) -----	
1. Clear Data.....	CLD
2. Set Data	SED
3. Clear Bit Mask	CBM
4. Set Bit Mask.....	SBM
5. Clear Word Mask	CWM
6. Set Word Mask	SWM
Dump Received Data (Type E).....	DRD
-----	
Channel Edit (Type F) -----	
1. Clear channel data Valid entries: 1 or -.....	CCD....
Example: CCD 11-- --11 <CR LF>	
2. Set channel data Valid entries: 1 or -	SCD....
3. Clear channel mask Valid entries: 1 or -	CCM....
4. Set channel mask.....	SCM....
Valid entries: 1 or -	
5. Copy channel Valid entries: 1=Source 2=Destination - Skip channel	COC....
6. Exchange channels Valid entries: 1=Selected channels.....	XCH....
-=Skip channel	

TITLE	COMMANDS
Insert Line (Type I).....	.ILI....
-----	
Delete Line (Type I).....	.DLI....
-----	
Roll Down Memory (Type I).....	.RDO....
-----	
Range: 0 to 1023	
Roll Up Memory (Type I).....	.RUP....
-----	
Range: 0 to 1023	

COMMANDS OF THE MISCELLANEOUS PAGE

Store Actual Parameter Set (Type S)

-----	
Store Actual Set to SET 1.....	.STO 1
Store Actual Set to SET 2	.STO 2
Store Actual Set to SET 3	.STO 3

Recall Parameter Set (Type S)

-----	
Recall SET 1.....	.RCL 1
Recall SET 2	.RCL 2
Recall SET 3	.RCL 3
Recall Standard Set.....	.RCL 4

COMMANDS OF THE STATE LIST PAGE

Display Errors (Type S)

-----	
YES.....	.DSE 1
NO	.DSE 2

Top Address (see EXPECTED DATA PAGE)

-----

COMMANDS OF THE TIMING DIAGRAMS PAGE

TITLE	COMMAND
Cursor Address (Type I) -----	
Range:.....	.CAD...
+0000 to +1008 in OPR 1 & GLD 2 (OFF) or OPR 3	
+0000 to +0496 in OPR 1 & GLD 1 (ON)	
-1023 to -0015 in OPR 2 & GLD 2 (OFF)	
-0511 to -0015 in OPR 2 & GLD 1 (ON)	
Display Errors (Type S) -----	
YES.....	.DSE 1
NO	DSE 2
Horizontal Zoom (Type S) -----	
Zoom Factor = 1.....	.HOZ 1
Zoom Factor = 2	HOZ 2
Zoom Factor = 4	HOZ 3
Zoom Factor = 8	HOZ 4
Vertical Zoom (Type S) -----	
Zoom Factor = 1.....	.VEZ 1
Zoom Factor = 2	VEZ 2
Vertical Window (Type I) (Display Window).....	.DSW....
-----	
The integer number following the "DSW" statement marks the right bottom of the vertical window. The range depends on the channel configuration Min.: =0; Maximum: 0 to 40	

COMMANDS OF THE ERROR MAP PAGE

TITLE	COMMAND
Next Error (Type E).....	.NXE
-----	
Previous Error (Type E).....	.PRE
-----	
Error Count (Type S) -----	
Error Count ON.....	.CTE 1
Error Count OFF	CTE 2

Display Glitches (Type S)

```

-----
YES.. . . . .DSG 1
NO . . . . .DSG 2

```

OPERATION COMMANDS

```

RUN (Type E).....RUN
---
STOP (Type E).....STP
----
SAMPLE (Type E).....SPL
-----

```

MENU SELECT COMMANDS

TITLE	COMMAND
Select Page (Type S)	
-----	
CONTROL PAGE.....	PAG 1
INPUT PAGE	PAG 2
EXPECTED DATA PAGE.....	PAG 3
MISCELLANEOUS PAGE	PAG 4
STATE LIST PAGE.....	PAG 5
TIMING DIAGRAMS PAGE	PAG 6
ERROR MAP PAGE.....	PAG 7

Select Report (Type S)

```

-----
Same as page, but will not affect th softkeys.....REP 1-8
after return to LOCAL

```

REP 8 is the REMOTE MESSAGE Report (-PAGE).  
 Only REP 8 (not PAGE 8 or KEY 8) is allowed because  
 no softkeys are available for this page.

Select Softkeys (Type S)

```

-----
Same as Page 3, but will only affect softkeys after
returning to LOCAL

```

Model 8182A

## UNIVERSAL COMMANDS

Group Execute Trigger (GET); Trigger <Device Select Code>  
Same as RUN, but preferred, because synchronize  
buffer

Selected Device Clear (SDC); Clear <Device Select Code>  
Same as STOP, but preferred, because synchronize  
buffer

Device Clear (DCL) ; Clear <Interface Select Code>  
Same as STOP, but preferred, because synchronize  
buffer

Go to LOCAL (GTL) ; LOCAL <Device Select Code>

Local Lockout (LLO) ; Local Lockout <Interface Select Code>

Serial Poll Enable (SPE)

Serial Poll Disable (SPD)

## HP-IB TRANSFER

TITLE	COMMAND
-------	---------

Mask Status Byte of the HPIB (Type I)	
-----	
Range: 0 to 63; Default 63.....	MSK.....
(see page 3-42)	
Default forced at: Power on and HPIB address switch change	
Set Buffer Synchronize Character (Type I)	
-----	
Range: 0 to 255; Default 13 (=CR).....	SYN.....
Default forced at: power on and HPIB address switch change	

```

20  OUTPUT 701;"SYN 33"
21  !SYN 33: THIS ALLOWS DEFINITION OF A SYNC
22  !CHARACTER, IN THIS CASE 33, WHICH IS THE
23  !DECIMAL EQUIVALENT OF ASCII "!". THE RESULT
24  !IS THAT THE ANALYZER WILL LOCK THE
25  !CONTROLLER VIA HP-IB UNTIL IT HAS EXECUTED
26  !THE RECEIVED DATA IN ITS BUFFER. IMAGINE
27  !THE FOLLOWING OUTPUT COMMAND WHICH REQUIRES
28  !SEVERAL SECONDS FOR THE 8182A TO PROCESS.THE
29  !PROGRAM IS STOPPED FOR THIS TIME IF THE
30  !DEFINED SYNC CHARACTER, IN THIS CASE
31  !"!",OCCURS AT THE END OF THE STRING. THE
32  !DEFAULT SYNC CHARACTER IS 13, WHICH
33  !IS CR IN ASCII.
35  OUTPUT 701;"RUP 1000 RDO 1000 RUP 1000 RDO 1000 !"

```

SPECIAL COMMANDS

TITLE COMMAND

Transfer Start Address (Type I)

-----

Range:.....TSA....  
 +0000 to +1023 in OPR 1 & GLD 2 (OFF) and OPR 3  
 +0000 to +0511 in OPR 1 & GLD 1 (ON)  
 -1023 to -0000 in OPR 2 & GLD 2 (OFF)  
 -0511 to -0000 in OPR 2 & GLD 1 (ON)

Default value is TSA DISABLED, so this address must be set the first time the 8182A is commanded to talk in TALK 4,5,6 or 7, or if the Expected Data is altered using the DAT and DAM commands. The default value is forced at: power on, HP-IB address switch change, Recall Setx, OPR or GLD change.

If TSA is disabled:TALK 4,5,6 and 7 return empty string (<CR LF>).

If TSA is enabled: The TSA is incremented within allowed range if you enter a string in TALK 4, TALK 5,TALK 6 or TALK 7; or if you output a string to alter the Expected Data (commands DAT and DAM).

after TLK 4: TSA <-- (TSA+1) Modulo Range  
 after TLK 5: TSA <-- (TSA+1) Modulo Range  
 after TLK 6: TSA <-- (TSA+1) Modulo Range  
 after TLK 7: TSA <-- [(TSA-TSA modulo 64)+63]  
 Modulo Range

after DAT or DAM: TSA <-- (TSA+1)

TITLE COMMAND

Select Line to Display (Type I).....LIN....

-----

Selects the line in which the string entered by the "DSP" command will be displayed, and selects the line which will be output from the 8182A in Talk Mode 3 (Display-Dump).

Range: 1 to 26  
 Incremented by 1 after entering a string in a calculator in Talk Mode 3 or after sending a string to the REMOTE MESSAGE PAGE by the DSP command.  
 Reset to 1 after power on.

Transfer Parameter Set (Type SP).....SE....

-----

The current 8182A parameter set can be transferred over the HP-IB to a mass storage device using the TLK 2 command.This set can then be restored to one of 3 parameter set locations in the 8182A memory using the SE command.A more detailed description of this command is given on page 3-34.

## SECTION 4

### PERFORMANCE TESTS

#### 4-1 INTRODUCTION

4-2 The test procedures detailed in this section are for electrical performance of HP8182A unit using the instrument specifications of Table 1-2 as performance standards. Access to the interior of the instrument is not necessary for any of the following tests.

#### 4-3 EQUIPMENT REQUIRED

4-4 Equipment necessary for performance testing is listed in Table 1-1, Recommended Test Equipment. Alternative test equipment may be substituted for recommended models, provided that it satisfies the critical specifications given in the table.

#### 4-5 TEST RECORD

4-6 When carrying out the performance tests, a tabulated record of all the tested specifications and their acceptable limits should be maintained by the operator.

Test results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

#### 4-7 PERFORMANCE TESTS

4-8 During any performance test, all shields and connecting hardware must be in place. All tests are designed to verify the published specifications. It is recommended that tests be performed in the sequence given, and that all data be recorded on the test record provided at the end of the test procedures.

4-9 Each test is arranged in the order that its specification appears in Table 1-2. Note that the instrument should be given a 30 minute warm-up period before the commencement of any of the following tests.

PERFORMANCE TEST

TRIGGER WORD AND OPERATING MODES TEST

DESCRIPTION

The Data Generator HP-Model 8018A is used to generate the trigger word (bit) for two 8182A data channels. The error display indicates the trigger word position. Because of the cleared memory, the trigger word appears as error. When selecting the Trigger Event Start Compare Mode, the Trigger Delay is set to 0001. This causes the trigger word to be displayed in address 1023.

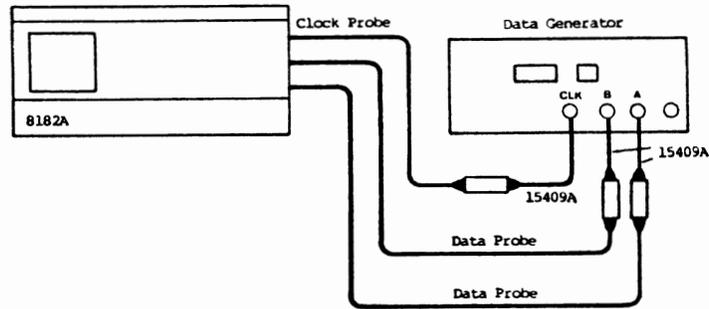


Figure 4-1 Operating Mode Test Setup

EQUIPMENT

Data Generator	HP 8018A
Plug-on BNC Adapter(3ea)	HP 15409A
Clock Probe Assy.	HP 15406A
Data Probe Assy.	HP 15407A

Set 8018A to.

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int.Clock	Amplitude	2.5V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm 1.

1. Clear both 8018A Data Channels by selecting the channel and pressing the toggle switch to Channel Clear.
2. Select Word Address 01 and load bit 1 to high in channel A and channel B.
3. Program 8182A STANDARD SET (PAGES > Miscellaneous > Recall > Standard Set > Execute)
4. CLEAR WORD MASK; CLEAR DATA  
(PAGES > Expected Data > Edit > Clear & Set > Clr Word Mask > Execute > Clr Data > Execute)
5. CLOCK DELAY 5 ns (PAGES > Control > Clock > Clock Delay > 5 > Nanosec)
6. AUTOARMING DELAY 1s (PAGES > Control > Autoarming > Delay 1s)
7. ERROR MAP; TRIGGER WORD IN SOFTKEY AREA (PAGES > Error Map > SOFTKEYS > Control > Trigger > Trigger Word)
8. Connect Equipment as shown in figure 4-1 and press RUN.

#### **TRIGGER START ANALYSIS TEST**

With trigger word set to X (don't care) one sporadic error should be displayed in the ERROR MAP.

9. Set trigger word for both connected data channels to 1.

The ERROR MAP should display only the trigger word in address 0000 as an error.

10. Set trigger word for one data channel to 0.

The 8182A should switch to ARMED (no trigger recognition).

11. Set trigger word back to 1 and the 8182A should trigger again.
12. Set the trigger word for the second channel to 0 and 1 and check trigger word recognition as described in steps 8 to 10.

**TRIGGER STOP ANALYSIS TEST**

13. Program 8182A TRIGGER STOP ANALYSIS  
(PAGES > Control > Operatg Mode > Trg Stop Anal)

14. ERROR MAP; TRIGGER WORD IN THE SOFTKEY AREA.  
(PAGES > Error Map > SOFTKEYS > Control > Trigger > Trigger Word)

With trigger word 1 for both connected data channels, the error display should stop always at address - 0000 (the trigger word in address - 0000 is as error indicated).

15. Set the trigger word for one connected channel to 0

The 8182A should stay in ACTIVE (no trigger)

16. Set the trigger word back to 1

The 8182A should trigger again.

17. Set the trigger word for the second connected data channel to 0 and 1 and check trigger word recognition as described in steps 14 to 16.

**TRIGGER EVENT START COMPARE TEST**

18. Program 8182A to TRIGGER EVENT START COMPARE  
(PAGES > Control > Operatg Mode > Trg Strt Comp > Execute)

19. ERROR MAP (PAGES > Error Map)

The error display should show the trigger word indicated as error in address 1023 (caused by trigger delay 0001) and errors in the channel marking display for both connected data channels.

20. Program TRIGGER START ANALYSIS and TRIGGER DELAY 0  
(PAGES > Control > Operatg Mode > Trg Strt Anal > Exit > Trigger > Trg Delay > 0 > Enter Number)

21. Repeat the procedure starting with step 5 for the remaining data channel pairs.

PERFORMANCE TEST

TRIGGER DELAY / STOP DELAY TEST

DESCRIPTION

This test can be performed with each available channel to check the Trigger Delay and Stop Delay Function. The data generator is used to generate the trigger word. The trigger word for not used data channels must be set to don't care (X).

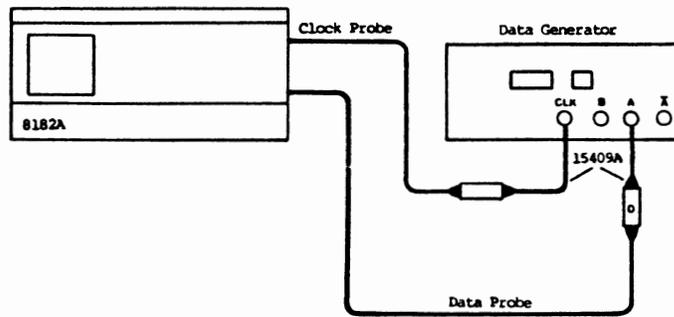


Figure 4-2 Trigger/Stop Delay Test Setup

EQUIPMENT

Data Generator	HP 8018A
Plug-on BNC Adapter (2ea)	HP 15409A
Clock Probe Assy.	HP 15406A
Data Probe Assy.	HP 15407A

Set 8018A to :

Bit Rate	50 MHz	Data Stream Length	1024
Clock Mode	Int. Clock	Amplitude (A)	2.5 V
Cycle Mode	Auto	Serializer	2x 1024
Row Address	1-16	Format	NRZ
Data Mode		Zs	50 Ohm

1. Clear 8018A channel A data by selecting channel A and pressing the toggle switch to Channel Clear position.
2. Select Word Address 01 and Load bit 1 to high.
3. Program 8182A: STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
4. CLEAR WORD MASK; CLEAR DATA  
(PAGES > Expected Data > Edit > Clear & Set > Clr Word Mask > Execute > Clr Data > Execute)
5. CLOCK DELAY 5ns  
(PAGES > Control > Clock > Clock Delay > 5 > Nanosec)
6. AUTOARMING DELAY 1s  
(PAGES > Control > Autoarming > Delay 1s)
7. Connect equipment as shown in figure 4-2 and press RUN.
8. TRIGGER WORD to 1 for connected data probe (all other channels X)  
(PAGES > Control > Trigger > Trigger Word > -> 1)
9. ERROR MAP; TRIGGER DELAY IN SOFTKEY AREA  
(PAGES > Error Map > SOFTKEYS > Control > Trigger > Trig Delay)

#### TRIGGER DELAY TEST

10. Increase trigger delay by pressing the increment softkey and check that the displayed error moves from address 1023 (for Trg Delay 1) backwards with increasing delay setting.
11. Set trigger delay back to 0000.

#### STOP DELAY TEST

12. Select STOP DELAY IN THE SOFTKEY AREA.  
(SOFTKEYS > Control > Stop > Stop Delay)
13. Vary the stop delay and check that the stop delay setting +1 is displayed as Stored Words in the upper right corner of the 8182A display.

## PERFORMANCE TEST

### SAMPLING POINT ACCURACY AND SKEW TEST

#### SPECIFICATION

Sampling point accuracy: +/- 5% of progr. clock delay +/- 1 ns

Channel skew <= 2 ns

#### DESCRIPTION

The test setup uses a pulse generator as clock and data source for the 8182A Data Analyzer. The data are delayed by a fixed 3 ns delay line. Setting the 8182A clock delay to 3 ns then corresponds to zero delay between clock and data. The clock can now be advanced by 3 ns and delayed with respect to the data to check when the incoming data signal is recognized as a high or a low level.

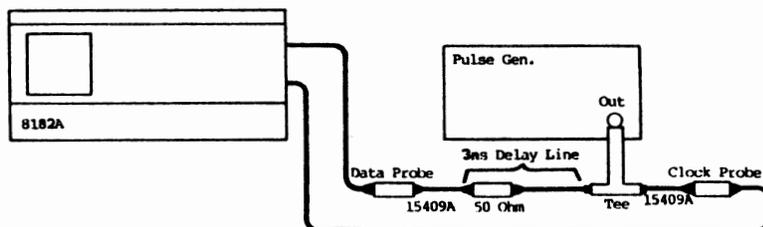


Figure 4-3 Skew Test Setup

#### EQUIPMENT

Pulse Generator  
 50 Ohm Feedthrough  
 BNC Tee  
 Plug-on BNC Adapter (2 ea)  
 Clock Probe Assy.  
 Data Probe Assy.  
 Delay Line (including 50 Ohm = 3 ns)

HP 8007B  
 HP 11048C  
 P.N.1250-0781  
 HP 15409A  
 HP 15406A  
 HP 15407A

1. Set Pulse Generator to:

Period 1 us

Pulse Width .5us

Leading Edge < 3 ns

Trailing Edge < 3 ns

Amplitude High Level + 2V into 50 Ohm

Low Level 0V

2. Program 8182A STANDARD SET

(PAGES > Miscellaneous > Recall > Standard Set > Execute)

3. CLOCK THRESHOLD + 1V

(PAGES > Controls > Clock > Clock Thres > 1 > Volt)

4. THRESHOLD LABEL A +1 V

(PAGES > Input > Threshold > 1 > Volt)

5. STOP DELAY 40

(PAGES > Control > Stop > Stop Delay > 40 > Enter Number)

6. AUTOARMING DELAY 0s

(PAGES > Control > Autoarming > Delay 0s)

7. TIMING DIAGRAM (PAGES > Timing Diagram)

8. Press SOFTKEYS > Control > Clock > Clock Delay > 3 > Nanosec.

9. Connect equipment as shown in figure 4-3 and press RUN. (Start with Connector 0 Channel 0)

10. Using the Increment softkey check that the displayed timing signal switches from low to high within 2 ns to 4 ns clock delay setting.

11. Program CLOCK SLOPE NEG

(Exit > Clock Slope > Neg Slope > Exit > Clock Delay)

12. Increment clock delay starting from 2 ns and check that the timing signal switches from high to low within 2 ns to 4 ns clock delay setting.

13. Repeat skew test for CLOCK SLOPE POS and CLOCK SLOPE NEG for the remaining channels as described in steps 10 to 12.

NOTE: When testing skew of connector 3 channel 0 upwards, change the vertical display window. (PAGES > Timing Diagr > Select Displ > Vertical Window > < [until the required channels are displayed])

Then press SOFTKEYS > Controls > Clock > Clock Delay.

## PERFORMANCE TEST

### CLOCK DELAY TEST

#### SPECIFICATION

+/- 5 % of progr. clock delay +/- 1 ns.

#### DESCRIPTION:

The test setup uses a pulse generator as external clock source. The clock delay is measured at the 8182A clock output referenced to 0.00 ns programmed clock delay. Ranges up to 10 ns are measured with an oscilloscope. A time interval counter is used for the higher ranges. Time offset of the counter is programmed to compensate internal delays and cable delays, instead of adding these delays manually.

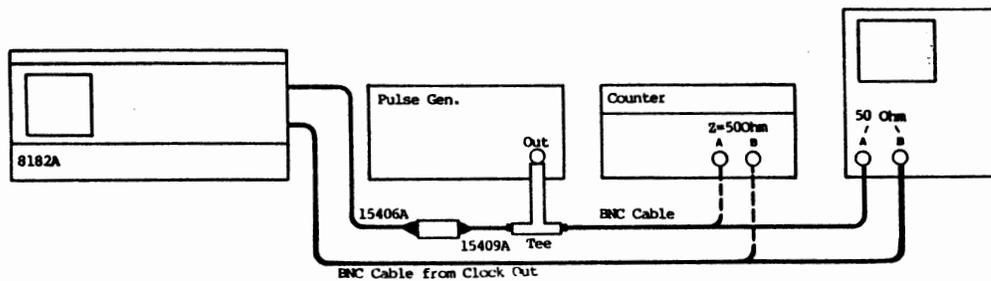


Figure 4-4 Clock Delay Test Setup

#### EQUIPMENT:

Pulse Generator	HP 8007B
Universal Counter	HP 5335A
Oscilloscope	HP 1725A
Plug-on BNC Adapter	HP 15409A
Clock Probe Assy.	HP 15406A
BNC Tee	P.N.1250-0781
BNC Cable Assy	HP 11170C
Time Mark Generator	

#### Set Pulse Generator to:

Period	approx. 110 us
Pulse Width	approx. 1.5 us
Transition Time	2 ns
Amplitude	2.5 V
(into 50 Ohm)	
Offset	OFF

#### Set Counter to:

Trigger Level A and B	+1.2 V
Time A -> B	
Statistics	MEAN
Gate Mode	MIN
Channel A and B Z	50 Ohm

1. Program 8182A STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
2. CLOCK THRESHOLD + 1.2 V; CLOCK DELAY 0.00 ns.  
(PAGES > Control > Clock > Clock Thres > 1.2 > Volt > Exit > Clock Delay > 0 > Nanosec)
3. Using the time mark generator check first the oscilloscope time base accuracy in the 10 ns/DIV x 10 range and take timebase error into account.
4. Connect equipment as shown in figure 4-4 trigger oscilloscope to channel A and position the 8182A clock output signal exactly on the left horizontal graticule line.
5. Using the increment softkey step through delay range 0 ns to 10 ns in 100 ps steps and check accuracy.
6. Program 8182A clock delay to 0.00 ns and connect counter as shown in figure 4-4.
7. Program counter time offset so that counter displays 0 ns when 8182A Clock Delay is set to 0.0 ns.  
  
 Example for 5335A: Counter display without offset is 41.6 Exponent -9 s.  
 Press: OFFSET > CHS > 41.6 > EEX > CHS > 9 > ENTER
8. Program 8182A clock delay as listed and check accuracy for +/- 5 % +/- 1 ns.

8182A Clock Delay	Min.	Max.
21.9 ns	19.8 ns	24.0 ns
22.0 ns	19.9 ns	24.1 ns
70.0 ns	65.5 ns	74.5 ns
117 ns	110.2 ns	123.9 ns
118 ns	111.1 ns	124.9 ns
500 ns	474.0 ns	526.0 ns
1.01 us	0.96 us	1.06 us
1.02 us	0.97 us	1.07 us
5.00 us	4.75 us	5.25 us
9.99 us	9.49 us	10.49 us
10.0 us	9.50 us	10.50 us
50.0 us	47.5 us	52.5 us
99.9 us	94.9 us	104.9 us

## PERFORMANCE TEST

### COMPARE WINDOW WIDTH TEST

#### SPECIFICATION

Compare window width accuracy: +/- 5% of progr. value +/- 1 ns

#### DESCRIPTION

The programmable clock width in TRIGGER EVENT START COMPARE mode is measured at 50% amplitude of the 8182A clock output signal. The 10 ns width range and increasing 100ps steps up to 31.9 ns are tested with the oscilloscope. A universal counter is used to measure the accuracy in higher ranges.

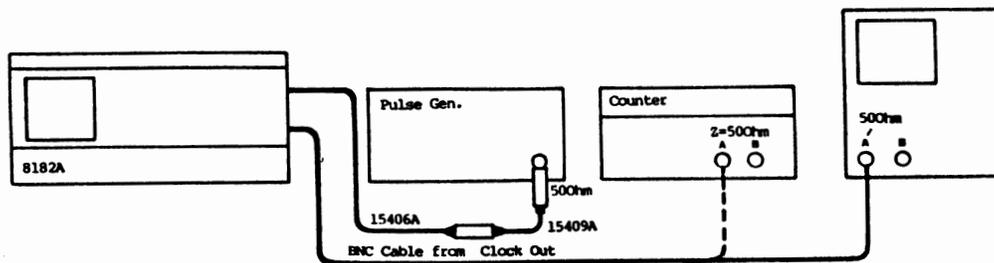


Figure 4-5 Clock Width Test Setup

#### EQUIPMENT

Pulse Generator	HP 8007B
Oscilloscope	HP 1725A
Universal Counter	HP 5335A
Clock Probe Assy.	HP 15406A
Plug-on BNC Adapter	HP 15409A
50 Ohm Feedthrough	HP 11048C
BNC Cable Assembly	HP 11170C
Time Mark Generator	

#### Set Pulse Generator to:

Period	approx. 1 us
Pulse Width	approx. .5 us
Transition Time	2 ns
Amplitude (into 50 Ohm)	+2.5 V
Offset	OFF

#### Set Counter to:

Trigger Level A and B	+ 1.2 V
Time A -> B	
Gate Mode	MIN
Channel A and B Z	=50 Ohm
Common A	
Slope Cha. B	\_

1. Program 8182A STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
2. TRIGGER EVENT START COMPARE  
(PAGES > Controls > Operatg Mode > Trg Strt Comp > Execute)
3. CLOCK WIDTH 10 ns  
(PAGES > Control > Clock > Clock Width)
4. Using the Time Mark Generator check the oscilloscope timebase accuracy at 10 ns/DIV x 10 and 10 ns/DIV range. Note error and take timebase error into account.
5. Connect equipment as shown in figure 4-5 (Clock Out to oscilloscope) and measure clock output pulse width at 50% of amplitude. Width min 8.5 ns max. 11.5 ns.
6. Set the trailing edge of the clock pulse to the left horizontal graticule line and check step linearity when incrementing the width to 20 ns.
7. Check clock width at following settings:

Width Setting	Min.	Max.
29.9 ns	27.4 ns	32.4 ns
30.0 ns	27.5 ns	32.5 ns
99.0 ns	93.0 ns	105 ns
100 ns	94.0 ns	106 ns

8. Change PULSE GENERATOR PERIOD to 120 ms
9. Connect 8182A clock output to counter channel A and check:

Width Setting	Min.	Max.
300 ns	284 ns	316 ns
999 ns	948 ns	1050 ns
100 ms	95.0 ms	105 ms

## PERFORMANCE TEST

### CLOCK THRESHOLD AND HYSTERESIS TEST

#### SPECIFICATION

Threshold accuracy:  $\pm 2\%$  of. progr. value  $\pm 10$  mV  
 Hysteresis  $< \pm 50$  mV

#### DESCRIPTION

The pulse generator is adjusted to generate a triangle waveform with a period of approx. 1 ms. When the 8182A clock threshold is reached a clock pulse is generated by the 8182A and available at the 8182A Clock Output. This clock pulse starts (triggers) the trace on the oscilloscope. The vertical offset from zero Volts corresponds exactly to the level where the 8182A recognizes a clock.

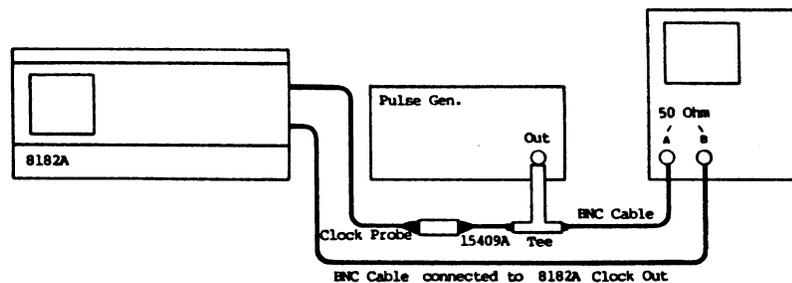


Figure 4-6 Clock Threshold and Hysteresis Test Setup

#### EQUIPMENT

Pulse Generator	HP 8007B
Oscilloscope	HP 1725A
BNC to BNC Cable Assy (2ea)	HP 11170C
BNC Tee	P.N.1250-0781
Plug-on BNC Adapter	HP 15409A
Clock Probe Assy.	HP 15406A

#### Set Pulse Generator to :

Period	1 ms
Width	.5ms
Transition Time	5 us to 250 us
Amplitude	4 Volt pp into 50 Ohm
Offset	ON

1. Adjust leading edge and trailing edge for a triangle waveform on the oscilloscope.
2. Using the pulse generator offset vernier, set the waveform symmetrical to 0 V graticule line.

### HYSTERESIS TEST

3. Program 8182A to STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
4. CLOCK SLOPE POS; THRESHOLD 0V.  
(PAGES > Control > Clock > Clock Slope > Pos Slope > Exit > Clock Thres > 0 > Volt)
5. Connect equipment as shown in figure 4-6, set oscilloscope timebase to .5 us and trigger with channel B (8182A clock out)
6. Set channel A to .02V/DIV, Input to GND and ensure that the baseline is exactly at center graticule line.
7. Switch oscilloscope input (A) to 50 Ohm.

The trace should start at less than +50 mV vertical deflection from center graticule.

8. Change to CLOCK SLOPE NEG (Exit > Clock Slope > Neg Slope)

The trace should start at less than -50 mV from center graticule.

### THRESHOLD TEST

9. Program THRESHOLD -1.4V (Exit > Clock Thres > -1.4 Volt)
10. Set oscilloscope channel A input to GND and .2V/DIV.
11. Position the baseline exactly on the upper graticule line and switch input A to 50 Ohm.

The trace should start between -1.49V and -1.31V.

12. Program POS SLOPE and THRESHOLD +1.4V  
(Exit > Clock Slope > Pos Slope > Exit > Clock Thres > 1.4 > Volt)

13. Ground channel A input and position the baseline exactly on the lower vertical graticule line and switch input back to 50 Ohm.

The trace should start between + 1.31V and +1.49V

## PERFORMANCE TEST

### DATA THRESHOLD LEVEL ACCURACY AND LINEARITY TEST

#### SPECIFICATION

Single threshold accuracy:  $\pm 2\%$  of progr. value  $\pm 10$  mV

Level detection accuracy 50 ms after input signal transition: actual threshold  $\pm 15$  mV.

#### DESCRIPTION

This test is used to measure the high and low level detection voltage to determine the actual threshold voltage. The check-sequence is selected to ensure that all data lines used for level programming are working properly. To get a better solution when adjusting the power supply, two 20 dB attenuators are used to reduce the output voltage. 20 W attenuators are recommended to avoid damage. The capacitor across the DVM input suppresses spikes generated by the DVM.

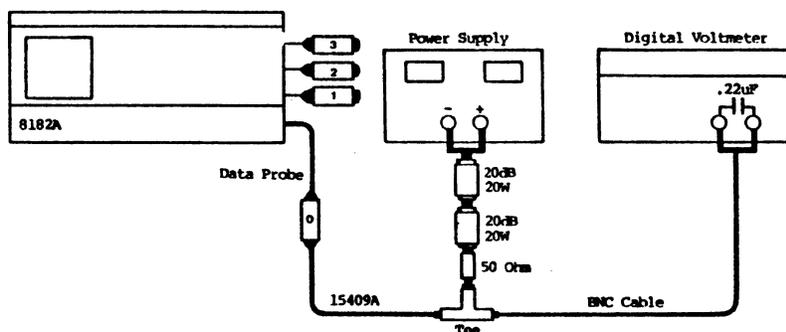


Figure 4-7 Linearity Test Setup

#### EQUIPMENT

Power Supply  
 Digital Voltmeter  
 Cable Assembly (dual banana-BNC (m) 30 cm)  
 Plug-on BNC Adapter  
 Data Probe Assy.  
 BNC - Tee  
 BNC (f) to dual banana Plug  
 50 Ohm Feedthrough  
 Capacitor  
 2 x Attenuator 20 dB (20W)

HP 6002A  
 HP 3456A  
 HP 11035A  
 HP 15409A  
 HP 15407A  
 P.N.1250-0781  
 P.N.1251-2277  
 HP 11048C  
 .22 uF

## 1. Program 8182A STANDARD SET

(PAGES &gt; Miscellaneous &gt; Recall &gt; Standard Set &gt; Execute)

## 2. CLOCK SOURCE INTERNAL

(PAGES &gt; Control &gt; Clock &gt; Clock Source &gt; Internal)

## 3. AUTOARMING DELAY 0s

(PAGES &gt; Control &gt; Autoarming &gt; Delay 0s)

## 4. STOP DELAY 40

(PAGES &gt; Control &gt; Stop &gt; Stop Delay &gt; 40 &gt; Enter Number)

## 5. CHANNEL CONFIGURATION CONNECTOR 0 CHANNEL 0 ONLY

(PAGES &gt; Input &gt; Chnl Config &gt; Delete Chnl [until only connector 0 channel 0 is displayed])

## 6. TIMING DIAGRAM; SINGLE THRESHOLD LABEL A IN SOFTKEY AREA

(PAGES &gt; Timing Diagr &gt; SOFTKEYS &gt; Input &gt; Threshold &gt; [Next Label if necessary])

## 7. SINGLE THRESHOLD LABEL A + 0.01 V

(.01 &gt; Volt)

CAUTION: Set power supply voltage to minimum. Do not overload attenuators.

8. Connect equipment as shown in figure 4-7 and press RUN.

9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading. [Voltage A]

10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading. [Voltage B]

The Level Detection Accuracy =  $V_A - V_B$  must be  $< 30 \text{ mV}$ The Actual Threshold =  $(V_A + V_B)/2$  must be within  $\pm 2\%$  of programmed value  $\pm 10 \text{ mV}$ 

EXAMPLE: Programmed Threshold = +0.01 V

High Level Voltage (measured in step 9) = +0.012 V

Low Level Voltage (measured in step 10) = 0.009 V

Level detection accuracy =  $0.012 \text{ V} - 0.009 \text{ V} = 0.003 \text{ V}$  Limit:  $< .03 \text{ V}$ Single threshold accuracy =  $(0.012 \text{ V} + 0.009 \text{ V})/2 = 0.011 \text{ V}$  Limit:  $.00 \text{ V}$  to  $.02 \text{ V}$

13. Program following thresholds and check for specifications as described in steps 10 to 12.

8182A Threshold	High Level VA	Low Level VB	Delta V < .03	Threshold Accuracy		
				Min.	Actual	Max.
0.01 V	.....V	.....V	.....V	0.000V	.....	0.020V
0.02 V	.....V	.....V	.....V	0.010V	.....	0.030V
0.04 V	.....V	.....V	.....V	0.020V	.....	0.050V
0.08 V	.....V	.....V	.....V	0.068V	.....	0.092V
0.16 V	.....V	.....V	.....V	0.147V	.....	0.173V

Remove one 20 dB attenuator

0.32 V	.....V	.....V	.....V	0.304V	.....	0.336V
0.64 V	.....V	.....V	.....V	0.617V	.....	0.663V
1.28 V	.....V	.....V	.....V	1.244V	.....	1.316V
2.56 V	.....V	.....V	.....V	2.499V	.....	2.621V

Both 20 dB attenuators and 50 Ohm feedthrough removed

5.12 V	.....V	.....V	.....V	5.008V	.....	5.232V
--------	--------	--------	--------	--------	-------	--------

## PERFORMANCE TEST

### DATA OFFSET AND GAIN TEST

#### SPECIFICATION

Single threshold accuracy:  $\pm 2\%$  of progr. value  $\pm 10$  mV

Level detection accuracy 50 ms after input signal transition: actual threshold  $\pm 15$  mV.

#### DESCRIPTION

To determine the actual threshold and to check the threshold accuracy, the hysteresis between high and low level detection must be measured first. The actual threshold is midway between high and low level detection voltage. This value must be within the specifications for single threshold.

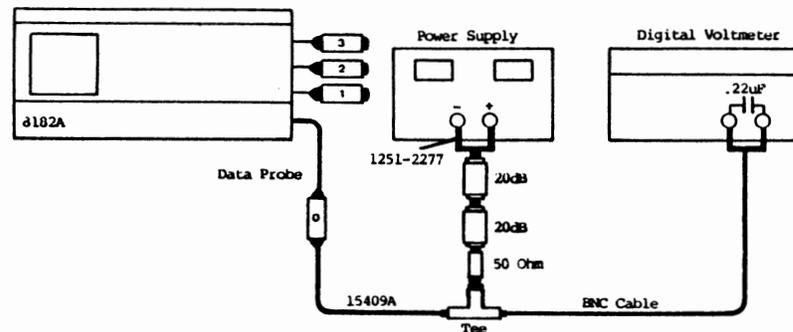


Figure 4-8 Offset Test Setup

#### EQUIPMENT

Power Supply  
 Digital Voltmeter  
 Cable Assembly (dual banana-BNC (m) 30 cm)  
 Plug-on BNC Adapter  
 Data Probe Assy.  
 BNC - Tee  
 BNC (f) to dual banana plug  
 50 Ohm Feedthrough  
 Capacitor  
 2 x Attenuator 20 dB

HP 6002A  
 HP 3456A  
 HP 11035A  
 HP 15409A  
 HP 15407A  
 P.N.1250-0781  
 P.N.1251-2277  
 HP 11048C  
 .22 uF

**POSITIVE OFFSET TEST****1. Program 8182A STANDARD SET**

(PAGES &gt; Miscellaneous &gt; Recall &gt; Standard Set &gt; Execute)

**2. CLOCK SOURCE INTERNAL**

(PAGES &gt; Control &gt; Clock &gt; Clock Source &gt; Internal)

**3. AUTOARMING DELAY 0s**

(PAGES &gt; Control &gt; Autoarming &gt; Delay 0s)

**4. STOP DELAY 40**

(PAGES &gt; Control &gt; Stop &gt; Stop Delay &gt; 40 &gt; Enter Number)

**5. CHANNEL CONFIGURATION CONNECTOR 0 CHANNEL 0 ONLY**

(PAGES &gt; Input &gt; Chnl Config &gt; Delete Chnl [until only connector 0 channel 0 is displayed])

**CAUTION:** Set power supply voltage to minimum. Do not overload attenuators.**6. SINGLE THRESHOLD LABEL A + 0.05 V**

(PAGES &gt; Input &gt; Threshold &gt; Next Label [if necessary] &gt; .05 &gt; Volt)

**7. TIMING DIAGRAM; CHANNEL CONFIGURATION IN SOFTKEY AREA**

(PAGES &gt; Timing Diagr &gt; SOFTKEYS &gt; Input &gt; Chnl Config.)

**8. Connect equipment as shown in figure 4-8 and press RUN.****9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading. [Voltage A]****10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading. [Voltage B]**The Level Detection Accuracy =  $V_A - V_B$  must be  $< 30 \text{ mV}$ The Actual Threshold =  $(V_A + V_B)/2$  must be within  $\pm 2\%$  of progr.value  $\pm 10 \text{ mV}$ **EXAMPLE:** Programmed Threshold = 0.05 V

High Level Voltage (measured in step 9) = 0.056 V

Low Level Voltage (measured in step 10) = 0.043 V

Level detection accuracy =  $0.056 \text{ V} - 0.043 \text{ V} = 0.013 \text{ V}$  Limit:  $< 0.03 \text{ V}$ Single thresh. accuracy =  $(0.056 \text{ V} + 0.043 \text{ V})/2 = 0.050 \text{ V}$  Limit: .039V to 0.061V**11. Select the connector and channel to be tested by pressing first the connector number and then the channel number on the data entry field. Connect in turn all data probes to the test setup and check for +50 mV  $\pm 10 \text{ mV}$  threshold accuracy.**

**NEGATIVE OFFSET TEST**

14. Change power supply polarity to neg. and program 8182A:
15. LABEL A SINGLE THRESHOLD -0.05 V (SOFTKEYS > Input > Threshold > -.05 > Volt)
16. CHANNEL CONFIGURATION (SOFTKEYS > Input > Chnl Config)
17. Proceed as described for POSITIVE OFFSET TEST and check all channels for - 50 mV +/- 10 mV threshold accuracy.

**GAIN TEST NEGATIVE**

18. Remove both 40 dB attenuators and the 50 Ohm feedthrough from the test setup and set the powersupply voltage to - 9.00 V reading on DVM.
19. Program INPUT STANDARD CONFIGURATION (PAGES > Input > Chnl Config > Std Config > Execute)
20. TIMING DIAGRAM;SINGLE THRESHOLD LABEL A IN SOFTKEY AREA (PAGES > Timing Diagr > SOFTKEYS > Input > Threshold)
21. Set the threshold to -8.81 V and check that the corresponding timing display is low. (-8.81 > Volt)
22. Set the threshold to -9.19 and when pressing the Volt softkey, the timing display should jump to high.
23. Repeat step 21 and 22 for all data channels.

**GAIN TEST POSITIVE**

24. Change power supply voltage to +9.00 V
25. Set the threshold to +8.81 V and check that the corresponding timing display is high. (8.81 > Volt)
26. Set the threshold to +9.19 and when pressing the Volt softkey,the timing display should jump to low.
27. Repeat step 25 and 26 for all data channels.

Note: When testing channels at connectors 3 to 7,move timing diagram up. (PAGES > Timing Diagr >Select Displ > Vert Window > <-- or --> [until required connectors are displayed] > SOFTKEYS > Input > Threshold)

## PERFORMANCE TEST

### QUALIFIER THRESHOLD AND IMPEDANCE TESTS

#### SPECIFICATION

Threshold accuracy:  $\pm 3\%$  of progr. value  $\pm 50\text{mV}$

#### DESCRIPTION

This test is used to measure the high and low level detection voltage (hysteresis) to determine the actual threshold voltage of the Qualifier Inputs (TTL setting). By measuring the voltage drop across the 20dB attenuator when switching the input to 50 Ohm proper input impedance selection can be verified.

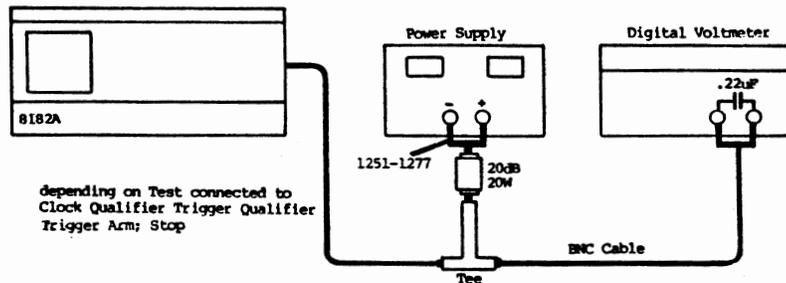


Figure 4-9 Threshold Test Setup

#### EQUIPMENT

Power Supply	HP 6002A
Digital Voltmeter	HP 3456A
Cable Assembly (dual banana-BBC (m) 30 cm)	HP 11035A
Cable Assembly BNC to BNC	HP 11170C
BNC - Tee	P.N. 1250-0781
BNC(f) to dual banana Plug	P.N. 1251-2277
Capacitor	.22 uF
Attenuator 20 dB 20W	

**CLOCK QUALIFIER THRESHOLD ACCURACY TEST**

1. Program 8182A STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
2. CLOCK SOURCE INTERNAL  
(PAGES > Control > Clock > Clock Source > Internal)
3. AUTOARMING Os (PAGES > Control > Autoarming > Delay Os)
4. CLOCK QUALIFIER HIGH LEVEL; THRESHOLD +1.4V  
(PAGES > Control > Clock > Clock Qual > Level > High Level > Exit > Threshold)
5. Connect equipment as shown in figure 4-9 and press RUN.
6. Increase power supply voltage slowly until a clock signal is just indicated in the upper left corner of the display and note DVM reading.
7. Decrease power supply voltage slowly until the clock indication just disappears and note DVM reading.
8. Change power supply polarity and program threshold to -1.40V.
9. Increase power supply voltage slowly until the clock indication just disappears and note DVM reading.
10. Decrease power supply voltage slowly until a clock signal is just indicated and note DVM reading

Result: The mean value should be between -1.31V and -1.49V.

**50 OHM IMPEDANCE TEST**

11. Set power supply voltage for -1.40V reading on the DVM.
12. Program CLOCK QUALIFIER INPUT IMPEDANCE 50 OHM  
(Exit > Impedance > 50 Ohm)

The DVM should show approx -0.7 V.

**TRIGGER QUALIFIER THRESHOLD ACCURACY TEST****1. Program 8182A STANDARD SET**

(PAGES > Miscellaneous > Recall > Standard Set > Execute)

**2. CLOCK SOURCE INTERNAL**

(PAGES > Control > Clock > Clock Source > Internal)

**3. AUTOARMING 0s (PAGES > Control > Autoarming > Delay 0s)****4. TRIGGER QUALIFIER HIGH LEVEL; THRESHOLD +1.4V (PAGES > Control > Trigger > Trg Qualifier > Level > High Level > Exit > Threshold)****5. Connect equipment as shown in figure 4-9 and press RUN**

6. Increase power supply voltage slowly until the status display in the upper right corner of the display jumps just from ARMED to IDLE (IDLE toggles) and note DVM reading.

7. Decrease power supply voltage slowly until the display just jumps to ARMED and note DVM reading.

Result: The mean value should be between +1.31V and +1.49V

**8. Change power supply polarity and program threshold to -1.40V.**

9. Increase power supply voltage slowly until the display just jumps from IDLE to ARMED and note DVM reading.

10. Decrease power supply voltage slowly until the display just jumps back to IDLE and note DVM reading.

Result: The mean value should be between -1.31V and -1.49V

**50 OHM IMPEDANCE TEST**

11. Set power supply voltage for -1.4 V reading on the DVM.

12. Program TRIGGER QUALIFIER INPUT IMPEDANCE 50 OHM (Exit > Impedance > 50 Ohm)

The DVM should show approx. - 0.7V.

**TRIGGER ARM THRESHOLD ACCURACY TEST**

1. Program 8182A STANDARD SET  
(PAGES > Miscellaneous > Recall > Standard Set > Execute)
2. CLOCK SOURCE INTERNAL ; CLOCK PERIOD 1 s  
(PAGES > Control > Clock > Clock Source > Internal > Exit > Clock Period > Increase [until 1 s is displayed])
3. STOP DELAY 0 (INTERNAL)  
(PAGES > Control > Stop > Stop Delay > 0 > Enter Number)
4. AUTOARMING DELAY 0s  
(PAGES > Control > Autoarming > Delay 0s)
5. TRIGGER ARM POS SLOPE (threshold +1.40)  
(PAGES > Control > Trigger > Trigger Arm > Slope > Pos Slope)
6. Connect equipment as shown in figure 4-9 and press RUN.
7. Increase power supply voltage slowly until the 8182A switches from ARMED to ACTIVE (upper right corner of display). Note: Continuous toggling may be caused by noise when the threshold level is just reached.

The DVM reading should be between +1.31 V and +1.49 V.

8. Program NEG SLOPE. THRESHOLD -1.4 V  
(Neg Slope > Exit > Threshold > -1.4 > Volt)
9. Change power supply polarity, press RUN and increase power supply voltage slowly again until the 8182A switches from ARMED to ACTIVE (see Note)

The DVM reading should be between -1.31 V and -1.49 V

**50 OHM IMPEDANCE TEST**

10. Set power supply voltage for -1.40 V reading on the DVM.
11. Program TRIGGER ARM INPUT IMPEDANCE 50 OHM  
(Exit > Impedance > 50 Ohm)

The DVM should show approx. -0.7 V.

**EXTERNAL STOP THRESHOLD ACCURACY TEST****1. Program 8182A STANDARD SET**

(PAGES > Miscellaneous > Recall > Standard Set > Execute )

**2. CLOCK SOURCE INTERNAL; CLOCK PERIOD 100ms**

(PAGES > Control > Clock > Clock Source > Internal > Exit > Clock Period > Increase [until 1 s is displayed])

**3. STOP DELAY 0 (INTERNAL)**

(PAGES > Control > Stop > Stop Delay > 0 > Enter Number)

**4. AUTO ARMING DELAY 1s (PAGES > Control > Autoarming > Delay 1s)****5. EXTERNAL STOP POS SLOPE (threshold + 1.40V)**

(PAGES > Control > Stop > Stop Slope > Pos Slope)

**6. Connect equipment as shown in figure 4-9 and press RUN.****7. Increase power supply voltage slowly until the 8182A switches from ACTIVE to IDLE (upper right corner of display).**

Note: Continuous toggling may be caused by noise when the threshold level is just reached.

The DVM reading should be between +1.31V and 1.49V.

**8. Program NEG SLOPE; THRESHOLD -1.4 V (Neg Slope > Exit > Stop Thres > -1.4 > Volt)****9. Change power supply polarity, press RUN and increase power supply voltage again until the 8182A switches from ACTIVE to IDLE. (see Note)**

The DVM reading should be between -1.3 1V and 1.49 V.

**50 OHM IMPEDANCE TEST****10. Set power supply voltage for -1.40V reading on the DVM.****11. Program EXT. STOP INPUT IMPEDANCE 50 OHM**

(Exit > Stop Imp > 50 Ohm)

The DVM should show approx -0.7V.

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Arranged Alphabetically by Country



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 Telex: 32375  
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 Tel: 0732 51585  
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*Telex: 84419*  
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*P.O. Box 648*  
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CH

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F-33700 MERIGNAC  
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CH,E,MS

Hewlett-Packard France  
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CH

Hewlett-Packard France  
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Z.A.C. de Bois Briand  
F-44085 NANTES Cedex  
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Hewlett-Packard France  
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F-91947 Les Ulis Cédex ORSAY  
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Hewlett-Packard France  
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Telex: 947234 CH,CS,E

Hewlett-Packard Ltd.  
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Telex: 66678 HEWPA HX  
Cable: HEWPACK HONG KONG  
E,CH,CS,P

**CET Ltd.**  
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199-203 Hennessy Rd.  
**Wanchia, HONG KONG**  
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Telex: 85148 CET HX  
CM

**Schmidt & Co. (Hong Kong) Ltd.**  
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Connaught Road, C.  
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Telex: 74766 SCHMX HX  
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Hafnarvoll-Tryggvagotu  
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**Blue Star Ltd.**  
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Prabhadevi  
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Tel: 422-3101  
Telex: 011-3751  
Cable: BLUESTAR  
A,M  
**Blue Star Ltd.**  
Sahas  
414/2 Vir Savarkar Marg  
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**BOMBAY 400 025**  
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Telex: 011-4093  
Cable: FROSTBLUE  
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**Blue Star Ltd.**  
Kalyan, 19 Vishwas Colony  
Alkapuri, **BORODA, 390 005**  
Tel: 65235  
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A  
**Blue Star Ltd.**  
7 Hare Street  
**CALCUTTA 700 001**  
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Telex: 021-7655  
Cable: BLUESTAR  
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**Blue Star Ltd.**  
133 Kodambakkam High Road  
**MADRAS 600 034**  
Tel: 82057  
Telex: 041-379  
Cable: BLUESTAR  
A,M

**Blue Star Ltd.**  
Bhandari House, 7th/8th Floors  
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**NEW DELHI 110 024**  
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Telex: 031-2463  
Cable: BLUESTAR  
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**Blue Star Ltd.**  
15/16-C Wellesley Rd.  
**PUNE 411 011**  
Tel: 22775  
Cable: BLUE STAR  
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**Blue Star Ltd.**  
2-2-47/1108 Bolarum Rd.  
**SECUNDERABAD 500 003**  
Tel: 72057  
Telex: 0155-459  
Cable: BLUEFROST  
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**Blue Star Ltd.**  
T.C. 7/603 Poornima  
Maruthankuzhi  
**TRIVANDRUM 695 013**  
Tel: 65799  
Telex: 0884-259  
Cable: BLUESTAR  
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**JAKARTA**  
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**BERCA Indonesia P.T.**  
P.O. Box 174/SBY.  
Jl. Kutei No. 11  
**SURABAYA**  
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Telex: 31146 BERSAL SB  
Cable: BERSAL-SURABAYA  
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### INDONESIA

**BERCA Indonesia P.T.**  
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Telex: 46748 BERSAL IA  
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Telex: 212-455 HEPAIRAQ IK  
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Telex: 25231 AB/PAKRD IL  
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*Motorola Israel Ltd.*  
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Hewlett-Packard Italiana S.p.A.  
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**KUMAMOTO-SHI,860**  
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CH,E

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Woluwedal  
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*P.O.Box 1917*  
*Kuching, SARAWAK*  
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Telex: MA 70904 PROMAL  
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**MRIEHEL**  
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Hewlett-Packard Mexicana, S.A. de  
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Tepepan, Xochimilco  
**MEXICO D.F. 16020**  
Tel: 676-4600  
Telex: 17-74-507 HEWPACK MEX  
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Effective November 1, 1982:  
Hewlett-Packard Mexicana, S.A. de  
C.V.  
Ejercito Nacional #570  
Colonia Granada  
11560 **MEXICO, D.F.**  
CH\*\*

Hewlett-Packard Mexicana, S.A. de  
C.V.  
Rio Volga 600  
Pte. Colonia del Valle  
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Telex: 038-2410 HPMTY ME  
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Effective Nov. 1, 1982  
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Col. del Valle  
*Municipio de garza garcia*  
**MONTERREY, N.V.**

*ECISA*  
*Taihe 229, Piso 10*  
*Polanco MEXICO D.F. 11570*  
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Telex: 17-72755 ECE ME  
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*Gerep*  
*2 rue d'Agadir*  
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CH,CM,E,P

*Northrop Instruments & Systems*  
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A,M

*Northrop Instruments & Systems*  
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**NORTHERN IRELAND**

*Cardiac Services Company*  
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**OMAN**

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Telex: 3289 BROKER MB MUSCAT  
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## Arranged Alphabetically by Country

**Suhail & Saud Bahwan**  
P.O. Box 169  
**MUSCAT**  
Tel: 734 201-3  
Telex: 3274 BAHWAN MB

**PAKISTAN**  
**Mushko & Company Ltd.**  
1-B, Street 43  
Sector F-8/1  
**ISLAMABAD**  
Tel: 26875  
Cable: FEMUS Rawalpindi  
A,E,M

**Mushko & Company Ltd.**  
Oosman Chambers  
Abdullah Haroon Road  
**KARACHI 0302**  
Tel: 511027, 512927  
Telex: 2894 MUSKO PK  
Cable: COOPERATOR Karachi  
A,E,M,P\*

**PANAMA**  
**Electrónico Balboa, S.A.**  
Calle Samuel Lewis, Ed. Alfa  
Apartado 4929  
**PANAMA 5**  
Tel: 64-2700  
Telex: 3483 ELECTRON PG  
A,CM,E,M,P  
Foto Internacional, S.A.  
Colon Free Zone  
Apartado 2068  
**COLON 3**  
Tel: 45-2333  
Telex: 8626 IMPORT PG  
P

**PERU**  
**Cia Electro Médica S.A.**  
Los Flamencos 145, San Isidro  
Casilla 1030  
**LIMA 1**  
Tel: 41-4325, 41-3703  
Telex: Pub. Booth 25306  
A,CM,E,M,P

**PHILIPPINES**  
**The Online Advanced Systems Corporation**  
Rico House, Amorsolo Cor. Herrera Street  
Legaspi Village, Makati  
P.O. Box 1510  
**Metro MANILA**  
Tel: 85-35-81, 85-34-91, 85-32-21  
Telex: 3274 ONLINE  
A,CH,CS,E,M  
**Electronic Specialists and Proponents Inc.**  
690-B Epifanio de los Santos Avenue  
Cubao, **QUEZON CITY**  
P.O. Box 2649 Manila  
Tel: 98-96-81, 98-96-82, 98-96-83  
Telex: 40018, 42000 ITT GLOBE  
MACKAY BOOTH  
P

**PORTUGAL**  
**Mundinter**  
Intercambio Mundial de Comércio S.a.r.l  
P.O. Box 2761  
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**P-LISBON**  
Tel: (19) 53-21-31, 53-21-37  
Telex: 16691 munter p  
M

**Soquimica**  
Av. da Liberdade, 220-2  
1298 LISBON Codex  
Tel: 56 21 81/2/3  
Telex: 13316 SABASA P  
**Telectra-Empresa Técnica de Equipamentos Eléctricos S.a.r.l.**  
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CH,CS,E,P

**PUERTO RICO**  
**Hewlett-Packard Puerto Rico**  
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Urb. Country Club  
**RIO PIEDRAS, Puerto Rico 00924**  
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A,CH,CS

**QATAR**  
**Nasser Trading & Contracting**  
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**DOHA**  
Tel: 22170, 23539  
Telex: 4439 NASSER DH  
M  
**Computeabria**  
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**DOHA**  
Tel: 883555  
Telex: 4806 CHPARB  
P

**Eastern Technical Services**  
P.O. Box 4747  
**DOHA**  
Tel: 329 993  
Telex: 4156 EASTEC DH

**SAUDI ARABIA**  
**Modern Electronic Establishment**  
**Hewlett-Packard Division**  
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**AL-KHOBAR**

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Telex: 671 106 HPMEEK SJ  
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Telex: RS 26283  
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**DAMASCUS**  
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Cable: ELECTROBOR DAMASCUS  
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M,P

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CH,CS,E

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E,P

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1 ter. Av. de Carthage  
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M

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Telex: 42155 TKNM TR  
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E\*,CH\*,CS\*

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LIVERPOOL, NY 13088  
Tel: (315) 451-1820  
A,CH,CM,E,MS

Hewlett-Packard Co.  
No. 1 Pennsylvania Plaza  
55th Floor  
34th Street & 8th Avenue  
NEW YORK, NY 10119  
Tel: (212) 971-0800  
CH,CS,E\*,M\*





# SALES & SUPPORT OFFICES

## Arranged Alphabetically by Country

Hewlett-Packard Co.  
250 Westchester Avenue  
WHITE PLAINS, NY 10604  
CM,CH,CS,E

Hewlett-Packard Co.  
3 Crossways Park West  
WOODBURY, NY 11797  
Tel: (516) 921-0300  
Telex: 510-221-2183  
A,CH,CM,CS,E,MS

### North Carolina

Hewlett-Packard Co.  
4915 Water's Edge Drive  
Suite 160  
RALEIGH, NC 27606  
Tel: (919) 851-3021  
C,M

Hewlett-Packard Co.  
P.O. Box 26500  
5605 Roanne Way  
GREENSBORO, NC 27450  
Tel: (919) 852-1800  
A,CH,CM,CS,E,MS

### Ohio

Hewlett-Packard Co.  
9920 Carver Road  
CINCINNATI, OH 45242  
Tel: (513) 891-9870  
CH,CS,MS

Hewlett-Packard Co.  
16500 Sprague Road  
CLEVELAND, OH 44130  
Tel: (216) 243-7300  
Telex: 810-423-9430  
A,CH,CM,CS,E,MS

Hewlett-Packard Co.  
962 Crupper Ave.  
COLUMBUS, OH 43229  
Tel: (614) 436-1041  
CH,CM,CS,E\*

Hewlett-Packard Co.  
P.O. Box 280  
330 Progress Rd.  
DAYTON, OH 45449  
Tel: (513) 859-8202  
A,CH,CM,E\*,MS

### Oklahoma

Hewlett-Packard Co.  
P.O. Box 32008  
Oklahoma City, OK 73123  
1503 W. Gore Blvd., Suite #2  
LAWTON, OK 73505  
Tel: (405) 248-4248  
C

Hewlett-Packard Co.  
P.O. Box 32008  
OKLAHOMA CITY, OK 73123  
304 N. Meridian Avenue, Suite A  
OKLAHOMA CITY, OK 73107  
Tel: (405) 946-9499  
A\*,CH,E\*,MS

Hewlett-Packard Co.  
Suite 121  
9920 E. 42nd Street  
TULSA, OK 74145  
Tel: (918) 665-3300  
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### Oregon

Hewlett-Packard Co.  
1500 Valley River Drive  
Suite 330  
EUGENE, OR 97401  
Tel: (503) 683-8075  
C

Hewlett-Packard Co.  
9255 S. W. Pioneer Court  
WILSONVILLE, OR 97070  
Tel: (503) 682-8000  
A,CH,CS,E\*,MS

### Pennsylvania

Hewlett-Packard Co.  
1021 8th Avenue  
King of Prussia Industrial Park  
KING OF PRUSSIA, PA 19406  
Tel: (215) 265-7000  
Telex: 510-660-2670  
A,CH,CM,CS,E,MP

Hewlett-Packard Co.  
111 Zeta Drive  
PITTSBURGH, PA 15238  
Tel: (412) 782-0400  
A,CH,CS,E,MP

### South Carolina

Hewlett-Packard Co.  
P.O. Box 21708  
Brookside Park, Suite 122  
1 Harbison Way  
COLUMBIA, SC 29210  
Tel: (803) 732-0400  
CH,E,MS

Hewlett-Packard Co.  
Koger Executive Center  
Chesterfield Bldg., Suite 124  
GREENVILLE, SC 29615  
Tel: (803) 748-5601  
C

### Tennessee

Hewlett-Packard Co.  
P.O. Box 22490  
224 Peters Road  
Suite 102  
KNOXVILLE, TN 37922  
Tel: (615) 691-2371  
A\*,CH,MS

Hewlett-Packard Co.  
3070 Directors Row  
MEMPHIS, TN 38131  
Tel: (901) 346-8370  
A,CH,MS

Hewlett-Packard Co.  
230 Great Circle Road  
Suite 216  
NASHVILLE, TN 32228  
Tel: (615) 255-1271  
MS\*\*

### Texas

Hewlett-Packard Co.  
Suite 310W  
7800 Shoal Creek Blvd.  
AUSTIN, TX 78757  
Tel: (512) 459-3143  
E

Hewlett-Packard Co.  
Suite C-110  
4171 North Mesa  
EL PASO, TX 79902  
Tel: (915) 533-3555, 533-4489  
CH,E\*,MS\*\*

Hewlett-Packard Co.  
5020 Mark IV Parkway  
FORT WORTH, TX 76106  
Tel: (817) 625-6361  
CH,CS\*

Hewlett-Packard Co.  
P.O. Box 42816  
HOUSTON, TX 77042  
10535 Harwin Street  
HOUSTON, TX 77036  
Tel: (713) 776-6400  
A,CH,CM,CS,E,MP

Hewlett-Packard Co.  
3309 67th Street  
Suite 24  
LUBBOCK, TX 79413  
Tel: (806) 799-4472  
M

Hewlett-Packard Co.  
417 Nolana Gardens, Suite C  
P.O. Box 2256  
McALLEN, TX 78501  
Tel: (512) 781-3226  
CH,CS

Hewlett-Packard Co.  
P.O. Box 1270  
RICHARDSON, TX 75080  
930 E. Campbell Rd.  
RICHARDSON, TX 75081  
Tel: (214) 231-6101  
A,CH,CM,CS,E,MP

Hewlett-Packard Co.  
P.O. Box 32993  
SAN ANTONIO, TX 78216  
1020 Central Parkway South  
SAN ANTONIO, TX 78232  
Tel: (512) 494-9336  
CH,CS,E,MS

### Utah

Hewlett-Packard Co.  
P.O. Box 26626  
3530 W. 2100 South  
SALT LAKE CITY, UT 84119  
Tel: (801) 974-1700  
A,CH,CS,E,MS

### Virginia

Hewlett-Packard Co.  
P.O. Box 9669  
2914 Hungary Spring Road  
RICHMOND, VA 23228  
Tel: (804) 285-3431  
A,CH,CS,E,MS

Hewlett-Packard Co.  
3106 Peters Creek Road, N.W.  
ROANOKE, VA 24019  
Tel: (703) 563-2205  
CH,E\*\*

Hewlett-Packard Co.  
5700 Thurston Avenue  
Suite 111  
VIRGINIA BEACH, VA 23455  
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CH,MS

### Washington

Hewlett-Packard Co.  
15815 S.E. 37th Street  
BELLEVUE, WA 98006  
Tel: (206) 643-4000  
A,CH,CM,CS,E,MP

Hewlett-Packard Co.  
Suite A  
708 North Argonne Road  
SPOKANE, WA 99206  
Tel: (509) 922-7000  
CH,CS

### West Virginia

Hewlett-Packard Co.  
4604 MacCorkle Ave., S.E.  
CHARLESTON, WV 25304-4297  
Tel: (304) 925-0492  
A,MS

### Wisconsin

Hewlett-Packard Co.  
150 S. Sunny Slope Road  
BROOKFIELD, WI 53005  
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A,CH,CS,E\*,MP

### URUGUAY

Pablo Ferrando S.A.C. e L.  
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Casilla de Correo 370  
MONTEVIDEO  
Tel: 80-2586  
Telex: Public Booth 901  
A,CM,E,M

Guillermo Kraft del Uruguay S.A.  
Av. Lib. Brig. Gral. Lavalleja 2083  
MONTEVIDEO  
Tel: 234588, 234808, 208830  
Telex: 22030 ACTOUR UY  
P

### VENEZUELA

Hewlett-Packard de Venezuela C.A.  
3A Transversal Los Ruices Norte  
Edificio Segre  
Apartado 50933  
CARACAS 1071  
Tel: 239-4133  
Telex: 25146 HEWPACK  
A,CH,CS,E,MS,P  
Colimodio S.A.  
Este 2 - Sur 21 No. 148  
Apartado 1053  
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Tel: 571-3511  
Telex: 21529 COLMODIO  
M

### Headquarters offices

If there is no sales office listed for your area,  
contact one of these headquarters offices.

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Hewlett-Packard Asia Ltd.  
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Hewlett-Packard (Canada) Ltd.  
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### ZIMBABWE

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45 Kelvin Road, North  
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C,E,M,P

### MEDITERRANEAN AND

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Hewlett-Packard Co.  
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Rockville, MD 20850  
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#### MIDWESTERN USA

Hewlett-Packard Co.  
5201 Tollview Drive  
ROLLING MEADOWS, IL 60008  
Tel: (312) 255-9800

#### SOUTHERN USA

Hewlett-Packard Co.  
P.O. Box 105005  
450 Interstate N. Parkway  
ATLANTA, GA 30339  
Tel: (404) 955-1500

#### WESTERN USA

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