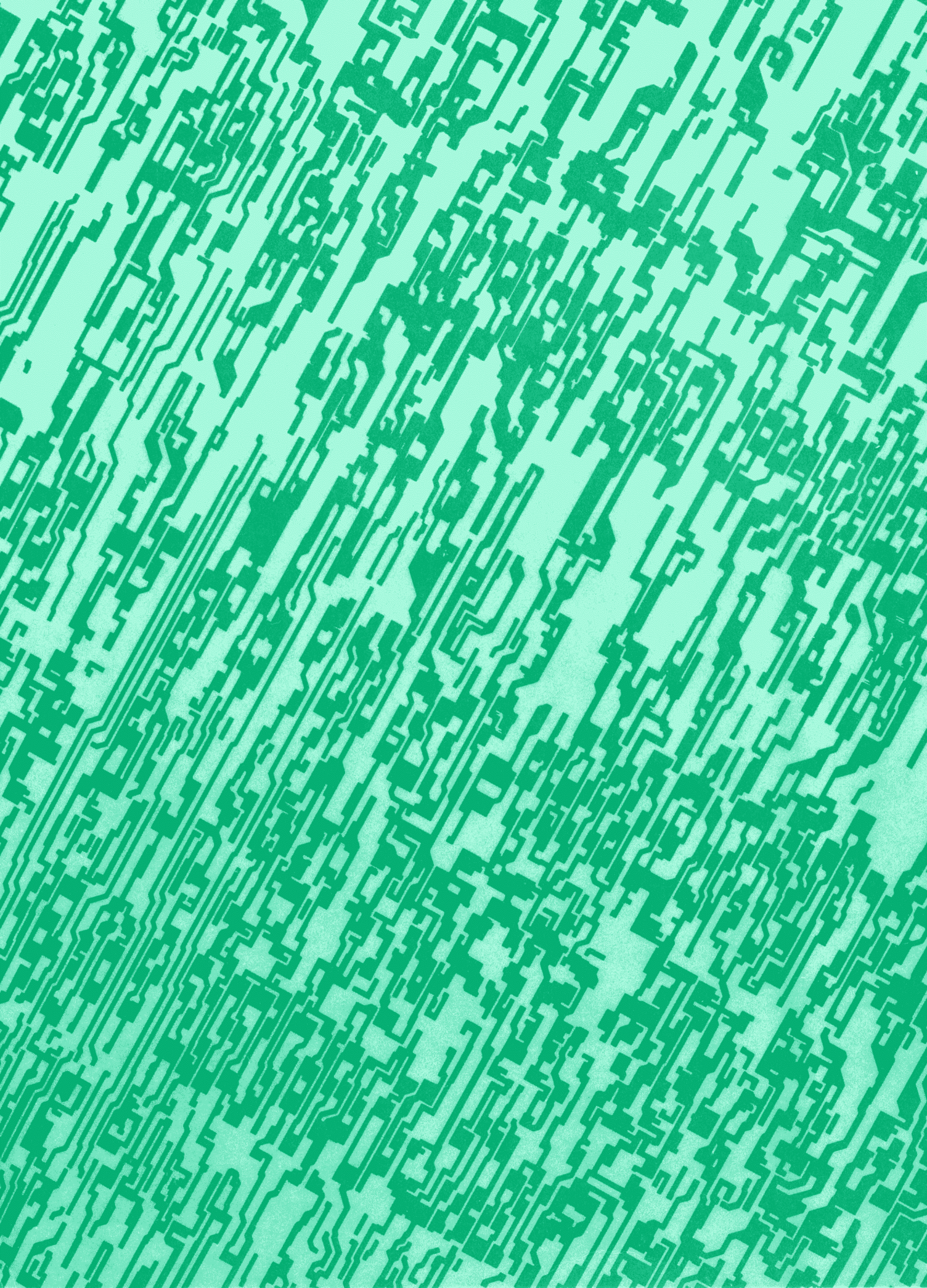
Zilog Z80® Family

Zilog

Technical Overview

August 1980



Zilog Z80® Family

Technical Overview

Zilog Z80® Family

New Faster Z80B Peripheral Controllers

August 1980

Zilog has become an industry leader, thanks to innovation in microcomputer concepts and integrated design exemplified in the Z-80 Family of microcomputer products.

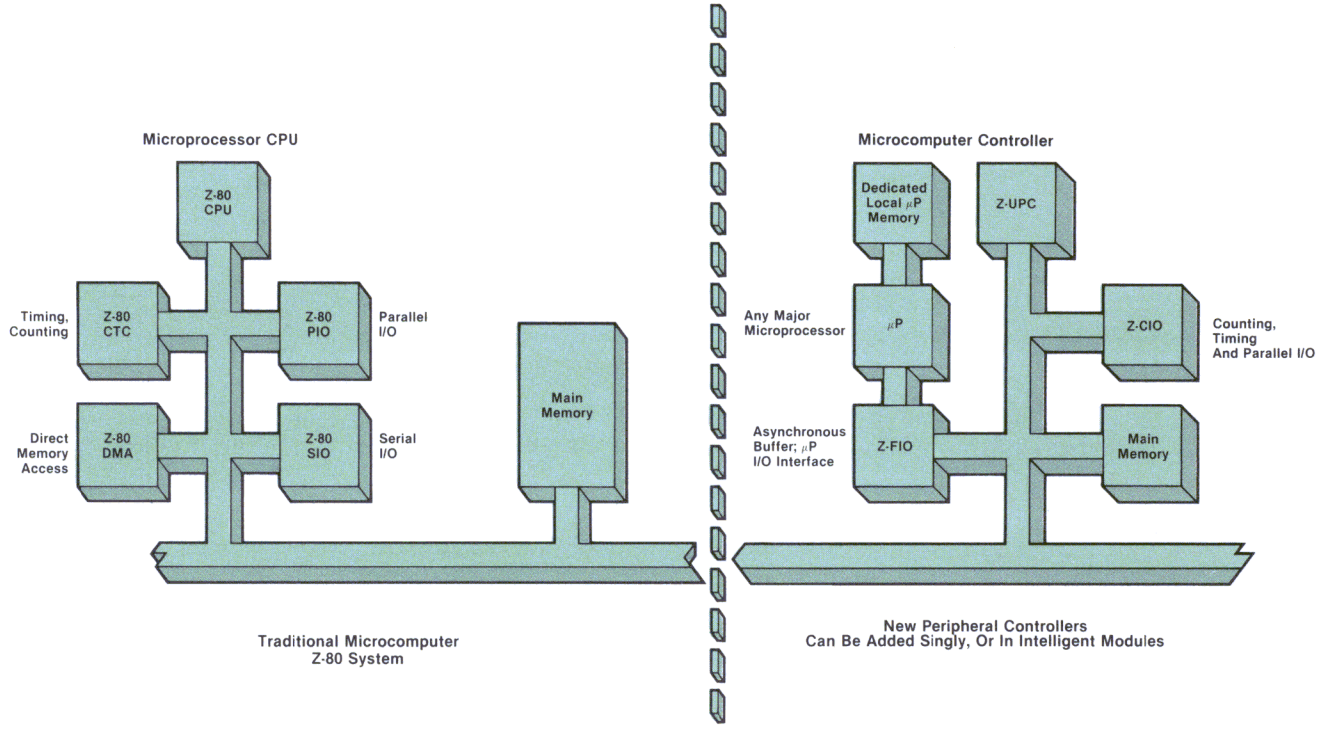
At Zilog, innovation means using proven, sophisticated mainframe and minicomputer concepts and translating them into the latest LSI technologies. Integration means more than designing an ever-greater number of functions onto a single chip. Zilog integrates technologies—LSI design enhanced by advances in computer-based system architecture and system design technologies.

Zilog offers microprocessor solutions to computing problems: from components and development systems to OEM board-level products and general-purpose microcomputer systems.

This guide to the Z-80 Family of state-of-the-art microprocessors and intelligent peripheral controllers demonstrates Zilog's continued support for the Z-80 microprocessor and the other members of the Z-80 product family—a family first introduced in 1976 that continues to enjoy growing customer support while family chips are upgraded to newer and ever-higher standards.

Three new peripheral controllers give fresh life to existing microprocessor applications while greatly broadening the application horizon of the Zilog Family of microprocessor components.

The design philosophy of all Z-80 Family members is to help engineers design microcomputer systems with fewer components that have more functions per chip. The Z-80 CPU offers many more features and functions than its main competitor, along with a large and flexible instruction set. All Zilog peripheral controllers are specialized processors dedicated to providing functions that previously required a much larger amount of



discrete circuitry or a great deal of software overhead.

Each programmable peripheral unburdens the CPU and increases system throughput. All Z-80 Family members and Universal Bus Peripherals can operate in interrupt-driven or polled environments. A daisy-chained interrupt structure prioritizes peripheral interrupts to the CPU, saving an external interrupt controller.

Chip count is further reduced both by multiple channels and by extensively programmable capabilities. The CPU addresses peripherals using a common I/O command structure that tailors each peripheral to the precise configuration required by the application.

The **Z-80 CPU Central Processing Unit** has rapidly established itself as the most sophisticated, most powerful, and most versatile 8-bit microprocessor. Now Zilog offers the Z-80B microprocessor, whose 6 MHz performance supports an expanded range of throughput-critical applications formerly reserved for minicomputers. Although source-code compatible with the 8080A microprocessor, the Z-80 CPU offers many more instructions (158 vs 78) and numerous other features that simplify hardware requirements and reduce programming effort while increasing throughput.

The dual-register set of the Z-80 CPU allows high-speed context switching and more efficient interrupt processing. Two index registers give additional memory addressing flexibility and simplify the programming task. Interfacing to dynamic memory is simplified by on-chip programmable refresh logic. Block move plus string- and bit-manipulation instructions reduce programming effort, program size and execution time.

The Traditional System. The four traditional microcomputer-system functions—parallel I/O, serial I/O, counting/timing, and direct memory access—are handled by the established Z-80 Family peripherals: Z-80 PIO, Z-80 SIO, Z-80 DART, Z-80 CTC, and Z-80 DMA.

Easily programmed, the dual-channel **Z-80 PIO Parallel Input/Output Controller** offers two 8-bit I/O ports with individual handshake and pattern-recognition logic. Both ports operate in either byte or bit modes. In addition, interrupts can be programmed for peripheral status conditions and eight outputs are capable of driving Darlington transistors.

All common data communications protocols, asynchronous as well as synchronous, are handled by the **Z-80 SIO Serial Input/Output Controller.** This dual-channel receiver/transmitter also offers on-chip parity and CRC generation/checking, FIFO buffering, as well as flag and frame detection/generation logic.

Asynchronous-only applications are handled by the **Z-80 DART Dual Asynchronous Receiver/Transmitter.** This cost-effective device offers all Z-80 SIO asynchronous-mode features in two channels.

Timing and event-counting functions are the forte of the **Z-80 CTC Counter/Timer Controller.** Its four counters all have individually programmable prescalers. Three counter outputs can drive Darlington transistors. The CTC is a convenient source of programmable clock rates for the SIO.

Data can be transferred directly between any two ports (I/O and memory, typically) with the **Z-80 DMA Direct Memory Access Controller.** The DMA transfers, searches, or search/transfers data in byte-at-a-time, burst, or continuous modes. This device can achieve an impressive 2M bytes per second data rate in the search mode.

Three New Members. The popular, well established Z-80 Family of peripherals is supported by three new controllers*. The Z-CIO/U, Z-UPC/U, and Z-FIO/U feature sophisticated counting/timing and parallel I/O on one chip, off-line CPU processing, and asynchronous I/O interfacing.

Although they function smoothly in most Z-80 systems, these controllers are not dedicated to the Z-80 bus. Instead, they fit a general-purpose bus that allows them to be incorporated into most 8-bit microprocessor systems.

In addition to its three independent 16-bit counters, the **Z-CIO/U Counter and Input/Output Controller** offers two 8-bit bidirectional I/O ports plus a special-purpose 4-bit port. Its four handshake modes include 3 wire (like IEEE-488). Furthermore, the CIO pattern recognition logic allows it to double as a 16-input interrupt controller.

Z-UPC/U Universal Peripheral Controller solves general-purpose control and data-manipulation problems. This complete microcomputer-on-a-chip executes the same friendly, capable instruction set as the Z8 MCU Microcomputer. The UPC also offers 2K of on-chip ROM, three I/O ports and two programmable 8-bit counter/timers with 6-bit prescalers.

Bits and pieces of asynchronous parallel-processing systems are interconnected by the **Z-FIO FIFO Input/Output Interface Unit.** This surprisingly flexible device interfaces any major microprocessor and most peripherals to a system bus and can interface any Z-80 Family part to the powerful Z-Bus, used by the 16-bit Z8000.

The Zilog 8-bit Microprocessor Family is the most popular microcomputer-component family in the world. Now you know why.

*Available in the summer of 1980.

Z80® CPU Central Processing Unit

Zilog

Product Brief

August 1980

Features

- 158 instructions, software compatible with all 78 of the 8080A instructions.
- High speed—up to 4 MHz rate with a minimum 1.0 μs instruction execution time for the Z-80A and 2.5 MHz and 1.5 μs for the Z-80.
- Duplicate set of general-purpose and flag registers (16 total) eases design and operation of such system software programming, single context switching, background-foreground programming, single-level interrupt processing. Two 16-bit index registers allow efficient processing of tables and arrays.
- Extensive instruction set includes string, bit, byte, word operations and block transfers along with efficient addressing modes such as indexed and relative.
- All Z-80 Family components offer bus-request and prioritized interrupt request daisy chains that can be implemented without external logic.
- Three modes of high-speed interrupt processing: 8080 compatible, non-Z-80 peripheral and Z-80 Family peripheral daisy chain.

General Description

The Zilog Z-80 microprocessor is the central element of the Z-80 Microprocessor Family, which includes a variety of compatible peripheral circuits. The Z-80 Family handles most microprocessor applications with little additional logic. Z-80 designs are efficient and cost effective microcomputer systems.

The Z-80 CPU is a third generation 8-bit microprocessor with exceptional capabilities and computational power. The powerful instruction set, dual register sets and other features of the Z-80 CPU provide higher throughput and greater efficiency in memory utilization. In addition, the Z-80 CPU is easy to use in a system because of its single +5 V supply requirement and fully compatible family of peripheral circuits. All Z-80 Family members are fabricated with scaled n-channel silicon-gate depletion-load technology.

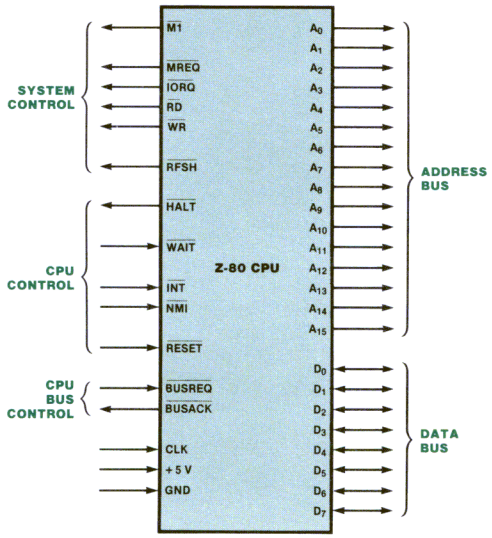


Figure 1. Pin Functions

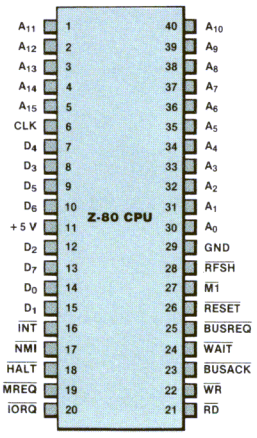


Figure 2. Pin Assignments

General Description (Continued)

The internal register configuration contains 208 bits of Read/Write memory accessible to the programmer. The registers include two sets of six general-purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers.

The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper eight bits of a pointer to an interrupt service address table, while the interrupting device supplies the lower eight bits of the pointer. An indirect call is then made to this service address.

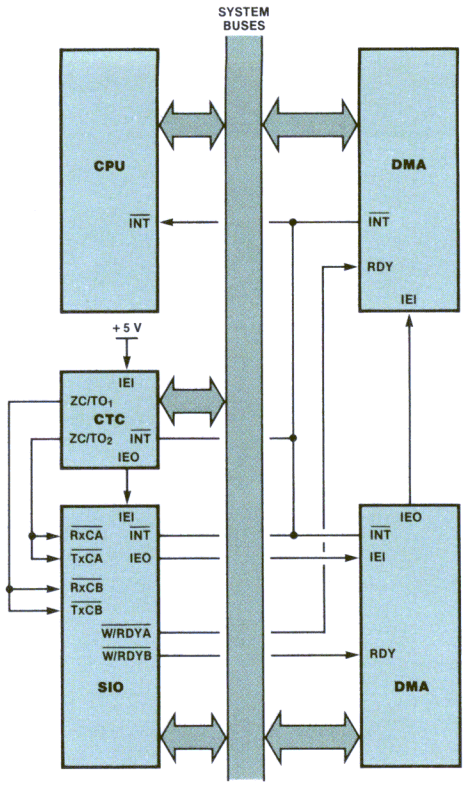


Figure 3. Typical Z-80 Family Environment

Instruction Set

The Z-80 CPU has one of the most powerful and rich instruction sets available in any 8-bit microprocessor. It includes such unique operations as block move for fast and efficient data transfers between memory and I/O and bit operations on any location in memory. The Z-80 CPU offers instructions in the following catagories:

8-bit loads	General-purpose Accumulator and Flag operations
16-bit loads	Bit set, reset and test operations
Register exchanges	Input and output operations
Memory block moves	Jumps
Memory block searches	Calls
bit arithmetic and logic operations	Restarts
16-bit arithmetic operations	Returns
Rotates and shifts	

Z80® PIO Parallel Input/Output Controller

Zilog

Product Brief

August 1980

Features

- Provides a direct interface between Z-80 microcomputer systems and peripheral devices.
- Both ports have interrupt-driven handshake for fast response.
- Four programmable operating modes: byte input, byte output, byte input/output (Port A only), and bit input/output.
- Programmable interrupts on peripheral status conditions.
- Standard Z-80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic.
- The eight Port B outputs can drive Darlington transistors (1.5 mA at 1.5 V).

General Description

The Z-80 PIO Parallel I/O Circuit is a programmable, dual-port device that provides a TTL-compatible interface between peripheral devices and the Z-80 CPU. The CPU configures the Z-80 PIO to interface with a wide range of peripheral devices with no other external logic. Typical peripheral devices that are compatible with the Z-80 PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc.

One characteristic of the Z-80 PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under interrupt control. The interrupt logic of the PIO permits full use of the efficient interrupt capabilities of the Z-80 CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO.

Another feature is that the PIO can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the time the processor must spend in polling peripheral status.

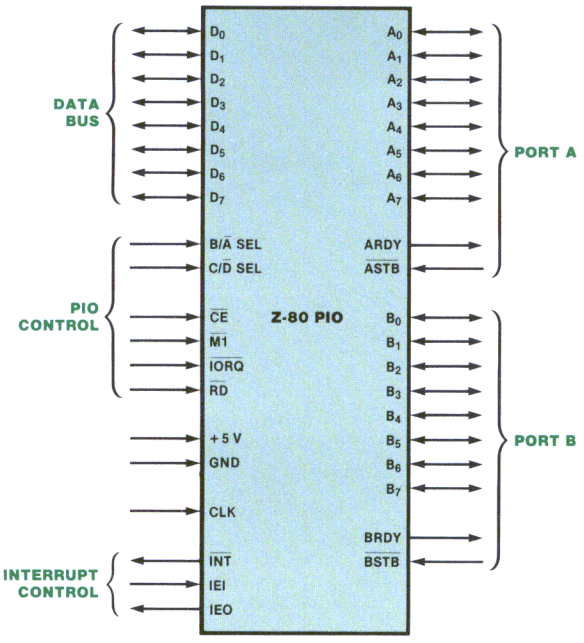


Figure 1. Pin Functions

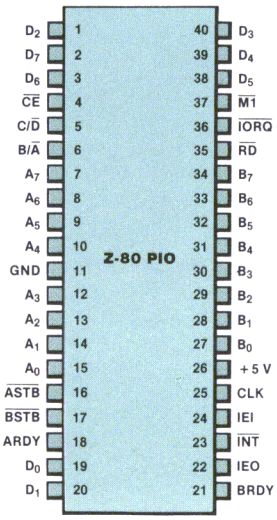


Figure 2. Pin Assignments

General Description (Continued)

The Z-80 PIO interfaces to peripherals via two independent general-purpose I/O ports, designated Port A and Port B. Each port has eight data bits and two handshake signals, Ready and Strobe, which control data transfer. The Ready output indicates to the peripheral that the port is ready for a data transfer. Strobe is an input from the peripheral that indicates a data transfer has occurred.

Operating Modes. The Z-80 ports can be programmed to operate in four modes: byte output (Mode 0), byte input (Mode 1), byte input/output (Mode 2) and bit input/output (Mode 3).

In Mode 0, either Port A or Port B can be programmed to output data. Both ports have output registers that are individually addressed by the CPU; data can be written to either port at any time. When data is written to a port, an active Ready output indicates to the external device that data is available at the associated port, and is ready for transfer to the external device. After the data transfer, the external device responds with an active Strobe input, which generates an interrupt, if enabled.

In Mode 1, either Port A or Port B can be configured in the input mode. Each port has an input register addressed by the CPU. When the CPU reads data from a port, the PIO sets the Ready signal, which is sensed by the external device. The external device then places data on the I/O lines and strobes the I/O port, which latches the data into the Port Input Register, resets Ready, and triggers the Interrupt Request, if enabled. The CPU can read the input data at any time, which again sets Ready.

Mode 2 is bidirectional and uses Port A, plus the interrupts and handshake signals from both ports. Port B must be set to Mode 3, and must be masked off. In operation, Port A is used for both data input and output. Output operation is similar to Mode 0 except data is allowed out onto the Port A bus only when $\overline{ASTB}$ is Low. For input, operation is similar to Mode 1, except that the data input uses the Port B handshake signals and the Port B interrupt (if enabled).

Both ports can be used in Mode 3. In this mode, the individual bits are defined as either input or output bits. This provides up to eight separate, individually defined bits for each port. During operation, Ready and Strobe are not used. Instead, an interrupt is generated if the condition of one input changes, or if all inputs change. The requirements for generating an interrupt are defined during the programming operation; the active level is specified as either High or Low, and the logic condition is specified as either one input active (OR), or all inputs active (AND). For example, if the port is programmed for active Low inputs, and the logic function is AND, then all inputs at the specified port must go Low to generate an interrupt.

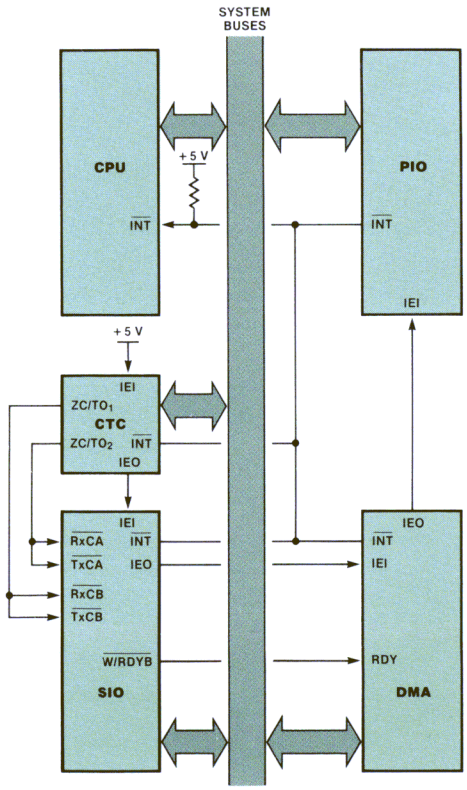


Figure 3. PIO in a Typical Z80 Family Environment

Z80® CTC Counter/Timer Circuit

Zilog

Product Brief

August 1980

Features

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- Selectable positive or negative trigger initiates timer operation.
- Standard Z-80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- Interfaces directly to the Z-80 CPU or—for baud rate generation—to the Z-80 SIO.

Description

The Z-80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z-80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z-80 CPU and the Z-80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, reloads its time constant automatically, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z-80 CTC requires a single +5 V power supply and the standard Z-80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in a 28-pin plastic or ceramic DIP.

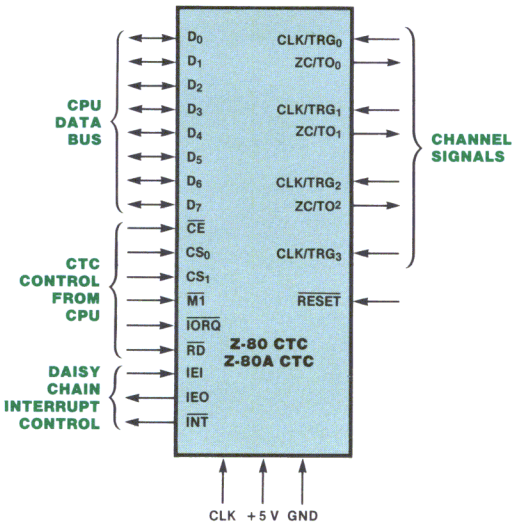


Figure 1. Pin Functions

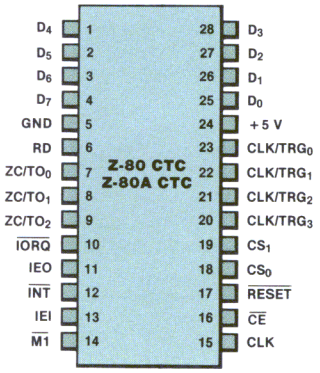


Figure 2. Pin Assignments

Architecture

The CTC has four major elements: CPU bus I/O, internal control logic, interrupt logic, and counter timer circuits (Figure 3).

The CPU bus I/O circuit decodes the address inputs. It also interfaces the CPU data and control signals to the CTC for distribution on the internal bus.

The internal control logic controls overall chip operating functions such as the chip enable, reset, and read/write logic.

The interrupt control logic assures that the CTC interrupts interface properly with the Z-80 CPU interrupt system, and also controls the interrupt priority of the CTC.

The counter/timer circuits are functionally described below. There are four of them, each independent, and each containing the logic shown in Figure 4.

Functional Description

Each individual channel of the Z-80 CTC operates in two modes: counter or timer. The logic is shown in Figure 4. In the counter mode, the down-counter counts down from the pre-set time constant (1 to 256), decrementing on each of the CLK/TRG input pulses until zero is reached. At zero, the down-counter is automatically reset with the time constant. Each decrement is synchronized by the system clock. More than one counter can be cascaded for counts greater than 256. The CPU can read the count remaining at any time without disturbing the down-counter.

In the timer mode, time intervals are generated by a prescaler which divides the system clock frequency by 16 or 256. The time interval is an integral multiple of the clock period, the prescaler value (16 to 256) and the time constant pre-set in the down-counter. Time intervals as small as 4 microseconds (Z-80A) or 6.4 microseconds (Z-80) can be determined without additional logic or software timing loops.

At zero, channels 0, 1, and 2 have two outputs available: zero-count/timeout pulse at the ZC/TO output, and an interrupt request which occurs if the channel has its interrupt enabled during programming. Channel 3 has only the interrupt request. When the CPU acknowledges an interrupt request, the CTC places an interrupt vector on the data bus.

Each channel is individually programmed with two words: a time-constant word and a control word. The time-constant word is a value from 1 to 256. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets the prescaler.

The channel control logic receives the channel control word when the counter/timer channel is programmed. The channel control logic decodes the control word and sets the following operating conditions: interrupt enable/disable; operating mode; timer mode; prescaler factor; active slope for CLK/TRG input; timer mode trigger (automatic or CLK/TRG input; time constant data word to follow; and software set.

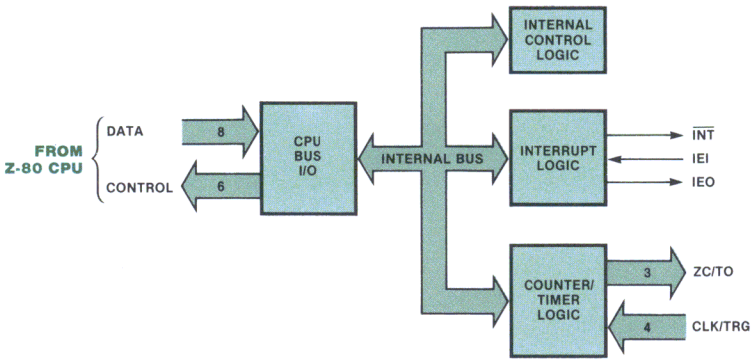


Figure 3. Functional Block Diagram

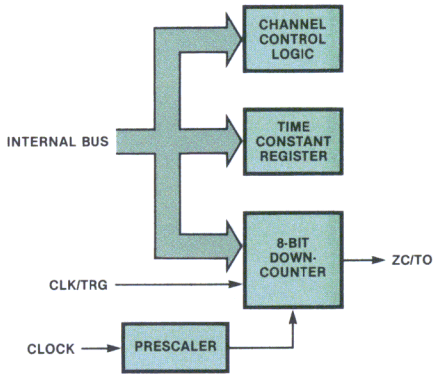


Figure 4. Counter/Timer Block Diagram

Z80® SIO Serial Input/Output Controller

Zilog

Product Brief

August 1980

Features

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (Z-80 SIO), or 0 to 800K bits/second with a 4.0 MHz clock (Z-80A SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

General Description

The Z-80 SIO Serial Input/Output Controller is a dual-channel data communication interface. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for most serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions of a UART, USART and synchronous communication controller combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an interrupt structure that allows very fast transfers. Full interfacing is provided for CPU or DMA control.

As a peripheral to other microprocessors, the SIO offers valuable features such as vectored/non-vectored interrupts, polling, and I/O handshake capability.

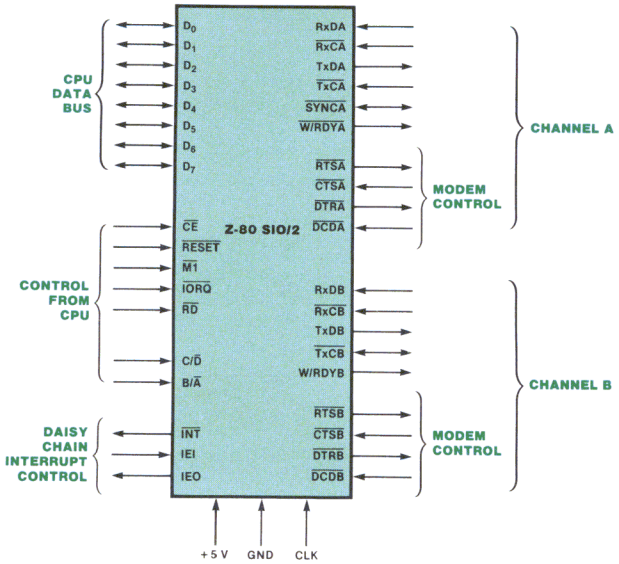


Figure 1. Z-80 SIO Pin Functions

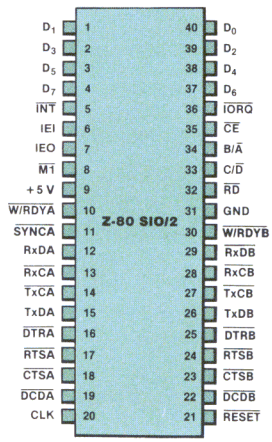


Figure 2. Z-80 SIO Pin Assignments

Functional Description

Data Communications, Asynchronous Modes. Transmisssion and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occured. Vectored interrupts allow fast servicing of error conditions using dedicated routines.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with a Z-80 CTC or many other clock sources.

Data Communications, Synchronous Modes. The SIO supports both byte-oriented and bit-oriented synchronous communication.

Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (monosync), any 16-bit sync pattern (bisync), or with an external sync signal.

I/O Interface. The SIO offers the choice of polling, interrupt (vectored or non-vectored) and block-transfer modes to transfer data, status and control information to and from the CPU. The block-transfer mode can also be implemented under DMA control.

Bonding Options

Figures 1 and 2 illustrate one of the three possible pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together.

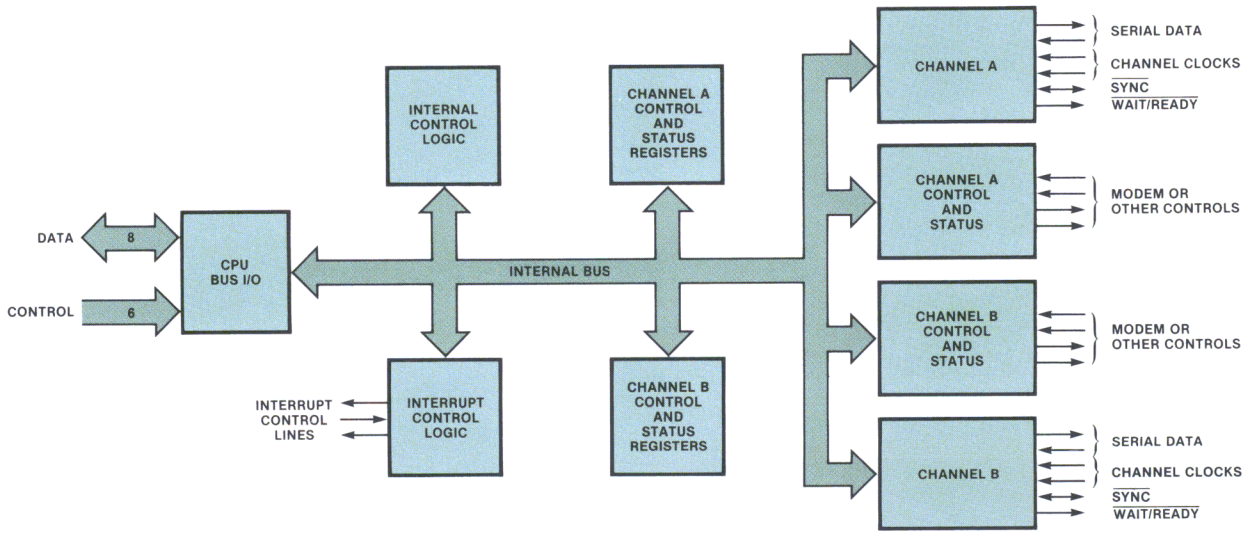


Figure 3. Z-80 SIO Block Diagram

Z80® SIO/9 Serial Input/Output Controller

Zilog

Product Brief

August 1980

Features

- One full-duplex channel, with separate control and status lines for a modem or other device.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (Z-80 SIO), or 0 to 800K bits/second with a 4.0 MHz clock (Z-80A SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity, overrun and framing error detection.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

General Description

The Z-80 SIO/9 Serial Input/Output Controller is a single-channel data communication interface with extraordinary versatility and capability. Functionally this device is identical to the Z-80 SIO, except that it operates in one channel only. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions

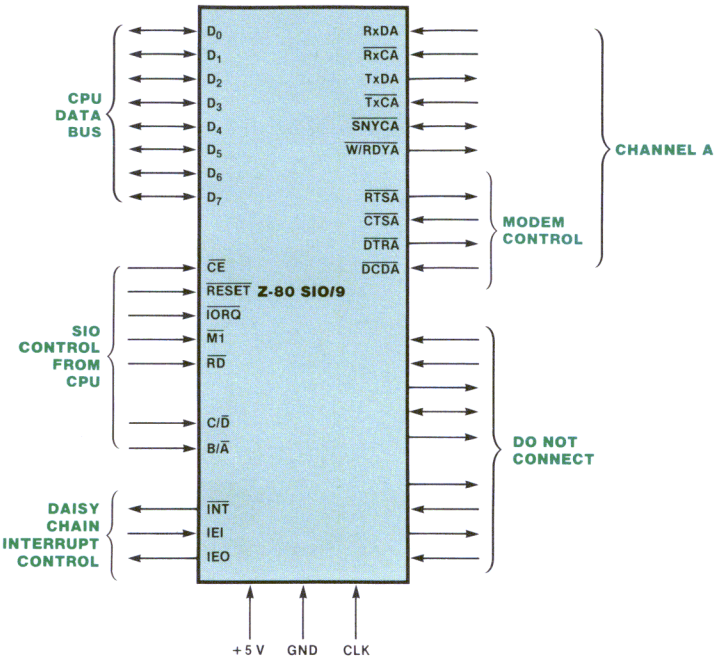


Figure 1. Z-80 SIO/9 Pin Functions

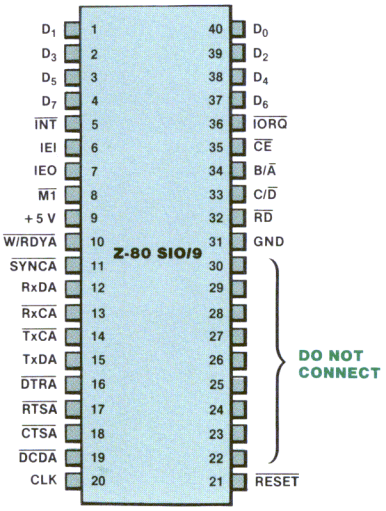


Figure 2. Z-80 SIO/9 Pin Assignments

General Description (Continued)

traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU and DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z-80 family, its versatility makes it well-suited to many other CPUs.

The Z-80 SIO/9 is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic or ceramic DIP. It uses a single +5 V power supply and standard Z-80 family single-phase clock.

Refer to the *Z-80 SIO Product Specification* and the *Z-80 SIO Technical Manual* for detailed functional and electrical descriptions. All functional and electrical descriptions in these publications are applicable to the Z-80 SIO/9, except that Channel B cannot be used for data input or output and pins 22 through 30 must not be connected.

Write Register 2 (interrupt vector) and the Status Affects Vector bit in Write Register 1 are, however, still programmed by selecting Channel B with the B/$\overline{A}$ input. All other bits in Write Register 1 or Channel B must be programmed to 0.

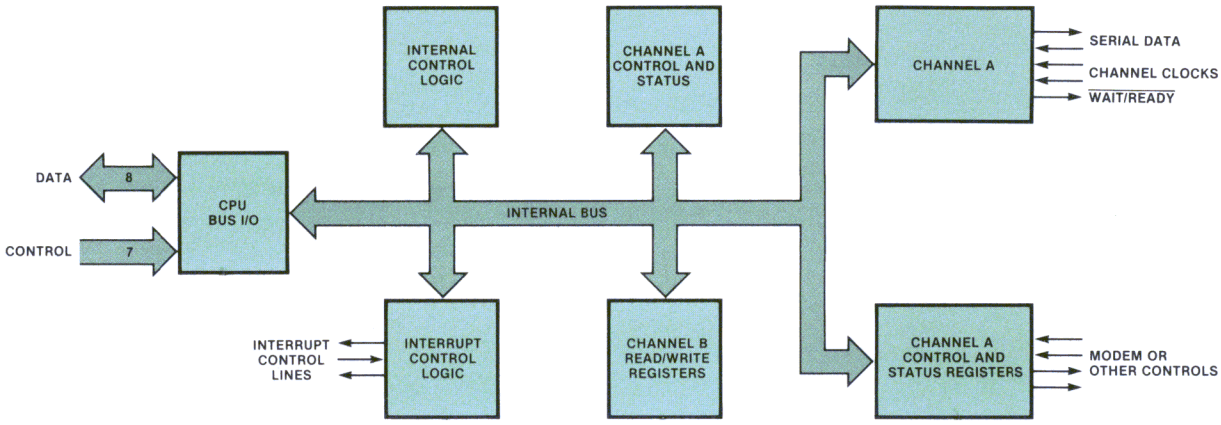


Figure 3. Block Diagram

Z80® DART Dual Asynchronous Receive/Transmitter

Zilog

Product Brief

August 1980

Features

- Two independent full-duplex channels with separate modem controls. Modem status can be monitored.
- Receiver data registers are quadruply buffered; the transmitter is doubly buffered.
- Interrupt features include a programmable interrupt vector, a "status affects vector" mode for fast interrupt processing, and the standard Z-80 peripheral daisy-chain interrupt structure that provides automatic interrupt vectoring with no external logic.
- In x1 clock mode, data rates are 0 to 500K bits/second with a 2.5 MHz clock, or 0 to 800K bits/second with a 4.0 MHz clock.
- Programmable options include 1, 1½ or 2 stop bits; even, odd or no parity; and x1, x16, x32 and x64 clock modes.
- Break generation and detection as well as parity-, overrun- and framing-error detection are available.

Description

The Z-80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multi-function peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z-80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.

Zilog also offers the Z-80 SIO, a more versatile device that provides synchronous (Bisync, HDLC and SDLC) as well as asynchronous operation.

The Z-80 DART is fabricated with n-channel silicon-gate depletion-load technology, and is packaged in a 40-pin plastic or ceramic DIP.

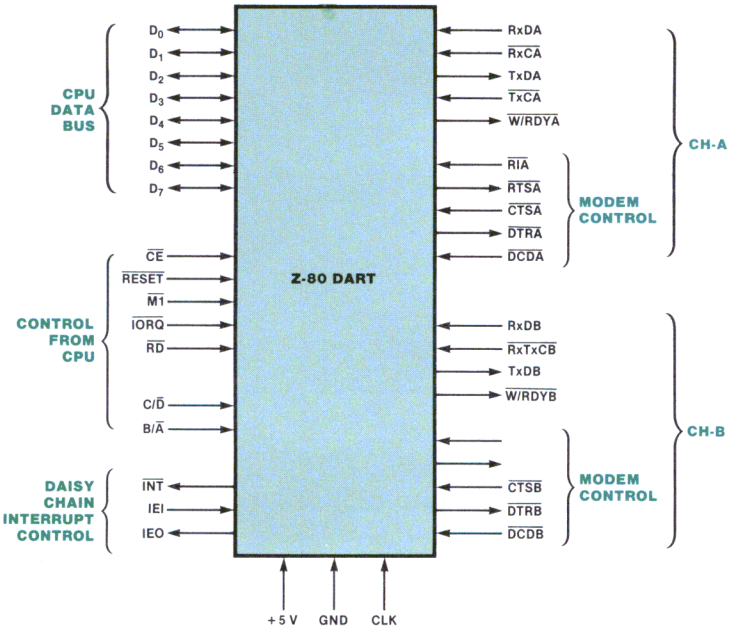


Figure 1. Z-80 DART Pin Functions

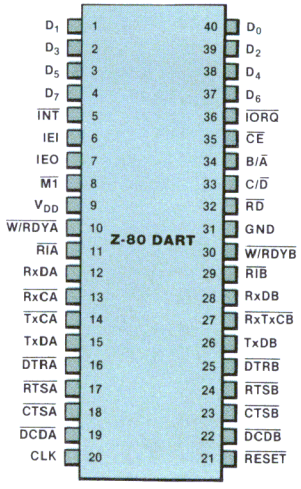


Figure 2. Pin Assignments

Functional Description

The functional capabilities of the Z-80 DART can be described from two different points of view: as a data communications device, it transmits and receives serial data, and meets the requirements of asynchronous data communications protocols; as a Z-80 family peripheral, it interacts with the Z-80 CPU and other Z-80 peripheral circuits, and shares the data, address and control buses, as well as being a part of the Z-80 interrupt structure. As a peripheral to other microprocessors, the Z-80 DART offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

The first part of the following functional description introduces Z-80 DART data communications capabilities; the second part describes the interaction between the CPU and the Z-80 DART.

Communications Capabilities. The Z-80 DART provides two independent full-duplex channels for use as an asynchronous receiver/transmitter. The following is a short description of receiver/transmitter capabilities. For more details, refer to the Asynchronous Mode section of the *Z-80 SIO Technical Manual.* The Z-80 DART offers transmission and reception of five to eight bits per character, plus optional even or odd parity. The transmitter can supply one, one and a half or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the Receive Data input. If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the character on which they occurred. Vectored interrupts allow fast servicing of interrupting conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The Z-80 DART does not require symmetric Transmit and Receive Clock signals—a feature that allows it to be used with a Z-80 CTC or any other clock source. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the Receive and Transmit Clock inputs. When using Channel B, the bit rates for transmit and receive operations must be the same because $\overline{RxC}$ and $\overline{TxC}$ are bonded together ($\overline{RxTxCB}$).

I/O Interface Capabilities. The Z-80 DART offers the choice of Polling, Interrupt (vectored or non-vectored) and Block Transfer modes to transfer data, status and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

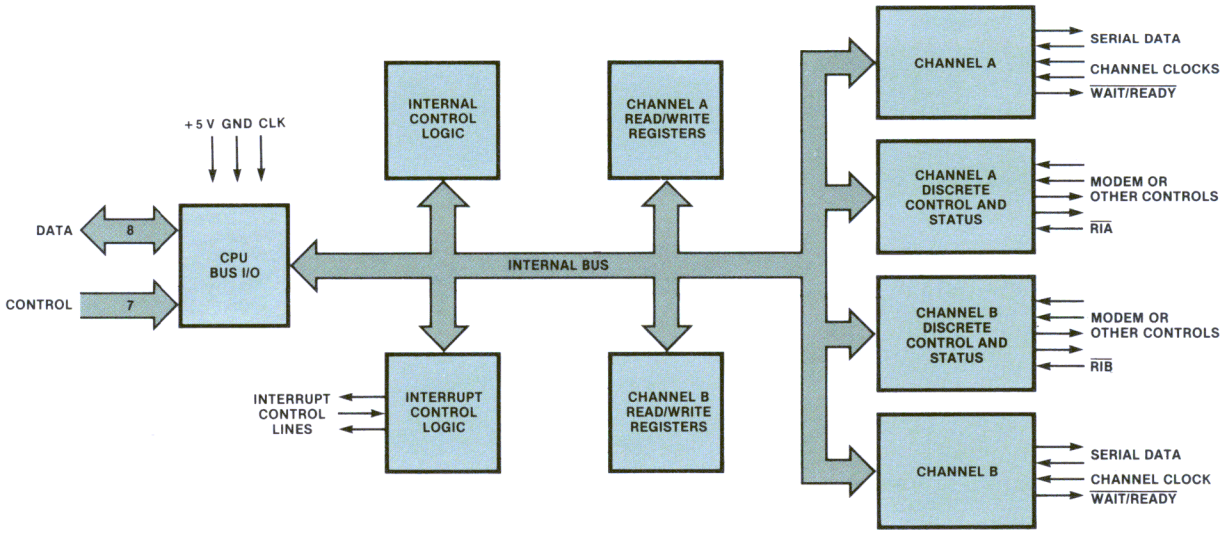


Figure 3. Block Diagram

Z80® DMA Direct Memory Access Controller

Zilog

Product Brief

August 1980

Features

- Transfers, searches and search/transfers in Byte-at-a-Time, Burst or Continuous modes. Cycle length and edge timing can be programmed to match the speed of any port.
- Dual port addresses (source and destination) generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations. Addresses may be fixed or automatically incremented/decremented.
- An entire previous sequence can be repeated automatically.
- Extensive programmability of functions. CPU can read complete channel status.
- Standard Z-80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic. Sophisticated, internally modifiable interrupt vectoring.
- Direct interfacing to system buses without external logic.

General Description

The Z-80 DMA (Direct Memory Access) is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches can be performed either concurrently with transfers or as an operation in itself.

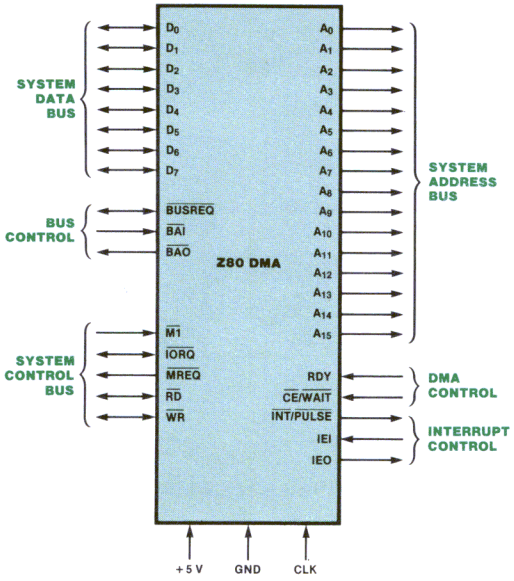


Figure 1. Pin Functions

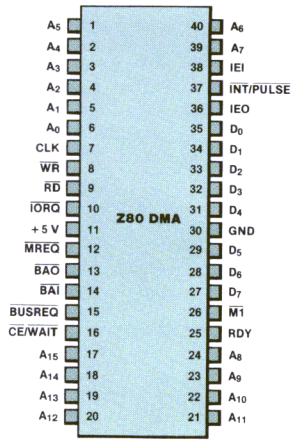


Figure 2. Pin Assignments

General Description (Continued)

The Z-80 DMA contains direct interfacing to and independent control of system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart, minimize CPU software overhead and help adapt the Z-80 DMA to memory, I/O and CPU environments. Figure 3 in the Z-80 CPU Product Brief illustrates a typical Z-80 Family environment which includes the Z-80 DMA.

The Z-80 DMA is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic or ceramic DIP. It uses a single +5 V power supply and the standard Z-80 Family single-phase clock.

Functional Description

Classes of Operation. The Z-80 DMA has three basic classes of operation as shown in Figure 3:

- Transfers of data between two ports
- Searches for a particular 8-bit maskable byte at a single port in memory or an I/O peripheral
- Transfers with a simultaneous search between two ports

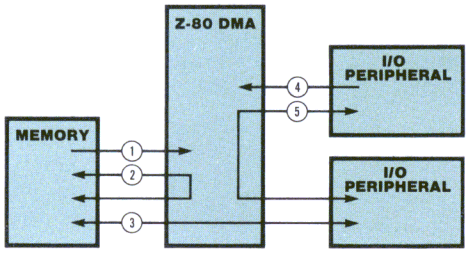
During a transfer, the DMA assumes control of the system address and data buses. Data is read from one addressable port and written to the other addressable port, byte by byte. The ports may be programmed to be either system main memory or peripheral I/O devices. Thus, a block of data may be written from one peripheral to another, from one area of main memory to another, or from a peripheral to main memory and vice versa.

During a search-only operation, data is read from the source port and compared byte by byte with a DMA-internal register containing a programmable match byte. This match byte may optionally be masked. Search rates up to 1.25M bytes per second (Z-80 DMA) or 2M bytes per second (Z-80A DMA) can be obtained.

Data transfers or searches can be programmed to stop interrupt under various conditions, and CPU-readable status bits can be programmed to reflect the condition.

Modes of Operation. The Z-80 DMA can be programmed to operate in one of three transfer and/or search modes:

- *Byte-at-a-Time:* Between each byte operation the system buses are released to the CPU. The buses are requested again for each succeeding byte operation.
- *Burst:* data operations continue until a port's Ready line to the DMA goes inactive. The DMA then stops and releases the system buses after completing its current byte operation.
- *Continuous:* data operations continue until the end of the programmed block of data is reached before the system buses are released. If a port's Ready line goes inactive before this occurs, the DMA simply pauses until the Ready line comes active again.



1. Search memory
2. Transfer memory-to-memory (optional search)
3. Transfer memory-to-I/O (optional search)
4. Search I/O
5. Transfer I/O-to-I/O (optional search)

Figure 3. Basic Functions of the Z-80 DMA

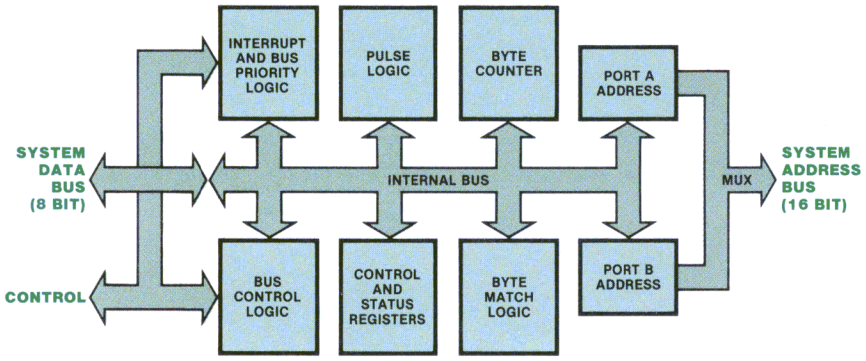


Figure 5. Block Diagram. All registers are 8 bits wide.

Z-UPC/U Universal Peripheral Controller

Zilog

Product Brief

August 1980

Features

- Complete slave microcomputer, for distributed-processing use.
- Unmatched power of Z8 architecture, instruction set.
- Three programmable I/O ports, two with 2-wire handshake, or any combination of data and control lines.
- Six levels of priority interrupts to Z-UPC/U.
- Two programmable 8-bit counter/timers with 6-bit prescalers.
- 256-byte register file, accessible by both master CPU and Z-UPC/U, as allocated by Z-UPC/U program.
- 2K bytes of on-chip program ROM for efficiency, versatility.

Description

The Z-UPC/U Universal Peripheral Controller is a distributed microcomputer that can perform the basic interfacing functions needed to interface a CPU with peripherals: device control by ROM-resident internal software, data manipulation (reformatting, arithmetic, etc.) and data buffering in internal registers.

The Z-UPC/U is similar to the Z8 microcomputer and uses the Z8 instruction set. Under program control, its three 8-line I/O ports can be tailored to the needs of its user. Permanently configured as a single-chip controller with 2K bytes of internal ROM, the Z-UPC/U executes instructions in 2.2 μs average using a 4-MHz clock source. Its register file contains 256 bytes, of which 234 are general-purpose registers, 19 are status and control registers, and three are port registers.

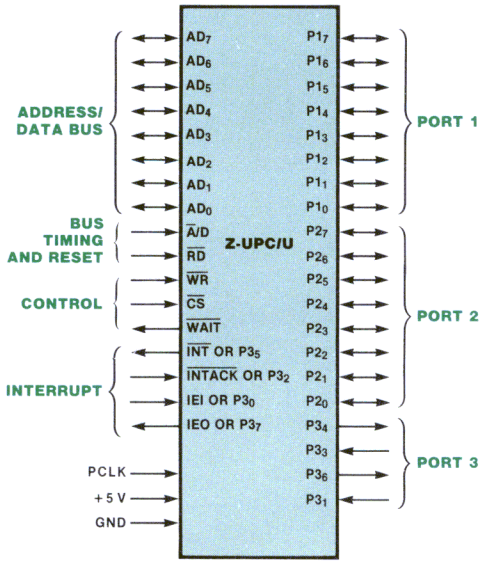


Figure 1. Pin Functions

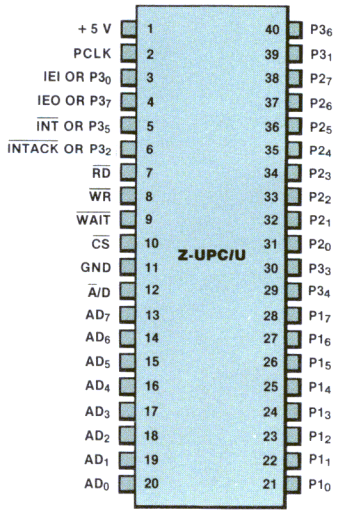


Figure 2. Pin Assignments

Description (Continued)

The Z-UPC Universal Peripheral Controller is an intelligent device that generates all the control signals peripheral devices need. Because it does off-line arithmetic, translates data before transmitting, and buffers data, the Z-UPC unburdens the master CPU, thereby increasing the overall speed and efficiency of the system in which it resides.

Based upon the Z8 microcomputer architecture, the Z-UPC offers fast execution time, efficient use of memory, and sophisticated interrupt, I/O, and bit manipulation. Its powerful and extensive instruction types, combined with its efficient internal register addressing scheme, not only speeds program execution, but also efficiently packs program into the on-chip ROM.

A unique characteristic of the Z-UPC is its register file, which contains I/O port and control registers that can be accessed both by the Z-UPC program and by its associated master CPU. This results in byte efficiency, programming efficiency, and address space efficiency because Z-UPC instructions can operate directly on I/O data without moving it to and from an accumulator. It also allows the Z-UPC user to allocate as data buffer between the CPU and the peripheral all register space not in use as accumulators, address pointers, index registers, or stack. Registers not used as buffer are protected against CPU access. The register file is divided into 16 groups of 16 working registers each. A register pointer uses fast, short-format instructions to access any one of these groups quickly, resulting in fast and easy task switching. Two-way communication between the master CPU and the register file is facilitated by another pointer that positions 16 interface registers anywhere within the register file. These registers are accessed directly by both the master CPU and the slave Z-UPC. Four more registers, similarly accessed, convey control and status information.

All of Zilog's daisy-chained priority interrupt system can be implemented in the Z-UPC under software control, or the Z-UPC can be programmed to function in a polled environment. In all, the Z-UPC has 24 pins that can be dedicated to I/O functions. Grouped logically into three 8-line ports, they can be programmed in many combinations of inputs, outputs, and bidirectional lines, with or without handshake and with push-pull or open-drain outputs.

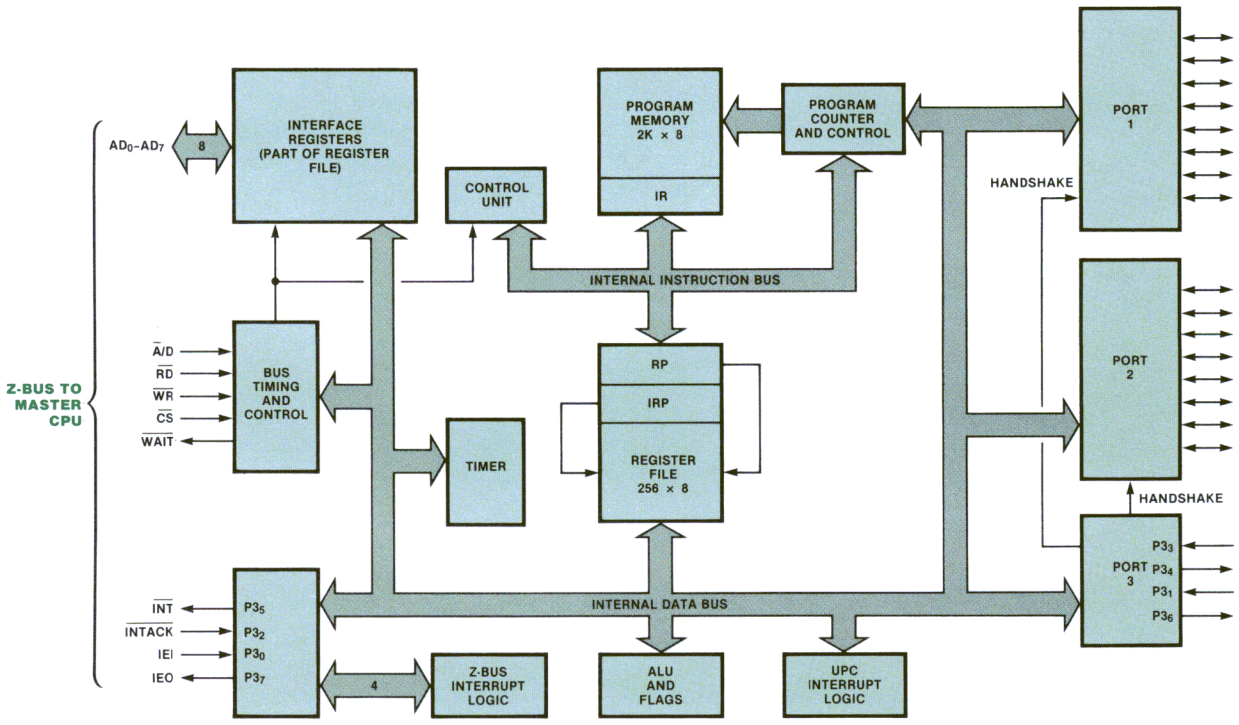


Figure 3. Functional Block Diagram

Z-CIO/U Counter/Timer and Parallel I/O Unit

Zilog

Product Brief

August 1980

Features

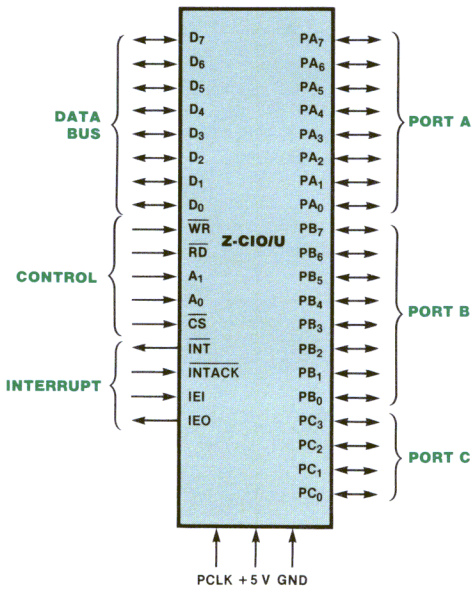
- Two independent 8-bit double-buffered bidirectional I/O ports plus a special-purpose 4-bit I/O port
- Four handshake modes including 3-wire (like the IEEE-488) and Wait/Ready line for high speed data transfer
- Three independent 16-bit counters
- All registers read/write and directly addressable
- Flexible pattern recognition logic

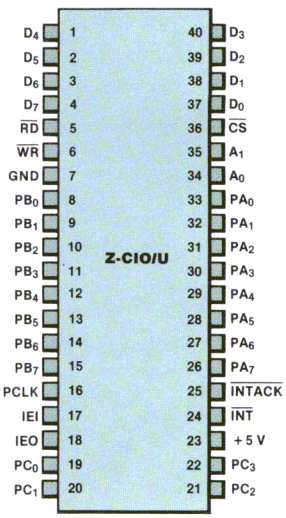
Description

The Z-CIO Counter/Timer and Parallel I/O element is a general purpose peripheral circuit that satisfies most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable.

Either 8-bit I/O port can be a handshake byte port or a bit port. In the bit mode, data direction is programmable bit by bit. In the handshake mode, the ports can be input, output, or bidirectional, and they may be linked to form a 16-bit port. The four handshake modes include 3-wire (like IEEE-488), interlocked (for interfacing to a Z-UPC, Z-FIO or another Z-CIO), strobed and pulsed. The pulsed mode connects one counter/timer with the handshake logic for interfacing a mechanical device such as a printer. The 4-bit port provides handshake controls, special controls (Wait/Request) or general-purpose I/O.

The counter/timer section contains three 16-bit counters, two of which can be software configured as a 32-bit counter/timer. Up to





Description (Continued)

four I/O lines for each counter are available for direct external control and status information. All counters have a programmable output duty cycle, continuous or single-cycle operation, and the counting process can be programmed to be either retriggered or nonretriggered.

The two general-purpose 8-bit ports are similar. They can be programmed as handshake driven, double-buffered ports (input, output, or bidirectional) or as control ports in which the direction of each bit is individually programmable. Port B can also be specified to provide external access for two of the counter/timers. Each port includes pattern recognition logic allowing interrupt generation when a specified pattern is detected. The pattern recognition logic can be programmed so that the port functions like a priority interrupt controller.

To control these capabilities, each port contains 13 registers. Three of these, the input, output, and buffer registers, are data path registers. Two others, the mode specification and handshake specification registers, define the mode of the port and specify what handshake to use, if any. The reference pattern for the pattern recognition logic is defined in three registers, the pattern polarity, pattern transistion, and pattern mask registers. The detailed characteristics of each bit path (for example, the direction of data flow, or whether a path is inverting or noninverting) are programmed using the data path polarity, data direction, and special I/O control registers. The primary control and status bits are grouped in a single register so that after the ports are configured initially, only this register need be accessed often. One register contains the interrupt vector associated with each port. To facilitate intialization, the port logic is designed so that if a capability of the port is not required the registers associated with that capability are ignored and need not be programmed.

The function of Port C depends upon the roles of Ports A and B. Port C provides handshake lines for the other two when required. Any bits of Port C not so used can be used as I/O lines or as external access to the third counter/timer.

Besides the data input and output registers, three registers are needed. These specifiy the details of each bit path: data path polarity, data direction, and special I/O control.

The three counter/timers are all identical. Each is composed of a 16-bit down-counter, a 16-bit time constant register (which holds the value loaded into the down-counter), a 16-bit current count register (used to read the contents of the down-counter), and two 8-bit registers for control and status (the mode select and control registers). All three share a common vector register.

Each counter/timer can be programmed as either counter or timer. Up to four port I/O lines can be designated as external access lines for it. The lines are: Counter Input, Gate Input, Trigger Input, and Counter/Timer Output. Three different counter/timer output duty cycles are available: pulse, one-shot, or square wave. The operation of the counter/timer can be specified to be either single cycle or continuous. The counting sequence may be retriggered or nonretriggered, under program control.

Z-FIO
FIFO Input/Output Interface Unit

Zilog

Product Brief

August 1980

Features

- Asynchronous bidirectional FIFO buffer, used with most major microprocessors as CPU/CPU or CPU/peripheral interface.
- Interlocked 2-wire or 3-wire handshake port mode; Empty, Full, and Request/Wait lines for high-speed data transfer.
- 128 x 8 organization, expandable to any width; cascadable to any depth.
- Preset byte count in FIO buffer can interrupt CPU.
- All registers directly addressable.
- Vectored/non-vectored interrupts on pattern/status match, over/underflow error, buffer status.

Description

The Z-FIO is a general-purpose microprocessor interface that provides elastic buffering between asynchronous CPUs in a parallel-processor network or between CPU and peripheral circuits. The Z-FIO can interface a Z-Bus microprocessor or any other major processor to another microprocessor or to a peripheral circuit or port.

In Z8000 systems, the FIO furthers distributed-processor operation because it can interconnect components or subsystems operating at different speeds. Also, it can increase system throughput by transferring words as well as bytes. This bidirectional device accepts data and holds it until it can be used by another device in the system. In most I/O transactions, introducing a 128-deep buffer cuts interrupt servicing overhead by two orders of magnitude.

The Z-FIO greatly facilitates system throughput by moving variable-size blocks under either direct memory access or interrupt control—an especially important consideration when fast peripheral circuits need interfacing. Complete status information is also provided for operation in polled environments.

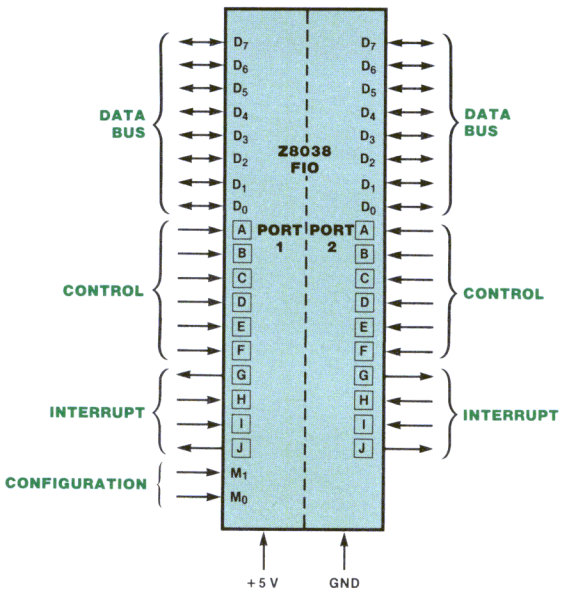


Figure 1. Pin Functions

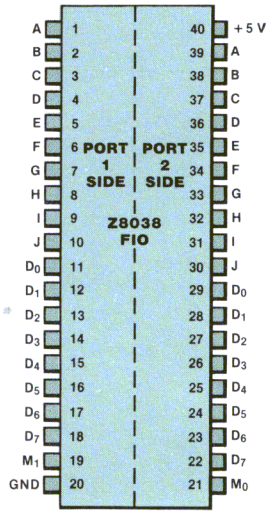


Figure 2. Pin Assignments

Pin Assignments

	Z-Bus Low Byte	Z-Bus High Byte	Non-Z-Bus	2-Wire HS Port*	3-Wire HS Port*
A	$\overline{REQ}/\overline{WT}$	$\overline{REQ}/\overline{WT}$	$\overline{REQ}/\overline{WT}$	RFD/$\overline{DAV}$	RFD/$\overline{DAV}$
B	$\overline{DMASTB}$	$\overline{DMASTB}$	$\overline{DACK}$	ACKIN	$\overline{DAV}$/DAC
C	$\overline{DS}$	$\overline{DS}$	$\overline{RD}$	FULL	DAC/RFD
D	R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$	EMPTY	EMPTY
E	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	CLEAR	CLEAR
F	$\overline{AS}$	$\overline{AS}$	C/$\overline{D}$	DATA DIR	DATA DIR
G	$\overline{INTACK}$	A_0	$\overline{INTACK}$	IN_0	IN_0
H	IEO	A_1	IEO	OUT_1	OUT_1
I	IEI	A_2	IEI	$\overline{OE}$	$\overline{OE}$
J	$\overline{INT}$	A_3	$\overline{INT}$	OUT_3	OUT_3

*Port 2 side only. See table below.

Description (Continued)

The internal functions of the Z-FIO are shown in the block diagram (Figure 3). It is made up of two ports that are identical except for programming. The port programmed by pins M_0 and M_1 is called Port 1; the port programmed by bits B_0 and B_1 is called Port 2.

Each port of the FIO has sixteen programmable registers that define operating protocols and pin signals. Common to both ports, and situated between them, is the 128 × 8 RAM used for data storage. The RAM is capable of simultaneous, independent read and write operations. This means, for example, that the Port 1 CPU can write a byte of data into the FIO without disturbing a simultaneous read operation by the Port 2 CPU. The outputs of the read and write counters are used to address the buffer RAM, and also are fed into a subtractor to determine the current number of bytes in the memory. This number can be read by either CPU from a status register dedicated to each port. Another programmable register is compared against the status register to generate interrupts and/or start and stop DMA transfers. A pair of port registers allows for communication between CPUs, bypassing the main buffer memory.

Operating Modes. The Z-FIO has twelve different programmable modes (Table below). The states of two package pins determine the mode of operation of Port 1, and Port 2 is programmed by two bits (B_0 and B_1) in one of the Port 1 control registers.

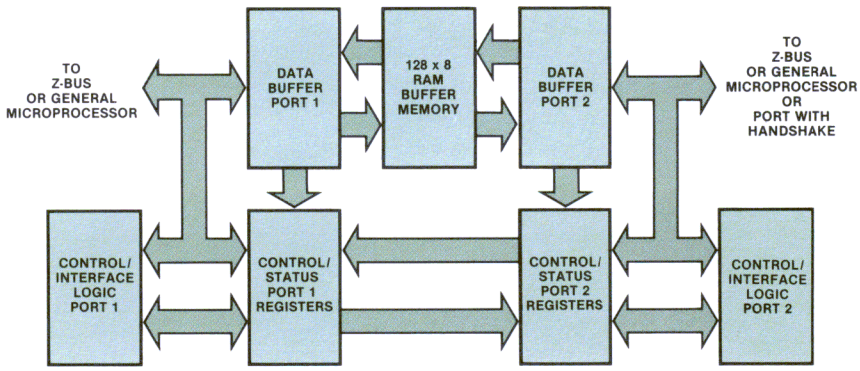
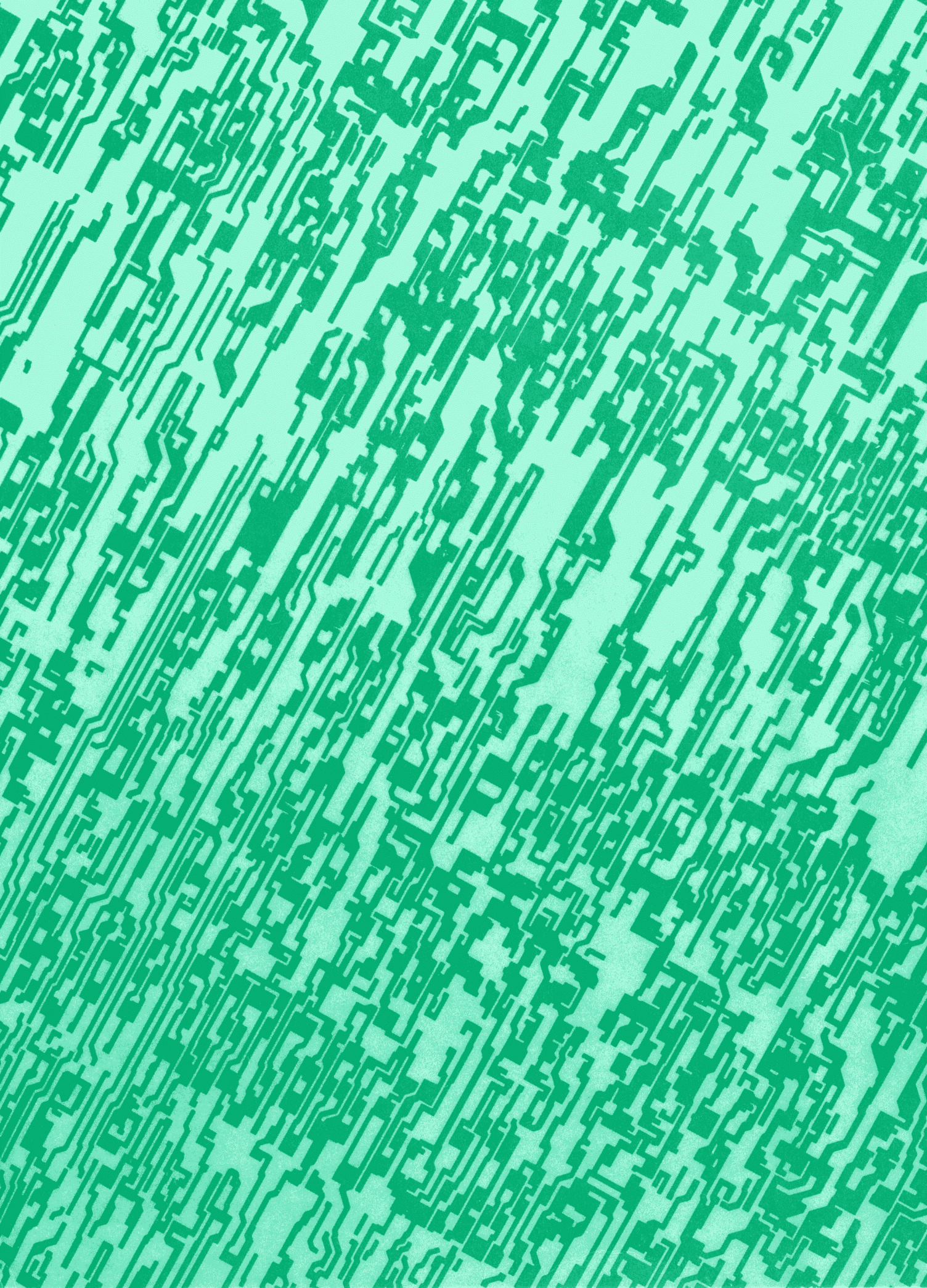


Figure 3. Functional Block Diagram

Operating Modes

Mode	M_1	M_0	B_1	B_0	Port 1	Port 2
0	0	0	0	0	Z-Bus Low Byte	Z-Bus Low Byte
1	0	0	0	1	Z-Bus Low Byte	Non-Z-Bus
2	0	0	1	0	Z-Bus Low Byte	3-Wire HS
3	0	0	1	1	Z-Bus Low Byte	2-Wire HS
4	0	1	0	0	Z-Bus High Byte	Z-Bus High Byte
5	0	1	0	1	Z-Bus High Byte	Non-Z-Bus
6	0	1	1	0	Z-Bus High Byte	3-Wire HS
7	0	1	1	1	Z-Bus High Byte	2-Wire HS
8	1	0	0	0	Non-Z-Bus	Z-Bus Low Byte
9	1	0	0	1	Non-Z-Bus	Non-Z-Bus Low Byte
10	1	0	1	0	Non-Z-Bus	3-Wire HS
11	1	0	1	1	Non-Z-Bus	2-Wire HS



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