MAY 20, 1983

## MAILING LIST FOR HP MICROCOMPUTER BUILDERS:

| | | | |
|---|---|---|---|
| D POCIUS | 11L | D NUNGESTER | 2I |
| S HOFFMAN | 11L | A GREEN | 35 |
| M HODAPP | 11L | D VAWTER | 3US |
| W BECKETT | 11L | D LEE | 47U |
| M BUTTERWORTH | 11L | T WATANABE | 47U |
| M PIRAMOON | 11U | T BOYLE | 47U |
| J KIM | 11U | D OLLINS | 47U |
| D VANDERWATER | 11U | B SCHUCHARD | 47L |
| B WARD | 11U | S ERNST | CTD |
| J THOMPSON | 11U | C WEI | 10 |
| C SMITH | 12 | M GREEN | 10 |
| V MARIAN | 12 | S JOINER | 10 |
| H WILSON | 42L | D HARDING | 52U |
| J YOUDEN | 42U | R BURRELL | 53U |
| K HICKOX | 42L | R FROID C/O B GARCIA | 5L |
| B GOODMAN C/O K HICKOX | 42L | K TOBIN | 5L |
| T GILDEA | 18 | B GARCIA | 5L |
| W HINTON (IBM) | 20CH | P ZANDER | 5M |
| R RANDALL | 20BD | J SOCHA C/O C FRANK | 5M |
| J ENGELHARDT | 20BR | G THOMAS C/O P ZANDER | 5M |
| L CUTLER | 25 | N LYONS | 5M |
| D WEIGEL | 25U | J VADEBONCOEUR | 5U |
| L KIYAMA | 25 | K LANE | 5U |
| R DINKEY | 25U | S THOMAS | 5U |
| G HARKINS | 25U | P GRAY | 5U |
| K BATES | 28C | D NELSON | 30 |
| B KNAPP | 28A | R PINGER | 30 |
| D LIDDEL | 28B | D PUNG | 90U |
| D MOBERLY | 28B | B LEWIS | 90L |
| R WALKER | 3U32 | R WONG | 9E |
| S HESSEL | 3U32 | L ROBERTSON | 8U |
| E LITTAU | 1U | L STAFFORD | 6L |
| R MCBRIDE | RB-1 | M TALLMON | 6L |
| B WELLS | | | |

## GENERAL NEWS:
May 20, 1983

The memory boards are completed and distributed.  Included
in this newsletter is a copy of the final engineering report.

The disc controller boards are assembled and testing has begun.
The boards are 90% functional, but there remains a noise problem
with a few controller functions.  Several modifications have been
suggested to correct these problems and they are now being implemented.

The terminator board has been layed out (taped) and PCB prototypes
should soon be ready for testing.

...Most members should soon have a running system and the need
for software development is rising.  If you would like to help out on
the software committee, contact Barry Lewis at 1-163-2601.

Work is underway on video boards.  The club will soon make two
official offerings: the first is the CAT-100 board and the second is
the WAMECO CRT-1 board.  The writeup on these boards was too late to
include  in this newsletter, but will be distributed sometime next
week. ...These boards will really nicely round out the club system.

There will be a club meeting in the 5M-2 conference room the
the last Wednesday of every month.  These informal meetings will be
open to all interested members.  The first regular meeting will be
held May 25 and the topic of discussion will be hardware.  Mark your
calendars!

## FOR SALE OR TRADE:

Cabinet hardware, fully loaded motherboard, front panel board,
Schematics. Best offer. Telnet 857-6825 ...Steve Hoffman

Keyboard (+cover), power supply, cabinet, motherboard (12 connectors)
front panel board, CPU board, schematics and notes. All HPMCIG
hardware, brand new.  $350/Best offer. Telnet 922-3387 or
(509) 926-9048 ...Dick Nungester Bldg. 2I (Spokane)


## HP MICROCOMPUTER INTEREST GROUP OFFICERS:

| | | | |
|---|---|---|---|
| Moderator | Rick Pinger | 30 | 969-0880 |
| Treasurer | Doug Pung | 90 | 1-263-2655 |
| Hardware Committee Chairman | Steve Hessel | 3U | x5514 |
| Software Committee Chairman | Bob Wells | (408) | 255-5027 |
| Meeting Coordinator | | | |
| Newsletter Editor | Rick Walker | 3U | x3754 |

# Memory Board Final Engineering Report

This report is intended to inform all club members of
the problems encountered with the memory board, the changes made to
solve them, the testing performed on all boards, and the final status
of the project.  The majority of the engineering work done on this
board was done by Steve Hessel, Paul Zander, Doug Pocius, and myself;
any questions should be addressed to one of us.

- Dave Vanderwater, May 1983


## Board Features:


The club memory board is the Memory Merchant MM65K16S rev 3
board, a 64K byte static S-100 compatible memory board.  As it
was constructed by the club, this board should be capable of reliable
service at CPU speeds of at least 6 MHz (the boards were all tested
at 6.6 MHz).  These boards feature both extended addressing (24 bit
addressing), and I/O mapped bank selecting for systems containing
more than 64K of memory.  In addition these boards can be jumpered
to respond to PHANTOM (necessary when used with the CCS disc controller
board).
One feature that exists, but we recomend that it not be used,
is the selective disable of a 2K segment of memory.  When this feature
is used, the output buffer on this memory board will be enabled for a
short time early in any buss cycles that would read from this memory.
It is only latter in the cycle that it is possible to turn off this
buffer (the why will become apparent farther on down).  The possibility
therefore exists of having 2 buffers (one on this board, and one on
annother board) enabled at the same time.  Obviously, 2 buffers
fighting for the buss like this will generate a lot of excess
noise.


## Standard Board Jumper Configuration

This configuration is for a standard club system, containing
a single 64K memory board.

```
J1 - shorted   to make the lower bank recognize phantom
J2 - shorted   to make the upper bank recognize phantom
J3 - shorted   to select I/O mapped bank selecting
J4 - shorted   to enable lower bank
J5 - open
J6 - shorted   to enable upper bank
J7 - open

switch 1C -      positions 6,7  on
                 positions 1,2,3,4,5,8  off
switch 5D -      positions 1,2,3,6  on
                 positions 4,5,7,8  off
```

jumper areas A7 and A8 are not used (storage of spare jumpers).

## Description of Our Modifications to the Board:

When originally supplied by Memory Merchant, this board did not function in our system. The board improperly responded to an I/O write cycle by writing into memory. Additionally, a carefull timing analysis of the board indicated that it would not work reliably at 6 MHz. This board uses Programmable Logic Arrays (PLA's, or PAL's, or FPLA's) for almost all of the 'random' logic. By rearranging the logic in one of these PLA chips, we were able to solve these problems.

Instead of trying to decide if the current cycle is a memory cycle that this board should respond to, and then enabling the Chip Select (CS) line at the appropriate 6116 ram chip; we decided to enable the CS very early in all cycles, and then latter use the Output Buffer Enable (OBE) and the Write Enable (WE) pins to either complete the memory operation, or not as appropriate. This allowed the overall timing to be determined by the faster ram response to the OBE and the WE signals. To accomplish this we simply rearranged the contents of the 82S100 chip (ic 6C on your schematic). Several listings of the contents of this chip are included with the supplemental manual that you should have recieved with your board.

After the 82S100 had been reprogrammed, there remained one problem with the board function. The signal from the 82S100 (pin 12) that controlled the WE at the 6116 array also controlled the input buffer enable (ic 11D pins 1,19). If the I/O mapped bank selecting is to be used, the information on the data buss must get through this buffer to the 16L2 PLA chip (ic 16D on your schematic). Obiviously our method of using this line to prevent memory write during I/O cycles will also prevent the data from reaching this PLA during a valid I/O write to the control port.

To solve this problem, we made use of a previously unused output (pin 13) on the 82S100 PLA to enable the input buffer independently of the 6116 array operations. This change required that one trace be cut on the back of your boards, and a jumper be added. The schematic in the Memory Merchant manual does not reflect this change (it is included on the much more readable schematic in the supplemental manual).

## Testing of the Boards

All memory boards supplied loaded with chips were tested. A listing of the test routine is attached. The test was performed from RAM (you have to test an op-code fetch cycle) with the CPU running at 6.6 MHz (10% margin at 6 MHz). No serious problems were encountered, in fact one board loaded with 150 ns chips passed (all standard boards have 120 ns chips).

## Final Status of Boards

All boards tested 100% functional at speed (we didn't even find any bad chips)! All boards distributed.

```
;
;           Memory test routine
;
;
;
            ld      hl,(00f0h)          ;get starting addr of memory to test
            ld      d,(00f2h)           ;get ending addr of memory to test
;
loop1:
            xor     a                   ;first clear out memory
            ld      (hl),a
            inc     hl
            ld      a,h
            cp      d
            jp      nz,loop1
;
;           run first pass with aah as the test value
;
            ld      de,00aah
;
;           main loop begins here
;
;
loop:
;
;           routine first checks all memory for proper value
;
            ld      hl,(00f0h)
loop2:
            ld      c,(hl)
            ld      a,d
            cp      c
            call    nz,error
            inc     hl
            ld      a,(00f2h)
            sub     h
            jp      nz,loop2
;
;           now check each location for 'cross' errors by writing
;           all bit patterns there (while all other memory should
;           not be affected)
;
            ld      hl,(00f0h)
loop3:
            ld      c,(hl)              ;first check location for proper value
            ld      a,d
            cp      c
            call    nz,error
            xor     a                   ;now clear a
loop4:
            ld      (hl),a              ;write a pattern
            ld      c,(hl)              ;read it back
            cp      c
            call    nz,error
            cpl                         ;compliment pattern
            ld      (hl),a              ;write that
            ld      c,(hl)              ;read it back
            cp      c
            call    nz,error
            cpl                         ;restore pattern
            inc     a
            jp      nz,loop4            ;try all patterns
;
```

```
        ld        (hl),e              ;leave proper next value
        inc       hl
        ld        a,(00f2h)
        sub       h
        jp        nz,loop3            ;do next location
;
;       now print out value to indicate proper function, and continue
;       untill stopped from front panel
;
        ld        (sp),de             ;save values
        ex        hl,de               ;put values in de
        call      (0f5fbh)            ;use monitor routine to print
        ld        de,(sp)             ;restore values
        ld        d,e
        inc       e                   ;set up next values
        jp        loop
;
;       print out error message
;
error:
        ld        (sp),af
        xor       c
        call      (0f2a1h)            ;use monitor to do the printing
        ld        af,(sp)
        ret
```