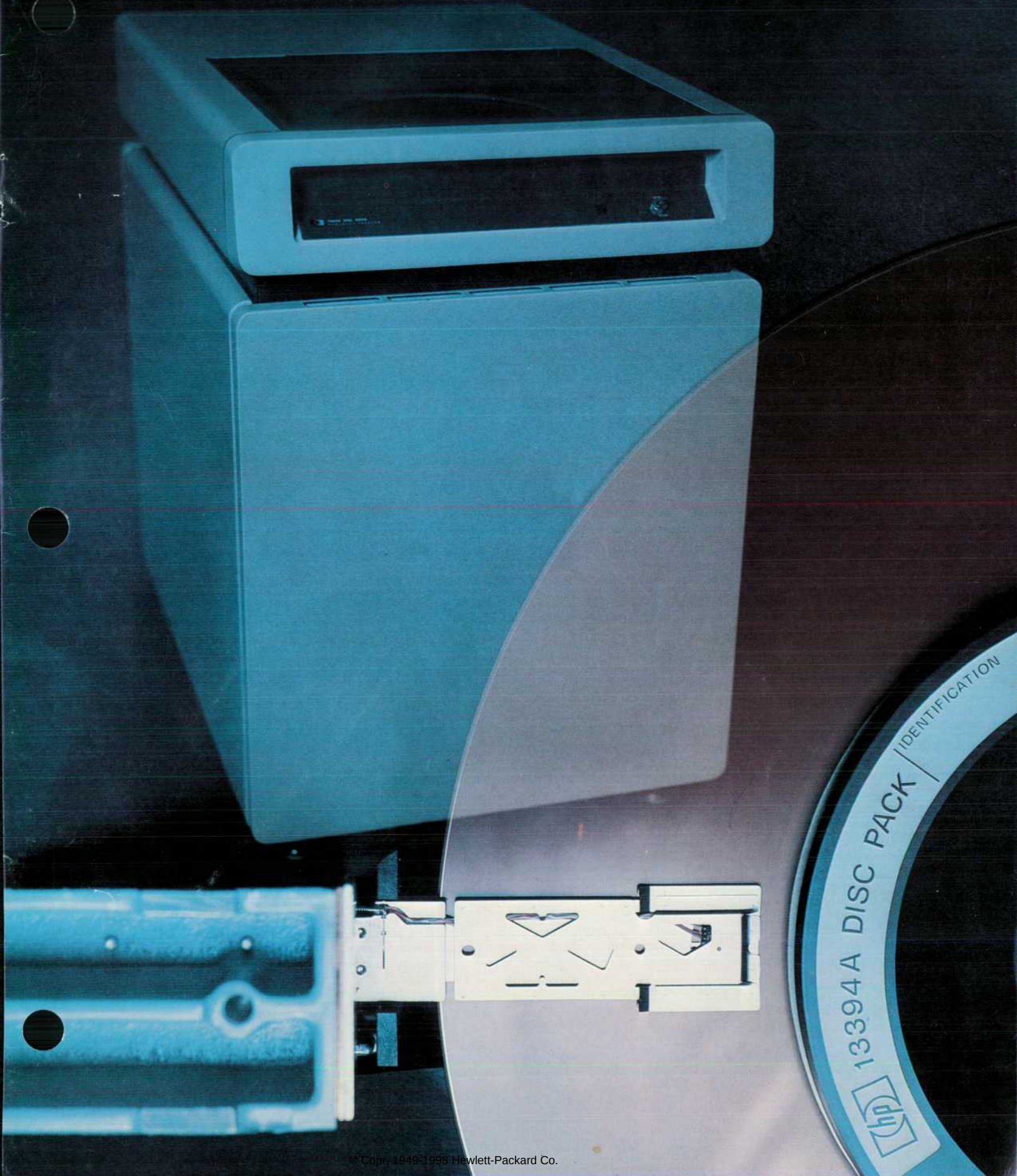
AUGUST 1977

HEWLETT-PACKARD JOURNAL



New 50-Megabyte Disc Drive: High Performance and Reliability from High-Technology Design

Achieving its high performance and large storage capacity required sophisticated design methods and tested the known limits of some manufacturing processes.

by Herbert P. Stickel

THE PRINCIPAL DESIGN OBJECTIVE for the new Model 7920A Disc Drive (Fig. 1) was to provide a 50M-byte formatted storage capacity for the HP 3000 2000, and 1000 computer families. Desired characteristics were fast data access times, high reliability, low maintenance requirements, and a friendly man-machine interface. Other important objectives were disc pack interchangeability over a wide range of environmental conditions, data integrity, and easy manufacturability.

The new drive has a maximum track-to-track seek time of 5 milliseconds and an average seek time of 25 milliseconds. The five-disc removable disc pack is scanned by voice-coil actuated heads under feedback control using track-following techniques. The unit operates at temperatures between 10°C and 40°C (50°F to 104°F) and humidities up to 80%. The direct spindle-drive motor maintains constant speed at all power-line frequencies between 47.5 Hz and 66 Hz.

Fig. 1. *Model 7920A Disc Drive provides a 50M-byte formatted storage capacity for HP 1000, 2000, and 3000 Computer Systems. Average access time is 25 milliseconds. Up to eight drives can be interfaced to one disc controller.*

Within this complete range disc pack interchangeability is guaranteed.

The 7920A Disc Drive is available for HP 1000, 2000 and 3000 Computer Systems. It can be connected to the controller used with earlier 15M-byte 7905A Disc Drives. As many as eight disc drives, 7905As and 7920As in any combination, can be connected to one controller. The controller can communicate with as many as eight computers with limited software operating system support.

Fig. 2 shows the interior of the new drive.

Achieving 50M-Byte Capacity

Existing HP drives are the 7900A[1] and the 7905A

Cover: *Model 7920A Disc Drive is pictured in a double exposure with its disc pack and one of its read/write heads. The disc pack consists of two protect discs and three data discs and holds 50 megabytes of data. Average seek time is 25 ms.*

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Fig. 2. *Interior of 7920A Disc Drive, showing the linear motor (voice coil) that moves the heads. Mechanical design emphasis was on simplicity, reliability, and accessibility.*

Disc Drives. The 7900A has a 5M-byte capacity on two discs, one fixed and one removable. It uses an optical encoder for head positioning.

The 7905A has a 15M-byte capacity, also on one fixed disc and one removable disc. Its higher capacity is the result of higher track density and higher bit density. Instead of an optical encoder, the 7905A uses one of the surfaces of its fixed disc for head positioning purposes. On this surface are precisely prerecorded servo tracks that are used by the head-positioning servomechanism to position the read-write heads over the chosen data tracks. As track density is increased beyond the 7900A value of 100 tracks per inch the optical positioning scheme runs into differential thermal expansion problems, and the servo track positioning method overcomes these difficulties. The 7905A has a track density of 196 tracks per inch.

The 50-megabyte capacity of the new 7920A Disc Drive was achieved by increasing the number of data discs and increasing the track density. The bit density is the same as the 7905A's.

The 7920A track density is 384 tracks per inch. The corresponding track-to-track spacing of 0.002604 inch required careful design of the tolerances of all components between the magnetic centerline of the flying heads and the tracks on the disc coating (usually called the *media*). Analysis of the tolerance loop revealed that the heads had to move radially over the disc surface (in-line heads) instead of along the customary line displaced from the radius (chordal displacement heads).This confronted the design team with the challenge of fitting two heads without offset into the 0.300-inch space between two adjoining disc surfaces (Fig. 3). Thinning down the head structure required thinning the flying head element and the head support structure without increasing its mass or sacrificing rigidity. At the same time it was essential to prevent harmful head resonances on this new head design. Making the tracks narrower entailed making the head sensing element narrower without deteriorating its electrical characteristics.

Similar effort went into the analysis of the disc pack, which has three data discs (one surface containing the servo tracks) and two protect discs. Commercially available disc packs were analyzed for electrical performance and the topographical characteristics that determine head electrical output and head flyability.

Head and Media Development

Much work went into the head design and media interface analysis to assure reliable data transfer and media life. Important requirements are head flight stability, adequate signal-to-noise ratios, and minimum data timing shifts.

As a coarse approximation we can assume that head-media noise is all media noise and that the better the ability of the head-media system to record and read the highest and lowest frequencies in the data waveform the smaller the timing shift produced. The ratio of the amplitude of the highest frequency to the amplitude of the lowest frequency at any location on

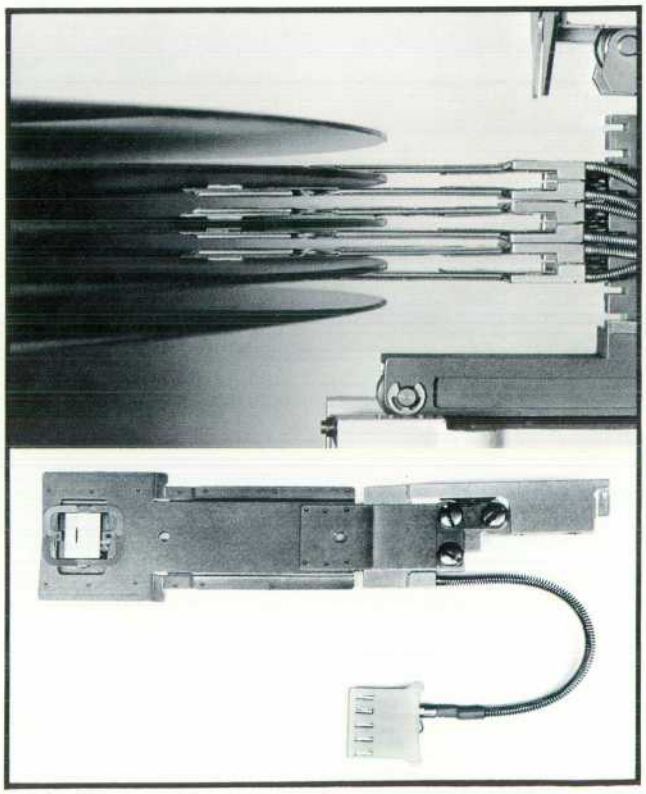


Fig. 3. *7920A Disc Drive uses in-line heads instead of the more usual chordal displacement heads. Thinner heads had to be designed to fit between discs.*

the disc is defined as resolution. We strive for high ratios bounded by both high and low limits to control timing shifts. Typically, the worst resolution on the disc is 75%.

High outputs and high resolutions do not go hand in hand. Making the oriented-particle-oxide media thick raises output and minimizes defects in the coating, simply because there is more effective magnetic material per unit volume. The thicker the media the poorer the resolution and the higher the write currents required. Conversely, by making the coating thinner, resolution can be improved, but noise and output suffer, and the number of defects in the oxide coating increases.

It is desirable to fly heads high to reduce the possibility of "head crashes" stemming from air contamination. However, output and resolution suffer. The loss for the space between the transducer in the flying head and the media is $(-55\ \text{dB})/\lambda$, where λ is the recorded playback wavelength. Increasing flying height lowers the head output at all frequencies, but the higher frequencies degrade more because λ is smaller, so the resolution is reduced.

The 7920A head flying height and oxide thickness were selected within these bounds to give the best resolution with adequate output.

In redesigning for a thinner head support structure the problem of arm resonance had to be resolved. One major excitation is the recording surface itself. The surface of a recording disc is not absolutely flat, and if the magnitude and periodicity of the surface undulations are in the proper relationship, a head arm or servo loop resonance may be stimulated. This leads to degraded data recovery, servo instability, and head-to-disc collisions (Fig. 4). The higher-frequency components of the media surface motion are on the order of only a few microinches, but in an improperly designed system, they are sufficient to excite the resonance to the point of head crashing.

Early in the project, head-media incompatibility caused the track-follower servo loop to generate a high-pitched audio tone. Measurement showed spikes in gain for the track-follower error signal at 1.7 kHz and 5.1 kHz. The problem was isolated using the HP 5451B Fourier Analyzer. The closed-loop transfer function for the entire electrical and mechanical servo system was determined. From this data, the open-loop transfer function was computed and stability information derived. Each mechanical component's open-loop transfer function was examined until the cause of the high-pitched audio tone was traced to the motion of the head gimbal in the radial direction of the disc. The resonance characteristic of the head gimbal was changed by suitably redesigning the gimbal. In the new design the resonance frequency was shifted and its amplitude reduced, thus eliminating the parasitic resonance.

Steady-state flying stability is not the whole story; the head loading process is also critical. The heads are loaded onto the discs while the discs rotate at 3600 r/min. At the time of landing the outer edge of the disc is traveling at about 140 mi/hr with respect to the

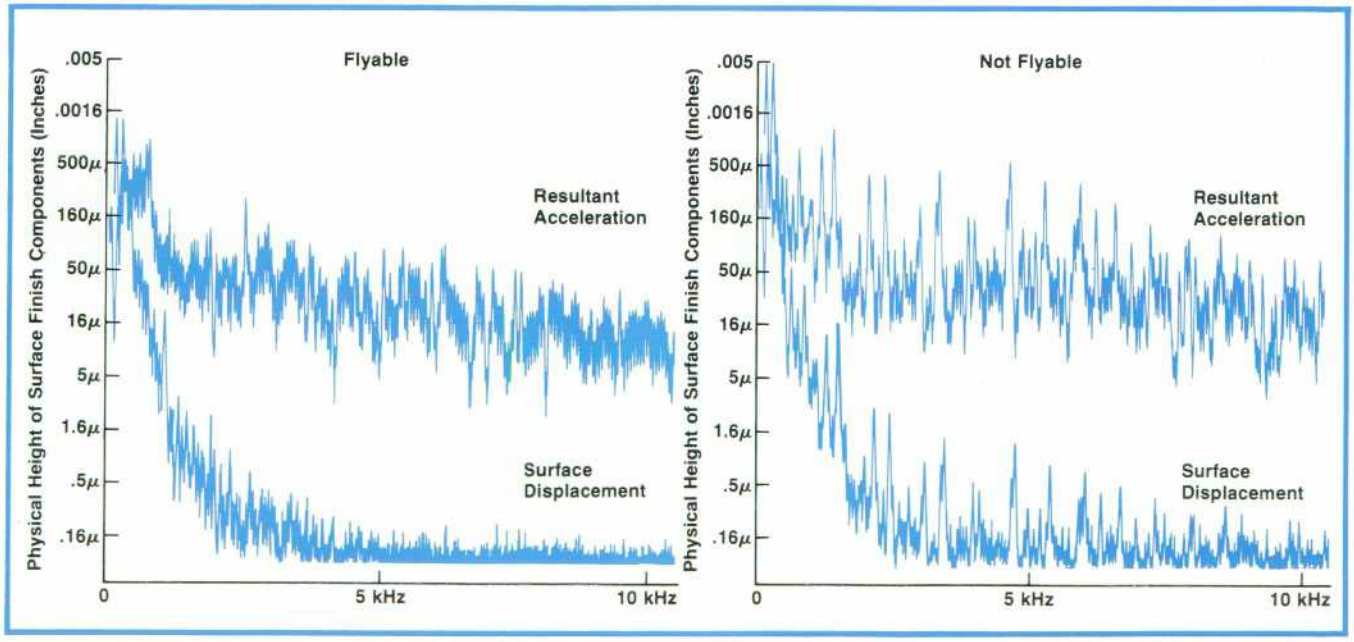


Fig. 4. *Disc surface undulations can cause head accelerations that lead to head-disc crashes. Shown here are flyable and non-flyable head-disc combinations. Head-media compatibility in the 7920A Disc Drive was investigated using an HP Fourier Analyzer to measure the transfer functions of various system components.*

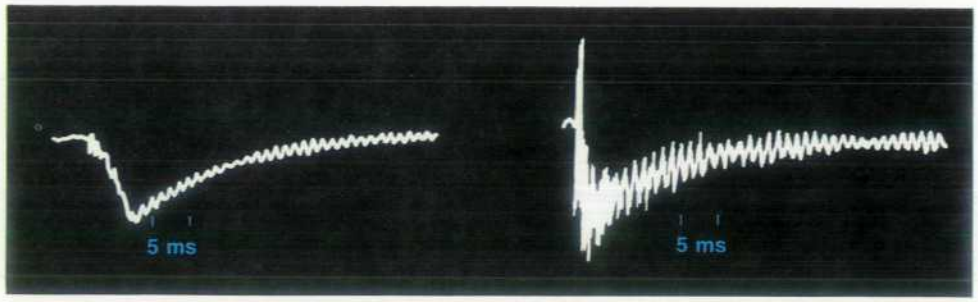


Fig. 5. *Head seating and settling were investigated using heads with sliders containing crystal accelerometers. Desirable output at left shows rapid seating and settling times. Output at right shows hard impact of the slider on the disc, slow seating, and long periods of ringing.*

head. The head geometry, the pitch and roll of the slider, and the loading velocity must all be carefully controlled to assure smooth non-abrasive loading. The seating and settling times were investigated using heads with sliders that had crystal accelerometers within them.

Fig. 5 shows desirable and undesirable loading characteristics. The output on the left shows rapid seating and settling times. The output on the right shows hard impact of the slider on the disc, slow seating, and long periods of ringing before the behavior of the heads is controlled.

To assure continued performance, worst-case data and servo-signal testing is done on each disc pack. Disc pack certifying drive systems in HP manufacturing facilities test the margins of the data recovery performance of each pack to make certain that all disc packs will perform in all drives over the specified temperature range. Similarly, careful in-house construction and testing of the HP-designed heads assures quality in these parts.

Head-to-Media Tolerance Loop

To transduce data reliably the read/write heads must be positioned over the data tracks within certain accuracy limits. Fig. 6 shows that for the 7900A Disc Drive a deviation of 0.002 inch from track centerline would cause a degradation of 2 dB in the read-back signal. The same deviation for the 7905A Disc Drive results in a 4-dB degradation, and for the new 7920A Disc Drive, a 16-dB degradation. In practice we can allow only a small fraction of this deviation in the 7920A; this is because of the 0.002604-inch track spacing, the effects of noise from adjacent tracks, and tolerances between drives and between disc packs.

The maximum deviation from nominal track centerline that a head core can be allowed to move towards an adjacent track can be determined from a track shape analysis. To guarantee disc pack interchangeability between any two drives for data written at one temperature extreme and read at the other temperature extreme, the maximum allowable deviation cannot exceed 300 microinches in the x-y plane (ϵ_x in Fig. 7). This means that the sum of all of the individual components of this loop can not exceed this amount. Every change of one of the elements of the loop affects the sum of the remaining tolerances.

In-line heads greatly reduce off-track head positioning caused by roll and yaw motion of the carriage. To clarify this it helps to envision the actuator servo head being held on the centerline of the servo track and imagine what happens if the carriage, which holds the heads, experiences a roll, yaw, or pitch error caused by inaccuracies of the carriage rails. Since the heads move along a radial line from the center of the disc, roll and yaw contribute little to the amount that any data head is off track. Pitch of the carriage, however, will cause a data head tracking error ϵ_x proportional to the pitch angle θ_P and the distance of the data head from the servo head ($S_2 - S_0$).

The pitch error θ_P in the carriage motion is a function of the concentricities of the ball bearings b_1 and b_2 at the bottom of the carriage and the straightness of the rail r_1. The tolerance study yielded an allowable taper in the rail of 0.001 inch and a required flatness of the surface that supports rail r_1 of 0.0001 inch over the length of the carriage travel.

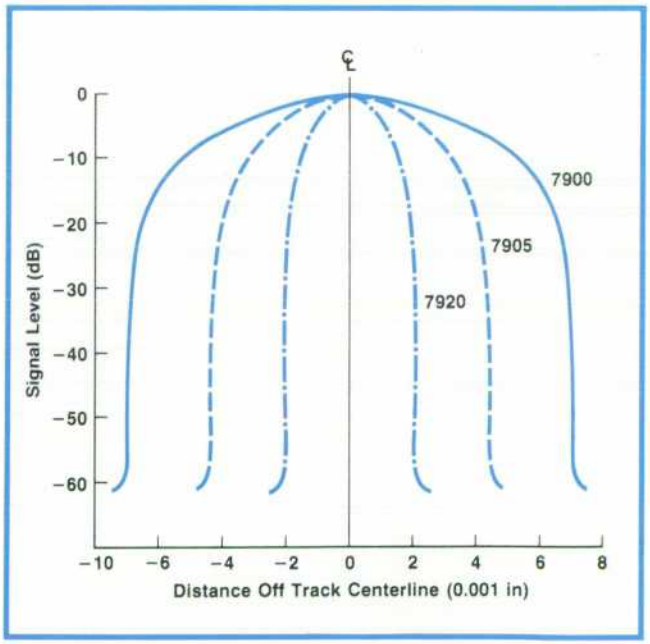


Fig. 6. *Normalized read-back track shapes for HP disc drives determine how far the heads can be allowed to deviate from track centerline.*

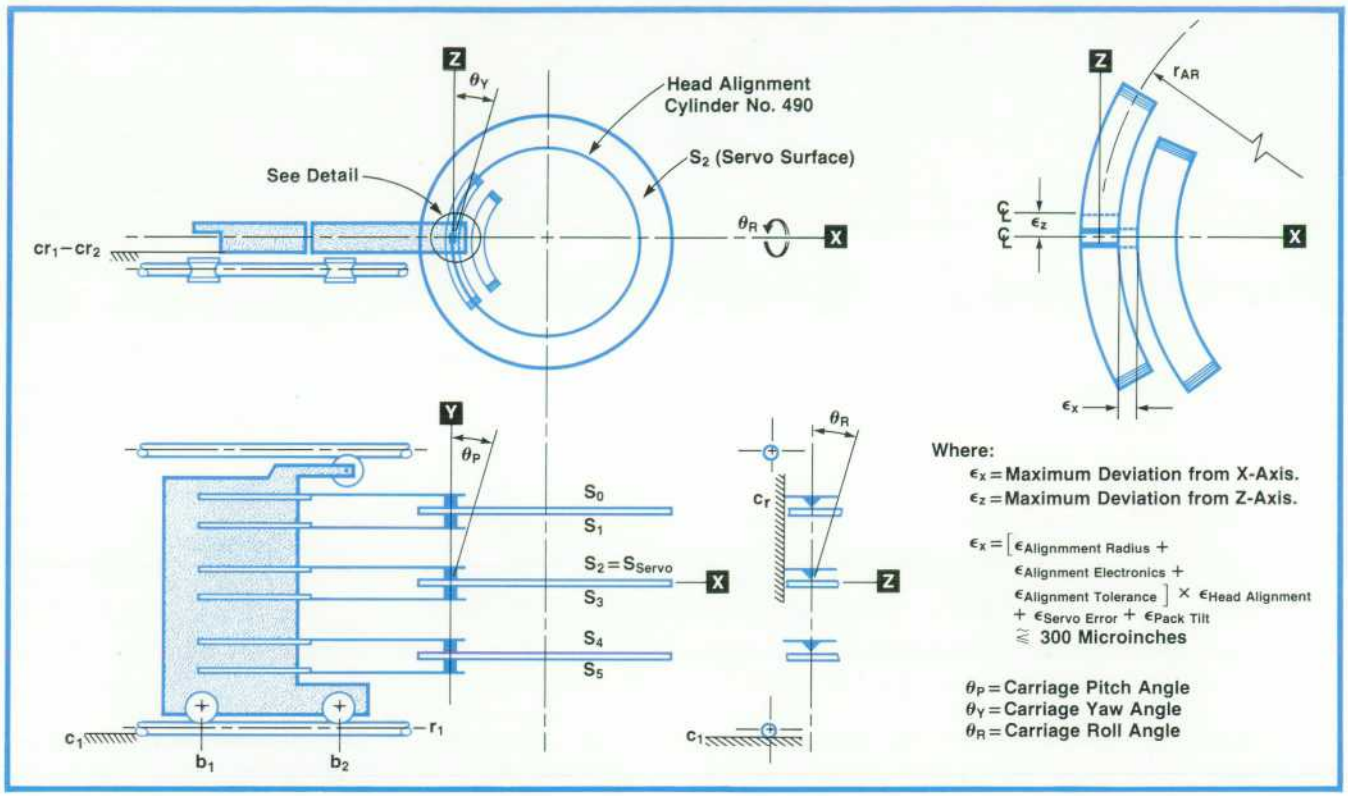


Fig. 7. *Components of the head-to-media tolerance loop. Maximum allowable deviation of the heads from nominal track centerline is 300 μin in the x-y plane (sum of all loop components).*

These tolerances were achieved by lapping the rails, which are made of tungsten carbide to ensure that the tolerances are retained over the life of the drive. The support surface c_1 is made of an aluminum casting that has been heat treated for maximum stability instead of the more usual heat treatment for maximum strength. Support surface c_1 is precision ground and inspected using air gauges.

Error ϵ_z, if excessive, may result in signal timing problems. One of the components of this error is the plane cr_1-cr_2, which is on the carriage. The carriage is made from an aluminum investment casting and the plane cr_1-cr_2 is machined using a numerically controlled (NC) milling machine. Making this part pushed both the casting process and the machining processes to the present limits of their capabilities.

The mechanical design of the drive achieves true parts interchangeability in the tradition of the automobile industry. As a result of careful design and sophisticated tooling of all of the components that affect head location, the drive requires only one mechanical adjustment during assembly or preventive maintenance. The single adjustment is alignment of the heads after they are installed in the carriage.

The heads are adjusted with a head alignment disc pack installed in the drive, and the drive electronics connected to a disc service unit. The service unit amplifies and processes the track signals of the alignment pack. Using a simple screwdriver-like tool, the service person moves the data heads until the service unit's digital display shows the heads are positioned over the alignment tracks. The resolution of the display is 6 microinches.

Drive Electronics

The drive is organized into eight functional systems (see Fig. 8). These are the input/output, spindle rotation, head positioning, sector sensing, read/write, fault detect, and power distribution systems.

The input/output system provides the communication link between the controller and the disc drive. One controller can handle up to eight drives, which may be 7920As and 7905As in any combination. A four-bit unidirectional tag bus and an 11-bit bidirectional control bus form the communication path for control information. A command is placed on the tag bus by the controller to specify what function the disc drive should perform. Data is transferred between the controller and the selected disc drive via bidirectional data lines dedicated to the drive. Illegal cylinder, head, or sector requests are checked at this process point.

The spindle rotation system, Fig. 9, provides power to the spindle motor to maintain its operational speed at 3600 revolutions per minute. A combined start-stop time of less than 70 seconds is achieved with the 10-pound disc pack in place, using a dc brushless motor driven by a 20-ampere highly efficient switch-

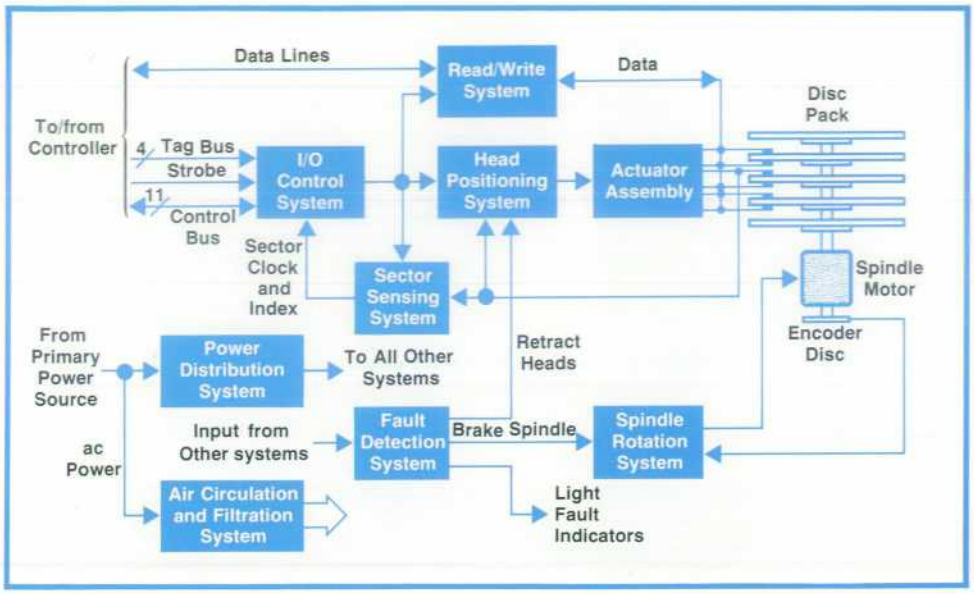


Fig. 8. *7920A Disc Drive is organized into eight functional systems.*

ing amplifier. The spindle motor amplifier is controlled by two rotational position sensors (optical switches) that detect motor shaft position, speed, and direction. The speed information is phase-locked to a crystal reference to maintain spindle speed in spite of line voltage and frequency variations. Using the sensor information, the amplifier provides the proper magnitude and polarity of current to the appropriate motor winding by rapidly chopping the output stage at a constant frequency of 22 kHz with a variable duty cycle.

Since the spindle motor and disc pack are dynamically braked, energy must be removed from the spinning assembly by the amplifier circuits. Because the amplifier is highly efficient in transferring power from and to the load, the braking energy is pushed into the main unregulated supply, causing its voltage to rise to a potentially excessive level. This condition is prevented by a shunt voltage regulator that inhibits amplifier operation and quickly bleeds down the offending supply voltage until normal operating voltages are reached.

Head Positioning System

The head positioning system, Fig. 10, controls the application of power to the head positioning actuator assembly to cause the heads to be accurately positioned over a specified cylinder. This system also controls head loading and unloading, seeking, programmed offsets, and servo recalibration.

With the disc pack installed and the RUN/STOP switch set to RUN, the head positioning system waits for the spindle to reach operational speed. Current is then applied to the linear actuator coil to load the heads onto the spinning disc pack at a constant velocity. Once the first track is detected by the servo head and the head positioning servo, the heads remain settled over cylinder 0 and the controller is notified that the drive has completed an initial loading operation. The heads are unloaded in a similar fashion.

A seek operation is used to move the heads from their present cylinder position to some other cylinder position. The controller issues a seek command on the tag bus and places the cylinder address on the control bus. This address is clocked into the next cylinder address register to provide destination information for the seek servo loop. The cylinder address comparator compares the cylinder address stored in the next cylinder address register with the address stored in the present location counter, and produces a digital difference word. The digital-to-analog converter converts this digital difference word into an analog signal that is applied to the velocity curve generator. This circuit produces an output proportional to the square root of its input, since for constant deceleration, velocity is proportional to the square root of the target distance. The servo system compares this square-root command signal with a velocity (tachometer) signal and controls the motor speed accordingly. The velocity signal is produced by a magnetic velocity transducer mounted in the linear motor (voice coil) that moves the heads.

When the present location count equals the address stored in the next cylinder address register, the velocity command is disabled and a fine-positioning (track-following) switch is closed. The heads then remain settled over the addressed cylinder until a new command is received. In this state the servo system is locked to the position signal derived from the servo tracks by the track-follower circuitry (not shown in Fig. 10). This signal is a linear function of the distance of the heads from the track centerline. The servo system attempts to null the position signal by controlling the heads.

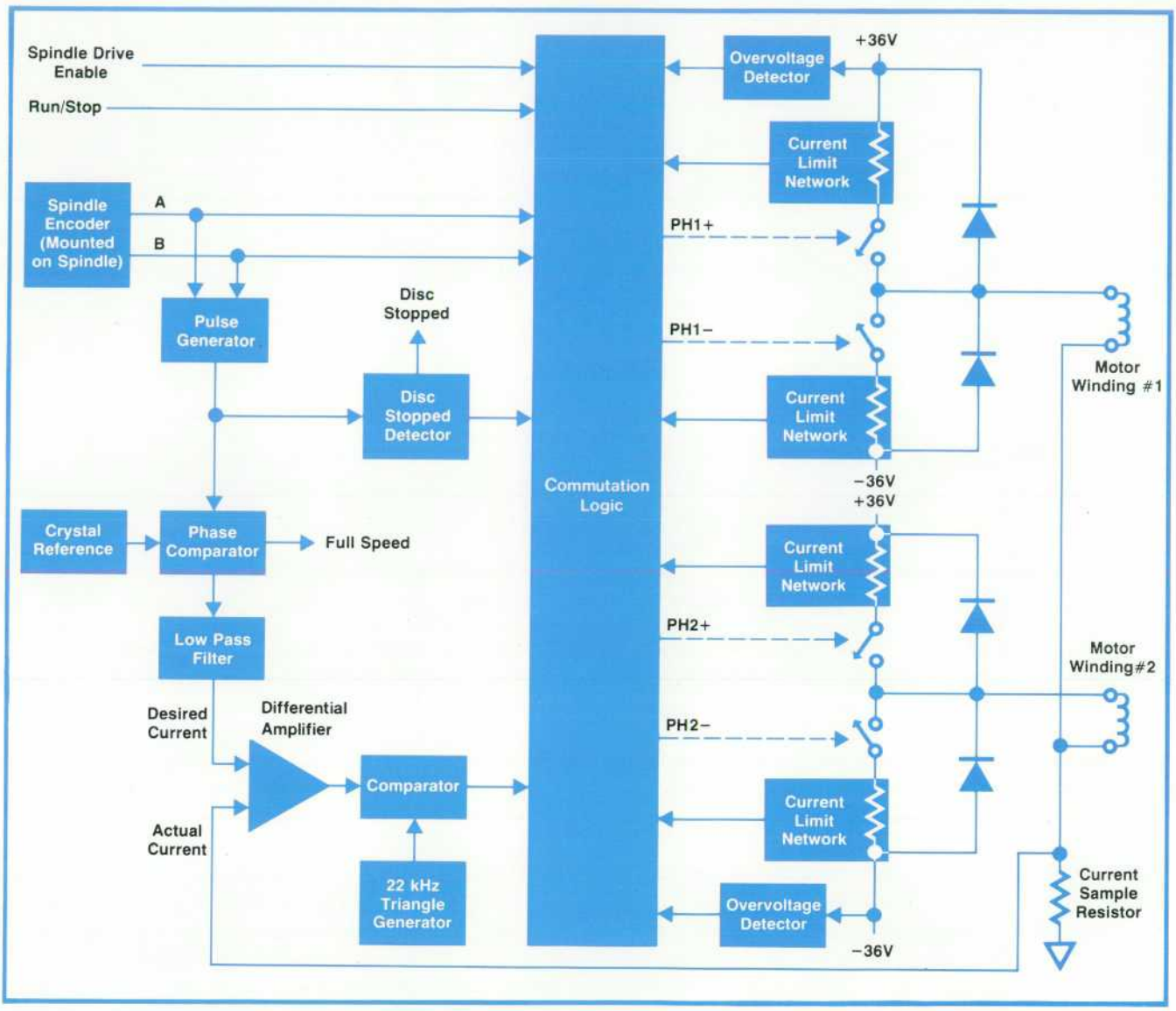


Fig. 9. *Spindle rotation system is basically a highly efficient switching amplifier. (The switches shown are actually transistor switches.) The system maintains the spindle speed at 3600 r/min. To stop the drive, change the disc pack, and restart the drive takes only 70 seconds.*

When the servo is locked on track over the addressed cylinder the track-following system is capable of following servo tracks that may have over 0.001-inch peak-to-peak radial movement within 30 microinches.

A programmed offset operation moves the heads in small increments to either side of track center to permit recovery of marginal data. The controller issues an offset command on the tag bus with the offset magnitude and sign on the control bus. 63 increments of ±12.5 microinches each can be specified.

A recalibrate operation is used to move the heads from their present position to a home position over cylinder 0. The controller issues this recalibrate command to establish a reference head position.

The purpose of the sector sensing system, Fig. 11, is to monitor circumferential head position by monitoring the location of each data sector as it passes beneath the heads. It notifies the controller when the present sector count equals the addressed sector, enables the read/write system for a data transfer operation, and gates the unit identity of the disc drive to the controller upon request.

The fault detect system continuously monitors various conditions within the disc drive. It controls the fault indicator lights, retracts the heads, and brakes when a fault is detected.

The 7920A Disc Drive is provided with an emergency head retracting system to prevent head crashes in the event of component or line voltage failure. Upon detection of a dangerous condition a relay immediately opens, connecting the linear motor to a

Head Alignment Disc Pack

The device for writing head alignment packs is a special-purpose disc drive designed and manufactured by Siemens (SW 333-11 Servo Track Writer). It uses an HP laser interferometer for precise positioning of the carriage that moves the read-write heads. The carriage moves on an air bearing slide that has a straightness of better than ±20 microinches. The disc pack on which the alignment tracks are written rotates on an air spindle that has a runout of less than 10 microinches. The two-ton granite surface plate is mounted off the floor on air cushions to eliminate vibrations from the floor. The packwriter room is temperature controlled, and the alignment pack, when it is being written, is in a very carefully controlled temperature environment. Fig. 1 is a block diagram of the packwriter.

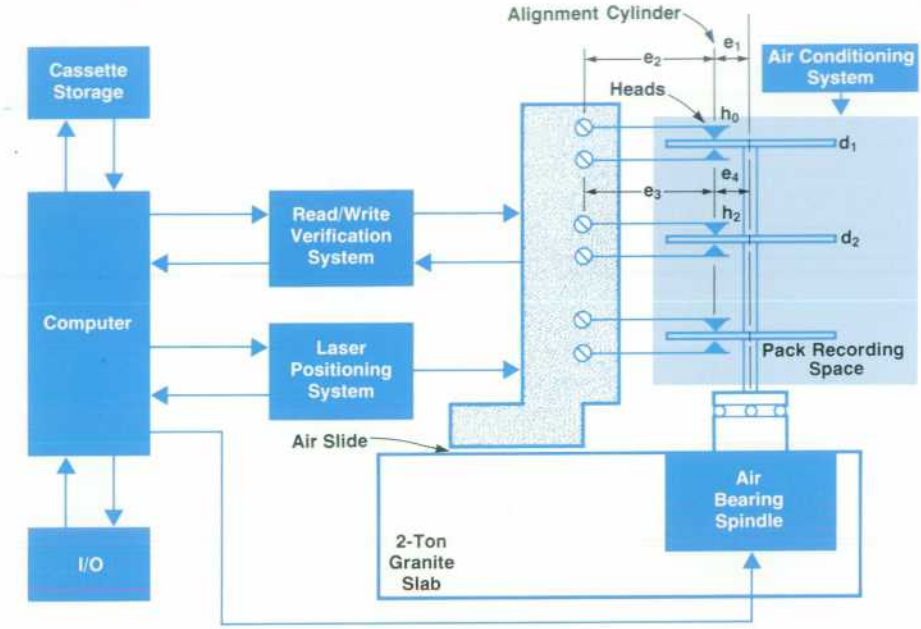


Fig. 1. *Block diagram of the packwriter, a high-precision disc drive used to write disc alignment packs for 7920A Disc Drives.*

At 20°C: $e_1 = e_3 = 5.110$ in.
$e_2 = e_4 = 3.250$ in.

At 20.5°C:

$e_1' = 5.11\,[\,1 + \alpha_{AL}\,(T-20)]$
$= 5.11\,[\,1 + 22.9 \times 10^{-6} \times 0.5] = 5.1105825$
$e_1' - e_1 = 58.5\mu$in increase
$e_2' = 3.25\,[1 + \alpha_{SS}\,(T-20)]$
$= 3.25\,[1 + 17.3 \times 10^{-6} \times 0.5] = 3.2500281$
$e_2 - e_2' = 28.1\mu$in increase

Hence: Track Offset = 58.5μin + 28.1μin = 86.6μin

Fig. 2. *Track offset caused by temperature gradient in pack recording space.*

Of all the variables that affect the accuracy of the recorded information on the head alignment pack, the most critical is temperature. An example, considering only the stainless steel support of the heads and the aluminum disc, illustrates this sensitivity (see Fig. 2). Suppose that the center disc and head support are at 20°C and that head h_2 and disc d_2 are at 20.5°C. If the data is written on disc d_2 under these conditions and then the temperatures equalize, the track on d_2 will be dislocated from the y-axis by 87 microinches. This shows that when the alignment tracks are written the temperature of the pack must be controlled within at least an order of magnitude better than 0.5°C.

Recorded information is read back at a different radial location from where it was written. This read-write offset must be known to write alignment packs accurately. For a given set of heads this information is stored in the memory of the computer that controls the operation of the packwriter, and is used for compensation of this variable. With enough iterations an alignment pack can be written within 25 microinches of a calibration pack at a given temperature.

When the alignment pack is used in the 7920A Disc Drive additional factors affect the accuracy of the positions of the data heads. The resulting accuracy is within ±75 microinches over a 10-to-40°C operating temperature range.

-James Hood

retract voltage regulator. This regulator derives its power from the power supply filter capacitors and the energy stored in the spinning disc pack, so it remains operational to retract the heads in all failure modes.

Read/Write System

The read/write system, Fig. 12, reads information from and writes information onto the data surfaces of the disc pack. In the read mode the motion of the head gap through the stored flux field induces a voltage in the windings on the head core. This induced voltage is analyzed by the read circuitry to define the data recorded on the disc. Data is written by passing a current through the read/write winding in the selected head.

Much of the data electronics in the 7920A Disc Drive is similar in form and function to circuitry found in most disc systems, particularly the 7920A's

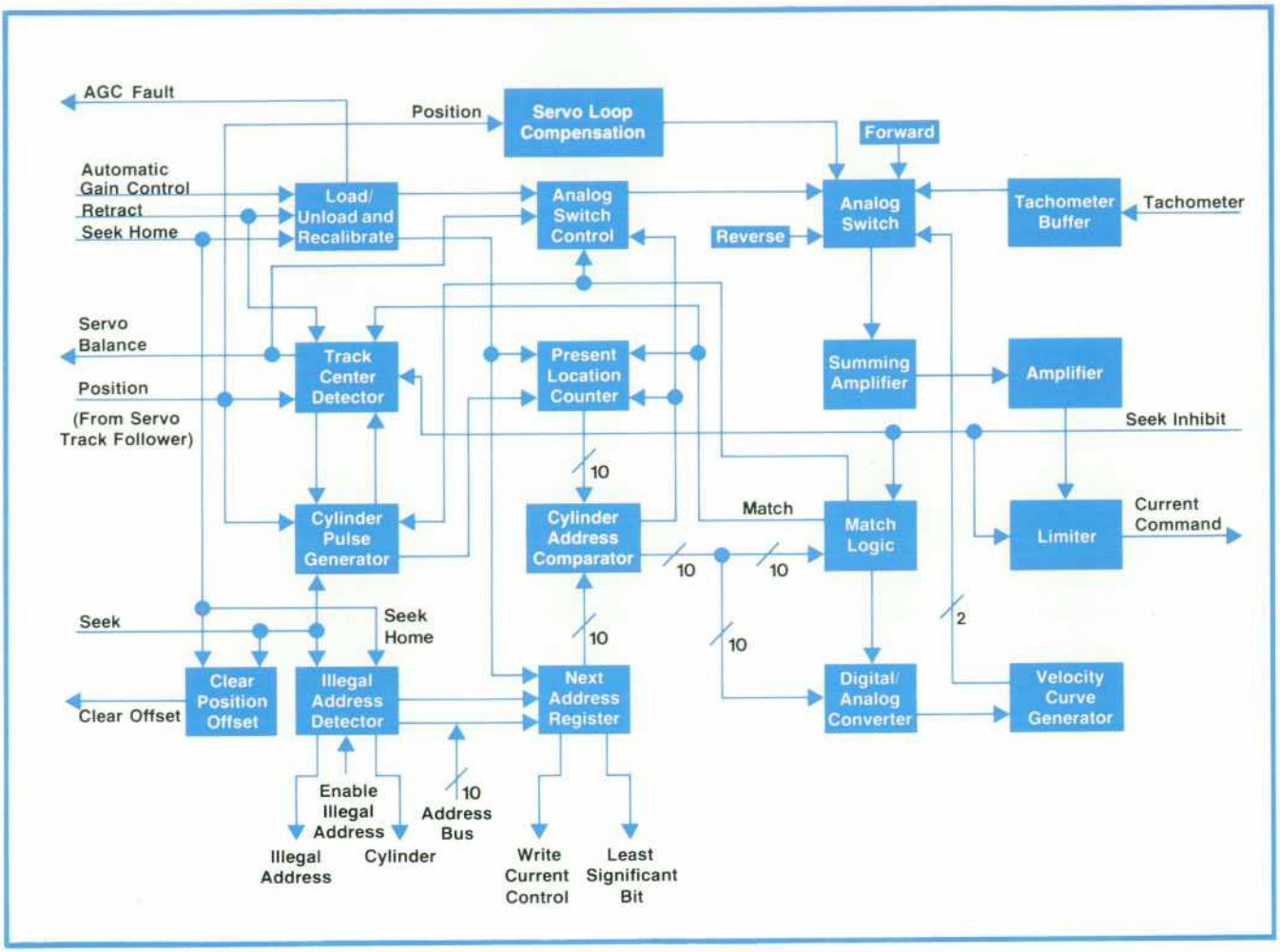


Fig. 10. *Head positioning system can follow tracks that have over 0.001-in peak-to-peak radial movement within 30 μin.*

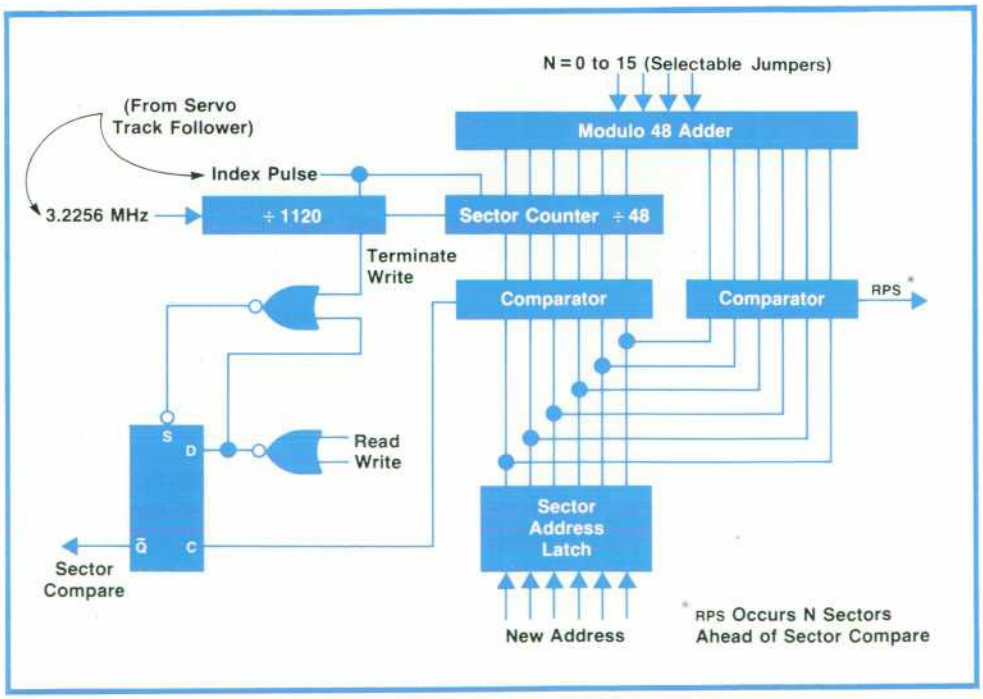


Fig. 11. *Sector sensing system monitors circumferential head position.*

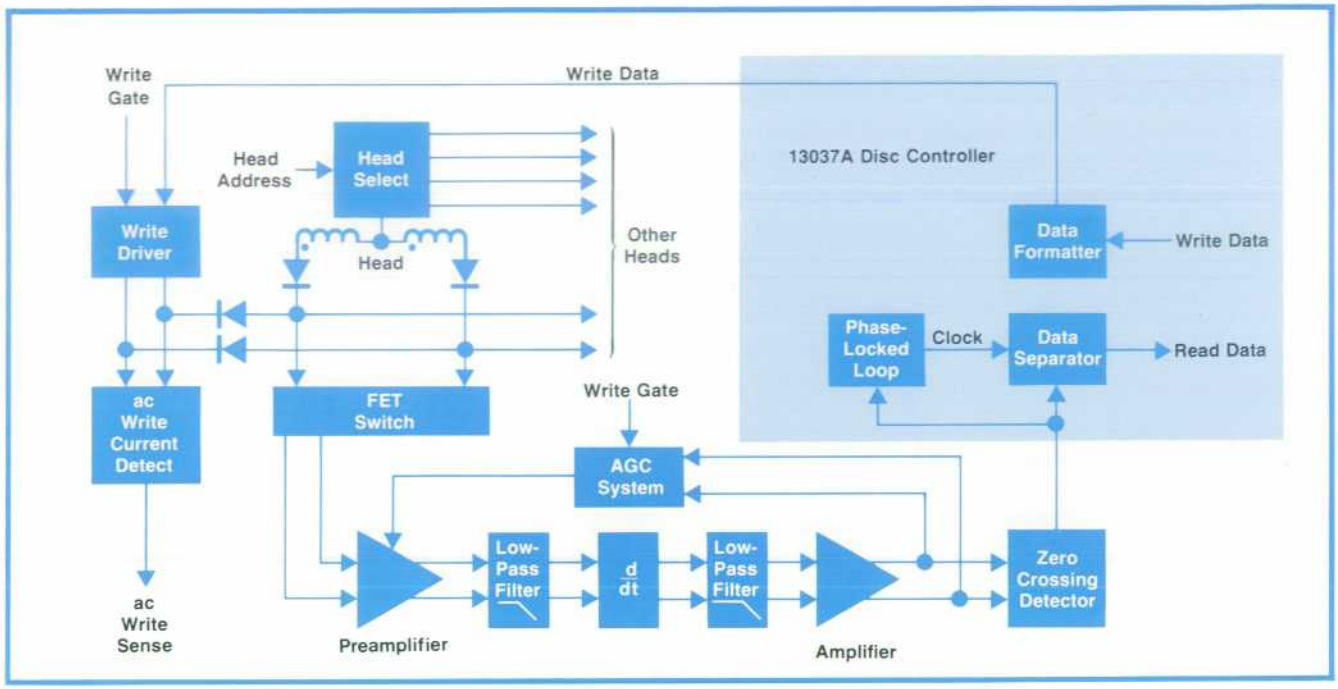


Fig. 12. *Read/write system uses automatic gain control (AGC) to maintain the read amplifiers in a linear operating range.*

direct ancestors, the 7900A[2] and 7905A. With the increase in track and bit density has come an increase in the sophistication of the data electronics. The increased track density has led to lower output from the magnetic transducers (heads) because of the decrease in the area swept by the heads. This has required more amplification and filtering in the read electronics to attain the signal-to-noise level required for decoding.

The increased bit density is the result of using a different code to write the data on the disc (see Fig. 13). The common NRZ (non-return-to-zero) data format, with a high level representing a one and a low level representing a zero, is unsuitable for magnetic recording because it requires separate clock, or timing information. The 7900A Disc Drive used the FM (frequency modulation) code, also called double frequency code. It is self-clocking, with a transition at the boundary of every bit cell and another in the center of each bit cell containing a one. The 7905A and 7920A use MFM (modified frequency modulation) code, also called delay modulation code. This code has a transition in the center of each bit cell containing a one and at each bit cell boundary between consecutive zeros. Although the clock is not so regular in this code, it is easily reconstructed with suitable logic and a phase-locked loop. MFM code requires fewer transitions than FM. Because the distance between transitions is the limiting factor in bit density, more data may be written with MFM with the same transition spacing.

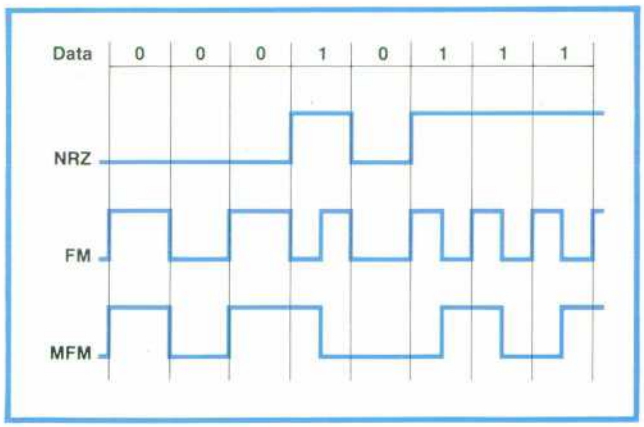


Fig. 13. *NRZ data format is unsuitable for magnetic recording because it requires a separate clock, while FM and MFM codes are self-clocking. The MFM code used in the 7920A requires fewer transitions than FM. It therefore allows greater bit density, but demands finer precision in the read/write system.*

Increased bit density is not without cost. MFM code requires higher precision. Certain data patterns are precompensated when written to maximize readability, and the entire read electronics chain must function within very tight constraints. In the 7900A generation of electronics, the read amplifiers could saturate and limit signal swing, much as in a common FM receiver, and produce output data of satisfactory accuracy. The nonlinearities inherent in this type of operation would degrade the more advanced MFM code too much, so the read chain uses an AGC (automatic gain control) system to maintain the read

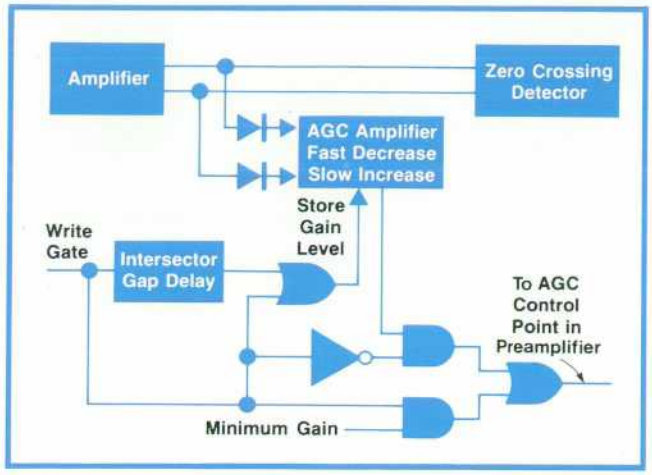


Fig. 14. *During read operations the AGC circuit increases the gain during intersector gaps. During write operations the AGC turns off to keep the large write signal out of the read channel.*

amplifiers in a linear region (Fig. 14). This AGC circuit must deal with some interesting problems. Between sectors of data returning from the disc there are gaps containing no signal. These gaps represent about 8% of the time. The AGC responds to a gap by increasing the gain. Then at the end of the gap it responds even faster, returning the gain to an appropriate level.

During a write operation the AGC is very important. The write signal at the heads is about 24V p-p compared to a read signal of 1 mV p-p. No feasible isolation can keep this write signal out of the read amplifiers. To keep the write signal from influencing the read channel gain, the AGC is turned off. Thus the ACG is a sample-and-hold circuit, with the gain control level stored in the amplifier for the duration of the write operation. The gain of the read channel is lowered by the write gate independently of the AGC circuit to minimize the impact of the write signal on the read circuits.

When writing consecutive sectors, and when the write gate is turned off, the AGC would normally be enabled between sectors. This would cause the AGC to be influenced by samples of "no signal." To prevent this, a time delay circuit keeps the AGC disabled for the duration of the intersector gap after the write gate turns off. Thus the read channel is held off for consecutive writes, and begins the next read operation at the beginning of the data signal with the correct gain.

Another advance in the data circuitry of the 7920A Disc Drive is a very effective ac write current detect system. This is a fail-safe system that checks that data is being written normally any time there is a write command. The voltage generated by the switching of write current through the head is sensed and tested for sequence and timing. Abnormalities indicating absent or distorted data at the head are detected, stopping the write process and causing a system fault condition.

In the 7920A Disc Drive a well filtered air supply is achieved through the use of an absolute filter. The absolute filter, a high-efficiency cellulose paper folded for maximum area in a limited volume, was selected on the basis of pressure drop. A more efficient absolute filter has the accompanying drawback of a high pressure drop, which decreases the velocity of air leaving the head-disc area. The absolute filter selected will allow enough air flow even when its pressure drop has doubled. In the 7920A Disc Drive a pressure of 0.60 inch of water inside the head-disc area was necessary to keep exiting air velocities high enough to prevent contamination through openings, especially those caused by eddy currents set up by the rotating discs. With an air flow rate of 29 cubic feet per minute through the disc drive, a filter restricting 99% of all particles 0.3 microns or larger operates at 0.40 inch of water pressure drop across the filter. Since the worst case pressure without a filter is 1.45 inches of water, the 99% filter will still operate above the required 0.60 inch of water even when its pressure drop doubles ($1.45-2\times0.40=0.65$). Thus the 99% absolute filter is the most efficient filter that will operate within the design restrictions.

To extend the absolute filter's life, a prefilter is employed upstream from the absolute filter and the blower (see Fig. 15). The prefilter is a low-cost, standard-size, medium-efficiency pleated filter that can be replaced in seconds by opening a door, sliding the dirty filter out, and sliding in a clean filter.

Since filter life depends on the drive's operating environment, a pressure reading in the head-disc area is required to determine when the filters need to be

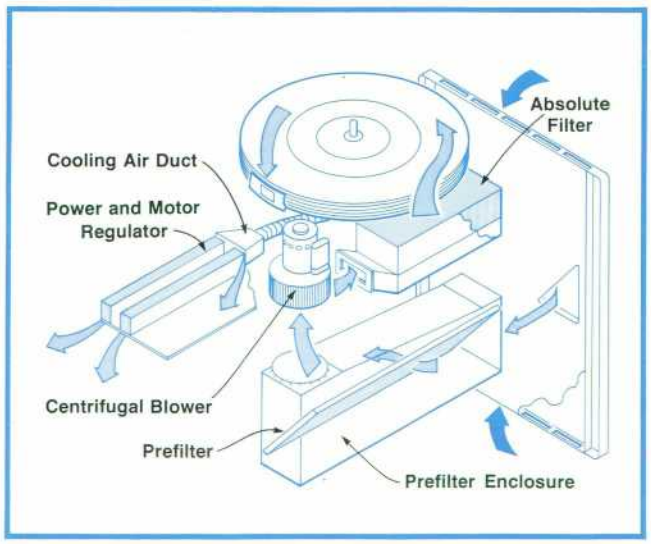


Fig. 15. *7920A air supply is filtered by an absolute filter. A prefilter extends the absolute filter's life.*

A Mechanical Vibrations Analogy for Servo System Design

The performance of servo feedback systems is usually analyzed in the frequency domain using Laplace transform methods. An insightful alternative for analyzing an electromechanical servo system is to use a mechanical vibration analogy. In this analogy, mechanical springs model proportional feedback loops and viscous dampers simulate the damping of the moving mass in the system. This method is especially useful for determining the proper frames of reference for the control system variables.

In today's high-performance disc memories the data heads are positioned radially on the discs by tracking information encoded directly on the surface of a disc. In the HP 7920A disc pack, one of the six active surfaces is devoted entirely to head positioning. This servo surface and the associated servo head provide a radial position scale in each individual disc pack. This scale is used to move the heads to the desired track and to keep the heads centered over that track.

The servo head must follow the tracks on the servo surface as accurately as possible to assure disc pack interchangeability. In practice these circular servo tracks are not perfectly centered and can be slightly non-circular. The small deviations provide an input command signal to the servomechanism. Among the possible causes for servo track deviations are mechanical vibrations in the disc drive, vibrations in the machine that wrote the servo surface, ball bearing noise from the disc drive spindle, and most important, eccentricity between the centers of the servo track and the disc drive spindle. This eccentricity or runout is a result of the displacement of the center of rotation of the disc pack at the time the servo track was written from the center of rotation at the time of playback.

The HP 7920A spindle rotation speed is 3600 revolutions per minute. Any runout of the disc pack results in a 60-Hz sinusoidal motion that can have peak amplitudes as large as 500 microinches. The signal derived from this motion can also contain noise at frequencies up to 600 Hz with amplitudes up to 100 microinches peak.

The mechanical vibration analogy can be conveniently applied to a disc-drive track-following servo system for following circular runout. Linear feedback of carriage displacements with respect to the moving servo track can be viewed as a mechanical spring joining these two elements (K in the drawing). The natural frequency of dynamic response can be calculated by applying mechanical vibration theory using the above spring constant and the moving carriage mass (M in the drawing):

$$\omega_r^2 = \sqrt{K/M}$$

Damping for the servo system may be accomplished in several ways. One commonly used method is a moving magnet tachometer that produces a signal proportional to the velocity of the moving carriage relative to the disc drive mainframe. When this signal is amplified and fed back through the force transducer, a force is applied on the moving mass proportional to carriage velocity. This has the same form as a viscous damper joining the carriage to the mainframe.

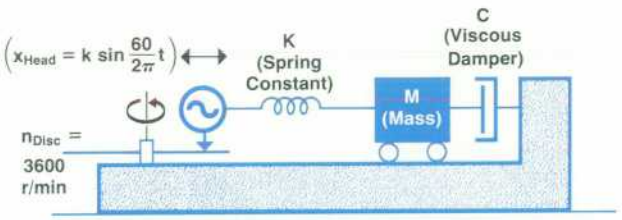
An alternative for generating viscous damping is a phase shifting network in the forward path of the electromechanical system. A properly designed lead compensator can be viewed as a dashpot joining the moving servo track to the moving carriage (C in the drawing). This analogy is plausible because, over a frequency range below the system's natural frequency, the output of the phase shifting network can be viewed as the sum of position and tachometer feedback signals combined in the proper proportions.

It is instructive to note the performance differences that result from the different frames of reference of the two damping methods described above. A tachometer-based system produces a damping force on the moving mass proportional to the velocity difference between the carriage and the mainframe. The null position for such a servo system has the carriage motionless with respect to the mainframe. The phase-lead compensator damped system, however, produces its damping force proportional to the velocity difference between the moving servo track and the moving carriage. Its null position locus has the carriage exactly following the moving servo track.

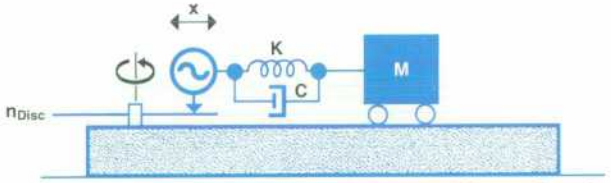
In the design of the HP 7920A track-following servo system three alternatives were considered for damping the system:

- A tachometer damped system
- A phase-lead compensator damped system
- A combination of the above.

System parameters defined the natural frequency of the system at about 600 Hz, or ten times the servo track runout frequency. For proper dynamic response a system damping ratio of about 0.70 was chosen. With these parameters fixed, the potential runout-following capabilities of the three alternatives can be evaluated.



Track-Following System with Tachometer. Viscous Damping Achieved by Tachometer (Velocity Transducer).



Track-Following System Without Tachometer. Viscous Damping Achieved with Electronic Compensation Network.

Steady-state vibration analysis shows that the tachometer damped system can reduce the servo track open-loop runout to only about 14%. Thus a servo track with 1000 microinches of open-loop peak-to-peak runout would result in a system error of 140 microinches peak-to-peak. For a phase lead damped system, however, the same open-loop runout can theoretically be reduced to 1%.

For a practical servo system this mechanical analogy gives no indication of overall servo system stability. Thus a frequency domain stability analysis is required. Stability analysis showed that the tachometer-based system is inherently stable but inadequate for following runout. However, the phase-lead compensated system proved to have stability problems. One workable solution for stabilizing the phase lead system was to intro-

duce a tachometer in series with a high-pass filter. This system could be easily stabilized but still did not follow servo track runout as well as the theoretical limit of the ideal phase-lead compensated system.

For the 7920A Disc Drive a second-order lead-lag compensator was chosen for the track-following servo system. The phase lag was introduced to stabilize the system for frequencies above its natural frequency. This system is capable of following servo tracks with over 0.001 inch of peak-to-peak servo track runout within 20 microinches. Noise components at higher frequencies may increase this error signal to as much as 30 microinches peak.

-Joel Harrison
-Lynn Weber

replaced. This reading is taken with a pressure gauge plugged into a specially designed fitting that leads to the head-disc area. A reading below 0.60 inch of water indicates that the prefilter and possibly the absolute filter must be replaced. Extrapolated long-term tests in a worst-case environment indicate an absolute filter life of several years.

Testing for Reliability

The new disc drive was designed with heavy emphasis on the specified error performance. To verify this performance, drives were tested continuously during the development cycle. These drives transferred data to or from removable disc packs written on the same drive or by other drives. Data transfer and data interchangeability were tested beyond the specified temperature range (10° to 40°C) to insure an adequate margin of safety. The tests were also conducted at all line voltage limits and line frequency limits, and throughout the specified altitude and humidity ranges in a special test chamber.

The drive was stress tested by operating it on a vibration table. The results of these tests made it possible to evaluate the physical structure for proper static and dynamic integrity and performance under extreme conditions.

In many cases, accelerated life tests do not lead to meaningful results and must be replaced by real-life tests. Assemblies of the drive that had to be real-life tested were identified early during the development cycle. A typical case was the head contamination characteristics. The airflow system that prevents contamination of the heads was tested from the beginning of the project, with the result that by the time of introduction of the product there was reasonable assurance that the drives would perform as specified over their expected lifetimes. The result of this and many similar real-life and accelerated life tests, combined with pre-introduction tests by HP's quality assurance group, showed that the drive will meet its performance and reliability goals.

Serviceability

Ease of servicing was a prime consideration in the design of the enclosure for the 7920A Disc Drive. Access to the primary service area is through a wrap-around shroud that requires no tools to remove. Secondary service access is through easily removable side panels and doors. Complete removal of all panels, main assemblies, and circuit boards can be accomplished in less than five minutes using only a screwdriver and a nutdriver (see Fig. 16).

During preventive maintenance the user or service person can observe eight fault indicator lights that assure that the drive's internal fault indication circuitry has not detected a problem. Faults in the read/write system, faulty head positioning, improper voltage conditions and other problems can be seen here. At the same time, the drive's single mechanical adjustment, the head alignment, can be checked. The only other adjustment, an electronic adjustment that assures that the drive's fast seek time specification is met, can also be checked at each 6-month preventive maintenance interval.

Acknowledgments

A multi-discipline product such as a disc drive is designed with the help of many people. Many thanks to all of them. Dick Monnier supplied the overall technical and managerial know-how for the product. The members of the drive design team deserve special mention: Jack Alten, Kent Anderson, Fred Goodman, Joel Harrison, Jim Hood, Bill Moon, Bob Nordman, Jim O'Briant, Don Reeves, Lynn Weber, Bob Widmayer and Dave Willis. As was demonstrated, disc drives need flyable heads and workable disc packs. For this and the information on heads and media in this article we relied on Bill Girdner's head-media

Fig. 16. *For ease of servicing, a 7920A Disc Drive can be disassembled in less than five minutes using only a screwdriver and a nutdriver.*

team: George Clifford, John Miller, and Rick Sayers. Kail Peterson's work was on the industrial design. Gordon Smith and his model makers made the hardware. Chuck Habib's team provided the PC boards.

It is not sufficient to have a workable product in the lab. The product must also be producible and profitable. Proper tooling achieves these objectives. The 7920A Disc Drive received its tooling support from Jim Hergert's group: Laslo Zsidek, William Voros, Hector Payan, Dick Chinoweth and Tom Andrews.

Product reliability was a continuous goal of the design team. Third-party perspective for this was provided by Chuck Tracy and Ron Morgan.

The introduction of a disc drive into manufacturing is complex. Many times the efforts of those who do this are not apparent. Steve DePaoli, Joe Arata, Dave Handbury and Dick Lawson played a major role in this transition.

No matter how good the product is, the field service organization must have support. This was furnished by Harry Albert, who trained the field service personnel. Bill Marquette and Al Hopkins supplied the service manuals.

Many concepts of the drive are based on the architecture of the 7905A Drive that was developed by Bill Lloyd. Winston Mitchell's head positioning circuitry and disc service unit and Wally Overton's read/write circuitry were successfully used with modifications on the 7920A.

Herbert P. Stickel

Herb Stickel, project manager for the 7920A Disc Drive, joined HP in 1969 with fifteen years' experience in the design of linear accelerators and computer peripherals. He contributed to the design of HP's first disc drive, the 7900A, and its successor, the 7905A, before taking on the 50M-byte unit. Born in Buffalo, New York, Herb received his BSME degree from the University of California at Berkeley in 1954, and his MS degree in engineering from Stanford University this year. He's single, lives in Menlo Park, California, and claims to have "no hobbies whatsoever, except taking it easy."

References

1. J.E. Herlinger and J.R. Barnes, "A Faster, Tougher Disc Drive for Small Computer Systems," Hewlett-Packard Journal, May 1972.
2. W.I. Girdner and W.H. Overton, "Reading and Writing on the Fast Disc," Hewlett-Packard Journal, May 1972.

SPECIFICATIONS
HP Model 7920A Disc Drive

Functional Specifications

SEEK TIME
TRACK-TO-TRACK: 5 ms, maximum
AVERAGE RANDOM: 25 ms
MAXIMUM (823 TRACKS): 45 ms
GROSS CAPACITY: 64.32×10^6 bytes

DATA CAPACITY

48 Sectors/Track - 815 Tracks*

	Data Bits Per	Data Bytes Per	Sectors Per	Tracks Per
Byte	8			
Sector	2,048	256		
Track	98,304	12,288	48	
Surface	80.11776×10^6	10.01472×10^6	39,120	815
Drive	400.5888×10^6	50.0736×10^6	195,600	4,075

*Total number of tracks per surface is 823, 8 of which are used as spares or for defective track allocation. 815 tracks per surface (minimum) are guaranteed to be good.

ROTATION
SPEED: 3,600 rpm
AVERAGE ROTATIONAL DELAY: 8.3 ms

RECORDING CHARACTERISTICS
BITS/INCH (INSIDE TRACK): 4,680
TRACKS/INCH: ~384
TRACKS/SURFACE: 815 (plus 8 used as spares or for defective track allocations)

DATA TRANSFER RATE
BITS/SECOND: 7,500,000
KILOBYTES/SECOND: 937.5

ACTUATOR
Voice coil actuator with velocity feedback, position feedback from top surface of the center disc. Carriage is mechanically locked in the retracted position when power is removed to protect heads and disc pack.

DISC PACK INTERCHANGEABILITY
Worst case tests of both the 7920A Disc Drives and 13394A Disc Packs ensure that any 13394A Disc Pack written on any 7920A Drive within the operating specifications may be read on any other 7920A operating within that range. Error performances/interchangeability can be guaranteed only if HP 13394A Disc Packs are used.

Electrical Specifications

7920M MASTER DRIVE (INCLUDES 13037B CONTROLLER)
AC VOLTAGES (all +5%–10%): 100V, 120V, 220V, 240V
FREQUENCY: 47.5 to 66 Hz
PHASE: Single
POWER: 700 watts, typical at 120V, 60 Hz
CURRENT: 6.6 amperes, typical at 120V, 60 Hz

7920S ADD-ON DRIVE
AC VOLTAGES (all +5%–10%): 100V, 120V, 220V, 240V
FREQUENCY: 47.5 to 66 Hz
PHASE: Single
POWER: 460 watts, typical at 120V, 60 Hz
CURRENT: 4.5 amperes, typical at 120V, 60 Hz

Environmental Specifications

TEMPERATURE
OPERATING: +10°C to +40°C (50°F to 104°F), rate of change not to exceed 10°C (18°F)/hr. Above 3,048m (10,000 ft) altitude maximum ambient temperature is reduced from 40°C to 30°C (104°F to 86°F).
NON-OPERATING: –40°C to +75°C (–40°C to +167°F), rate of change not to exceed 20°C (36°F)/hr.

RELATIVE HUMIDITY
OPERATING: 8% to 80% (non-condensing)
Wet bulb temp: <25.6°C (78°F)
NON-OPERATING: 5% to 95% (non-condensing)
Wet bulb temp: <25.6°C (78°F)

HEAT DISSIPATION
7920M MASTER DRIVE: 600 kg-cal/hr (2,390 BTU/hr), maximum
7920S ADD-ON-DRIVE: 396 kg-cal/hr (1,570 BTU/hr), maximum

ALTITUDE
OPERATING: Sea level to 4,572m (15,000 ft)
NON-OPERATING: 304.8m (1,000 ft) below sea level to 15,240m (50,000 ft)

Physical Characteristics

DIMENSIONS: 82.5 cm (32.5 in) H × 50 cm (19.65 in) W × 81.3 cm (32 in) D

WEIGHT
7920M MASTER-DRIVE (INCLUDES 13037B CONTROLLER):
NET: 158.7 kg (350 lb)
SHIPPING: 236 kg (520 lb)
7920S ADD-ON DRIVE
NET: 142.8 kg (315 lb)
SHIPPING: 220 kg (485 lb)

CABLE LENGTHS
7920M MASTER DRIVE
MULTI-UNIT CABLE: 1.5m (5 ft)
DATA CABLE: 3.0m (10 ft)
INTERFACE CABLE: 5.5m (18 ft)
7920S ADD-ON DRIVE
MULTI-UNIT CABLE: 2.4m (8 ft)
DATA CABLE: 15.2m (50 ft)
Maximum cumulative multi-unit cable length from controller to last drive in daisy-chain is 22.5m (74 ft).

PRICE IN U.S.A.: 7920M, $17,500. 7920S, $14,000.

MANUFACTURING DIVISION: DISC MEMORY DIVISION
11311 Chinden Boulevard
Boise, Idaho 83707 U.S.A.

An Individualized Pulse/Word Generator System for Subnanosecond Testing

A high-speed pulse/word generator is constructed in modular form so it can be configured according to specific testing requirements.

by Christian Hentschel, Günter Riebesell, Joel Zellmer, and Volker Eberle

THE INSTRUMENT SHOWN IN FIG. 1 is one version of HP's Model 8080 high-speed pulse generator system. This version, intended for the test and development of state-of-the-art digital systems, has a maximum repetition rate of 1 GHz with pulse rise and fall times less than 300 ps and a maximum pulse amplitude of 1.2V. It has two outputs with the pulse train from one delayed with respect to the other by a controllable amount.

Fig. 2 shows another version. This one is a digital word generator capable of generating serial words up to 64 bits long at bit rates up to 300 MHz. Pulse amplitude can be up to 2 volts with rise and fall times of less than 800 ps or, with the high-speed output amplifier module, 300 ps with pulse amplitudes up to 1.2 volts.

This pulse/word generator system evolved as a modular system that can be configured to meet a wide range of high-speed digital applications, such as those involved with subnanosecond IC development, CPU design, digital modulator and multiplexer development, fiber-optic system development, and nuclear research. The modules, which include rate generators, output amplifiers, a delay generator, and a word generator, are available in two compatible families—one for 1-GHz operation and one for 300 MHz. The modules bolt into a mainframe that provides dc power for the modules.

Some of the varieties of pulse and word generators that can be configured using these modules are shown in Fig. 3.

The Modules

The rate generators are basically square-wave generators that operate at repetition rates between 10 Hz and 300 MHz (Model 8081A) or 100 Hz and 1 GHz (Model 8091A). Pulse generation can be gated by external waveforms with the pulse train automatically synchronized to the start of each gate.

The delay generator/frequency divider module (Model 8092A) accepts the output of either rate generator and produces two pulse trains in response. One pulse train can be delayed up to 9.9 ns with respect to the other in steps of 100 ps. The two-digit numeric readout presents the delay of channel B with respect to channel A, but since the delay can be inserted into either channel, channel B can appear to be advanced up to 9.9 ns with respect to channel A, as well as delayed.

In addition, this module has a ÷2 circuit so channel

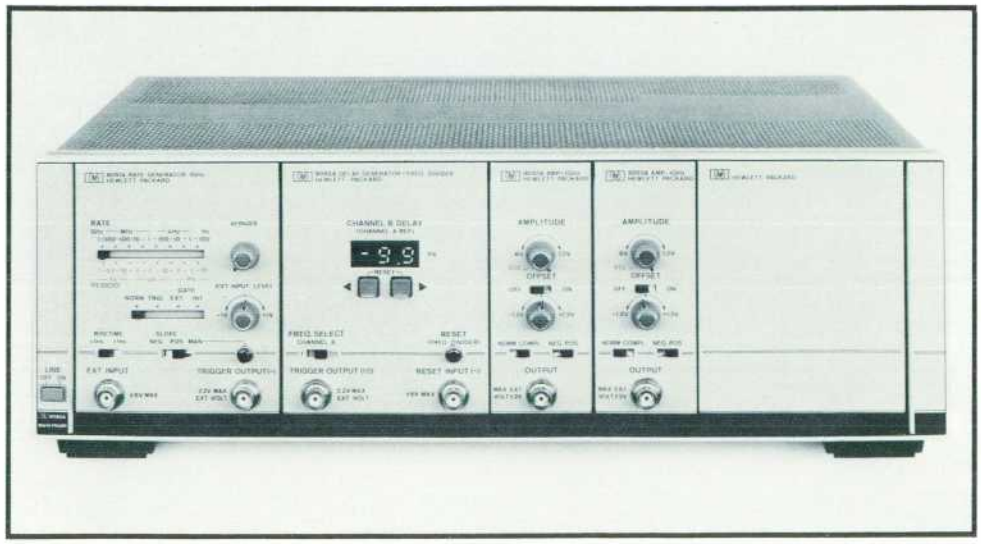


Fig.1. *1-GHz pulse generator assembled from HP 8080-series modules has 300-ps pulse transition time and controllable delay between channels.*

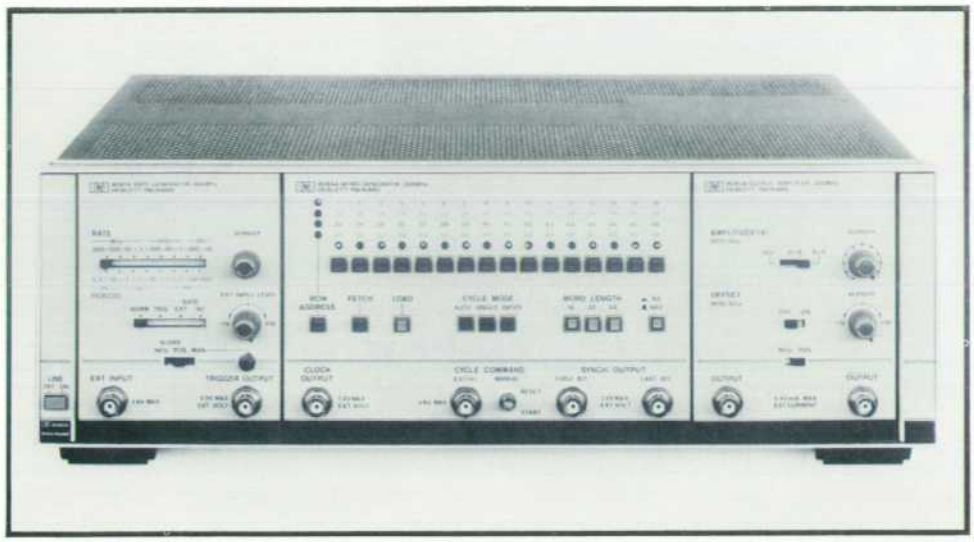


Fig. 2. *300-MHz word generator assembled from 8080-series modules produces words 16, 32 or 64 bits long, repetitively or in bursts. The dual-output amplifier supplies the word and its complement with transition times of 800 ps.*

B can produce a square wave at one-half the repetition rate of channel A. This can be very useful in tests of dual-input gates; the two outputs provide all combinations of two bits (00, 01, 10, 11) and the interchannel delay allows exploration of problems caused by race-induced signal overlaps and propagation delays.

The half-frequency mode is also useful for testing flip-flops and shift registers where the half-frequency channel supplies the data input while the full-frequency channel supplies the clock (Fig. 4). The interchannel delay then enables examination of setup and hold times. Previously, two synchronized pulse generators were needed for this kind of test.

The word generator (Model 8084A) generates serial words 16, 32, or 64 bits long, either repetitively or one word at a time in response to a manual pushbutton or an external trigger. The output can be in either RZ or NRZ format. Word data is loaded 16 bits at a time from a front-panel switch register.

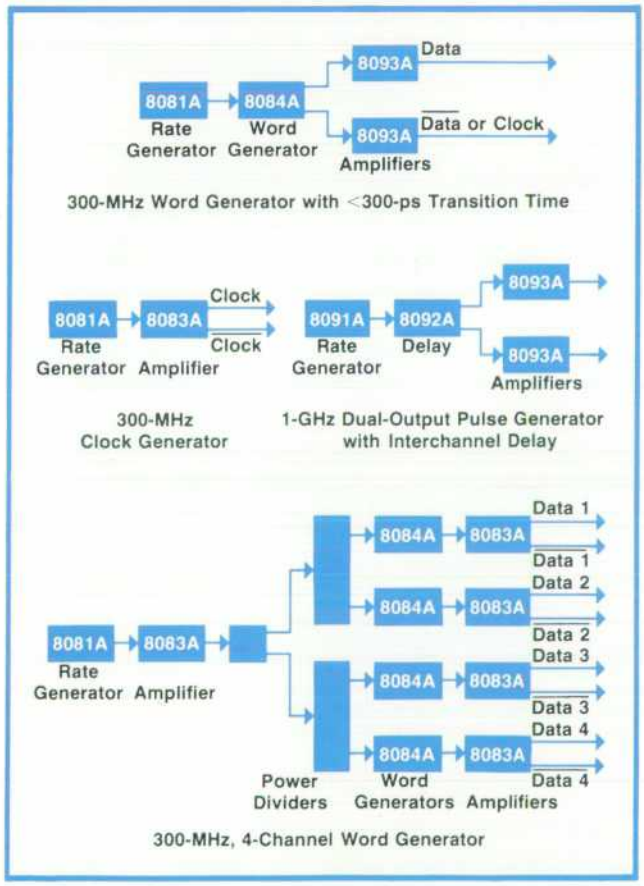


Fig. 3. *A few of the several pulse/word-generator configurations possible using modules in the 8080 series. Some configurations, such as the multichannel word generator, may require more than one mainframe to house all the modules.*

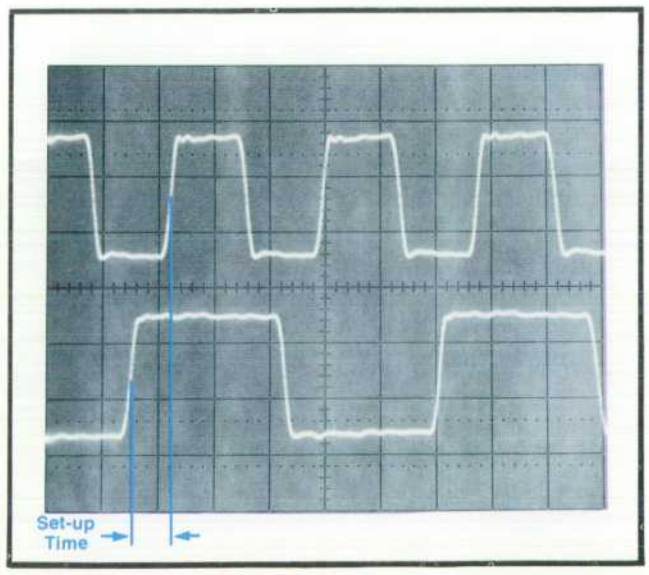


Fig. 4. *Channel B of the Model 8092A Delay Generator can be switched to function as a frequency divider, producing square waves at one-half the repetition rate of channel A. Use of the interchannel delay then allows examination of setup and hold times of flip-flops.*

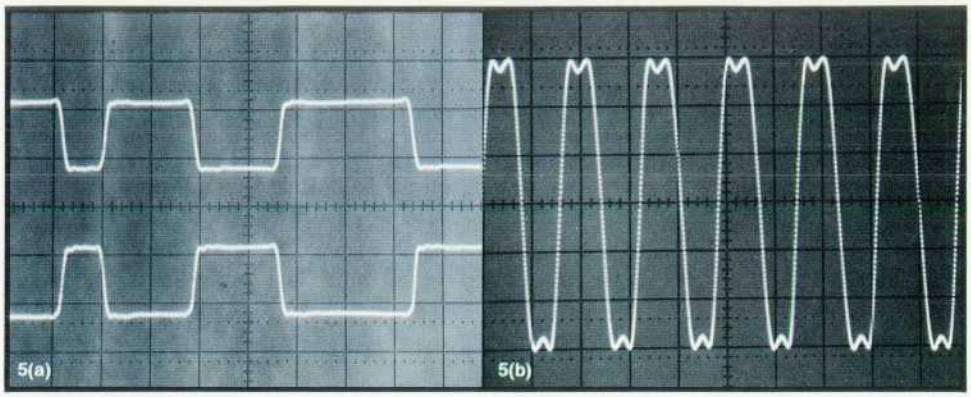


Fig. 5. *Dual output of the Model 8083A 300-MHz Output Amplifier (a) reproduces the amplifier input at the channel A output while supplying the complement of the input at the channel B output, enabling the generator to drive differential-input devices. Pulse polarity is also selectable. Model 8093A Output Amplifier supplies pulses with less than 300-ps transition times (b). Pulse repetition rate here is 600 MHz. (Oscilloscope sweep time: 1 ns/div.)*

The 300-MHz output amplifier (Model 8083A) reproduces the internally-supplied pulse train at two 50Ω outputs simultaneously, one normal and the other the complement of the input pulse train (Fig. 5a). The output pulse amplitude is adjustable from 0.2V to 2V, offsettable up to ±1V, with fixed transition times of less than 800 ps. Pulse polarity is selectable (positive-going above the baseline or negative-going below).

The 1-GHz amplifier (Model 8093A) reproduces the pulse train supplied to it with output pulse amplitude controllable between 0.6 and 1.2V, offsettable ±1.2V, and with transition times less than 300 ps (Fig. 5b). The normal/complement format and the output polarity are selectable. This module can also serve as a pulse amplifier, giving 300-ps transition times to any external pulse train with amplitudes 600 mV or greater and transition times less than 10 ns at repetition rates up to 300 MHz.

Technical Details

The 300-MHz modules use monolithic integrated circuits developed for the Model 8082A Pulse Generator[1], made by a process that gives transistors with cut-off frequencies of 2 GHz. The 1-GHz modules use thin-film hybrid circuits with discrete 5-GHz transistor chips. Thin-film tantalum-nitride resistors and gold conductors are deposited on alumina substrates and the transistor chips, Schottky beam-lead diodes, and ceramic capacitors are bonded to the substrate.

For the 100-Hz-to-300-MHz frequency range, the 8091A Rate Generator module uses the same monolithic-IC oscillator circuit as the Model 8082A 250-MHz Pulse Generator. For frequencies above 300 MHz, a thin-film hybrid circuit based on the well-known emitter-coupled oscillator circuit is used (Fig. 6.). It is a relaxation oscillator with a repetition rate determined by capacitor C and the collector load resistors.

As shown in the diagram of Fig. 6, a third transistor (Q1) was added to the basic circuit. This makes the oscillator gateable. With no signal at the GATE input, Q1 is fully on, diverting the Q3 emitter current (I_3) while holding Q3 off.

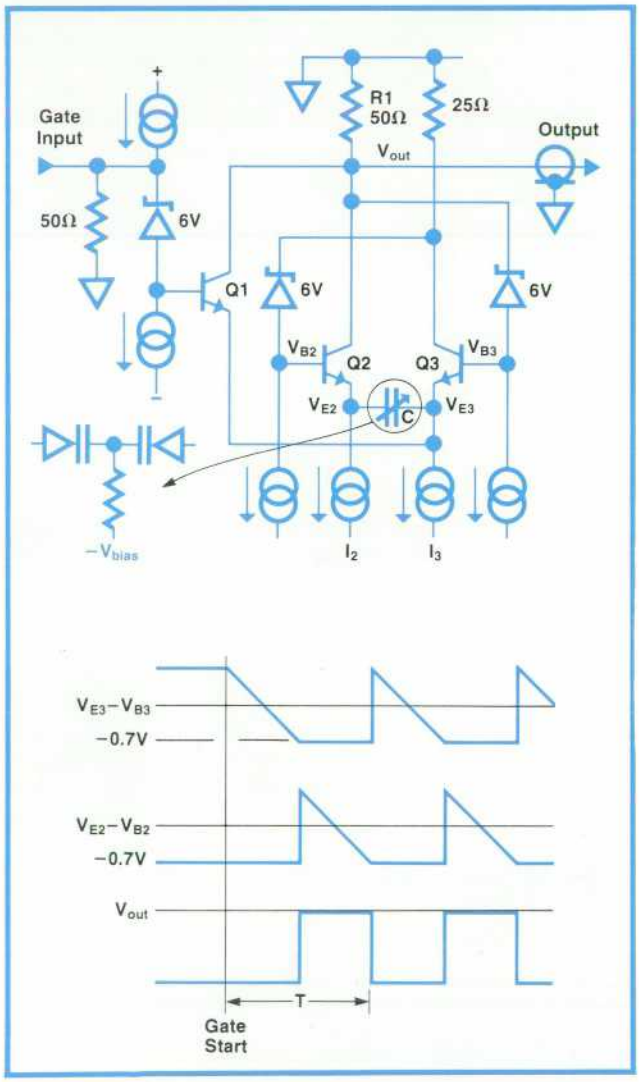


Fig. 6. *Emitter-coupled oscillator for repetition rates to 1 GHz. Waveforms show time-varying voltages within the oscillator. In the absence of a gating pulse, transistor Q1 clamps the oscillator in a state that corresponds to the running state at the end of time interval T so the first pulse of a burst will be identical to subsequent pulses.*

When a negative pulse is applied to the GATE input, transistor Q1 turns off and current I_3 now goes through capacitor C and transistor Q2, charging capacitor C. When the charge accumulating on capacitor C allows the emitter voltage of Q3 to fall to the turn-on level, regenerative action sets in, turning Q3 fully on and Q2 off. Current I_3 now flows through Q3 while I_2 flows through C and Q3, charging C in the opposite direction. This continues until Q2 turns on again, starting a new cycle.

As shown by the timing diagram, while transistor Q1 is on it establishes a "stop" state in the oscillator that is identical to the state of the oscillator at time T with both emitter currents (I_2 and I_3) flowing through the load resistor R1. Thus, a GATE pulse starts the oscillator from a state that occurs during free-running operation, making the first pulse identical to the following ones (except for a minor perturbation caused by switching current I_3 from Q1 to Q2). As a result, the oscillator is always synchronized to the gating pulse.

Capacitor C actually consists of two back-to-back varactor diodes with bias applied at their common point. Varying the bias with the front-panel, three-turn, high-resolution potentiometer varies the capacitance, which in turn varies the repetition rate over the 300-MHz-to-1-GHz range.

The oscillator output goes through an amplifier-limiter and then to the next module in the chain (signal connections between modules are made internally by means of coaxial cables). When the module is switched to the EXTERNAL mode, the oscillator is bypassed with the external signal going through a Schmitt trigger circuit directly to the amplifier. The module output is then a shaped version of the input signal, be it pulsed or sinusoidal, with the polarity and trigger level selectable.

A Fast-Switching Amplifier-Limiter

Two of the most challenging problems faced during the design of the system were: (1) how to achieve wideband pulse response from dc to more than a gigahertz; and (2) how, with extremely fast transition times of only 200 ps, to keep pulse perturbations at a very low level.

The first problem was resolved largely by using differential amplifiers wherever possible. However, since fast transistors are all NPN types, some means of level shifting is needed at least after every two amplifier stages. Otherwise the signal baseline would shift to higher and higher levels. It is desirable to have the signal level at ground at both the input and output of a hybrid microcircuit so the external transmission lines can be terminated simply with 50Ω resistors to ground.

Two ways of level shifting are commonly used: (1) zener diodes in series with the signal path between stages; and (2) capacitive coupling between stages with the bias levels chosen to establish the appropriate dc levels. Zener diodes can introduce problems with noise and temperature-induced level changes while capacitive coupling impairs low-frequency response, especially troublesome in a word generator where it may be necessary to maintain the 0 or 1 level for many clock periods.

The solution chosen for the 8080 system was to use capacitive coupling with dynamic dc restoration. In the circuit diagram of Fig. 7, C is the input coupling capacitor while operational amplifier A1 functions as the dc restoration circuit.

Note that the input signal goes to both inputs of A1 through identical voltage dividers so it appears to amplifier A1 as a common-mode signal. Hence, the signal does not appear at the output of A1 nor at the base of transistor Q2. Because of the degradation of op-amp common- mode rejection at high frequencies, a low-pass filter is used at the base of Q2 to attenuate any fast transients that may get through A1.

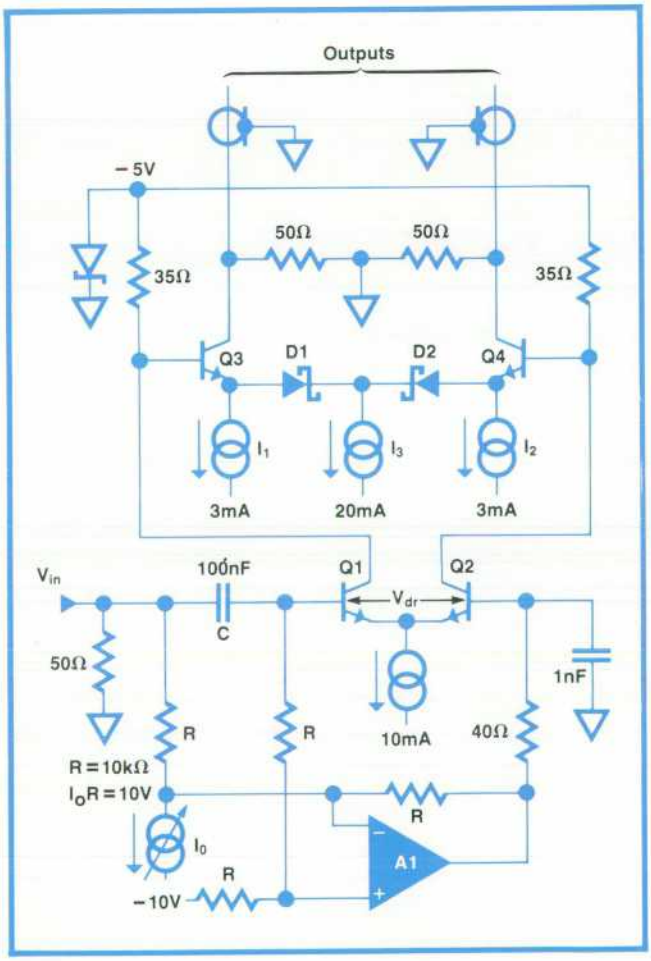


Fig. 7. *Broadband pulse amplifier uses capacitive coupling with dynamic dc restoration to obtain good low-frequency response, and current switching by Schottky diodes to achieve 200-ps transition times.*

To see how the dc restoration works, suppose that a positive-going step, V_{in}, were applied to the input. It would also appear as the drive voltage, V_{dr}, across the inputs of differential amplifier Q1-Q2. However, while the voltage step remains at its upper level, capacitor C charges, allowing the voltage at the base of Q1 and at the non-inverting input of A1 to sag. Because this sag appears to A1 as a differential input, it also appears at the output of A1 and at the base of Q2. The sag is thus a common-mode signal to Q1-Q2 so it does not affect the Q1-Q2 output, which retains the step level.

In other words, amplifier A1 responds to any voltage change across capacitor C and applies the change as a correction voltage to amplifier Q1-Q2.

Fast transitions at the amplifier output are achieved by inserting Schottky diodes (D1 and D2) in the emitter circuits of Q3 and Q4. The switching characteristics of transistors are degraded by the charge stored in a transistor when it is switched off but in the circuit shown in Fig. 7, transistors Q3 and Q4, biased by current sources I_1 and I_2 to operate always in the linear region, are never switched off. Current switching is performed by the Schottky diodes, which have practically no stored charge.

Suppose the signal at the base of transistor Q4 is in the low state and that of Q3 is high. Diode D1 would then be forward biased, so the Q3 collector current would be $I_1 + I_3$ (23 mA) while the Q4 collector current would be I_2 only (3 mA). Now, when the driving signal reverses state, D2 becomes forward biased, reversing the bias on D1 so current I_3 switches to Q4, leaving a collector current of 3 mA in Q3. This transition occurs very quickly because of the fast switching of the diodes.

Incremental Delay

Very little jitter can be tolerated in the pulse delay circuit of this pulse generator because of the fast rise time and very short pulse period. Hence, the Model 8092A Delay Generator uses delay lines rather than the usual one-shot multivibrator for the delay function. Delay lines of various lengths are switched in to vary the delay in 100-ps steps up to the maximum of 9.9 ns, an arrangement that also allows the delay to be made greater than the pulse period.

Delay lines of differing lengths are arranged in three groups in series. One line in each group is switched into the signal path by logic circuits that apply forward bias to PIN diodes at each end of each line, as shown in Fig. 8.

PIN diodes are used because of their very low capacitance when reverse biased; the switched-off diodes therefore do not load the driving signal appreciably. For low-frequency driving signals, they behave as conventional diodes. When a pair of diodes is switched on, the applied bias is sufficient to maintain the diodes in the "on" state for both states of the signal waveform with a diode resistance of about 0.5 ohm. At frequencies above a few megahertz, the diodes behave as pure resistors with a resistance of about 1 ohm.

To avoid the great expense of matching diodes during instrument production, the diodes are not selected. Diode mismatch could result in dc offsets of as much as 50 mV in the signal when switching from one delay line to another but offsets are eliminated by a circuit configuration that uses the average level of the "undelayed" signal, which has no dc offset, as a reference against which the average level of the delayed signal is compared. The result of the compari-

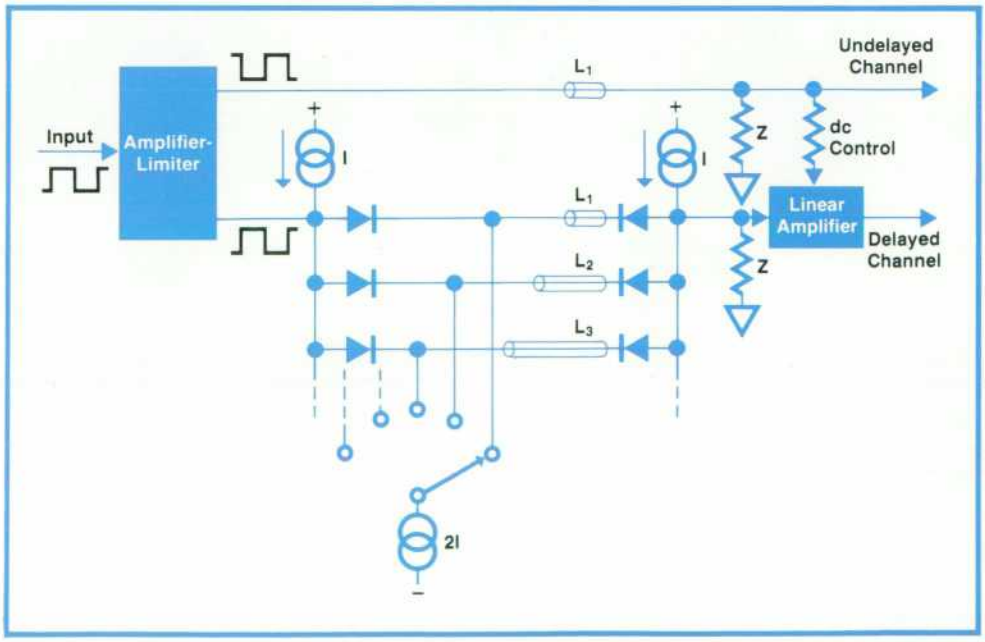


Fig. 8. *Method of switching transmission lines in the Model 8092A Delay Generator/Frequency Divider to select the pulse delay. With three groups of switched transmission lines in series, the total relative delay is selectable from 0 to 9.9 ns in 100-ps steps.*

son is used to correct the dc level of the delayed signal.

The half-frequency output is obtained by toggling a flip-flop. The flip-flop can be reset by a front-panel pushbutton or electrical signal so the half-frequency waveform may always start from a known state when the system is operating in the gated-pulse mode. A half-frequency trigger signal is also provided for use by an oscilloscope or other instrument.

Word Generation

The Model 8084A Word Generator module gives the 8080 system the ability to generate serial bit patterns up to 64 bits long at clock rates up to 300 MHz.

The bit patterns are stored in a 64-bit semiconductor memory organized into four 16-bit rows. A 4-state counter, advanced one count each time a front-panel pushbutton is pressed, addresses one row at a time for loading or readout. Data entered into a 16-bit load register by front-panel pushbuttons is loaded into the selected row of the memory when the LOAD pushbutton is pressed. Pressing the FETCH pushbutton results in a non-destructive readout of the selected row, returning the data to the load register for display. Bit data in the register is displayed by a row of LEDs.

The major design problem to be solved in this module was how to read out the data serially at bit rates up to 300 MHz. The solution chosen was to design the CMOS memory with a static, 64-bit, parallel output and serialize the data with multiplexers.

Recalling that a bit rate of 300 MHz corresponds to a bit period of 3.3 ns, it is easy to see that one-level multiplexing would require a large number of very fast—and hence expensive—integrated circuits. Therefore, multiplexing is done on a three-tier basis with only the last tier requiring the use of very high-

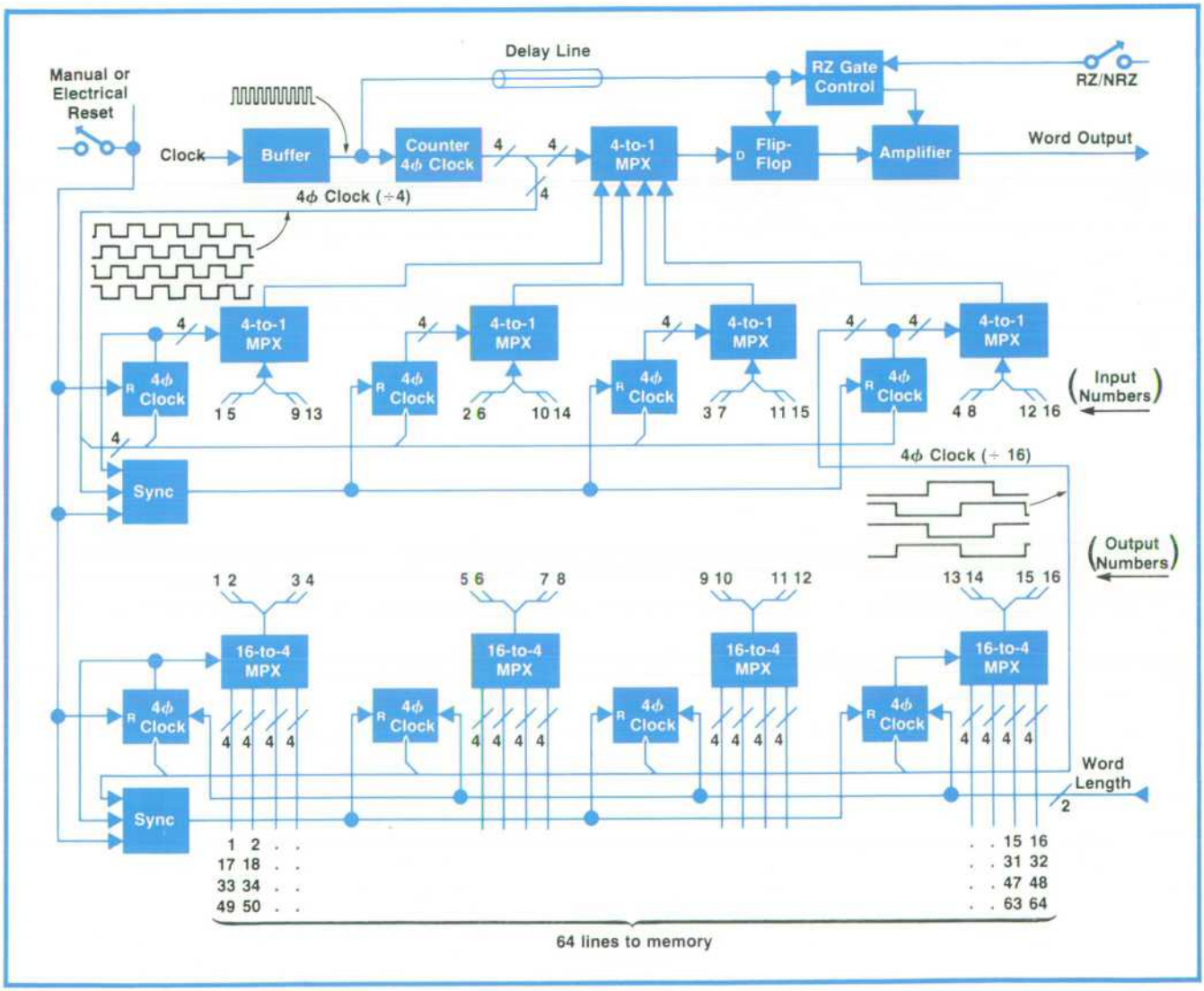


Fig. 9. *Multiplexing the memory output in three steps reduces the number of very fast circuits needed to generate digital words at a 300-MHz bit rate.*

speed circuits.

A block diagram of the serializer system is shown in Fig. 9. The high-speed circuits are in the top row of the diagram. The circuits in the next row operate at one-fourth the speed, i.e. a maximum of 75 MHz while the maximum speed of the circuits in the bottom row is one fourth of that (18.75 MHz).

Circuit operation is as follows. The output of the associated rate generator serves as the clock. It is applied to a ÷4 counter that produces a 4ϕ clock with each phase operating at one-fourth the input rate. The four clock outputs drive the final 4-to-1 multiplexer, sequentially gating the outputs of the second-row multiplexers into the output bit stream. The output bit stream is resynchronized by the input clock before going to the output amplifier (to derive the RZ format from the synchronizing flip-flop's normal NRZ format, the clock is used to gate the output amplifier).

Each of the four 4ϕ clock signals also goes to a ÷4 counter in the second row where each generates another 4ϕ clock with each phase operating at one-fourth the rate of the top-row counter. Each counter drives a 4-to-1 multiplexer that sequentially gates four inputs from multiplexers in the bottom row. To achieve correct sequencing, the states of the second-row counters must be properly coordinated. This is done by using the first phase of the first counter in the row to time the reset of the other counters.

Each of the second-row multiplexers can take up to three rate-generator clock periods to switch the next bit to its output before the top-row multiplexer interrogates it again. The switching time of the second row multiplexers therefore need not be as fast as the top-row multiplexer. Commercially available ECL circuits are used in the second row whereas HP-designed ECL circuits are used in the top row. In the same way, the switching time of the bottom-row multiplexers can be much slower than the second-row multiplexers.

The bottom-row circuits, shown here as 16-to-4 multiplexers, operate in the same manner as the second row. The counting sequence in the counters in the bottom row, however, can be changed to effect a change of word length. For a 16-bit word, the counters remain in the 0 state so only one bit out of the four supplied to each section of the bottom-row multiplexers is output. For a 32-bit word, only one of the flip-flops in each counter toggles, so each multiplexer outputs two bits alternately. For a 64-bit word, each counter is allowed to run its full cycle.

During GATED operation, the last word is always completed regardless of the time the GATE input waveform terminates. The module generates its own gating pulse to gate the input clock in response to a GATE input (or SINGLE word trigger). It also feeds the internally-generated gate back to the rate generator to turn the squarewave generator on and off at the appropriate times.

In addition to the data word, there are three trigger outputs: FIRST BIT, LAST BIT, and CLOCK (during SINGLE or GATED operation, the CLOCK signal is output only while a word is being generated).

Acknowledgments

Klaus Hoffman designed the mainframe tandem power supply, which uses a switching regulator for efficiency followed by a series-pass regulator for quietness. Horst Link did the mechanical design. Sigurt Krass contributed to the data control and memory in the word generator. Thanks are also due Robin Adler and Gerhard Herrmann for help in defining the system and to group leaders Arndt Pannach and Dieter Vogt for overall guidance.

Reference:

1. G. Globas, J. Zellmer, and E. Cornish, "A 250-MHz Pulse Generator with Transition Times Variable to Less than 1 ns," Hewlett-Packard Journal, September 1974.

Volker Eberle

A native of Swabia (the southeast portion of Germany), Volker Eberle earned his Diplom Ingenieur at the Technisch Universität Stuttgart (1975) and then joined Hewlett-Packard, going straight to work on the 8092A Delay Generator/Frequency Divider module for the 8080 system. During the final phase of the 8080 development, he became project leader, guiding the system into production. Leisure-time activities include gardening and accordion-playing (he's vice-president of his accordion club).

Christian Hentschel

Before joining HP in 1972, Christian Hentschel was involved at the Institut für Theoretische Elektrotechnik, Universität Aachen, in research on thin-film, high-frequency lumped circuit elements, a topic on which he based his doctoral dissertation when earning a Dr. Ing. degree. At HP, he worked initially on a risetime converter accessory, then on the 8082A 250-MHz Pulse Generator before becoming project manager for the 8080 system and ultimately group leader. Married (his wife is a systems analyst at the Technische Universität Stuttgart), but with no children, in off hours Christian enjoys tennis, sailing, scuba diving, and photography.

Corrections

In our July 1977 issue, Fig. 2 on page 9 and Fig. 3 on page 10 are interchanged. The captions are correct, but the drawings have been swapped. Also, the function listed as INDEXING in the summary on page 14 is called SUBSCRIPTION on page 19. Both names refer to the same function.

Günter Riebesell

A native of Hamburg, Germany, and a graduate (Diplom Ingenieur) of the Technische Universität Braunschweig, Günter Riebesell joined HP in 1973, going to work on the rate generator and output circuits for the 8016A Word Generator before becoming project leader for the 8084A 300-MHz Word Generator module for the 8080 system. A member of the HP GmbH soccer team, Günter also enjoys filming and skiing. He and his wife are expecting their first child this month.

Joel Zellmer

On obtaining BSEE and MSEE degrees from the University of Minnesota (1966), Joel Zellmer joined HP's Colorado Springs Division where he worked on squarewave generators and scope probes before becoming involved with IC design for the 8082A 250 MHz Pulse Generator. He transferred with that project to HP GmbH (Germany) in 1973 and also contributed to the 8080 1-GHz circuits before returning to the Colorado Springs Division in 1975. Off hours, Joel goes sailing or skiing, or builds and flies radio-controlled model sailplanes. He and his wife have two children, 7 and 12.

SPECIFICATIONS

HP 8080 Modular Pulse/Word Generator System

Repetition Rate Generators

OPERATING MODES

NORM: Repetition rate determined by front panel controls.
EXTERNAL TRIGGER: Repetition rate controlled externally. Shaped input signal is output at both internal and external trigger outputs.
EXTERNAL/INTERNAL GATE: External/internal gate signal turns repetition rate generator on synchronously.
MANUAL: All external functions can be triggered manually by pressing a pushbutton.

	8081A	8091A
TIMING		
REPETITION RATE:	10 Hz to 300 MHz.	100Hz to 1000 MHz.
PERIOD JITTER:	≤0.1%±50 ps.	≤0.1%±20 ps.
EXTERNAL INPUTS (50Ω typical input impedance)		
EXTERNAL TRIGGER		
Repetition rate:	0 to 300 MHz.	0 to 1000 MHz.
Pulse width:	≥1.7 ns.	≥0.5 ns.
EXTERNAL GATE		
ON/GATE OFF TIME:	>1 period/>1 period + 10 ns.	>1 period/>1 period + 10 ns.
TRIGGER LEVEL:	−1V to +1V.	−1V to +1V.
SENSITIVITY:		
1000 MHz to >300 MHz		pulse/sine: 600 mV p-p
≤300 MHz	200 mV p-p	pulse: 200 mV p-p; sine: 1.0 V p-p.
SLOPE/MAX. INPUT VOLTAGE	neg, pos selectable/±6V.	neg, pos selectable/±6V.
INTERNAL GATE INPUT (50Ω typical input impedance)		
GATE ON/GATE OFF TIME:	>10ns/>20ns.	>10ns/>20ns.
HIGH SIGNAL LEVEL:	0V±100 mV.	0V±50 mV.
LOW SIGNAL LEVEL:	more neg. than −500 mV.	more neg. than −500 mV.
MIN. AMPLITUDE:	≥500 mV p-p.	≥500 mV p-p.
MAXIMUM INPUT VOLTAGE:	±1V.	±1V.
EXTERNAL TRIGGER OUTPUT (50Ω typical output impedance)		
HIGH SIGNAL LEVEL:	more pos. than −100 mV.	more pos. than −100 mV.
LOW SIGNAL LEVEL:	more neg. than −500 mV.	more neg. than −500 mV.
MIN. AMPLITUDE:	≥500 mV p-p.	≥600 mV p-p.
TRANSITION TIMES (10%–90%):	≤1.2 ns.	≤500 ps.
DUTY CYCLE:	50%±10%	50%±10%
MAX. EXTERNAL VOLTAGE	±2V.	±2V.
INTERNAL OUTPUT (50Ω typical output impedance)		
FAN-OUT:	each module can drive one 8080 system module	
HIGH SIGNAL LEVEL:	more pos. than −100 mV.	more pos. than −100 mV.
LOW SIGNAL LEVEL:	more neg. than −500 mV.	more neg. than −500 mV.
MIN. AMPLITUDE:	≥500 mV p-p.	≥600 mV p-p.
TRANSITION TIMES (10%–90%):	≤1.2 ns.	≤500 ps.
DUTY CYCLE:	50%±10%	50%±10%
SIZE:	Quarter mainframe width.	Quarter mainframe width.

PRICES IN U.S.A.: 8081A, $795; 8091A, $3145.

Output Amplifiers

	8083A	8093A
OUTPUT PULSE		
AMPLITUDE (into 50Ω):	3 ranges: 2V to 0.6 V (by vernier); 0.6 V to 0.2 V (by vernier); ECL (−0.8 V to −1.6 V typical).	2 ranges: ≤0.6 V to 1.2 V (by vernier); ECL (−0.8 V to −1.6 V typical, internally adjustable: offset, ±0.9 V; amplitude, 0.5V to 0.9V).
OFFSET (into 50Ω load):	±1 V (common to both channels).	±1.2 V.
MAXIMUM LEVELS:	±4 V.	±4 V.
TRANSITION TIME (10% to 90%):	≤800 ps.	≤300 ps.
DUTY CYCLE:	Determined by duty cycle of driving (clock) pulse. Can be adjusted ±10% using trigger level control (inside), e.g. with 50% duty cycle input, output can be from 40%–60% duty cycle.	
PRESHOOT, OVERSHOOT, RINGING:	≤10%	≤10% up to 500 MHz; ≤15%>500 MHz.
OUTPUT CHANNELS	NORMAL and COMPLEMENT outputs provided simultaneously.	Selectable NORMAL or COMPLEMENT format.
SOURCE IMPEDANCE:	50Ω±5%.	50Ω±5%.
REFLECTION COEFFICIENT:	<15%.	<20%.
POLARITY:	neg/pos selectable.	neg/pos selectable.
DRIVE INPUT (Internal)		
INPUT FREQUENCY:	0 to 300 MHz.	0 to 1000 MHz.
INPUT IMPEDANCE:	50Ω typical.	50Ω typical.
HIGH SIGNAL LEVEL:	more positive than −100 mV.	more positive than −100 mV.
LOW SIGNAL LEVEL:	more negative than −500 mV.	more negative than −500 mV.
MINIMUM AMPLITUDE:	≥500 mV p-p.	≥500 mV p-p (tr, tf ≤350 ps). ≥600 mV p-p (tr, tf ≤500 ps).
TRANSITION TIMES (10%–90%):	≤3 ns.	≤350 ps/≤500 ps.
MAXIMUM EXTERNAL VOLTAGE:	±1 V.	±1 V.
PROPAGATION DELAY TIMES:	4.8 ns ± 500 ps.	4 ns ± 200 ps.
SCHMITT TRIGGER INPUT (Internal)		
INPUT FREQUENCY:		0 to 300 MHz.
INPUT IMPEDANCE:		50Ω typical.
HIGH SIGNAL LEVEL:		more positive than −100 mV.
LOW SIGNAL LEVEL:		more negative than −500 mV.
MINIMUM AMPLITUDE:		≥500 mV p-p.
TRANSITION TIMES (10%–90%):		≤10 ns.
MAXIMUM INPUT VOLTAGE:		±1 V.
PROPAGATION DELAY TIME:		7.8 ns ± 300 ps.
SIZE	Quarter mainframe width.	Eighth mainframe width.

PRICES IN U.S.A.: 8083A, $795; 8093A, $1525.

8092A Delay Generator/Frequency Divider

CHANNEL B DELAY/ADVANCE (Channel A reference)
RANGE: ±9.9 ns.
STEP SIZE: 100 ps.
ACCURACY OF DELAY: ≤±(1% + 50 ps) ± Δ (Δ is dependent on repetition rate, independent of delay setting). Δ = 0 for f = 0 to 100 MHz. Δ ≤ 80 ps for f = 100 MHz to 1 GHz.
FREQUENCY DIVISION (selectable by front panel switch):
FREQUENCIES AVAILABLE (channel B): $f_{\text{channel A}}$; $\frac{1}{2}f_{\text{channel A}}$.
OUTPUTS (Internal)
FAN OUT: one 8080 module can be driven from each output.
CHANNEL A:
HIGH LEVEL: more positive than −100 mV.
LOW LEVEL: more negative than −600 mV.
MINIMUM AMPLITUDE: ≥600 mV p-p.
TRANSITION TIMES (10%—90%): ≥500 ps.
CHANNEL B:
f MODE: same as channel A.
½f MODE:
HIGH LEVEL: more positive than −100 mV.
LOW LEVEL: more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p.
TRANSITION TIMES (10%—90%): ≤350 ps.
DUTY CYCLE: Determined by duty cycle of driving (clock) pulse. Can be adjusted ±10% using trigger level control (inside).
OUTPUT IMPEDANCES: 50Ω typical.
TRIGGER OUTPUT (supplied only in f/2 mode).
HIGH LEVEL: more positive than −100 mV.
LOW LEVEL: more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p.
TRANSITION TIMES (10%—90%): ≤1 ns.
OUTPUT IMPEDANCE: 50Ω typical.
DRIVE INPUT (Internal)
INPUT FREQUENCY: 0 to 1000 MHz.
INPUT SIGNAL:
HIGH LEVEL: more positive than −100 mV.
LOW LEVEL: more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p (t_r, t_f ≤350 ps).
≥600 mV p-p (t_r, t_f ≤500 ps).
TRANSITION TIMES (10%—90%): ≤350 ps/≤500 ps.
PULSE WIDTH: ≥0.5 ns.
INPUT IMPEDANCE: 50Ω typical.

MANUAL RESET: Pushbutton resets channel B to low level (only in f/2 mode and drive input low).
RESET INPUT (intended to be connected in parallel with ext. gate input of Repetition Rate Generator). Negative transition resets channel B to low level (only in f/2 mode and drive input low).
INPUT FREQUENCY: 0 to 2 MHz.
RESET TIME: ≥0.5 μs.
INPUT SIGNAL:
HIGH LEVEL: more positive than −100 mV.
LOW LEVEL: more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p.
TRANSITION TIMES (10%—90%): ≤10 ns.
INPUT IMPEDANCE: 1 kΩ typical.
SIZE: Quarter mainframe width.
PRICE IN U.S.A.: $2600.

8084A Word Generator

DATA CAPACITY
NUMBER OF DATA CHANNELS: 1.
WORD LENGTH: 16, 32 or 64 bits selectable.
CYCLE MODES
AUTO CYCLE: Data recycled continuously.
SINGLE CYCLE: One word per cycle command pulse.
GATED CYCLE: Words are generated as long as cycle command is active. Last word always completed.
CYCLE COMMAND INPUT
INPUT IMPEDANCE: 50Ω ± 10% or 600Ω ± 10%, selectable by PC-board switch.
AMPLITUDE/WIDTH: ≥+0.8 V/≥3 ns.
PERIOD BETWEEN CYCLE COMDMANDS: Word length + 2 × clock periods + 100 ns.
MAXIMUM INPUT VOLTAGE: 6 V.
MANUAL: by pushbutton on front panel.
CLOCK INPUT (Internal)
REPETITION RATE: 0—300 MHz; impedance: 50Ω typical.
HIGH SIGNAL LEVEL: more positive than −100 mV.
LOW SIGNAL LEVEL: more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p.
TRANSITION TIMES (10%−90%): ≤3 ns.
WIDTH FOR ≤100 MHz REP. RATE: ≤3 ns.
WIDTH FOR 100—300 MHz REP. RATE: 50% ± 10% duty cycle.
SLOPE: low to high transition generates bit.
INTERNAL OUTPUTS (Word, Word, Clock Gate)
FAN-OUT: each drives one 8080 system module.
GATE FUNCTION: high level stops rep. rate generator; low level starts rep. rate generator.
WORD AND WORD FORMAT: RZ or NRZ, selectable by front panel switch.
CLOCK: same as CLOCK output but inverted.
SOURCE IMPEDANCES: 50Ω ± 5%.
HIGH SIGNAL LEVEL (into 50Ω): more positive than −100 mV.
LOW SIGNAL LEVEL (into 50Ω): more negative than −500 mV.
MINIMUM AMPLITUDE: ≥500 mV p-p.
TRANSITION TIMES (10%—90%): Word, ≤1.2 ns; Gate, ≤1.5 ns.
RZ WIDTH (duty cycle): determined by duty cycle of drive (clock) pulse. WORD, $\overline{\text{WORD}}$ and $\overline{\text{CLOCK}}$ outputs can be adjusted ± 10% using internal trigger level control.
EXTERNAL OUTPUTS (Clock, First Bit, Last Bit)
CLOCK: Delivers one clock pulse per bit. Format: RZ
FIRST BIT (FB): Simultaneous with first bit of serial word. Format: NRZ.
LAST BIT (LB): Simultaneous with last bit of serial word. Format: NRZ.
SOURCE IMPEDANCES: 50Ω ± 5%.
SIGNAL LEVELS INTO 50Ω: selectable by PC board switch.
HIGH LEVEL: more positive than −100 mV or >+500 mV.
LOW LEVEL: more negative than −500 mV or > + 100 mV.
MINIMUM AMPLITUDES: >500 mV p-p.
TRANSITION TIMES (10%—90%): FB, LB ≤1.5 ns; CLOCK ≤1.2 ns.
RZ-WIDTH (duty cycle): determined by duty cycle of driving (clock) pulse. Can be adjusted ±10% using internal trigger level control.
TIME RELATIONSHIP (signal delay with reference to data output in NRZ mode, measured from leading edge to leading edge).
CLOCK: 1 ns ±0.5 ns.
FIRST BIT AND LAST BIT: 0 ns ± 0.5 ns.
Data output in RZ mode: 1 ns ± 0.5 ns.
NOTE: options 083 and 093 compensate for propagation time of output amplifier module so timing relationships are maintained. Tolerances increase to ±1 ns.
OPTIONS
001: replaces internal Clock input, Gate and Word outputs with front-panel BNC connectors.
083 AND 093: should be ordered when the 8084A is connected to an 8083A output amplifier (option 083) or an 8093A output amplifier (option 093) in the same mainframe. For other combinations, contact your Hewlett-Packard Service Office.
SIZE: half mainframe width.
PRICE IN U.S.A.: $2510.

8080A Mainframe

ELECTRICAL: provides dc power for two ½-size modules, four ¼-size or eight ⅛-size modules in any combination.
MECHANICAL: mainframe compartments accept up to two ½-size modules, four ¼-size modules, eight ⅛-size modules or combinations of half, quarter or eighth-size modules.
WEIGHT: 5 kg (11 lbs).
POWER: 115 or 230 V + 10%, −22%. 48 to 66 Hz single phase. Up to 200 VA.
POWER AVAILABLE FOR MODULES: 55 W dc.
DIMENSIONS: 426 mm W, 145 mm H, 450 mm D (16¾ in × 5 11/16 in × 17¾ in).
PRICE IN U.S.A.: $1000.
MANUFACTURING DIVISION: HEWLETT-PACKARD GmbH
Herrenbergerstrasse 110
D-7030 - Böblingen, Württemberg
Germany

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

HEWLETT-PACKARD JOURNAL

AUGUST 1977 Volume 28 • Number 12

Technical information from the Laboratories of Hewlett-Packard Company

Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
Amstelveen-1134 The Netherlands
Yokogawa-Hewlett-Packard Ltd., Shibuya-Ku
Tokyo 151 Japan

Editorial Director • Howard L. Roberts
Managing Editor • Richard P. Dolan
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