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A Self-Contained, Hand-Held Digital Multimeter—A New Concept in Instrument Utility

Aside from clipping the coiled lead to any convenient reference point, only one hand is needed to hold this instrument, and take a reading.

by Robert L. Dudley and Virgil L. Laing

IT IS GENERALLY ACCEPTED that a multimeter for measuring voltage and resistance is an indispensable tool for service specialists, technicians and engineers. There have been many improvements in the last few years, such as digital readout, high input impedance, better accuracy and resolution, and these improvements have helped the user make measurements more precisely with fewer errors. Little has been done, however, to make the multimeter easier to use and better suited to the technician or engineer who needs to make fast measurements in hard-to-get-at places.

Shown in Fig. 1 is a new battery-powered 3½ digit Probe Multimeter that is completely self-contained and can be held and operated in one hand. The instrument has autoranging, autopolarity, and autozero, which means the user need only set the function switch and depress the power bar to get an accurate reading.

To use the instrument, the coiled lead is attached to a suitable ground or reference point, and the probe tip is placed on the point to be measured. When the power switch is pressed, the voltage or resistance value appears on the display with range and polarity automatically selected.

Several advantages of this probe configuration are apparent. Portability is an obvious one, and the location of the display close to the point of measurement speeds reading time while eliminating the need to shift the eyes to get a reading.

Another advantage is the ability to invert the display to facilitate readings when the Probe is held upside-down to reach a hard-to-get-to place (Fig. 2). In addition, the probe tip can be pivoted into three detented positions: straight, tilted at 30°, and tilted at 60°. The tip can be folded back so that the Probe can be carried in a pocket or the belt-carrying case provided with the instrument.

A Real Instrument

This hand-held instrument is a true digital multimeter with three digits of readout plus a "1" for 10% overranging. The most sensitive range for both ac and dc measurements is 100 mV full scale with 0.1 mV resolution. Although the input is protected up to 1000 V, for safety reasons the maximum input voltage is specified at 500 V.

The accuracy of readings is better than 1% for dc voltages and between 2 and 5% for ac. The input



Cover: *The hand-held digital multimeter—a concept that's been in the back of many an engineer's mind ever since integrated circuits went large-scale—has become a reality. Doing it required more than an integrated circuit, however; it required a combination of technologies as described here. (Zero is added to 3-digit display here to indicate range.)*

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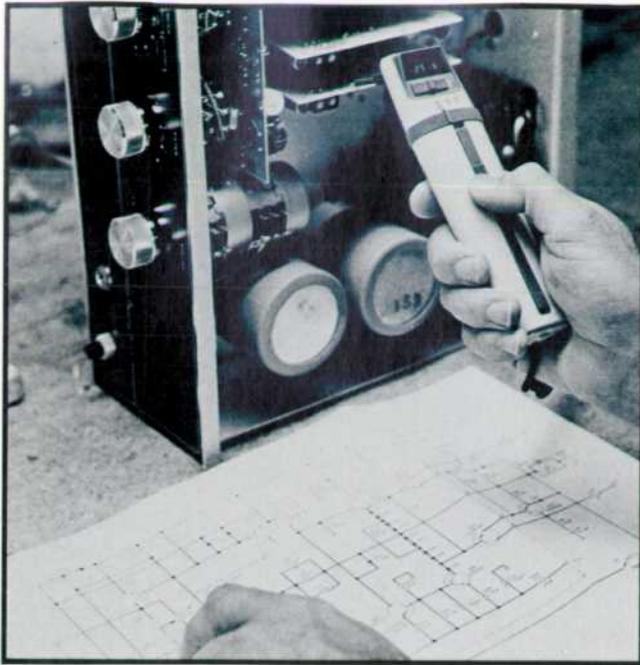


Fig. 1. Model 970A Digital Multimeter was designed for convenient hand-held operation. The user needs only to select the desired function and press the power switch (the long, flat bar) to take a reading; the instrument automatically selects the right measurement range.

impedance is 10 megohms paralleled by less than 30 pF. The ac frequency range is up to 3500 Hz, wide enough for power line and most voice-channel measurements.

As an ohmmeter, the new multimeter has full-scale ranges from 1 to 10,000 kilohms with a resolution of 1 ohm on the lowest range. The accuracy of ohms readings is better than 2%. In all functions, the instrument displays a reading in less than 2 seconds after the switch is pressed (to speed this up, it starts at mid-range and then ranges in the appropriate direction). In continuous operation, it makes 3 readings per second.

The Ni-Cad batteries that power the instrument can operate continuously for a minimum of 2½ hours before needing recharge, but by pressing the switch only when a reading needs to be taken, the user can make at least 2000 readings on one charge. The power switch has a lock position for those occasions when continuous monitoring may be desired. For recharge, the batteries slip out of the instrument and into a charger that plugs into a wall outlet (see Fig. 12). Where heavy use is anticipated, an extra set can be obtained so one set can be recharging while the other is used in the instrument.

Design Philosophy

The original objective at the start of the design phase was to design a 3½-digit multimeter at the

lowest possible cost consistent with traditional HP dependability. As the circuit design evolved it became apparent that the circuits could be contained within a surprisingly small space at modest cost, using recently-developed monolithic and thin-film hybrid integrated-circuit technologies. Thus, a hand-held, self-contained instrument was a possible configuration to be considered.

Other than the obvious operating conveniences, other advantages would accrue from a hand-held configuration. Since the display would be close to the point of measurement, it would not have to be read from a distance and therefore could be small and more economical. The miniature LED display developed for the HP hand-held calculators was ideal for this situation, and it uses less power than a larger display. Since the display could be in line and close to the point of measurement, a press-to-read type of operation could be used to further conserve power. Hence smaller batteries could be used. It was decided, then, to place project emphasis on providing the multimeter capability in a hand-held instrument.

Many shapes and configurations were evaluated. The elliptical cross-section was adopted as this fits the hand comfortably while providing a tactile clue as to the orientation of the instrument. In keeping with the concept of hand-held convenience, the case surface is textured to minimize slippage. The problem of where to place a multi-position function switch was solved by development of the "watch-band" switch. The power switch was designed as a bar that can be operated along most of its length. This, plus the invertible display and swiveled

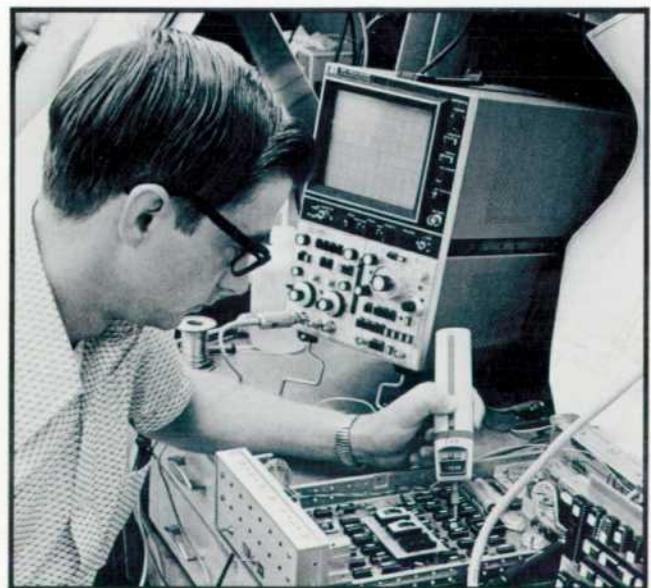


Fig. 2. Slide switch adjacent to the display inverts the numerals so readings can be taken with the probe upside down.

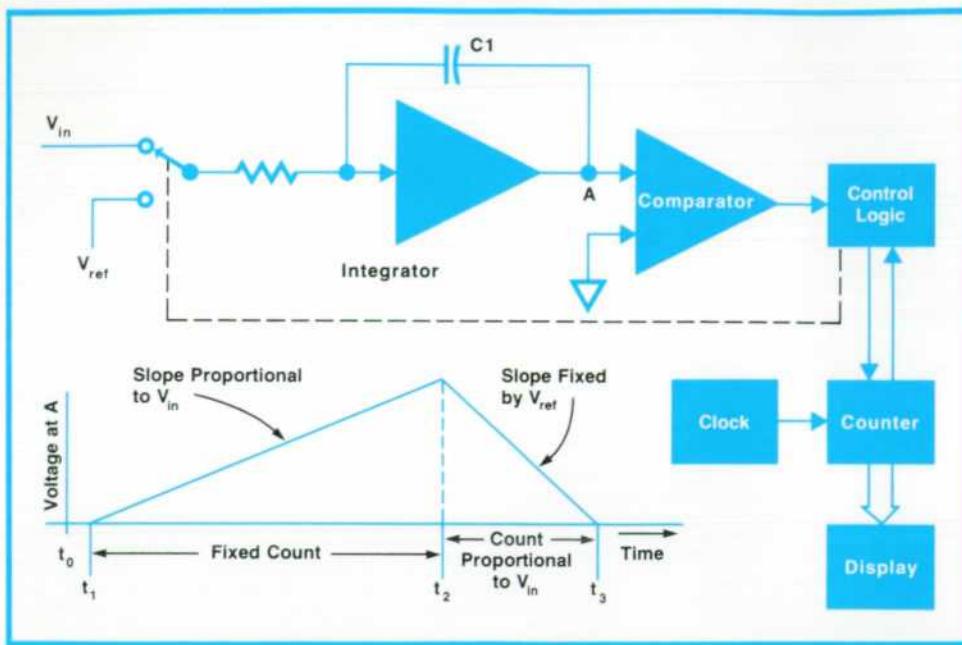


Fig. 3. Digital-to-analog conversion by the dual-slope technique is essentially a voltage-to-time conversion with digital measurement of the resulting time interval.

probe tip, allows the instrument to be used conveniently in a variety of positions. To protect the user against accidental contact to high voltages, the instrument was designed so there are no exposed metallic parts anywhere on the instrument, except for the probe tip and the ground clip.

Inside

The Probe Multimeter is an integrating digital voltmeter that employs the widely-used dual-slope technique to derive a digital display from a dc voltage. Although described recently in this publication¹, the description is repeated here for the sake of completeness.

With reference to the timing diagram of Fig. 3, at time t_1 the unknown input voltage V_{in} is applied to the integrator. Capacitor $C1$ then charges at a rate proportional to V_{in} .

The counter starts totalizing clock pulses at time t_1 and when a predetermined number of clock pulses has been counted, the control logic switches the integrator input to V_{ref} , a known voltage with a polarity opposite to that of V_{in} . This is at time t_2 . Capacitor $C1$ now discharges at a rate determined by V_{ref} .

The counter is reset at time t_2 and again it counts clock pulses, continuing to do so until the comparator indicates that the integrator output has returned to the starting level, stopping the count. This is at time t_3 .

The count retained in the counter is proportional to the input voltage. This is because the time taken for capacitor $C1$ to discharge is proportional to the charge acquired, which in turn is proportional to the input voltage. The number in the counter is then displayed to give the measurement reading.

The attractive characteristic of this technique is that many of the variables are self-cancelling. For example, long-term changes in the clock rate or in the characteristics of the integrator amplifier, resistor, or capacitor affect both the charge and discharge cycles alike. Considerable long-term deviation from normal values can be tolerated without introducing errors.

Also, since the input voltage is integrated during the up slope, the final charge on $C1$ is proportional to the average value of the input during the charge cycle. Noise and other disturbances are thus averaged out and have a reduced effect on the measurement. In particular, by making the charging cycle equal to an integral number of power line cycles, the effect of any power line hum is reduced by a substantial amount.

The Overview

A block diagram of the new multimeter is shown in Fig. 4. The input is applied to amplifier $A1$, which has feedback resistors that can be switched to change gain and hence the sensitivity range. The 10-megohm resistor in series with the input, besides being an essential part of the amplifier configuration, also provides protection against high input voltages.

The offsets in the amplifiers and integrator are compensated for by an autozero technique similar to that used in other HP digital multimeters.¹ Just prior to the integration cycle (see Fig. 4), MOSFET switches disconnect the input signal and connect a matching 10-megohm resistor to the input of amplifier $A1$. In the autozero mode, the comparator operates as a high-gain amplifier and a feedback loop is

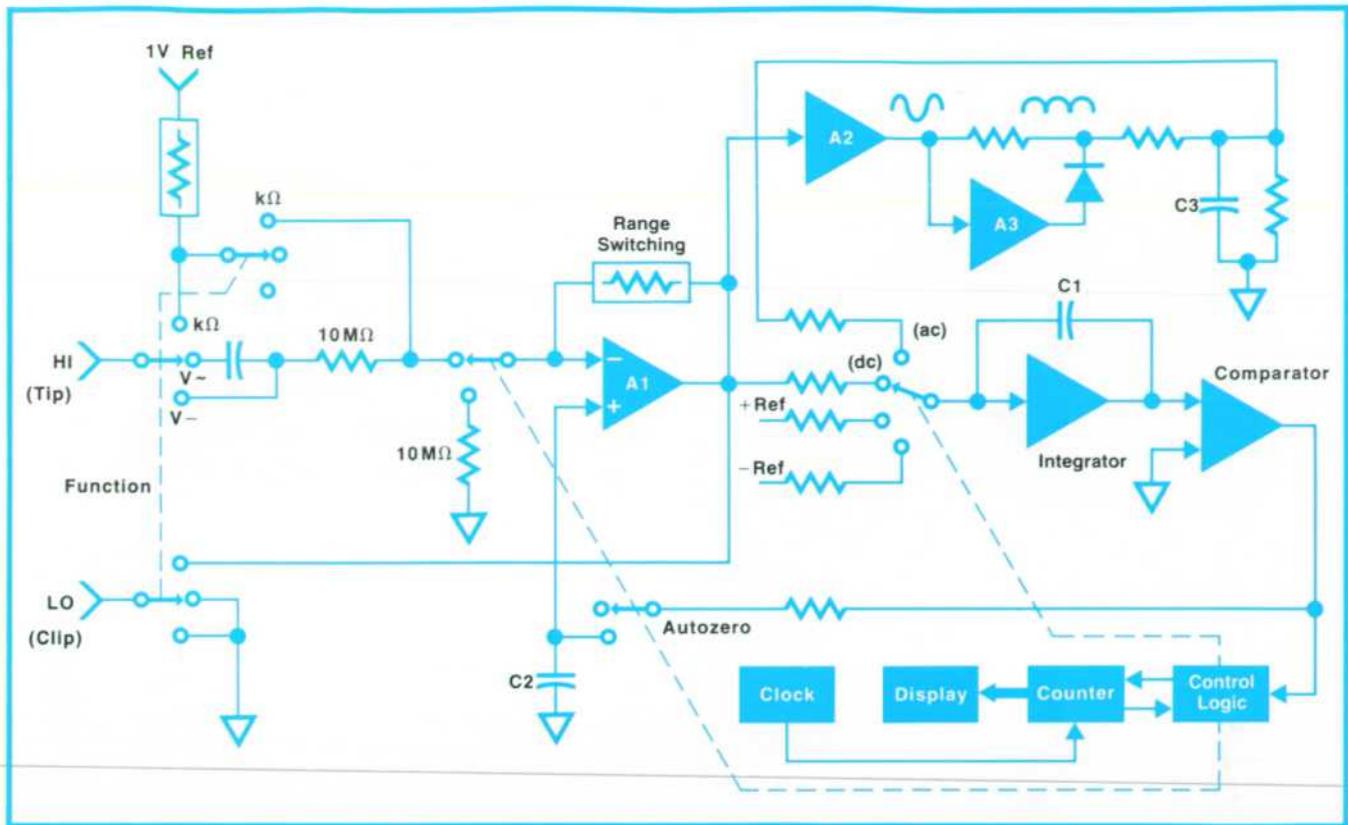


Fig. 4. Simplified block diagram of Model 970A Digital Multimeter. Except for the FUNCTION switch, all the switches shown here are MOSFET switches on the main monolithic IC chip.

closed around the input amplifier, integrator, and comparator, charging the autozero capacitor C2 to a voltage that compensates for the offset voltages in the entire feedback loop. When the input is reconnected to amplifier A1, the feedback to C2 is disconnected but the charge on C2 remains during the measurement to compensate for the offsets. The autozero circuit thus eliminates the requirement for a zero-adjust potentiometer.

Following the input amplifier, dc voltages are applied to the integrator for conversion to digital form. A number of changes were made, however, to the standard dual-slope integration to enhance the operation of the Probe Multimeter. For example, by using an integration time of 1/6 second on some ranges rather than 1/60 second (1/5 and 1/50 second in European versions), sensitivity can be increased by a factor of 10. Then, only three range resistors, providing 100:1 steps, are needed in the input amplifier with switching of the integration time to give the 10:1 range steps. This reduces the number of resistors and interconnections required in the feedback loop around the input amplifier.

With reference to the logic diagram of Fig. 5, operation of the A-to-D converter is as follows.

The counter is a modulus 3000 counter, which is

used to provide qualifying signals to the control logic as well as to help perform the analog-to-digital conversion. The counter is counting at time t_0 and the control logic maintains the autozero mode until the counter reaches the point at which either 159 or 1590 counts are left before it resets, depending on whether the range requires the short integration time (159 counts) or the long integration time (1590 counts). The integrator is then connected to the input amplifier and the integrator output ramps either up or down, depending on the polarity of the input signal.

When the counter reaches 3000 counts, the comparator output is sampled to determine whether the positive or negative reference voltage is to be connected to the integrator to return the output voltage to the starting level. When the comparator output is negative, the integrator output voltage goes in a positive direction when the reference voltage is connected, and the minus sign appears in the display. If the comparator output voltage is positive, the integrator output will decrease in a negative direction, and the minus sign will not appear.

When the comparator output voltage goes through zero volts and changes sign, the counter reading is tested for greater-than 1100 counts. If the

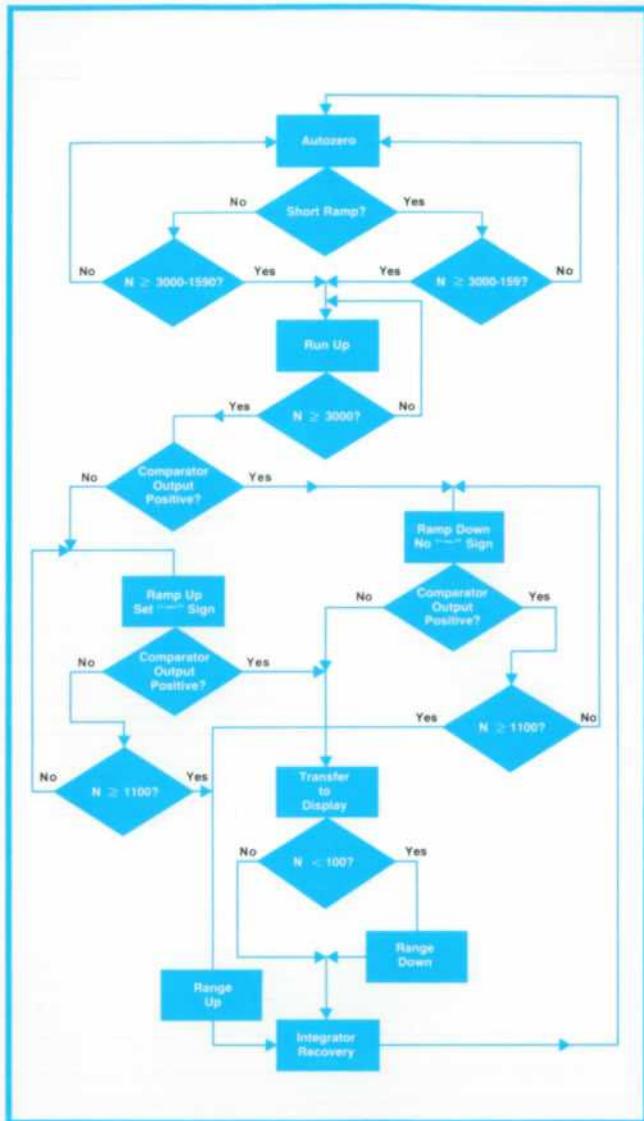


Fig. 5. Flow diagram of control logic in Multimeter's analog-to-digital converter.

counter output is greater than 1100 counts, the instrument is up-ranged one range and resequenced through an integrator recovery phase, to re-zero the integrator, and then sequenced to the autozero phase to repeat the measurement.

If the count is less than 1100 counts, the counter output is transferred to the display and is tested for less than 100 counts. If the count is less than 100, the instrument is down-ranged one range, and resequenced through the integrator recovery and autozero phases.

Multimeter Operation

Ac voltages are rectified to derive a dc voltage proportional to the average value of the ac waveform calibrated to the rms value for a sine wave, and the resulting dc voltage is applied to the integrator. To minimize the size of the filter capacitor

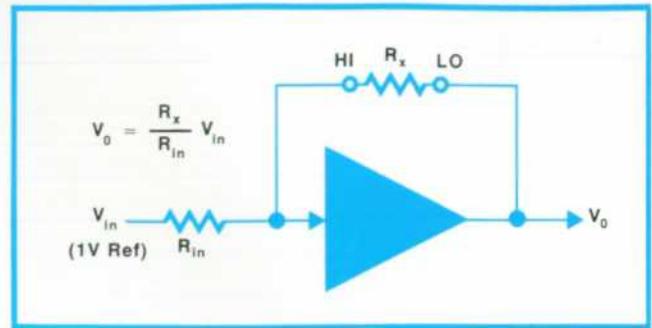


Fig. 6. Input configuration for resistance measurements.

C3, full-wave rectification is used. This is accomplished with inverter A3, which overrides the output of A2 on positive-going signal excursions at its output.

Resistances are measured by supplying a 1-volt reference signal to the input amplifier through a range resistor and configuring the amplifier to place the unknown as the feedback resistor, as shown in Fig. 6. The amplifier output is proportional to the ratio of the unknown resistance to the range resistor.

To protect the ohms circuit from inadvertent application of an external voltage, a series resistor protects the input and it also acts as a fuse for voltages greater than 130 volts. This resistor is clip-mounted to the circuit board so that it can be replaced easily without soldering.

Power Supply

A single 10-volt battery pack supplies all power for operation of the multimeter. Positive and negative reference voltages are established by tying the ground to a tap in a resistive divider that spans the battery (Fig. 7). Actually, three ground reference points are established: (1) analog circuit ground; (2) logic circuit ground; and (3) LED display ground. Separation of the analog circuit ground from the other grounds is necessary to prevent digital circuit transients from interfering with operation of the analog circuits, and to provide proper voltages for MOS switching.

As shown in the diagram, the analog and logic grounds are isolated from the resistive divider by operational amplifiers that provide low impedance sources for the ground circuits. The voltage across the resistive divider is maintained constant through all useful levels of battery charge by a zener diode with a thermistor providing compensation for the temperature characteristics of the zener. If the zener voltage should drift with age, it can be compensated for with the potentiometer provided. This is the only circuit adjustment required in the entire instrument.

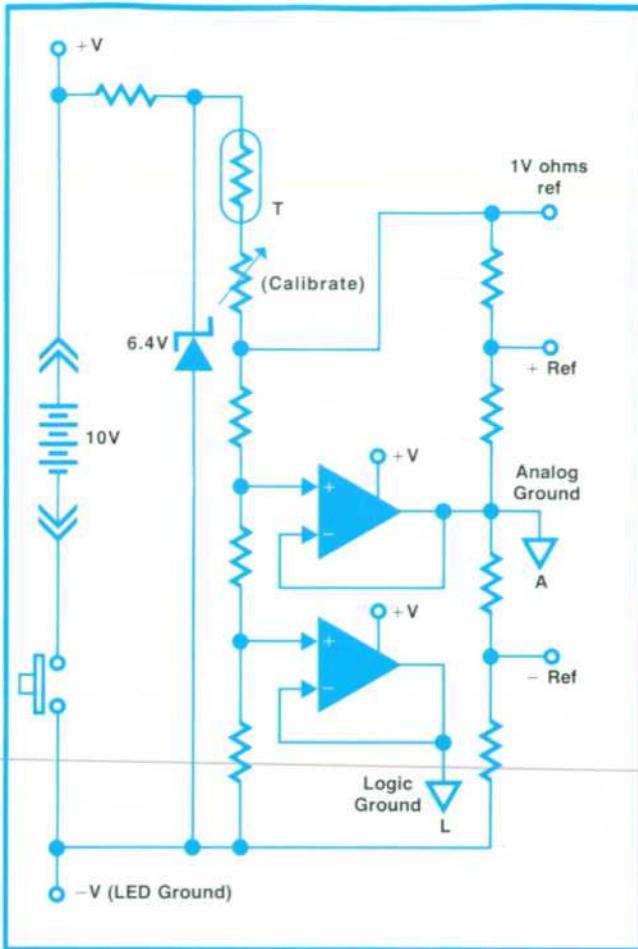


Fig. 7. Power supply isolates analog circuit ground from other grounds to minimize coupling of transients.

The LED display circuits work directly from the battery. As the battery charge depletes, the LED display dims and finally becomes unreadable, indicating that the battery needs recharging. The accuracy of readings is affected by only 1 or 2 counts in the least significant digit when the battery level is too low for a readable display, so this is a practical way to indicate the need for battery recharging.

Putting It All Together

Circuit simplification was a key factor in making the Probe Multimeter feasible. One step taken was to do as much digitally as possible because digital circuits can be implemented very inexpensively. For example, digital comparison, rather than analog comparison, is used to trigger autorange changes.

As much of the circuitry as possible was put on one monolithic integrated circuit, a 150×170 mil chip (3.9×4.3 mm) made by an N-MOS process developed for the 4096-bit ROM's used in HP calculators. This chip (Fig. 8) includes the counters, buffer storage, code conversion for the display, dis-

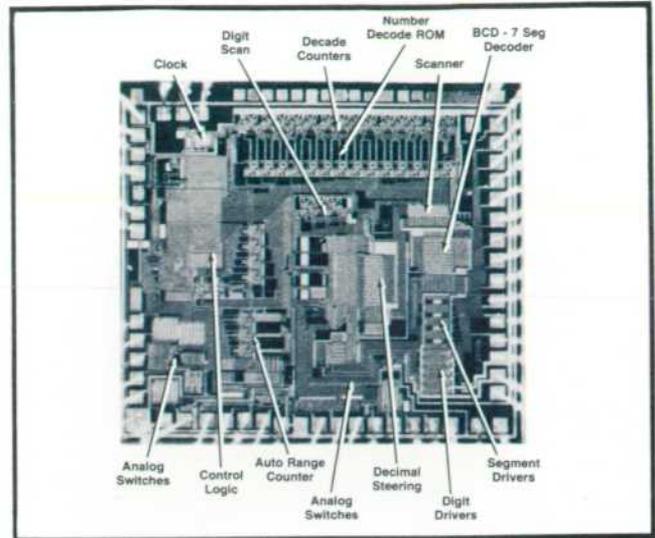


Fig. 8. As much of the circuitry as possible was placed on one custom-made monolithic IC chip. This chip has 40 flip-flops, 19 MOSFET switches and about 3500 bits of ROM.

play scanner, autorange circuits, several ROM's that store the programs needed to operate the multimeter (approximately 3500 bits are stored in ROM), and most of the analog switching.

A distinct advantage of placing all of the digital circuitry on a single chip is the large reduction in the number of interconnections required. This is particularly true in the case of the analog switches required for the analog-to-digital conversion and autoranging. The simplified circuit in Fig. 9 shows how this is accomplished. All of the MOSFET gates as well as many of the sources and drains are connected internally on the MOS chip. Only three mechanical switches are required to operate the instrument: the power switch, function switch, and display invert switch. The remaining 19 switches are on the MOS chip.

As much as possible of the remaining circuitry was put on a 28×38 mm thin-film hybrid circuit (Fig. 10). This includes six operational amplifiers (three chips, each with two op amps), the comparator, one chip with the two input FET's, the bipolar current amplifier that drives the display, four diode chips (rectifiers and protection diodes), capacitor chips, high-value resistor chips, and tantalum-nitride thin-film resistors.

For resistors with values higher than is practical with this thin-film process (greater than 60k ohms), resistor chips bonded to the substrate are used if the value is not critical, e.g. a pull-up resistor. But where accuracy and stability are required, such as in the high-value range resistors, discrete resistors mounted on a circuit board are used. To minimize size and cost, resistors with accuracies specified within 1% were chosen, rather than the larger high-

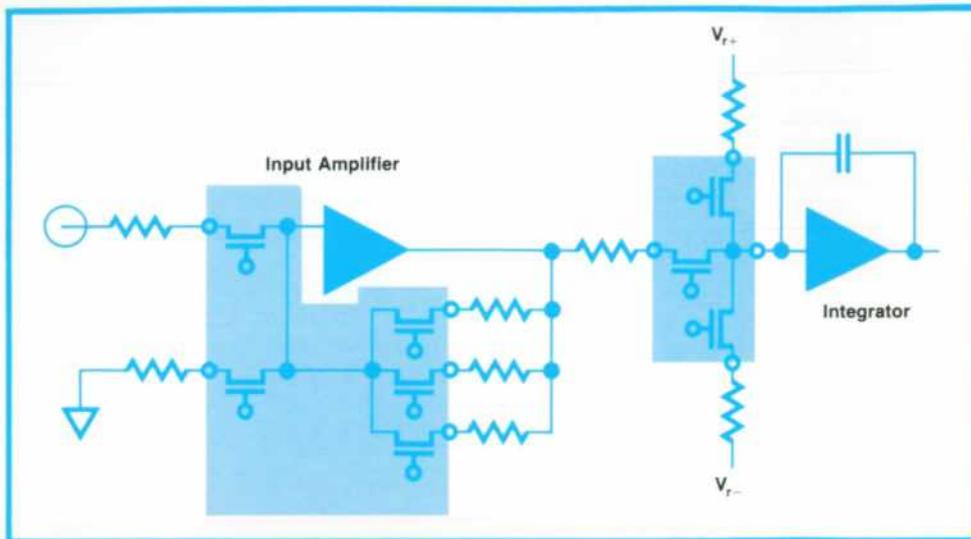


Fig. 9. Simplified diagram of the input amplifier and integrator input shows how MOSFET switches are used. Only ten external connections are required for eight switches.

precision resistors. However, a small-value thin-film resistor is in series with each of these resistors, and the thin-film resistors are laser trimmed to give the series combination the 0.1% accuracy desired. The thin-film resistors have a stability of 0.01% per year and a temperature coefficient of approximately $-75 \text{ ppm}^\circ\text{C}$.

Resistor trimming on the thin-film substrate is accomplished by a computer-controlled laser trim system. The value of a tantalum-nitride thin-film resistor is increased in steps by opening selected gold shorting bars placed across small and medium size resistive segments of the resistor. By this method, a resistor can be trimmed in a few seconds to an accuracy of 0.01%. An entire circuit can be functionally calibrated by actively trimming resistors to compensate for parameters such as amplifier gain, input offset voltages, and so on. In addition to trim-

ming resistors, the computer-controlled system pre-tests the substrate and printed-circuit board prior to trimming, and functionally tests the entire circuit after trim.

The printed-circuit board (Fig. 11) also holds the LED display cluster, large-value, high-voltage capacitors, power supply zener diode and its compensating thermistor, power supply trimmer pot, and the power switch, as well as the thin-film substrate.

Computer or calculator controlled tests are performed at various stages in the production process, beginning with evaluation of the MOS chip and finishing with evaluation of the completed instrument. These automated tests are far more thorough than would be economically feasible with manual point-by-point tests and are a major contribution towards the realization of quality at low cost.

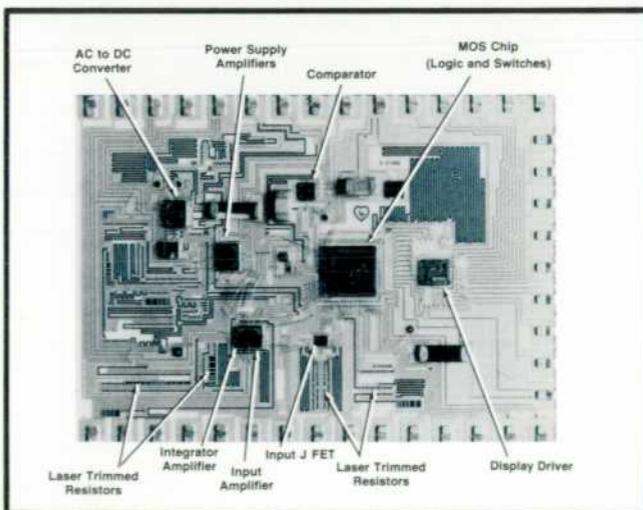


Fig. 10. Thin-film hybrid circuit contains the stable, laser-trimmed resistors and also serves as a high-density interconnect for the other circuits.

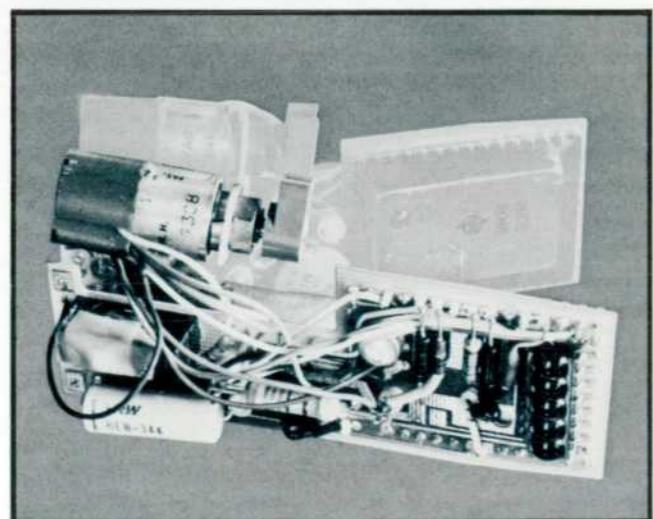


Fig. 11. Thin-film hybrid circuit mounts on the back side of the printed-circuit board that holds discrete components. All of the multimeter's electrical components, except for the battery and the invert-display switch are shown here.

SPECIFICATIONS HP Model 970A Digital Multimeter

DC Voltmeter

RANGES: 0.1 V, 1 V, 10 V, 100 V, 1000 V, 1000 V (500 V max input).
 ACCURACY (20° C to 30° C):
 $\pm 0.7\%$ of reading + 0.2% of range.
 INPUT RESISTANCE: 10 M Ω ; $\pm 5\%$.
 INPUT PROTECTION: ≤ 1000 V peak.
 TEMPERATURE COEFFICIENT: $\pm 0.05\%$ of reading + 0.02% of range/° C.

AC Voltmeter

RANGES: 0.1 V, 1 V, 10 V, 100 V, 1000 V (500 V rms sine wave max input).
 RESPONSE: Responds to average value of input waveform; calibrated to the rms value for sine waves.
 ACCURACY (20° C to 30° C):

Ranges	45 Hz to 1 kHz	1 kHz to 3.5 kHz
1 V to 1000 V	$\pm 2\%$ of reading + 0.5% of range)	$\pm 2\%$ of reading + 0.5% of range)
0.1 V (>3 mV)	$\pm 2\%$ of reading + 0.5% of range)	$\pm 5\%$ of reading + 0.5% of range)

INPUT IMPEDANCE: 10 M Ω ($\pm 5\%$) // < 30 pF.
 INPUT PROTECTION: ≤ 1000 V peak.
 TEMPERATURE COEFFICIENT: $\pm 0.05\%$ of reading + 0.05% of range/° C.

Ohmmeter

RANGES: 1 k Ω , 10 k Ω , 100 k Ω , 1000 k Ω , 10,000 k Ω .
 ACCURACY (20° C to 30° C): $\pm 1.5\%$ of reading + 0.2% of range.
 INPUT VOLTAGE PROTECTION (resistor fused): ≤ 115 V rms for up to 1 minute; ≤ 250 V rms for up to 10 seconds.
 TEMPERATURE COEFFICIENT: $\pm 0.05\%$ of reading + 0.02% of range/° C.

General

A/D CONVERSION: Dual slope.
 RANGING: Automatic.
 SAMPLE RATE: 3/second.
 OVERRANGE: 10%.
 OPERATING TEMPERATURE RANGE: 0° C to 40° C.
 POWER: Rechargeable batteries.
 TYPICAL OPERATING TIME (fully charged battery): 2.5 hours continuous at 25° C.
 TYPICAL BATTERY CHARGING TIME: ≥ 14 hours. (indefinite charging will not damage battery.)
 WEIGHT (with battery pack): 7 oz. (200 g).
 DIMENSIONS: 1 1/4 in. x 1 1/4 in. x 6 1/2 in. (32 x 45 x 165 mm).
 PRICE IN U.S.A.: HP 970A, \$275.
 Extra Rechargeable Battery Pack: \$25.
 MANUFACTURING DIVISION: LOVELAND DIVISION
 815 Fourteenth Street, S.W.
 Loveland, Colorado 80537

Acknowledgments

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Grateful acknowledgment is extended to Terry Pierce (IC R&D Supervisor), John Shea (MOS processing), Bob Jarvis and Bill Bruce (substrate layout and laser trim), LeMoyné Hadley (pre-test and functional test), Roy Barker (production manager), Dennis Colard (production supervisor), Marsh Faber and Jack Morrison (evaluation and life test), Les Wollschlaeger (reliability test), Glenn Gibson (parts coordination), and Rob Thurston (current shunt and accessory design).

The authors are indebted to Bill Beierwaltes, Marketing Coordinator, and Dick Moore, R&D Manager, for many helpful suggestions.

References

1. A. Gookin, "Compactness and Versatility in a New Plug-Together Digital Multimeter," Hewlett-Packard Journal, August 1972.



Fig. 12. Model 970A Digital Multimeter is supplied in a kit that includes a belt-mounted carrying case and a sunshade in addition to the three probe tips and battery charger. The battery pack (lower left) is shown here removed from the instrument.



Virgil L. Laing (Right)

Fresh out of the University of Minnesota with bachelor's, master's, and PhD degrees in electrical engineering, Virgil Laing went to work for the Loveland Division's IC department in 1968, subsequently becoming project leader for develop-

ing the N-MOS process for the 4096-bit ROM's used in the 9800-series Calculators. Transferring to instruments, he designed a major part of the N-MOS circuitry in the Probe Multimeter and later became group leader for probe products development. An outdoor sports enthusiast, Virgil also enjoys hiking and camping with his family and pheasant hunting with his two German Shorthair Pointers.

Robert L. Dudley (Left)

Among the many products Bob Dudley had project responsibility for since joining HP in 1959 are the 690-series Micro-wave Sweep Oscillators, the 3300A Function Generator, and the 3469A Digital Multimeter. As a group leader, he was also involved with the 204C and 209A Oscillators, the 3310A Function Generator, and the 970A Probe Multimeter. At present, he is section manager in charge of basic instruments. Bob obtained a Bachelor's degree in Engineering Science from Brigham Young University and later under the HP Honors Co-op program, an MSEE from Stanford. He enjoys golf and goes skiing on water or snow. He's also been president of the Loveland Optimist Club, regional music leader for his church, as well as a high council member, and student-activities chairman of the IEEE Denver section.

A Portable High-Resolution Counter for Low-Frequency Measurements

This snap-on functional module for the low-cost 5300 Measuring System makes six-digit measurements of frequencies between 0.833 Hz and 2 MHz. Special features help solve many low-frequency measurement problems.

by **Kenneth J. MacLeod**

DIRECT FREQUENCY COUNTERS provide a simple and accurate means of measuring the frequencies of electrical signals in the range from a few kilohertz to hundreds of megahertz. However, they suffer from reduced resolution at frequencies below this range. This is an unavoidable consequence of simply counting the number of periods of the signal during some gate time, typically one second. At 60 kHz, for example, the display will read 60000 ± 1 in a one second measurement, but at 60 Hz the reading will be only 60 ± 1 . The ± 1 count uncertainty is caused by the random phase of the input signal at the time the gate opens.

Model 5307A High-Resolution Counter (Fig. 1) is designed for users who need to measure low frequencies with higher resolution than is possible with direct counters, without resorting to longer measurement times. The new counter is a snap-on functional module for the 5300 Measuring System.^{1,2} In less than one second it counts any input frequency from 5 Hz to 2 MHz (or 0.833 Hz to 166 kHz in counts/minute mode) and displays a six-digit answer with appropriate decimal point and annunciator lights.

Because many of its potential users are outside the electronics laboratory, the new counter is designed to be easy to operate, even by someone not skilled in electronics. The counter is fully autoranging. For simple measurements, none of the front-panel buttons need be pressed and the sensitivity knob may be left in the fully clockwise position. If a frequency below 5 Hz is connected to the input, the gate light will blink slowly and the display will show 000000, clearly indicating an underrange condition.

As part of the 5300 Measuring System, the new counter is portable and has a rugged case. It is small and light, and can be battery powered using the 5310A Battery Pack.¹ Digital (BCD) output for re-

coding measurements is standard on the 5300A Mainframe, and analog output can be added by including the 5311A Digital-to-Analog Converter module.²

Solutions to Low-Frequency Problems

Low-frequency measurements have their own

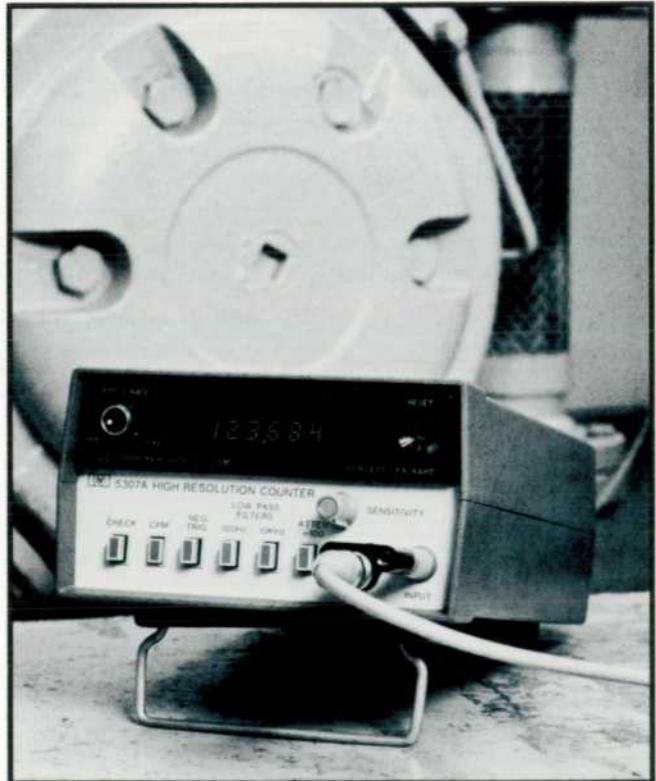


Fig. 1. Model 5307A High-Resolution Counter snaps onto the six-digit 5300A Measuring System mainframe. The combination measures low frequencies much more rapidly than a direct frequency counter for a given accuracy and resolution. A counts-per-minute mode is useful in many low-frequency applications.

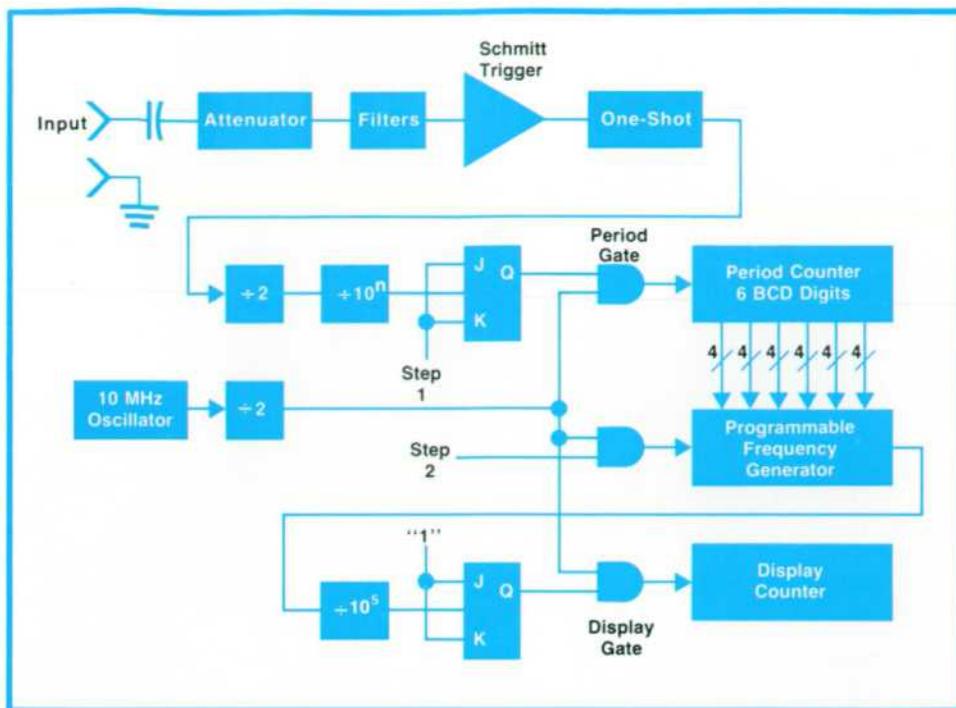


Fig. 2. Input circuit design provides flexible signal conditioning. Two-step measurement cycle consists of a multiple-period-average measurement followed by calculation of the reciprocal of the average period. The counter is autoranging, automatically selecting the number of periods to be averaged.

special problems, and the 5307A Counter is designed to offer solutions to these problems.

Unlike higher frequencies, which are universally expressed in counts per second, or hertz, lower frequencies are often expressed in counts per minute. Therefore the 5307A has a front-panel pushbutton that causes the frequency to be displayed in counts per minute. This button also reduces the lower limit of the measurable frequency range from 5 Hz to 50 counts/min (0.833 Hz). The counts/min mode makes the counter especially convenient for cardiology and tachometry; direct readings from a pacemaker can be displayed in beats per minute, and the output of any sensor that generates one pulse per revolution can be displayed in revolutions per minute.

Signal conditioning requirements at low frequencies are also somewhat special. Because the output levels of some sensors are quite low, the new counter has 10 mV rms input sensitivity. The input is ac coupled directly to a high-sensitivity FET Schmitt trigger (Fig. 2). Ac coupling makes triggering independent of any dc signal component, while elimination of the usual separate FET buffer amplifier provides exceptional freedom from the overshoot and ringing occasionally seen in ac-only input amplifiers.

Complex waveshapes and noisy signals are also more common in the low-frequency environment. To attenuate interfering high-frequency noise, either of two low-pass single-pole filters may be selected by front-panel pushbuttons. These filters have upper 3 dB frequencies of 100 Hz and 10 kHz,

and rolloffs of 20 dB per decade. They greatly reduce the triggering ambiguity caused by noise, an important consideration if only a few periods are being averaged. This improvement is shown in Fig. 3.

The sensitivity knob may also be used to improve triggering in the presence of noise. Fully clockwise, the sensitivity control sets the trigger level at +10 mV; fully counterclockwise the trigger level is 2.5V. For finer adjustments at the 10 mV end, the position of the sensitivity knob has a logarithmic rather than a linear relationship to the trigger level. The trigger level and slope are switched to negative values when the negative trigger button is pressed.

Very-high-level signals are also common in low-frequency measurements. For example, ac power mains usually have a frequency of 50, 60, or 400 Hz. The 5307A is well suited to measuring these frequencies, and will withstand up to 300V with the attenuator $\div 100$ button pressed. This front panel button also raises the trigger levels to a higher range, 1V to 250V. Note that ac mains measurements should always be made using an isolation transformer at the 5307A input and observing proper safety precautions.

Internal Controls

In addition to these problem-solving front-panel controls, two internal controls are useful under certain conditions. The first is a pulse-width adjustment. This control varies the pulse width of the input one-shot multivibrator. Its effect is to provide a variable delay after triggering, during which no further triggering can occur. There are two ranges

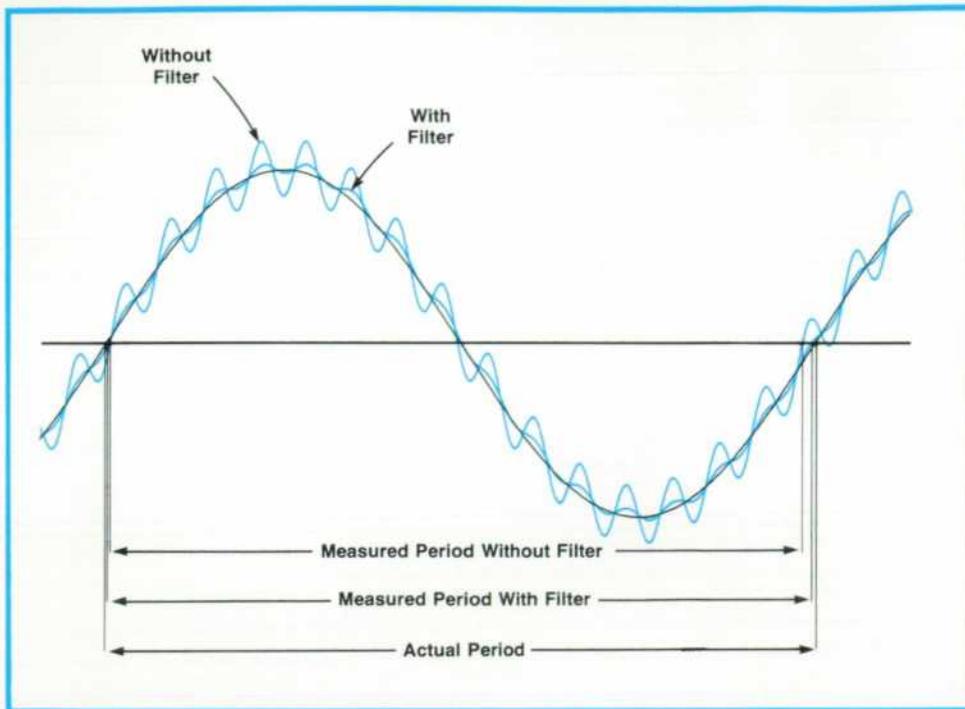


Fig. 3. To eliminate high-frequency noise that might cause triggering errors, the 5307A user can select one of two built-in low-pass filters. The filters have upper 3 dB frequencies of 100 Hz and 10 kHz and rolloffs of 20 dB per decade.

of delay, 0.35 μ s to 3.5 μ s and 1 ms to 10 ms. One situation in which delay is useful is when ringing follows the pulse to be counted, as shown in Fig. 4. The delay avoids false triggering by causing the counter to ignore the ringing.

The second internal control is the alternate range switch. This switch, in its normal position, allows the 5307A to change ranges automatically at every decade point. In either of the other two positions, it suppresses alternate range changes. The user can elect to suppress either even-numbered or odd-numbered range changes.

This feature is convenient when the 5307A is being used to measure a varying frequency that frequently crosses a range-change point. It is also specifically designed to reduce the number of range changes when the Model 5311A Digital-to-Analog Converter module is used. When the 5300A and 5307A are snapped apart to allow the 5311A to be inserted between them, the alternate range switch is conveniently exposed. The 5311A provides an analog output of the 5307A display, which can be used to drive a strip-chart recorder or to supply the feedback voltage for a closed-loop control system.

Obtaining High Resolution

There are several methods for improving resolution at low frequencies. A longer gate time may be used, but only at the expense of frequent readings.

A frequency multiplier may be used to produce a higher-frequency signal related to the input signal. This technique is usually implemented with a phase-locked loop. Such units typically are slow to

achieve lock at frequencies below a few tens of hertz, and track over a frequency range of only about 20:1. The latter problem requires that multiple range switches be used, and may cause signals outside of the selected range to be measured incorrectly with no clear indication of error. These units are also not suitable for measuring aperiodic or random inputs.

A third possibility for improving resolution is to measure the period of one or more cycles of the unknown. This requires the user to calculate the reciprocal of the period.

Two-Step System

The method chosen for the 5307A is a two-step

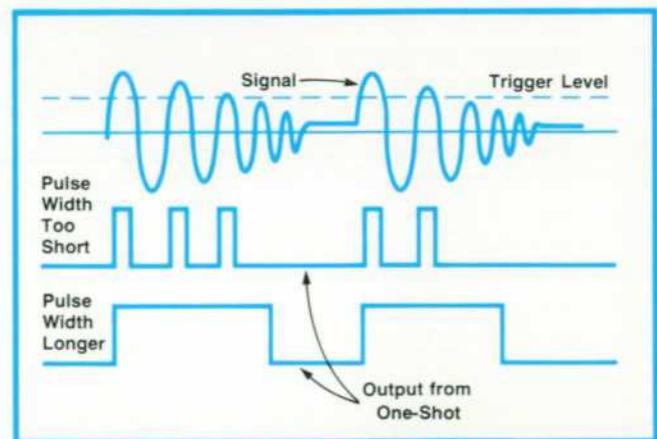


Fig. 4. Adjustable pulse width of the output monostable multivibrator in the 5307A trigger circuit is useful for eliminating false triggering in the presence of ringing.

system (Fig. 5). First, a period average of the input signal is measured, and then the reciprocal of the period average is calculated and displayed. During the first step, a six-digit period counter counts an internal reference frequency derived from the 10 MHz crystal oscillator in the 5300A mainframe.

The period average counter is active during 2×10^n periods of the input signal. Using the facilities for autoranging built into the mainframe, the 5307A automatically selects n to average from 2 to 200,000 periods ($n = 0$ to 5). Thus the average period of any input frequency from 5 Hz to 2 MHz (or from 50 counts/min to 10^7 counts/min) can be measured to an accuracy of at least 1×10^{-5} . The value of n is stored and used to control the position of the decimal point for the next display.

After the first step is complete, the period measurement still must be converted to frequency for display, that is, the reciprocal must be taken (frequency = $1/\text{period}$). This could be accomplished by BCD division, as is done in the 5323A Automatic Counter.^{3,4} But instead a method was chosen that takes the reciprocal of the period measurement by using hardware that is already built into the 5300A mainframe and the period average counter itself.

To implement this method, a digitally programmable frequency generator (PFG) is used. The PFG has six digits of static BCD programming inputs from the period average counter, a single reference frequency input, and a single variable frequency output. For each 10^6 pulses at the reference input, it generates as many pulses at the output as are specified by the six static BCD digits. For example, if the BCD programming inputs are 123456, the PFG will produce 123,456 output pulses for each million reference pulses. More details on the operation of the PFG are given in the box on page 14.

The time base unit in the 5300A divides the PFG output frequency by 10^5 , and the result is used to open and close the display gate. The display counts the 10 MHz reference frequency during the time the display gate is open. When the gate closes, the display counter contains the frequency of the input signal scaled by a factor of 10^n , and the previously stored value of n is used to set the proper decimal point and annunciator.

Because the PFG output frequency is proportional to the period average of the input signal, the average period of the PFG output is proportional to the input signal frequency. The second step of the 5307A measurement is equivalent to measuring the average of 10^5 periods of the PFG output. Thus the second step produces a number equal to the frequency of the input signal.

The reciprocation scheme has a worst-case error of $\pm 3 \times 10^{-5}$, and this is the basic accuracy speci-

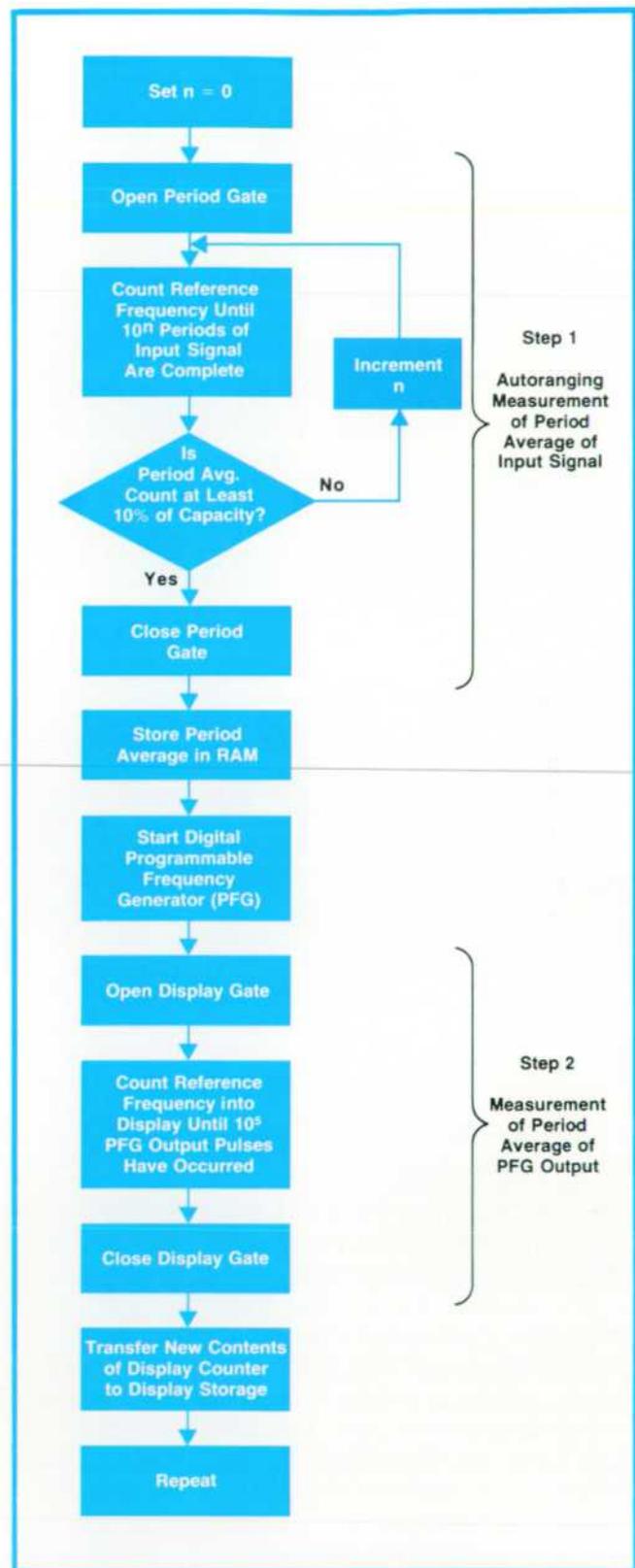


Fig. 5. Algorithm for the two-step frequency measurement. After the average period of the input signal is measured, the programmable frequency generator produces a frequency proportional to this average period. This frequency is then inverted to find the input frequency by measuring the average period of the PFG output.

Operation of the Digital Programmable Frequency Generator

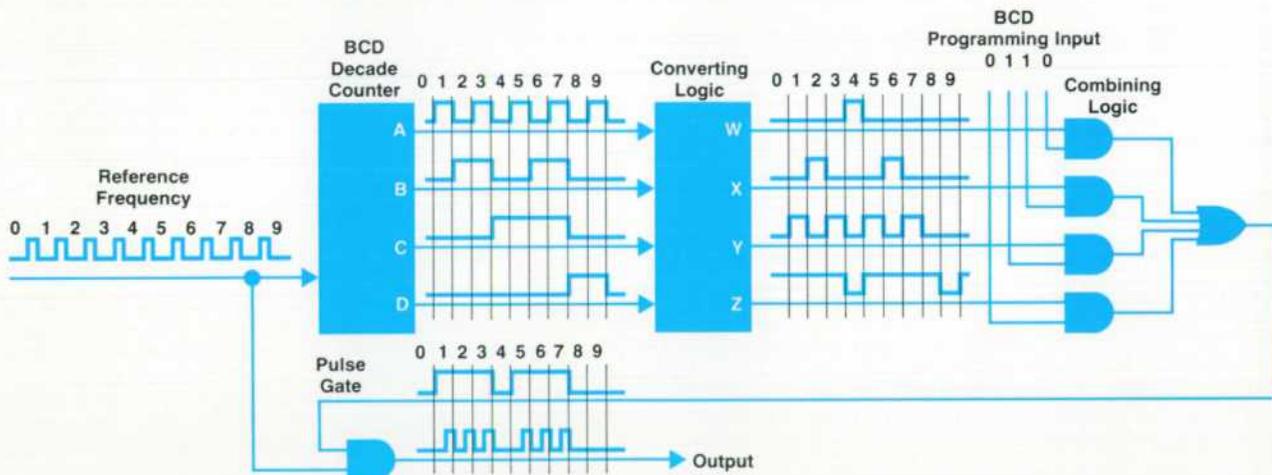
The PFG uses digital logic to generate an output pulse train that has an average frequency equal to a fraction of the input reference frequency. The fraction is specified by the BCD programming inputs.

The PFG is a type of decimal rate multiplier⁵. As an example of PFG operation, consider the one-digit PFG shown in the drawing. For each group of ten pulses of the reference frequency, this circuit produces from zero to nine output pulses, under control of the BCD programming input. Outputs A, B, C, and D of the BCD decade counter are used by the converting logic to generate waveforms W, X, Y, and Z, which are in the logic "1" state during one, two, four, and eight clock times out of ten, respectively. These waveforms are then selectively combined in the combining logic to produce a waveform that is in the logic "1" state from zero to nine clock times out of ten. This output controls the gating of reference frequency pulses from input to output. In the drawing, a BCD 6 (0110) at the programming input causes six reference frequency pulses out of ten to be passed through the pulse gate to the output.

The 5307A uses a six-digit PFG built around a six-digit decade counter. The output for each decade is formed as in the one-digit case, and all six outputs are multiplexed onto one line. Since each decade produces only zero to nine pulses out of a possible ten, there is one state in which it never produces a pulse. This state, by design, is the "9" state for all six decades. Thus each time the first decade is in the "9" state, a pulse from the second decade can be multiplexed onto the output line. Similarly, a pulse from the third decade can be output each time the first two decades are in the "99" state, and so on for each succeeding decade.

To reduce package count and power consumption, the 5307A has only one digit of converting and combining logic, and multiplexes the six decade counters to it, in the order outlined above.

While the spacing of the output pulses is generally not uniform, the average period over 10^5 pulses is very accurate, typically to one part in 10^5 , and the 5307A's accuracy is dependent only on the time taken to generate 10^5 pulses.



cation of the counter for pulse inputs. Fig. 6 compares the accuracy specification of the 5307A measurement with the accuracy of a one-second direct frequency count for pulse and sine-wave inputs.

This method of taking the reciprocal makes optimum use of the capabilities of the mainframe and the period counter. In the mainframe, it uses the crystal oscillator output for its reference frequency, the programmable time base divider to count 10^5 PFG output pulses, and the display counter to count the final answer. In the 5307A, it uses the six decades of the period average counter as the heart of the PFG. To allow this dual use of the decades, the results of the first step are stored in a small random access memory before the second step begins.

Such economy of hardware was necessary to meet the power and package size constraints of the portable, battery-powered 5300 System. Low-power TTL MSI circuits were used wherever possi-

ble in the logic sections to minimize power consumption.

Acknowledgments

Major contributions to the 5307A were made by the following people. Ian Band provided overall guidance and suggested the converting technique. Lew Masters designed the signal conditioning electronics. Bruce Corya was responsible for the mechanical design. Marketing was handled by Larry P. Johnson.

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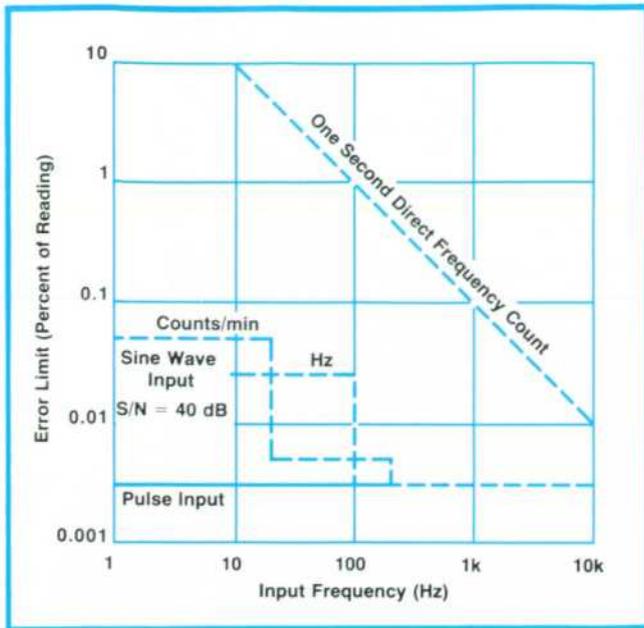
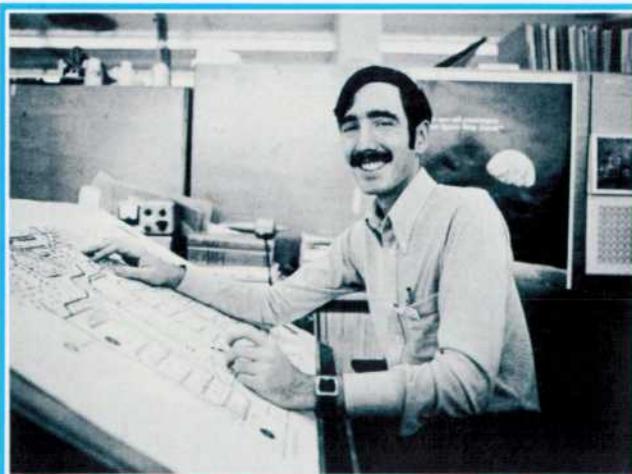


Fig. 6. Error limits for 5307A measurements. Limits include worst-case reciprocal-calculation error and worst-case trigger error for sine-wave inputs.

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Kenneth J. MacLeod

Ken MacLeod, a native of Philadelphia, Pennsylvania, holds a BA degree from Ursinus College (1969), a BSEE degree from the University of Pennsylvania (1970), and an MSEE degree from Stanford University (1973). With HP since 1970, Ken has designed hardware and software for a high-speed test system and served as principal designer of the 5307A Counter. He's a member of the IEEE Computer Society. Having lived on the west coast of the USA for only three years, Ken and his wife still spend much of their time exploring, using their home in San Jose, California as their base of operations. Ken's explorations also extend to outer space; he's an amateur astronomer.

4. F. Rodé and G. B. Gordon, "Computation for Measurement Flexibility", Hewlett-Packard Journal, May 1969.

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SPECIFICATIONS

HP Model 5307A High Resolution Counter Module

Input

RANGE: Hz mode 5 Hz to 2 MHz.

CPM mode 50 to 10 M counts/minute (0.833 Hz to 166 kHz).

SENSITIVITY (min.):

SINEWAVES	Hz	CPM
10 mV rms	5 Hz-1.2 MHz	120 CPM-10 MCPM
25 mV rms	1.2 MHz-2.0 MHz	50 CPM-120 CPM

PULSES

For low-duty-cycle pulses (<15%): 15 mV peak for 250 ns pulses. 100 mV peak for 100 ns pulses.

Basic sensitivity can be varied continuously up to 2.5 V rms by adjusting sensitivity control.

ATTENUATOR: +1 or +100 effectively raises basic input sensitivity by a factor of 100 (10 mV-2.5 V to 1 V-250 V).

LOW PASS FILTERS:

3 dB point	100 Hz	10 kHz
Max. attenuation	60 dB	40 dB
Rolloff	20 dB per decade	

IMPEDANCE:

No filter	1 MΩ shunted by <50 pF	
100-Hz filter	1 MΩ shunted by series of 100 kΩ and 0.015 μF	
10 kHz filter	1 MΩ shunted by series of 100 kΩ and 150 pF	

COUPLING: ac coupled amplifier.

OVERLOAD PROTECTION:

200 V rms below 10 kHz
 $2 \times 10^6 \text{ V} \cdot \text{Hz}$ rms to 0.4 MHz
 5 V rms above 0.4 MHz

With +100 attenuator, 300 V rms

TRIGGER LEVEL: Selected positive or negative for optimum triggering from sinusoidal inputs or pulses.

TRIGGER HOLDOFF: Adjustable from .35 μs to 3.5 μs and 1 ms to 10 ms.

Frequency Measurement

PERIODS AVERAGED: Automatically selected for maximum resolution. Two periods are averaged for signals up to 100 Hz. For each decade increase in the input signal, the number of periods averaged increases by a factor of ten up to 200,000 periods averaged above 1 MHz.

MEASUREMENT TIME: Varies from 312 ms for a display of 170000 to 815 ms for a display of 999000.

ACCURACY: $\pm 3 \times 10^{-5} \pm$ trigger error** \pm time base error.

DISPLAY:

In Hz mode, Hz and MHz with automatically positioned decimal point.

In CPM mode, M with automatically positioned decimal point.

General

CHECK: Measures internal reference frequency. Displays 1.00000 MHz in Hz mode, 100000 M in CPM mode.

OPERATING TEMPERATURE: 0° to 50° C.

POWER REQUIREMENTS: Including 5300A Mainframe, nominally 10 watts.

WEIGHT: Net, 2 lb (0.9 kg).

PRICES IN U.S.A.: Model 5307A, \$350. 5300A Mainframe, \$395. 5310A Battery Pack, \$195. 5311A Digital-to-Analog Converter, \$295.

* $\pm 3 \times 10^{-5}$ is due to reciprocation scheme and is worst case.

** Trigger error is less than $\pm 0.03\%$ of one period + periods averaged for sine waves with 40 dB or better signal-to-noise ratio.

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A High-Speed Pattern Generator and an Error Detector for Testing Digital Systems

The rate at which errors occur in transferring digits through systems operating at bit rates as high as 150 M bits/s can be determined by a new Error Detector working with a new Data Generator.

by Thomas Crawford, James Robertson, John Stinson, and Ivan Young

AS THE WORLD of electronics grows increasingly digital, bit rates go higher and higher. In particular, growth in the demand for local and international telephony and the need for new communications services, such as high-speed transfer of data between computer systems, is forcing an increase in transmission capacity. Digital transmission techniques like pulse-code modulation (PCM) will play a major role in providing this capacity.

Rapid development in these new digital systems is resulting in a requirement for test instruments that can accommodate the higher bit rates. Here, then, is a new pair of instruments (Fig. 1) intended for test

and evaluation of digital systems operating at bit rates as high as 150 Mb/s. Model 3760A Data Generator produces pseudorandom bit patterns up to 32,767 bits in length as a stimulus for the system under test. Model 3761A Error Detector generates an identical pattern internally, compares it bit by bit with the output of the system under test, and determines the rate at which errors occur.

Error rate is the important performance criterion in evaluating a digital transmission system. This kind of test could also be applied to digital magnetic recorders, memory systems, and some logic systems. A number of conveniences have been built in-



Fig. 1. Model 3760A Data Generator (lower unit) supplies a variety of bit patterns that are useful for testing digital systems and logic operations. Model 3761A Error Detector detects errors introduced into the data generator's pseudorandom sequences by equipment under test, and measures the rate at which errors occur.

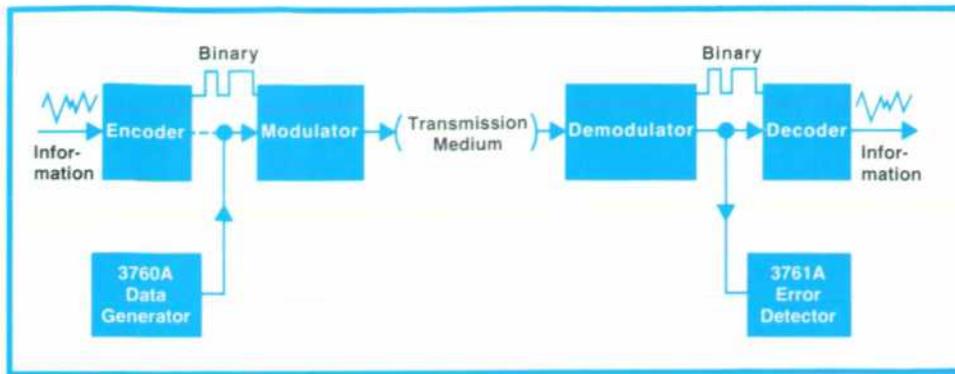


Fig. 2. Model 3760A Data Generator supplies digital sequences to a system at the point where the information is normally in binary form. Model 3761A checks the sequence at the output before any decoding occurs.

to these instruments to make them easier to operate and also to broaden their usefulness in the development lab and on the production line, as well as in the field.

Bit Error Rate

A typical application for these instruments is shown in Fig. 2. The Model 3760A Data Generator stimulates the system at any point where the information is normally in binary form. The Model 3761A checks the binary stream at the output of the system and counts the number of times that its internally generated bit sequence differs from that received. At the same time, it counts system clock periods so that it can determine the bit error rate (BER), the ratio of number of bits in error to number of bits transmitted. It continuously updates this information, presenting it on its digital display.

Test Signals

For best correlation between actual system performance and bit-error-rate measurements, the test signals should resemble normal information-carrying signals. In a typical PCM system, information from many independent sources is time-multiplexed to form a composite signal with a high bit rate. As the number of sources is increased, the statistics of the nominal aggregate signal more and more resemble those that would be obtained from a truly random noise source.

The 3760A/3761A measurement system uses pseudorandom binary sequences generated by shift registers with feedback taps. Since the statistical nature of a pseudorandom binary sequence is very close to that of a truly random pulse stream, this makes the test signal resemble typical signals, but it also enables the error detector to generate bit sequences identical to those of the data generator.

Model 3760A Data Generator produces pseudorandom sequences in nine different lengths selectable from 7 bits to 32,767 bits long. The shorter lengths are useful for debugging and for situations where it is desirable to observe the entire bit stream on an oscil-

loscope. The long sequences are more like typical signals. A sync pulse is generated once per sequence repetition to make it easy to synchronize an oscilloscope or other equipment to the bit pattern.

The new data generator also generates digital words up to 10 bits long for testing logic systems or for reproducing key system code words. A bank of front-panel switches allows a choice of any bit pattern for these words. Here too, a sync pulse is generated once per word.

The switches for selecting the digital word also select the point in the pseudorandom sequences where the sync pulse occurs. This arrangement permits the operator to shift the sync pulse along the sequence so he can observe the effect of every part of a long sequence in detail with an oscilloscope.

Runs of zeros up to 99 bits long can be inserted between repetitions of the words or pseudorandom sequences. These are useful for checking clock-recovery circuits that extract timing signals directly from the data stream. Such circuits tend to fail when pulse transitions do not occur frequently. Or, a run of zeros may be inserted following a run of 1's to test for dc shift in the system under test.

The instrument can also generate an alternating bit sequence, 1010..., where a maximum number of transitions may be wanted.

Deliberate errors can be inserted into the data generator's pseudorandom sequences to check the operation of the error detector. When operated in the "add error" mode, the data generator replaces two consecutive bits with their complements once every 4000 sequences. This corresponds to an error rate of 7.1×10^{-5} to 1.5×10^{-8} , depending upon the sequence in use.

Normally the data generator operates with clock pulses supplied from the equipment being tested, but it may also be equipped with an internal clock generator. The data generator in turn produces output clock pulses in synchronism with the clock source but gives the operator control over amplitude (0.1 to 3.2V), offset ($\pm 3V$) and polarity. To accommodate differing propagation delays in the

cables that connect the data generator to the system under test, the data stream may be delayed up to 100 ns with respect to the clock to ensure the correct phase relationship between the data and the clock at the system input.

To match the requirements of the system under test, the operator has control over the pulse characteristics of the data stream. He can select either the RZ format (return-to-zero, constant width pulses) or NRZ format (non-return-to-zero, output goes high on a "1" and stays there until the next "0" occurs). The width of the RZ pulses is determined by the width of the input clock pulses at the triggering level.

The operator also has a choice of amplitude, offset, and polarity for the output data, the same as for the clock pulses. Input and output impedances are 50Ω in the standard instrument but 75Ω is available as an option.

A second data output, delayed a fixed number of clock pulses with respect to the main data output, is available as an option. In the PRBS mode, the two outputs are effectively uncorrelated (first-order) and are therefore useful for checking out the operation of the duplexers and other modulators and demodulators used in digital radios. The delayed output has the same amplitude and offset capabilities as the main output.

The Error Detector

Model 3761A Error Detector accepts two inputs: the data stream to be examined, and clock pulses derived either from clock recovery or other external circuits, or directly from the data generator. The clock input has oscilloscope-type triggering controls to accommodate a variety of clock pulse amplitudes and offsets. A front-panel indicator lights up to show when proper triggering is achieved.

To make sure that the clock pulses do not sample the data stream on data bit edges, which would result in ambiguous operation, a variable phase control is provided. The operator needs only to adjust the phase control until a front-panel lamp lights up. This lamp turns off when transitions occur too closely.

With the clock trigger and phase controls set properly, all that remains is to set the pseudorandom sequence to the same length as the data generator. Although alignment of a locally-generated pseudorandom sequence with the transmitted sequence has been a troublesome procedure with closed-loop shift registers, alignment occurs automatically with the new error detector, requiring no intervention by the operator.

To ensure statistical significance, at least 100 errors must occur before the system will display bit-

error rate (BER). The BER display consists of two digits plus a power of ten in a range of 0.1×10^{-9} to 9.9×10^{-1} .

If the operator prefers to know the total errors, rather than have an indication of bit error rate, he may switch to a "count" mode, which totals errors up to 9999. He may choose to use this mode if errors occur at a very low rate, in which case he may not want to wait for the accumulation of the more than 100 errors needed for automatic BER computation. The time during which errors are counted may be controlled manually by a front-panel switch, externally through a TTL compatible input, or internally. The duration of the internal gate is selected by a front-panel switch.

Besides the front-panel numerical indication, the error detector outputs the numerical values in BCD form for a digital recorder. It also outputs a pulse whenever an error is detected, for use in further statistical processing.

Pseudorandom Sequence Generation

The heart of the Model 3760A Data Generator is a high-frequency 15-stage shift register that uses a feedback configuration similar to that in the Model 1930A PRBS Generator¹, as shown in Fig. 3. Feeding the shift register output back into the register through exclusive-OR gates alters the contents of the data stream as it passes through. By proper choice of the stages where feedback is introduced, a maximal length pseudorandom sequence is generated. A maximal length sequence is one where all possible combinations of N 1's and 0's (except all 0's) is generated without repeating any combination,

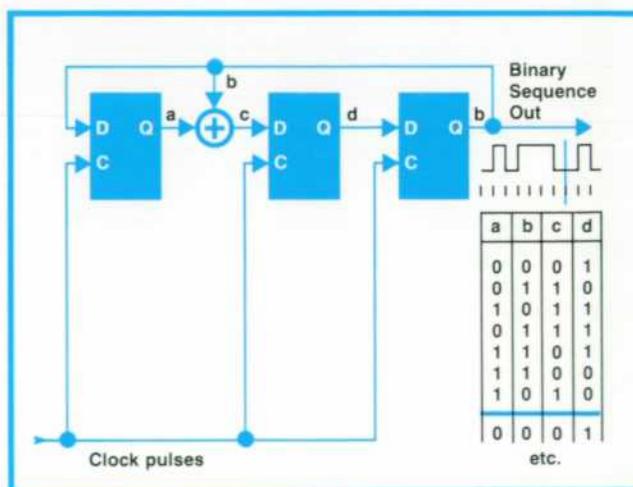


Fig. 3. A typical PRBS generator. This one has three active stages and feedback to two points to give a maximal length sequence of 7 bits ($2^3 - 1$). Models 3760A and 3761A have 15 stages with gates from the feedback tap line to establish the number of active stages and the points where feedback is introduced.

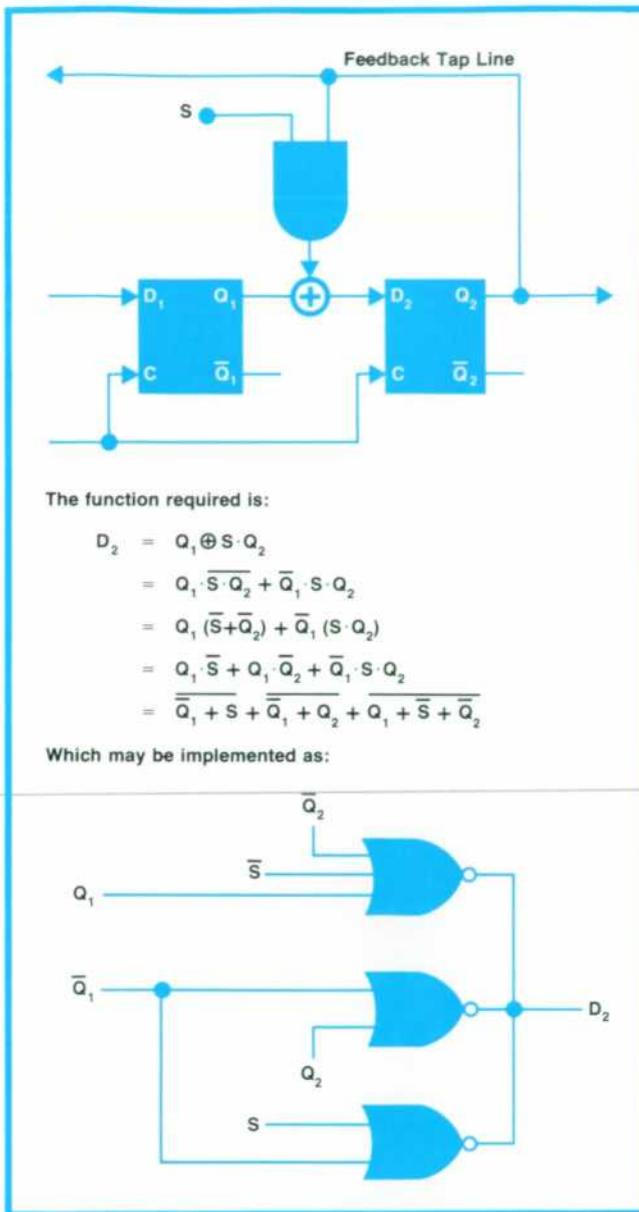


Fig. 4. Exclusive-OR gate and tap-line switch in upper diagram are implemented by logic circuit in lower diagram. This achieves minimum propagation delay.

where N is the number of stages in the shift register. The sequence length is $2^N - 1$.

The configuration chosen for the shift registers in the new instruments limits the amount of propagation delay in any feedback loop to that of one exclusive-OR gate, as contrasted with other configurations where feedback may be processed through two or more gates in series. An exclusive-OR gate that includes the feedback tap-line switch is shown in Fig. 4. Minimum delay circuits such as this, along with the use of high-speed emitter-coupled logic and stripline signal paths on multilayer circuit boards, enable operation at clock rates up to 150 MHz.

The front-panel PRBS LENGTH switch selects

the number of stages and the proper feedback taps for generating a maximal length sequence for that number of stages. The minimum is 3 stages, which gives a 7-bit sequence, and the maximum is 15 stages, which gives a 32,767-bit sequence.

A sequence sync pulse is generated whenever the contents of the shift register match the contents of the front-panel WORD switch register (the data stream output, however, is delayed one bit with respect to the sync pulse). It should be noted, though that following a sync pulse the data stream out of the register is not the same as the sync word selected. This is because the contents of the shift register are altered by the feedback taps as the word is shifted through. To aid the user in setting the sync pulse to a particular part of a sequence, the instruction manual contains information that relates the subsequent output sequence to the instantaneous contents of the shift register.

Modifying a Sequence

A run of zeroes is added simply by gating off the clock pulses to the shift register when a sequence sync pulse occurs. A counter, preset to the number selected by the ADD-ZERO switches, then starts counting down clock pulses. When it reaches zero, it reopens the clock pulse gate, restarting the register. Since zero insertion is triggered by the sequence sync pulse, zeroes can be added at any place in a sequence by appropriate setting of the switch register.

Deliberate errors are inserted by gating the complement of the data stream into the output for two clock periods. Error insertion is initiated by a counter that counts sequence sync pulses, triggering the error-insertion circuits on the 4000th count.

When the instrument is switched to the WORD mode, the shift register recirculates its contents without change. Each time the word circulates back to the starting position, a sync pulse is generated by the digital comparator. A low-pass filter derives a dc voltage proportional to the average value of the sync pulse train so if sync pulses do not occur regularly, the voltage drops to zero, enabling a reset pulse that loads the contents of the front-panel WORD switch register into the shift register. Thus, the front-panel register can be changed, and the new word will be loaded automatically.

The maximum-transition sequence (101010....) is generated by taking the output from a flip-flop.

The Overview

A block diagram of the Data Generator is shown in Fig. 5. The input signal conditioning circuit is somewhat similar to an oscilloscope time-base trigger circuit and need not be discussed here except to

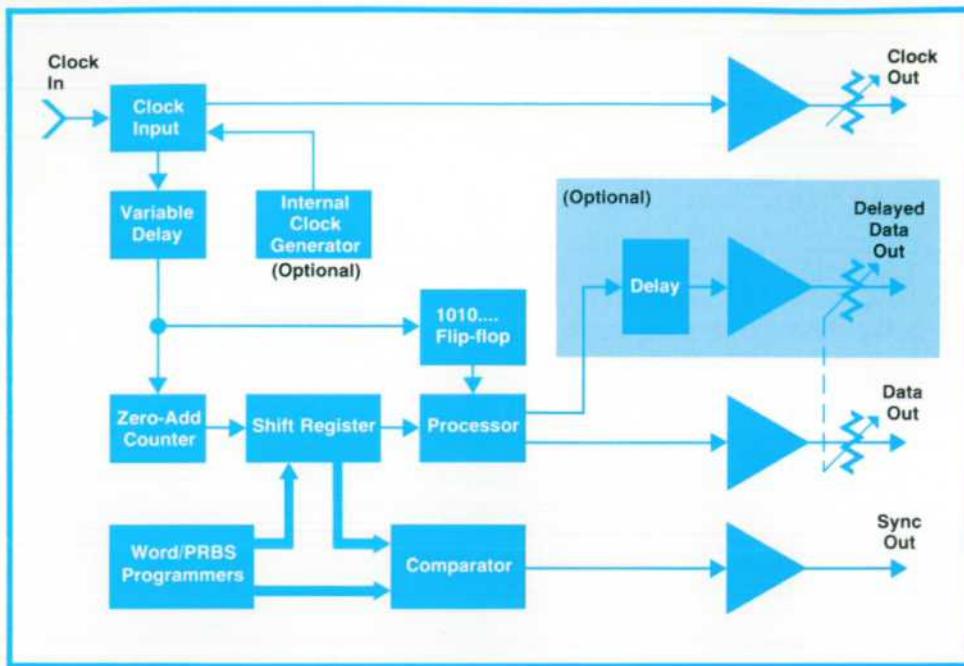


Fig. 5. Simplified block diagram of Model 3760A Data Generator.

point out that dc coupling is used at all times so that the trigger level will not be affected by any changes in the clock pulses.

The trigger level determines the width of the output pulses when the instrument is in the RZ mode. For example, if the clock input is a sine wave and the trigger level is set to midrange, the RZ output pulse width would be half the clock period. As the trigger level is raised towards the crest of the sine wave, the output pulses become correspondingly narrower.

When the "auto" trigger mode is used, the trigger level is established by a circuit that taps off the input waveform, passes it through a low-pass filter to derive the average waveform level, and uses the result to define the trigger level. This insures that the trigger level is always within the swing of the input waveform. The "auto" trigger works with any regularly recurring waveform that has a pulse width greater than 3 ns, a mark:space ratio between 1:10 and 10:1, and an amplitude of 0.5V p-p or greater. A front-panel indicator lights up to show that the input circuits are triggering.

The relative timing between the data and clock pulse edges is of concern, so provision was made for a controllable delay between the data stream and clock stream. Lumped delay lines give up to 90 ns delay in switched 10-ns increments and a continuous vernier extends the maximum to 100 ns. The vernier delay, diagrammed in Fig. 6, is also a lumped line but it uses varactors to vary the delay.

The output circuits are conventional pulse generator type circuits affording control of amplitude, polarity, and offset. Such flexibility was not

deemed necessary for the sequence sync pulse; it is a 1-volt positive-going pulse that has a duration equal to one clock period, except in the "add-zero" mode when it stays high for the duration of the zero block. This allows an oscilloscope to trigger on either the start or the end of a zero run according to the trigger polarity selected.

The Bit Error Detector

A block diagram of the Model 3761A Error Detector is shown in Fig. 7. The clock input conditioning circuits are similar to the Model 3760A Data Generator. The input for the data stream, however, always works in the "auto" mode, with only the polarity selectable.

Because the data is sampled at clock pulse edges, it is important that the data and clock pulse edges do not coincide. A phase delay for the clock circuits is therefore provided. A variable delay line similar to that in the 3760A Data Generator is used to give a controllable delay up to 12 ns but when the RATE switch is set on the 1.5 - 50 Mbits range, an RC variable phase shifter is used (this is the only function of the RATE switch). The front panel PHASE control then gives delay in a range of 0 to 180° of the clock period regardless of the clock repetition rate. This is accomplished by the circuit in Fig. 8.

An indication of proper phasing is needed for the operator. This is achieved by a circuit that produces an output pulse if a data transition occurs during the time that a narrow guard pulse, derived from the clock, is present (Fig. 9). A coincidence inhibits the front-panel PHASE indicator, so as long as this indicator is illuminated, the operator knows that

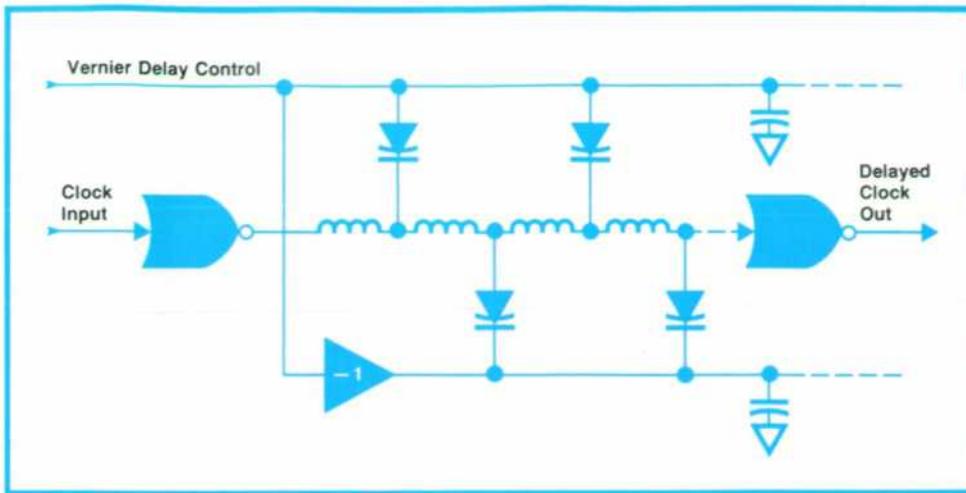


Fig. 6. Vernier delay line uses varactors to change the capacitance and thus the delay characteristics of the line. Push-pull arrangement compensates for the change of varactor bias during a clock pulse. The line uses printed-circuit inductors.

proper phasing is achieved.

Split Data Stream

Since the error detector operates only with pseudorandom sequences, it was possible to realize some economies by splitting the data stream, gating alternate bits so two half-rate data streams are derived (Fig. 9). Economies are realized because the cost of high-speed logic as a function of speed rises with a slope greater than 1. The properties of maximal-length PRBS's are such that each half-rate stream retains the same structure as the original full-rate sequence, as shown in Fig. 10. Each half-rate shift register may then have the same feedback connections as the full-rate shift register in the data generator.

Automatic Sequence Synchronization

Before errors can be detected, bit-by-bit corre-

spondence between the locally-generated sequences and the incoming sequence must be established. For a sequence of $2^N - 1$ bits, this can be accomplished within N bits simply by opening the feedback connection to the tap line, and feeding the incoming sequence to the tap line (Fig. 11). This switching is initiated automatically when an auxiliary error counter reaches a count of 20,000 errors. The counter is reset every 100,000 clock periods so resynchronization occurs only when more than 20,000 errors occur within 100,000 bits.

What happens if there should be an error in the data stream at the time that resynchronization is concluded? The error in effect causes the sequence to start from the wrong initial word, thus generating the sequence out of phase with the incoming stream. There is then the statistical likelihood that one half of the bits will be in error. The auxiliary error counter would then contain 50,000 counts

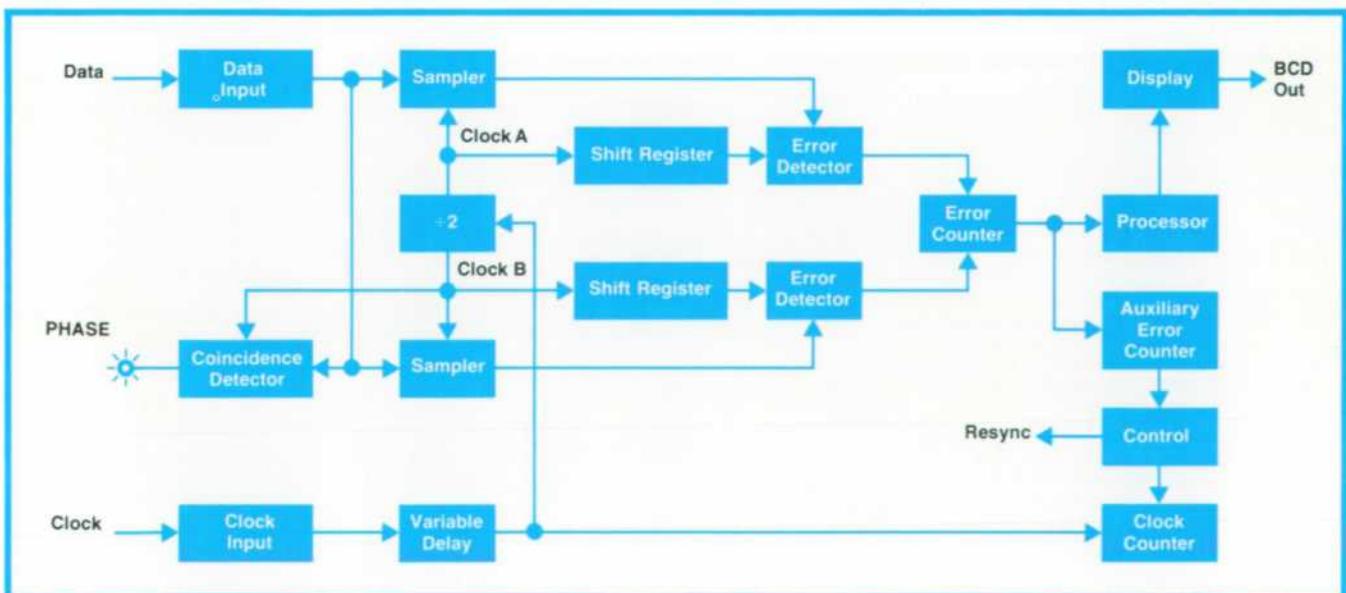


Fig. 7. Simplified block diagram of Model 3761A Error Detector.

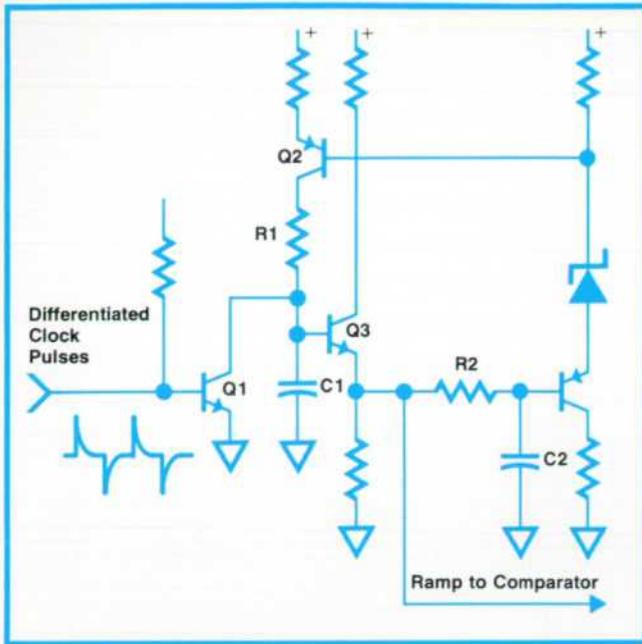


Fig. 8. Self-adjusting ramp generator accommodates varying clock rates. The ramp is generated by charging capacitor C1 with current supplied by transistor Q2. Capacitor C1 is discharged each time a pulse derived from the leading edge of each clock pulse turns on Q1. The resulting sawtooth waveform is low-pass filtered by R2 and C2, level-shifted by the zener diode, and used to control the current level through Q2. This holds the ramp amplitude nearly constant by adjusting the charging current to fit the clock rate.

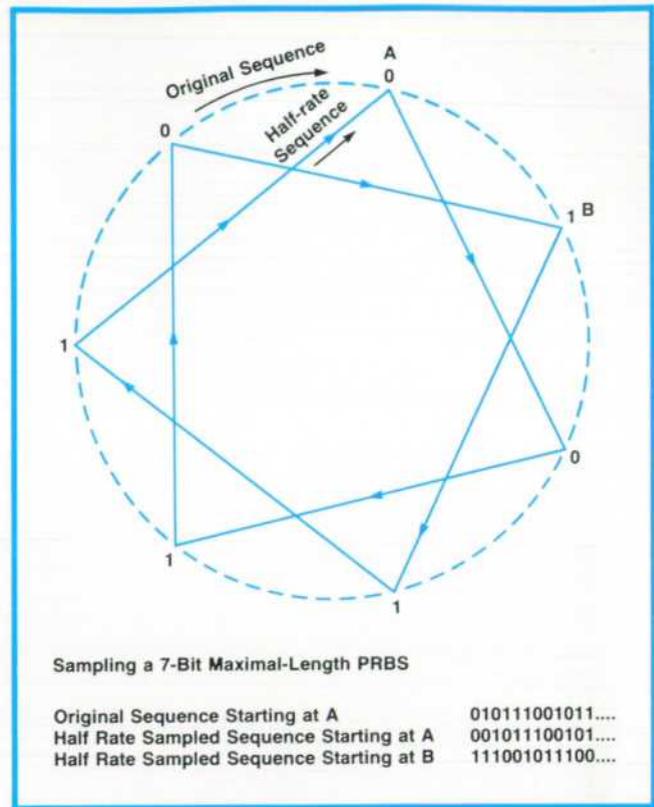


Fig. 10. Diagram representing 7-bit maximal length sequence shows that taking every other bit derives the same sequence as the original.

when reset.

A count of 20,000 errors is high enough to permit the system to accept bursts of errors without triggering resynchronization in an otherwise "quiet" transmission.

Synchronization can also be initiated manually or remotely by an external TTL signal. This is useful in lab or production test situations where it may

be desired to establish synchronization, and then degrade the data stream, say by adding noise and/or attenuating the signal level. The resulting high error rates, which otherwise would automatically initiate resynchronization, can then be measured.

Display Considerations

The BER display accommodates a wide range of

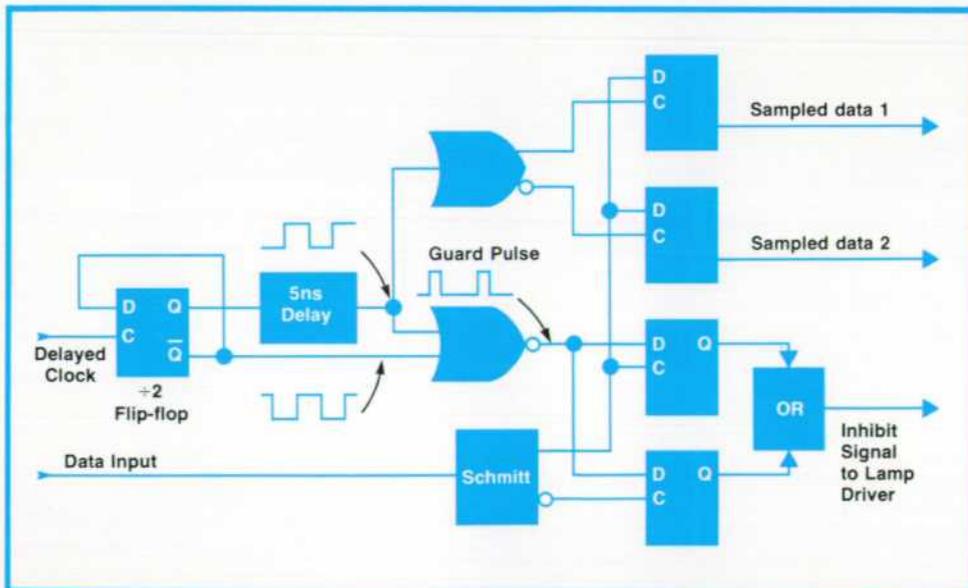


Fig. 9. Guard pulse, derived from the clock, is applied to the D inputs of two flip-flops. If a data transition, acting as a clock, occurs during the guard pulse, one of the flip-flops, depending on transition polarity, will produce an output that inhibits the front-panel PHASE indicator. Input data, following regeneration in a Schmitt trigger, is also applied to two other flip-flops that sample the data on alternate clock pulses to get two half-rate data streams.

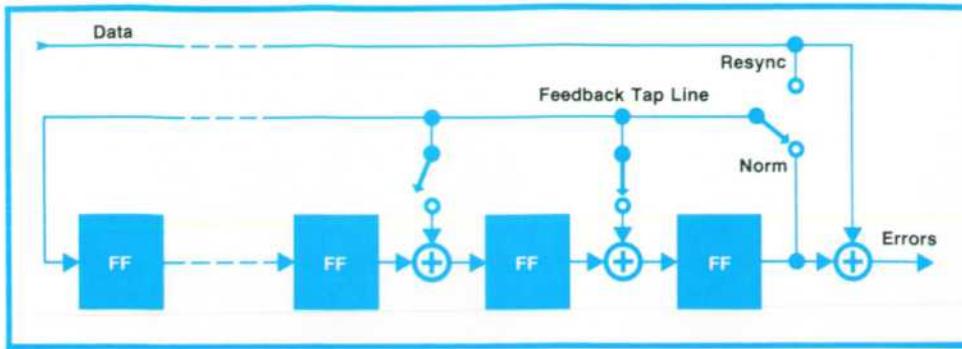


Fig. 11. By feeding data stream into PRBS generator's feedback tap line, the generator becomes synchronized with the data stream within N bits, where N is the number of shift register stages.

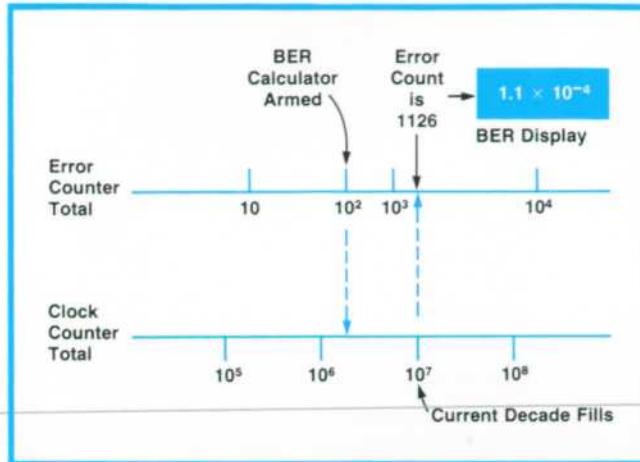


Fig. 12. Timing diagram of the system for deriving the bit-error-rate (BER) display. The system displays the number existing in the error counter at the time that the clock reaches the decade count that follows detection of 100 errors.

error rates without operator intervention. The theory is illustrated in Fig. 12. Two totalizers are employed—one that totals errors and one that simultaneously totals clock periods. First of all, to give statistical significance to the indication, 100 errors must be totaled before any action is taken. When 100 errors have been detected, the BER calculator is armed. When the currently-being-filled decade of the clock period totalizer is filled, the display circuit is enabled. The two most significant digits of the error count are then displayed and the exponent "n" of the $X10^{-n}$ portion of the display is derived by subtracting the number of filled decades in the error counter from the number of filled decades in the clock counter.

As discussed earlier, the instrument can be operated in a "count" mode wherein the error counter



John Stinson (Right)

A native of Scotland, John joined Hewlett-Packard in 1968 after obtaining a B.Sc. in Electrical Engineering at Strathclyde University in Glasgow. The first two years of his HP career was as a design engineer on instruments such as the 3710A Microwave Link Analyzer. John's involvement with the 3760A Data Generator began with the initial investigation when the Digital Communications Section was formed at HP Ltd. Currently he is Group Leader for the Low-Frequency PCM program.

Thomas Crawford (Far left)

Tom Crawford joined Hewlett-Packard Ltd. in 1966 after graduating with a B.Sc. degree from Heriot-Watt University. Tom worked on the 3701A Microwave Link Analyzer until returning to Heriot-Watt University under HP's sponsorship where he obtained a Ph.D. degree in 1970. He then returned to Hewlett-Packard and worked on the design of the 3761A Error Detector. Tom is presently leader of the High-Frequency PCM Group at HP Ltd.

James Robertson (Left)

After graduating with a B.Sc. degree from Glasgow University, James joined Hewlett-Packard Ltd. in 1968 and was engaged in early investigations related to high frequency digital communications. While working on the design of the 3761A Error Detector, James also obtained his M.Sc. degree from Heriot-Watt University in 1972.

Ivan Young (Far right)

Ivan graduated with a B.Sc. degree from Heriot-Watt University and joined Hewlett-Packard Ltd. in summer 1969. He has recently completed work leading to an M.Sc. degree in Digital Techniques. Since joining HP, Ivan has worked in the Digital Communications group and was involved in the design of the 3760A Data Generator from the initial investigation stage.

totals for a given period of time and the contents are displayed on the 4-digit display.

Acknowledgments

The authors wish to thank those in all departments who helped during the projects. In particular we would like to acknowledge the tenacity of our production engineer, Stewart Moulton. We would like to thank David Leahy, 3760A product designer, and Ken Coles, 3761A product designer, for their sustained efforts and likewise thank the engineers

who contributed to the design of the 3760A: Aileen Appleyard, Mike Roberts, Peter Rigby, Ralph Hodgson and Graham Cameron. Thanks also to David Guest for designing the 3761A power supply and to Lance Mills, project leader during the early stages, for defining the system.

References

1. E.S. Donn, "Manipulating Digital Patterns With a New Binary Sequence Generator," Hewlett-Packard Journal, April 1971.

SPECIFICATIONS HP Model 3760A Data Generator		Sync Output	
Modes of Operation PRBS NORMAL: Generates a repetitive 2^N-1 bit, maximal length, pseudorandom binary sequence where $N=3$ to 10 and 15. PRBS ADD ZEROS: Adds a block of 1 to 99 zeros into PRBS Normal, occurring after the sync pulse. PRBS ADD ERROR: Introduces two errors per 4000 sequences by changing two consecutive bits to their logic complements. 1010: Generates a preset repetitive word, content 1010. WORD NORMAL: Generates a continuous 3- to 10-bit word with selectable content. WORD ADD ZEROS: Addition of a block of 1 to 99 zeros into Word Normal, occurring between words.		RATE: Once per PRBS or WORD cycle. DURATION: PRBS and WORD NORMAL: 1 CLOCK period. ADD ZEROS: Length of zero block plus one clock period. POSITION: PRBS NORMAL: Front panel selectable. WORD NORMAL: Precedes word. ADD ZEROS: Precedes zero block by one clock period. SOURCE IMPEDANCE: 500 \pm 5% AMPLITUDE: +1 V nominal.	RATE: 1.5 to 150 Mb/s. IMPEDANCE: 500 \pm 5%, dc coupled (750 optional). TRIGGER LEVEL: Automatic. Input mark space ratio, 10:1 to 1:10. SENSITIVITY: Better than 500 mV pk-pk. DC OFFSET: \pm 3 V maximum. AMPLITUDE: 5 V pk-pk max. Limits \pm 5 V. PULSE WIDTH: 5 ns minimum at 50% pulse amplitude.
Clock Input RATE: 1.5 to 150 MHz. IMPEDANCE: 500 \pm 5%, dc coupled (750 optional). TRIGGER MANUAL: Level range, -3 to +3 V. Slope +ve or -ve. AUTO: Input mark-space ratio range, 10:1 to 1:10. SENSITIVITY: Better than 500 mV pk-pk. AMPLITUDE: 5 V pk-pk maximum. Limits, \pm 5 V. PULSE WIDTH: 3 ns minimum at 50% pulse amplitude.		General	Phasing
Internal Variable-Frequency Clock (Optional) RATE: 1.5 to 150 MHz. JITTER: <0.5% of period +0.5 ns pk-pk.		POWER: 90 to 125 or 200 to 250 V, 40 to 400 Hz, 90 W. WEIGHT: 30 lbs (13.6 kg). DIMENSIONS: 16 1/2 in. wide, 5 1/2 in. high, 18 1/2 in. deep (425 mm x 140 mm x 467 mm). PRICE IN U.S.A.: Model 3760A, \$4590. 750, no charge. Internal clock, \$170. Delayed data output, \$550.	CONTROL: Clock phase variable relative to data. INDICATION: Lamp off when clock and data edges coincide. RANGE: 1.5 to 50 Mb/s: 0 to 180°; 50 to 150 Mb/s: 0 to 12 ns.
Clock Output OUTPUTS: CLOCK or CLOCK, from external or optional internal clock.		HP Model 3761A Error Detector	Synchronisation
Data Output OUTPUTS: DATA or DATA. Delayed DATA output is optional. FORMAT: RZ (up to 130 Mb/s) or NRZ. IMPEDANCE: Source impedance 500 \pm 5% (750 optional). AMPLITUDE: Continuously variable in 5 ranges from 0.1 to 3.2 V into 500; symmetrical about offset level. RISE/FALL TIME: <1.4 ns into 500; <1.6 ns into 750 with 750 impedance option. OVERSHOOT: <10% of pulse amplitude. DC OFFSET: Zero, <2% of pulse amplitude. Variable, continuous 0 to \pm 3 V. DELAY: Data (and sync) delayed with respect to clock continuously in 10 ranges from 0 to 100 ns. DELAYED DATA OUTPUT (optional): Same bit pattern as DATA output but delayed 8 bits with respect to DATA output. Ganged controls give DELAYED OUTPUT same format, amplitude, and offset as DATA output.		Measurements	MODES: Auto, Manual, External. AUTO: Automatically searches for synchronism if more than 20,000 errors in 100,000 bits. EXTERNAL: Resynchronisation commanded by TTL input. MANUAL: Resynchronisation commanded from front panel.
Internal Variable-Frequency Clock (Optional) RATE: 1.5 to 150 MHz. JITTER: <0.5% of period +0.5 ns pk-pk.		BER (bit error rate): RANGE: 9.9×10^{-1} to 0.1×10^{-6} , automatically scaled. GATING: Automatic, at least 100 errors before computation. COUNT (total error count): 0 to 9999. GATING: INTERNAL: Repetitive or single shot. 10 ⁻⁶ clock periods where $n=3$ to 11. EXTERNAL: TTL logic level. MANUAL: Front-panel switch. SEQUENCES: Maximal length PRBS 2^N-1 bits long where $N=3$ to 10 and 15.	Display
Clock Input RATE: 1.5 to 150 MHz. IMPEDANCE: 500 \pm 5% dc coupled (750 optional). TRIGGER: SLOPE: +ve or -ve MANUAL: Level range, -3 to +3 V. AUTO: Input mark-space ratio range, 10:1 to 1:10. SENSITIVITY: Better than 500 mV pk-pk. AMPLITUDE: 5 V pk-pk max, limits \pm 5 V. PULSE WIDTH: 3 ns minimum at 50% pulse amplitude.		Data Input	Outputs
INPUT: DATA or DATA, selectable.			PRINTER: 8421 BCD. BER AND COUNT: Current display on command. FLAGS: SYNC LOSS: 0 printed in column 1. OVERFLOW: Output inhibited. PRINT COMMAND: Pulse at display change. ERROR OUTPUT RATE: One pulse per error. AMPLITUDE: +1 V into 500 nominal.
		General	General
			POWER: 90 to 125 or 200 to 250 V, 40 to 400 Hz, 70 W. WEIGHT: 23 lbs. (10.4 kg.) DIMENSIONS: 16 1/2 in. wide, 3 1/4 in. high, 18 1/2 in. deep (425 mm x 95 mm x 467 mm). PRICE IN U.S.A.: \$4140. 750 CLOCK and DATA input, no charge. MANUFACTURING DIVISION: Hewlett-Packard Ltd. South Queensferry West Lothian EH309TG Scotland

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

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