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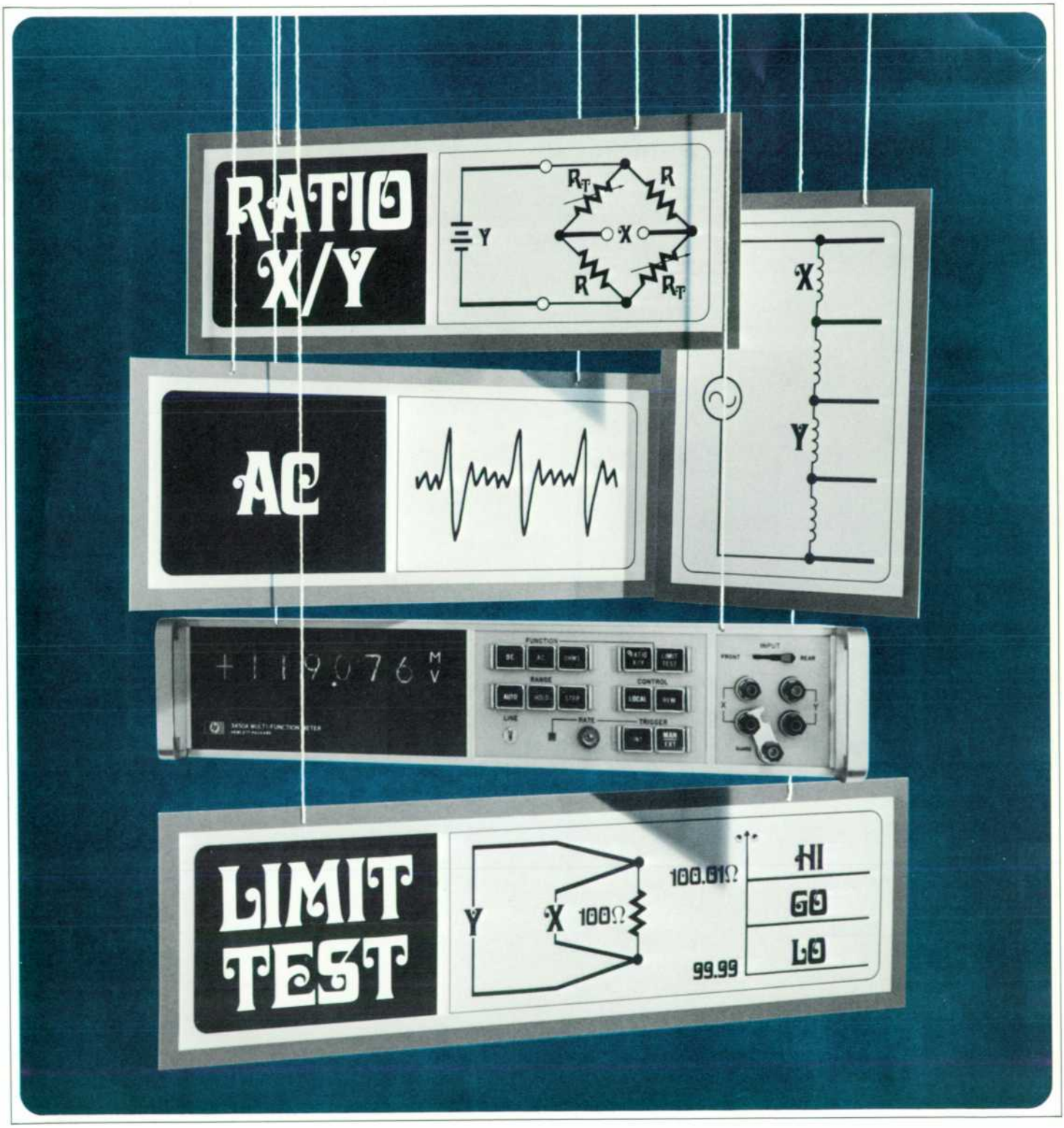

MARCH 1969

Twelve Functions in a New Digital Meter

Some common analog-to-digital conversion techniques, and benefits derived from dual slope as used in the new digital instrument.

By Bill Kay and Jerry L. Harmon

DIGITAL VOLTMETERS DIFFER BASICALLY from the commonly used analog voltmeters in one respect—their display or readout is a numeric display rather than a meter indication. Analog voltmeters seldom have accuracies greater than about 0.25%, and to achieve even these accuracies, a great deal of care is necessary in reading the meter. In the digital voltmeter, the analog signal is 'converted' into digital form. Since the required resolution in reading is obtained by the numeric readout, the accuracy of the signal being measured depends upon the accuracy of the conversion technique. The digital form of the signal may be easily read by the user, or the conversion may be done many times each second and the resulting binary signal transmitted to external processing or recording devices, such as computers or printers. By comparison to the meter instruments of 0.25% reading accuracies, there are digital voltmeters with accuracies on the order of 0.002% of reading.

Conversion Methods

Four basic analog to digital conversion techniques are being used.* These are: (1) single ramp, (2) successive approximation or potentiometric technique, (3) voltage

*In addition to the four logic techniques, there are several A-to-D Converters that use a combination of these to improve performance. For example the HP Model 3460A uses a potentiometric/integrating combination and the HP Model 2402A uses a voltage-to-frequency/interpolation combination.

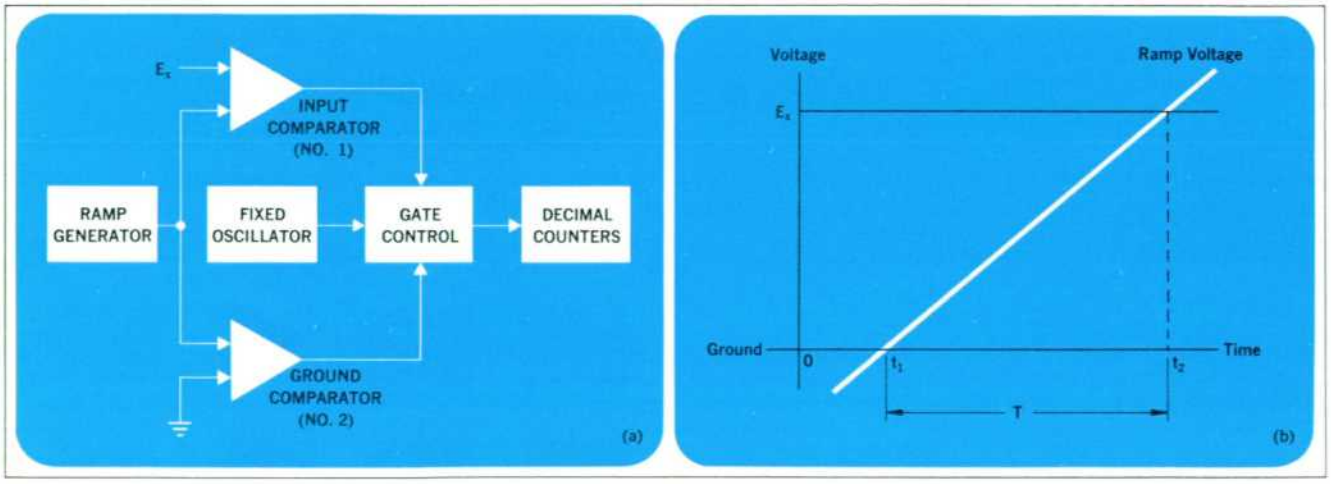

Fig. 1. *With the ramp technique* ***(a)****, dc voltage is measured by counting the number of cycles allowed through the gate during time T* ***(b)****.*

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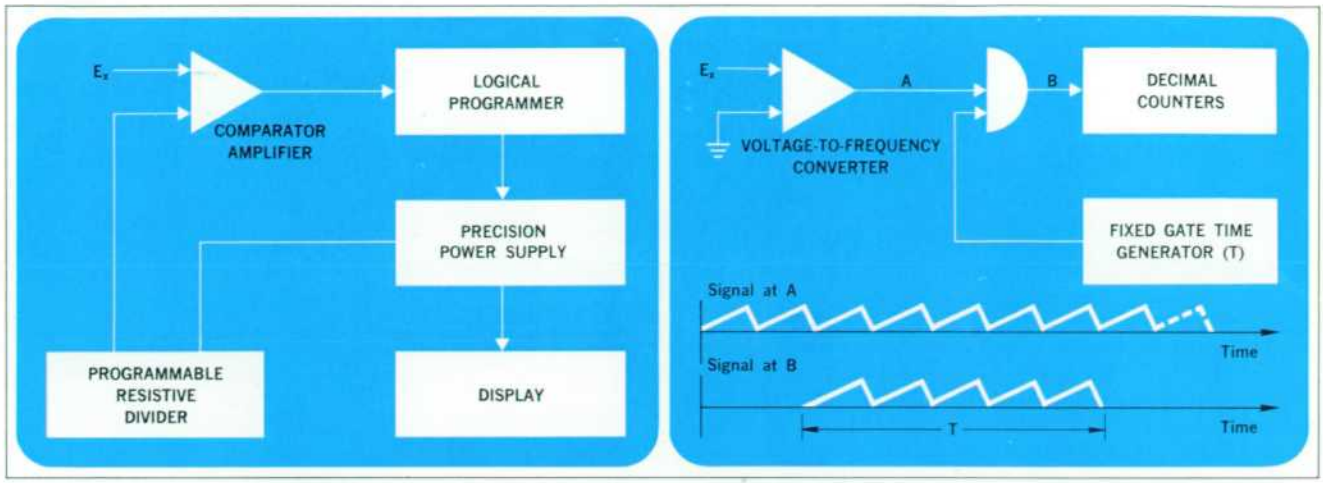


Fig. 2. *(left) Potentiometric digital voltmeter uses a comparator amplifier to drive a logical programmer. The programmer adjusts a precision power supply and resistive divider to null out the unknown voltage at the comparator input. The final setting of the divider is converted to a readout of input voltage.* **Fig. 3.** *(right) In an integrating digital voltmeter, the time interval rather than frequency is fixed. The unknown input voltage is converted to a frequency proportional to that voltage.*

to frequency conversion, and (4) dual-slope technique. Each technique has advantages, but any voltmeter design using a single technique may differ significantly due to certain basic compromises that must be made.

Ramp. The 'ramp' is the simplest and lowest cost analog to digital conversion.[1] The conversion is actually voltage to time. In Fig. 1, if the time is determined for a ramp voltage of known slope to pass between two voltage levels (a reference level and the unknown), that time value is proportional to the signal being measured. The time is determined by counting clock pulses of a known frequency as the ramp travels between the reference levels. The basic limitations on the accuracy, stability, and speed of reading are the nonlinearity and stability of the ramp, the stability of the clock, the accuracy of making the coincidence measurements, and the noise level. If the voltage levels are not noise free, the reading rate must be slowed because of the settling time of necessary noise filtering circuits.

Successive Approximation. The fastest and one of the most stable of the four basic analog to digital conversions is successive approximation or the potentiometric technique. A very simple converter, Fig. 2, has four parts — an analog comparator, a logical decision block, a basic dc reference, and a digital-to-analog converter. Successively decreasing values of voltage steps are generated to null the signal being measured. Since each voltage step has a numerical weight, the final setting of the digital-to-analog converter represents the unknown voltage. (The D-to-A converter usually consists of resistive networks that divide the dc reference voltage into discrete quantities.)

Reading speed is high since the reading rate is limited only by the number of voltage steps that must be generated and the time required per step. However, the unknown signal must be noise free. If it is not, it may be impossible to find a null. Therefore, most successive approximation instruments require noise filters to reduce 60 Hz line hum and other noise components. When these filters are required, the speed advantage is lost. For example, if a measurement requires a resolution of 10 μV, a five digit successive approximation instrument will typically require 1 second per reading.

Accuracy and stability depend upon the resolution of the comparator, the accuracy and stability of the dc

Cover: *Artistically portrayed on this month's cover are some of the unique measurement capabilities of the HP Model 3450A Multi-Function Meter. Four terminal ratio, true rms ac, ohms and ohms ratio and limit test are among its many uses discussed in the article starting on* ***page 2.***

In this Issue: *Twelve Functions in a New Digital Meter;* ***page 2.*** *A Computer-Controlled System for Testing Digital Logic Modules;* ***page 14.***

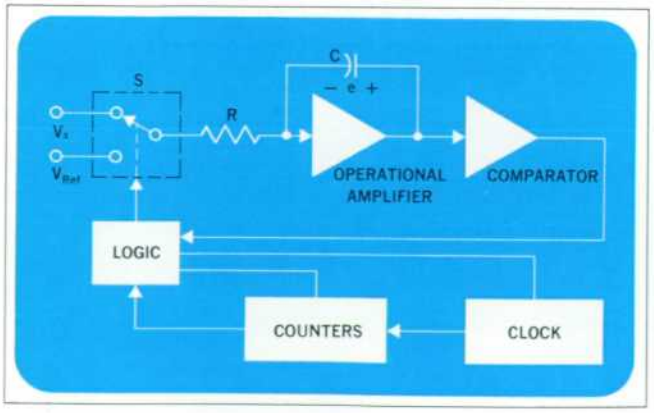
Fig. 4. *Basically a five-digit integrating DVM, the HP Model 3450A measures dc voltage and voltage ratios. With plug-in options, measurement capabilities including ac, ohms, limit tests, digital output and remote control may be added.*

reference and the D-to-A resistive dividers. Overall performance of the potentiometric technique may be limited by the characteristics of the switches in the D-to-A network. Solid state switching provides high reading speed, but generally electromechanical switching is used in the most critical positions because of superior on-off ratio characteristics.

Voltage to Frequency. A third major conversion technique is voltage to frequency conversion.[2] Its basic advantage is its high accuracy and respectable reading rate (5/s for a 5-digit instrument) even in the presence of a noisy signal. Voltage to frequency conversion differs substantially from voltage to time. In the first case, the clock signals have a rate proportional to voltage and are counted for a known time (Fig. 3). In the voltage to time conversion, the clock rate is fixed and counted for a time proportional to the input voltage.

The basic advantage of the voltage to frequency conversion is that it counts the *average* rate of the clock pulse for a known time. Thus, if the unknown signal has a symmetrical noise component with a period equal to or a multiple of the fixed time, it is averaged to zero and does not affect the reading. Generally, the time interval is chosen so that the line hum or 60 Hz is averaged out. In this manner, it is possible to achieve an essentially infinite rejection of line-related noise signals. Thus, noise filters which would reduce reading speed are not usually required.[3]

Voltage to frequency conversion is not inherently as stable nor as accurate as the successive approximation approach. The time base directly affects the reading but presents no problem since it may be crystal controlled. The basic limitations are the accuracy and linearity of the voltage to frequency conversion itself. For example, if it is desired to have a 5-digit instrument that can read at a rate of 5 readings per second, for a full scale reading of 1.00000 V on the 1 V range, the frequency output of the converter must be equal to 100,000 counts in 200 ms or 500 kHz. Its minimum rate must be 0 counts. Thus, if an accuracy of 0.01% of reading is required, the converter must operate between 0 Hz and 500 kHz with a



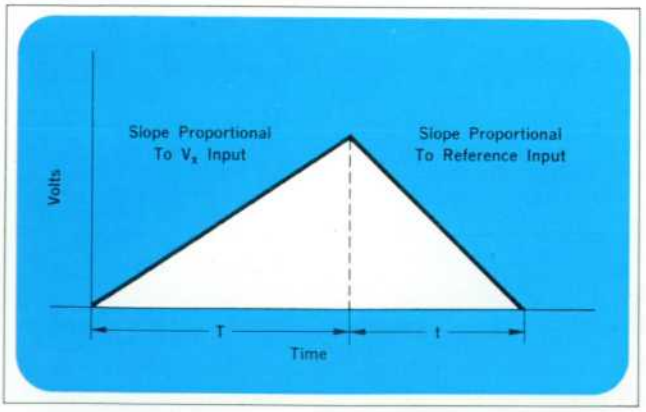


Fig. 5. *(left) The dual-slope DVM compares an unknown voltage for a known time with a known reference voltage for a variable time. Thus the variable time is proportional to the ratio of the unknown voltage to the reference voltage, and is counted to determine the readout.* **Fig. 6.** *(right) Dual slope conversion technique averages the unknown voltage V_x over a known time T, but the ultimate conversion is voltage to time, or V_x to t.*

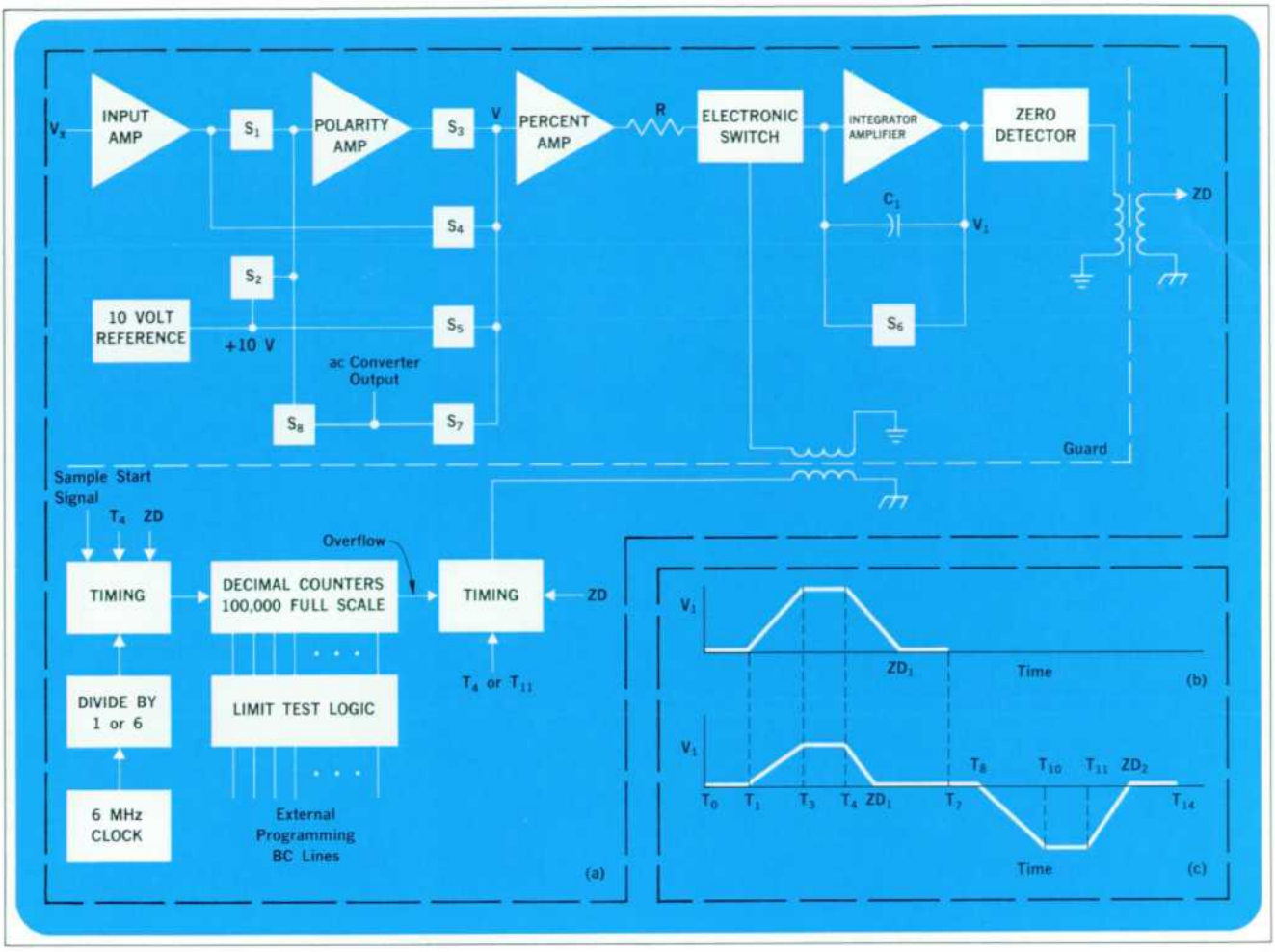


Fig. 7. *In addition to the basic blocks of Fig. 5, the HP Model 3450A includes the signal processing input amplifier and a limit test logic section* ***(a).*** *Voltage waveforms on the integrating capacitor C1 for dc measurements* ***(b)*** *and dc ratio measurements* ***(c).***

linearity of 0.01%. Such performance may be realized but the circuit complexity exceeds that of simple resistive dividers. The V/F converter is also referenced to a precision voltage source which directly affects the accuracy and stability of the reading.

Dual Slope. The dual slope technique is the newest form of analog to digital conversion to be utilized in a commercial digital voltmeter. This technique is used in the HP Model 3450A (Fig. 4). It is relatively simple without sacrificing the highly desirable characteristics of accuracy and stability. The dual slope A-to-D converter, Fig. 5, consists of five basic blocks—an operational amplifier used as an integrator in conjunction with its R and C, a level comparator, a basic clock, a set of decimal counters, and a block of logic circuitry.

The conversion is made by connecting the integrator input to the unknown voltage through a switch for a *known* period of time 'T'. The known period of time is usually determined by counting the clock frequency in the decimal counters. As shown in Fig. 6, a charge is stored in the integrating capacitor that is proportional to the input signal V_x during the known time interval 'T'.

At the end of time interval T, the input is switched from the unknown signal input to a reference voltage of opposite polarity. This causes a current to flow in the integrator in such a manner that the charge begins to decrease with time and results in a linear ramp voltage. During this second period of time a *known* voltage is then observed for an unknown time. The *unknown* time 't' is determined by again counting the clock pulses until the voltage across the capacitor reaches its basic refer-

Peltier Heating and Cooling

The HP Model 3450A comes up to operating accuracy in a relatively short time. This is achieved through the use of a Peltier chamber in place of an oven to control the thermal environment of temperature-sensitive components. It is possible to warm or cool a junction of two dissimilar conductors or semiconductors, depending upon the direction of the current flow through it. The heating and cooling effects are produced by causing the energy of the electron flow through the junction to change between lower and higher energy levels. Electron flow from a p-type to an n-type material causes cooling, while flow in the reverse direction causes heating. In the Model 3450A, the Peltier chamber is part of a closed-loop temperature control system. Controlling magnitude and direction of current through the Peltier junction allows precise control of the temperature in the chamber.

ence level. (In the example, the reference is ground, although any basic reference level may be used.) Mathematically the process may be written as a simple proportion:

$$\frac{V_X}{T\ (fixed)} = \frac{V_{Ref}}{t}.\ Thus\ t = \frac{V_X}{V_{Ref}}\ T.$$

Where: T = fixed integration time, V_x = unknown voltage, V_{Ref} = reference voltage and t = variable discharge time.

It is interesting to note that the ultimate conversion is voltage to time as it was in the simple ramp technique. It is also interesting to note that the unknown voltage is observed for a *fixed* time by an averaging circuit (the integrator). Thus, the dual slope technique is also a time integrating system and as such has all the inherent noise rejection characteristics of the more complex voltage to frequency conversion technique. Finally, it is important to note that the accuracy of the measurement does not depend upon R, C, or the clock frequency. In fact, the accuracy and stability of the measurement are dependent only upon the analog switch 'S', the amplifier (usually upon only its voltage and leakage characteristics), the comparator characteristics, and of course, the reference voltage. Thus, it is possible to built a dual slope instrument with accuracy and stability equal to the best of the other basic converters, yet with good speed.

Reading rate is another parameter of interest for digital voltmeters. In the dual slope technique, the limitations on reading rate are not nearly as obvious as in the other techniques. Compromises must be made depending upon which noise frequencies are to be rejected. For example, it is desirable to reject 60 Hz. Then the initial known time interval 'T' must be at least 1/60 s. In this case the maximum reading rate would be less than 30 readings per second due to the dual slope; and when switching and settling time is included, the reading rate is even less. Other compromises include the time responses of the integrator, comparator, and analog switch compared to the time for a single clock pulse.

In practice a dual slope instrument tends to be fast compared to a V/F instrument and slow compared to a successive approximation instrument without a noise filter. In the case of the HP Model 3450A, 60 Hz signals are integrated and the reading rate in the dc mode is 15 readings per second for full 5-digit resolution. This implies a basic clock frequency of 6 MHz (100,000 counts/1/60 s) which allows 167 ns per indicated count.

Although the dual slope technique offers simplicity, speed, accuracy, and stability, it has another very important advantage over the other techniques—increased versatility at low cost.

To date, in a single instrument package, a DVM user could expect dc, three terminal dc ratio, ac (either an averaging or limited rms converter), ohms, and perhaps frequency measurements. Now, by utilizing the dual slope principle, the HP Model 3450A contains dc, *four*

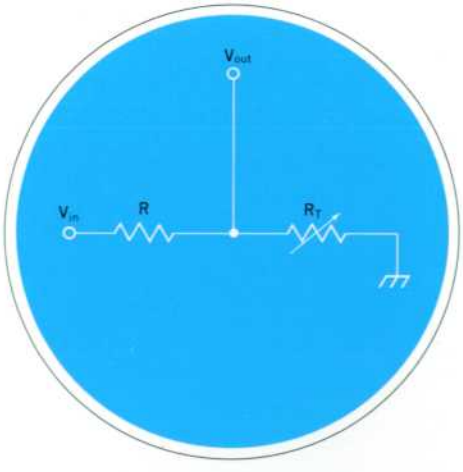


Fig. 8. *To accurately determine the value of R_T, the ratio of V_{out} to V_{in} is more important than the absolute value of V_{out}. Accuracy is then independent of variations in V_{in}.*

terminal dc ratio, ac (rms), *four* terminal ac ratio, ohms, *four* terminal ohms ratio, and a limit test capability that works in conjunction with *any* of the above functions.

Basic Technique

The basic analog system, Fig. 7(a), consists of a high quality input amplifier for 1 μV, high speed performance; a polarity amplifier to simplify the requirement that the reference signal be applied to the integrator with opposite sign to the actual unknown input voltage; a precision, stable 10 V reference voltage; a 'percent' amplifier which is used as a variable gain amplifier for all ratio measurements; and the heart of the system—the integrator, electronic switch, and zero detect network.

As shown in Fig. 7(a), the analog circuitry is enclosed in an electrical guard.[2] The logic circuits are referenced to chassis ground, so that they may either transmit or receive logic signals independent of the nature of the signal being measured. Any signals transmitted between the analog and logic section of the instrument either travel through guarded pulse transformers or through guarded reed switches.

In the Model 3450A, there is a 6 MHz crystal clock that generates an exact integration interval 'T' for noise rejection even though the instrument accuracy does not depend upon the clock stability; a divide by one or six circuit to allow the integration interval to be either 1/60 or 1/10 s; five decimal counting units plus an over range digit to achieve a full scale reading of 100,000; and the basic timing-logic circuits to complete the interaction among functional blocks.

A dc measurement is divided into five intervals in the Model 3450A measurement sequence, Fig. 7(b). The first interval, from the time the reading is initiated (T_0) until the first slope begins (T_1), allows for range switch settling time. That interval is generated by counting the basic clock frequency in the decimal counting units.

At T_1, a timing signal is generated by the logic and is transmitted to the electronic switch at the input of the integrator amplifier. It changes state from OFF to ON and allows a current to flow through the input resistor R into the primary integrating capacitor C. This action results in the first slope with a time duration (T_1 to T_3) of either 1/60 or 1/10 second. Again, the basic clock and decimal counting units determine this integration interval. At T_3 the electronic switch is set to OFF.

Between T_3 and T_4, the polarity of the final value of the signal stored on the capacitor C is determined and the proper polarity reference is connected to the percent

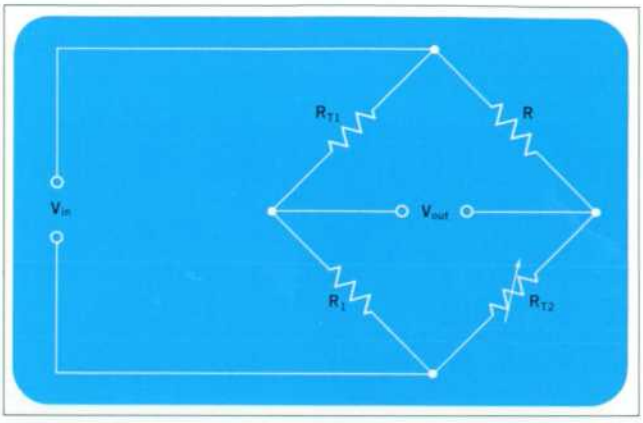


Fig. 9. *A four-terminal ratio measurement is required on this balanced bridge network to make V_{out} independent of any ΔV_{in}.*

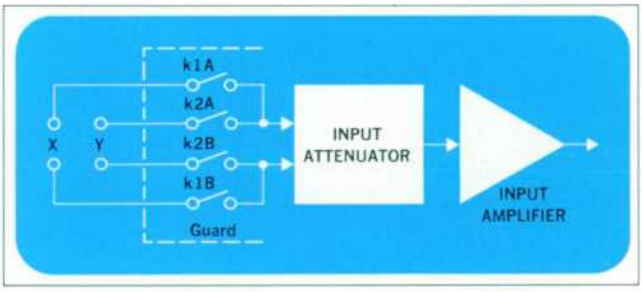


Fig. 10. *For a four-terminal ratio measurement, the Model 3450A converter is multiplexed between the two isolated sets of input terminals.*

amplifier (amplifier preceding the integrator with fixed gain for all functions other than ratio) either directly or through the polarity amplifier. Because of integration, an accurate measurement can be made even though the input signal may be composed of a small dc signal in the presence of a large ac noise signal. However, for that case, the voltage on C could pass through its reference point (ground) many times during the T_1 and T_3 interval. The final average value is the signal of interest, however, and its polarity must be used to determine the polarity of the reference signal that will be used to remove the charge from C1 during the second slope.

The interval T_1 to ZD (zero detect—i.e., the comparison of the capacitor C1 voltage to ground) is proportional to the value of the input signal stored during the first slope as noted in the earlier discussion of the dual slope technique. This interval is determined by again counting the basic clock frequency and at ZD, the total count value is in fact a numerical representation of the signal being measured.

Fig. 11. *Indication shows ratio underload on the HP Model 3450A when reference voltage drops below a usable level.*

The final time interval in the measurement (ZD to T_7) is used primarily to make the period of the total reading constant regardless of how long a time existed between T_4 and ZD. If this is not done, the reading rate of the instrument would vary by almost two to one depending upon the magnitude of the reading. For systems applications this could be quite disconcerting.

DC Ratio Measurements

Ratio capability is a good example of the increase in versatility that is required of digital voltmeters in an ever increasing number of applications. Often it is more convenient, less costly, and more accurate to determine the ratio of two signals rather than attempt to measure both absolutely.

In the simple resistive divider, Fig. 8, assume that R_T is a pressure transducer whose quiescent output has been established by V_{in} and R. As pressure is applied to R_T, the voltage division between R and R_T will change, resulting in an output signal ΔV_{out}. This is the quantity of interest. However, if V_{in} changes, V_{out} will also vary. Thus, a ratio measurement of V_{out}/V_{in} rather than an absolute measurement of V_{out} is desirable since one major error source can be eliminated.

In the above example, a three terminal ratio measurement would be perfectly satisfactory since the common lead for measuring the voltage may be connected to ground. Unfortunately, there are a large class of ratio measurements that *need* a four terminal ratio measurement—i.e., one where there cannot be a common connection between the two signals.

An example of a circuit that requires a four terminal measurement is shown in Fig. 9. Assume that R_{T1} and R_{T2} are pressure transducers where R_{T1} is connected to act in compression when R_{T2} is in tension. The output signal V_{out} will be affected by any instability of V_{in}. Even with a balance adjustment, any signal from the bridge that deviates from its quiescent point will still be affected by a ΔV_{in}.

In this circuit it would be very desirable to take the ratio of V_{out} to V_{in} but it cannot be done directly with a three terminal ratio measurement. With a true (isolated) four terminal measurement, however, the task becomes very straightforward.

Four Terminal Ratio

One of the primary benefits of the dual slope conversion technique is that four terminal ratio becomes possible using a single converter.

As pointed out in the discussion of the basic conversion process, a dc measurement is a ratio of the input signal V_x to an internal reference signal V_{Ref}. (So is any dc measurement in any of the other three techniques.) But with the dual slope ratio, the two signals are measured at two different times—i.e., for V_x/V_y, V_x is measured in the first slope and V_y is used to discharge the integrating capacitor during the second slope. Since the short term stability of even the most simple power supply is generally good, the small time difference between the signals is tolerable.

Since the measurement of V_x/V_y is made successively, it is possible to utilize the same input attenuator, the same input amplifier, and the same basic converter to make a totally isolated measurement of the two signals. This may be done quite simply by multiplexing the actual voltmeter input to two separate sets of terminals (Fig. 10). Of course, the reference signal could be alternately inserted into the instrument directly in place of the internal reference. However, there are several advantages to the multiplexing technique.

For example, by using the same input circuits for both signals, the input impedance for both can be identical and each signal may be attenuated or amplified as required to normalize it to the basic internal range of the instrument. As a result, the source resistance of a ratio measurement in the Model 3450A is not critical. In fact, for signals less than 10 volts, the input impedance for both the X and Y input signals is greater than 10,000 MΩ. Also, the dynamic range of ratio measurements is extremely wide. By using the range capability of the Model 3450A on both X and Y, it is possible to have a reference signal (Y input) of ±110 mV to ±110 V and to have an unknown signal (X input) of 0 V to ±1200 V.

In addition, the Model 3450A provides polarity detection and autoranging for both inputs. Thus a four terminal measurement may be made by connecting the two inputs to their respective terminals without regard to magnitude, isolation, or polarity (within the voltage breakdown limitations of the instrument). The polarity and range of each signal is determined automatically, and the reading is displayed with five-digit resolution.

Because of the automatic ranging feature for both input signals, the timing for a dc ratio measurement is different than that for dc, Fig. 7(c). The first portion of a ratio measurement (T_0 to T_7) is identical to a dc measurement except that the reference signal (Y) is measured to determine its polarity, approximate percent of full scale, and range. This information is stored internally but nothing is displayed on the panel.

From T_7 to T_{14}, the measurement is again similar to a dc measurement except that the properly scaled external reference (Y) is switched in for the second slope instead of the instrument's internal reference. One other difference in the measurement from T_7 to T_{14} is that the gain of the percent amplifier is preset prior to T_7 to insure that the slope of the second ramp is maintained at a value nearly equal to the slope due to V_{Ref}. The actual gain of the percent amplifier is of no consequence since $(V_x \cdot A)/(V_y \cdot A) = V_x/V_y$ where A is the gain of the amplifier. By maintaining the down slope approximately constant from measurement to measurement, errors in the zero detection circuits are minimized even though the level into the percent amplifier may change by approximately 10 to 1.

In making ratio measurements, a condition may occur where the reference signal level is too low. In the Model 3450A, a minimum signal level of ±110 mV for the reference was chosen in order to make the ratio sensitivity consistent with dc. For example, if a ratio of two signals were performed where each signal is 110 mV, then, with a five-digit readout, the last significant digit

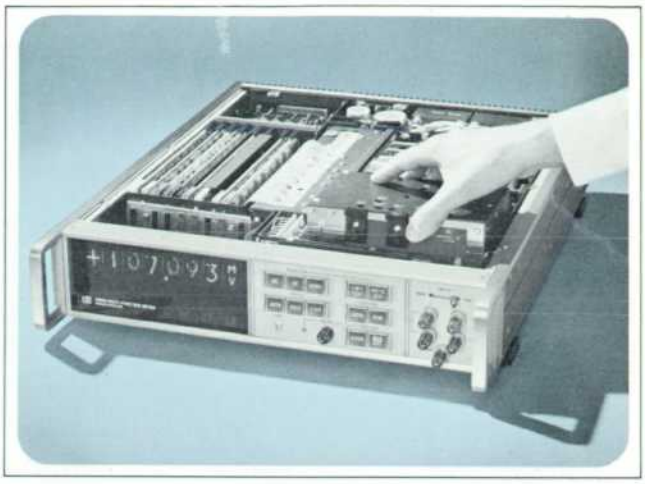


Fig. 12. *True rms ac-dc converter is installed in the HP Model 3450A as a plug-in.*

actually represents a sensitivity of 1 μV/count even though the reading is 1.00000 and dimensionless. In the event that a reference level less than 100 mV is put into the Model 3450A, the instrument displays the magnitude of the reference signal on the front panel in addition to an overload symbol ' Q ', Fig. 11. Thus, in a system operation, even if the reference signal is lost, a print command is issued at the same time the value of the signal on the reference terminal is displayed so that the system may sequence to its next point. The information shown on the front panel also exists on the digital output.

Four terminal ac or ohms ratio measurements are also possible with the dual-slope technique. For example, when the ac option is installed in the Model 3450A, the ac input still utilizes the front terminal switching shown

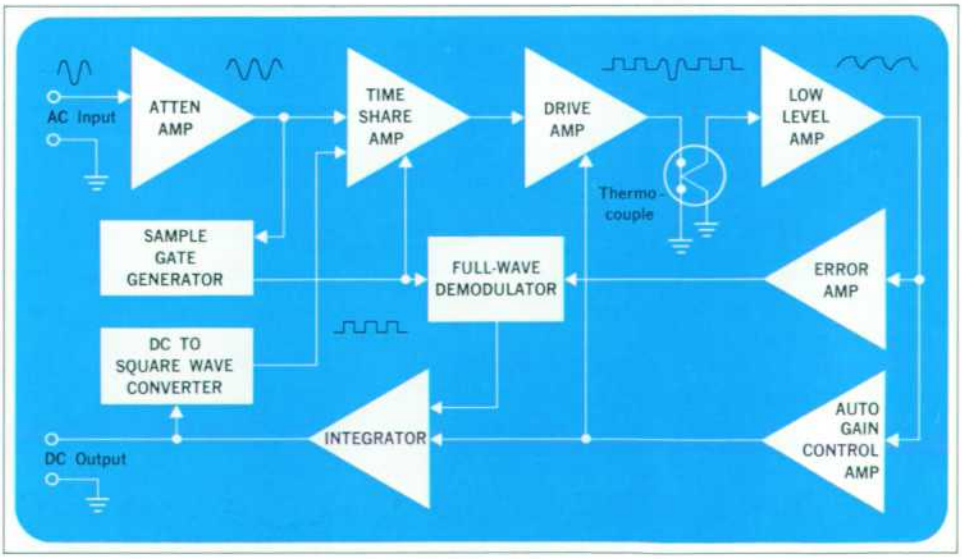


Fig. 13. *Ac to dc converter for the HP Model 3450A has a wideband accuracy of 0.05%.*

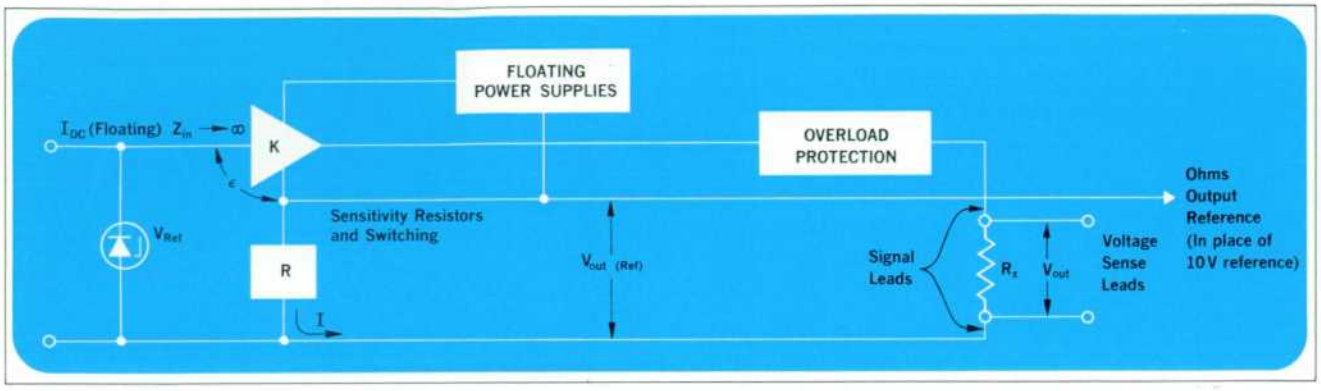


Fig. 14. *Ohms measurements are made by taking the ratio of V_{out} to $V_{out\ (Ref)}$. Resistor R determines current I which also flows through R_X. Thus the ratio of the two voltages is the ratio of R_X to R. Amplifier error ε and the magnitude of V_{Ref} do not affect measurement accuracy.*

in Fig. 10. The converter output is then switched into the basic system through either S_7 or S_8, Fig. 7(a). As a result, the Model 3450A can make true four terminal, ac true rms or resistance, automatic ratio measurements over a wide dynamic range for both X and Y inputs.

True RMS AC to DC Conversion

Most high accuracy ac to dc converters in modern digital voltmeters employ a technique which averages the absolute value of the ac signal. These units are calibrated to read the rms or effective value for a certain waveform (usually a pure sine wave). Distortion in sine waves, however, can cause significant errors in average responding instruments.[4] The accuracy with which an average detecting voltmeter will read the true rms value of a waveform depends upon the amount of distortion present and the phase relationships between the fundamental and its harmonics.

In practice, most waveforms that appear sinusoidal are not distortion free. It is often necessary to measure the rms value of other ac signals such as square and triangular waves or pulse trains. In such cases, average reading converters are severely limited.

Automatic Thermal Transfer

The basic, most highly regarded technique used to determine the rms value of an unknown ac voltage is accomplished by an ac to dc thermal transfer.[5] This method compares the heating value of a dc current to that of an ac current and yields accuracies in the vicinity of 0.01%.

The HP Model 11078A AC Converter, Fig. 12, is designed to be installed within the Model 3450A. This ac converter used in conjunction with the Model 3450A makes automatic, 5-digit, true rms ac and 4-terminal ac ratio measurements over a frequency range of 45 Hz to 1 MHz, with midband accuracy of 0.05%. The unit has four full scale ranges of 1 volt to 1000 volts in decade steps with 20% overranging capability. A crest factor* of 7:1 allows measurement of waveforms that differ greatly from sinusoidal.

The automatic thermal transfer technique used in the Model 11078A overcomes many of the disadvantages of the classical ac-dc transfer method, and at the same time retains most of the advantages. Instead of making time-consuming ac readings and manually adjusting the known dc (including reversal error), the automatic thermal transfer circuit makes a plus and minus dc to ac comparison several times each second. In the process, the dc output of the converter is adjusted until it is proportional to the rms value of the ac input.

In the Model 11078A conversion system, Fig. 13, a broadband, high accuracy attenuator amplifier adjusts the input signal to the desired level and applies it to one input of the time-sharing amplifier. The other input to the time-sharing amplifier is a precise square wave derived from the dc output of the converter. These signals are alternately applied to a fast rise time thermocouple via the drive amplifier. The feedback square wave is switched at a high frequency compared to the response time of the thermocouple. This automatically averages out the reversal error of the thermocouple. The input voltage is compared with the square wave five times each second. As a result, any error due to drift in the thermocouple output is eliminated.

*Crest factor is defined as the ratio of the peak voltage to the rms voltage of a waveform (with the dc component removed).

Since the time-sharing and driver amplifiers are common for both the ac and square wave signals, their gain accuracy and gain stability are of secondary importance. The basic design objectives for these amplifiers were therefore wide-band frequency response and large dynamic range.

If the rms value of the ac signal is different from that of the square wave, the output EMF of the thermocouple will change each time the time-sharing amplifier switches between the input and feedback signals. Thus, the thermocouple output contains both a dc and a 5 Hz component. The dc level represents the quiescent operating point of the couple and the 5 Hz component is the error signal. Following the thermocouple is a low level direct-coupled amplifier. Its output is applied to the automatic gain control amplifier which adjusts the gain of the driver amplifier to keep the dc operating point of the thermocouple constant. Therefore, the rms input to the thermocouple is constant for ac input levels from full scale down to where the AGC loop loses control—less than 1/300 of full scale. Two important benefits resulting from the use of the AGC loop are: low noise because the thermocouple is operated at a constant high level and the elimination of errors due to the thermocouple change in square law characteristics with changes in quiescent point.

The low level amplifier output is also ac coupled to the error amplifier which is designed to amplify only the 5 Hz signal. Its output is demodulated, amplified, and filtered by the integrator to develop the dc output for the converter. The overall loop stability of the converter is maintained by simultaneously adjusting the gains of the integrator and driver amplifiers via the AGC amplifier to maintain total loop gain constant.

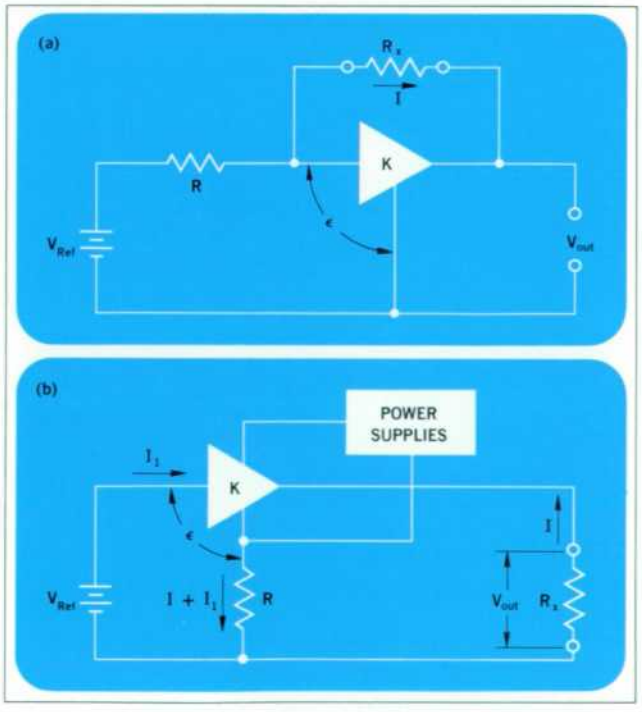
Ohms to DC Conversion

The ohms converter, Fig. 14, is a good example of the simplicity, versatility and reliability that result from the use of dual slope.

In making ohms measurements, a precision stable amplifier is usually used in conjunction with precision resistors and a precision voltage source to generate a controlled current to the resistor under test, Fig. 15.

In Fig. 15(a), an operational amplifier is used with the unknown resistor R_x in its feedback loop. Since the input of the amplifier is a virtual ground, the current through R_x is: $I = \frac{R}{V_{Ref} - \varepsilon}$ where ε is the offset voltage of the amplifier. V_{out} is then proportional to IR_x.

In Fig. 15(b), a floating amplifier is used as a unity gain amplifier with high internal feedback. As such, it



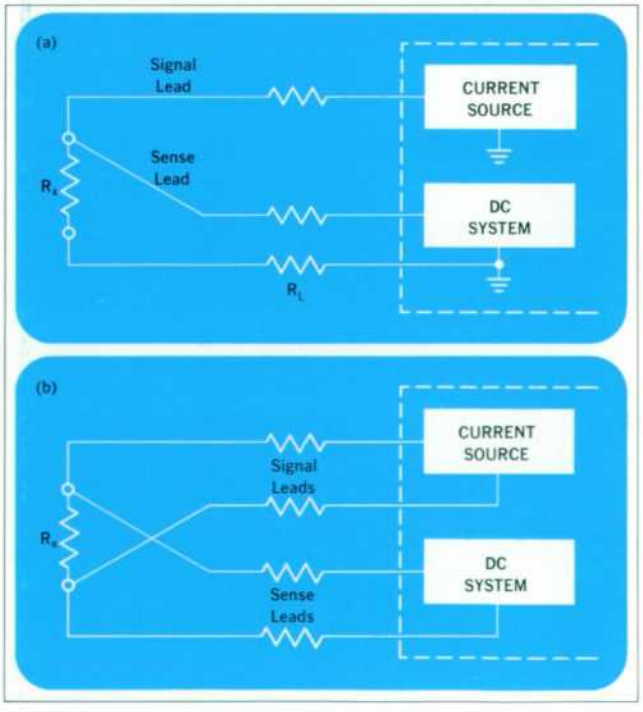


Fig. 15. *(left) In each of these techniques for measuring unknown R_x, current I must be well controlled.* **Fig. 16.** *(right) A two or three-wire ohms measurement (a) includes the effect of lead resistance R_L. If the signal and sense leads are isolated (b), R_L is not included as a possible error source.*

Harold Briggs (right) graduated from the University of Colorado in 1960 with a BSEE degree and joined HP as a development engineer in the Frequency and Time Division. While in Palo Alto he worked in frequency and standards, primarily on the 106A Quartz Crystal Standard. Harold attended Stanford University and San Jose State College on the HP Honors Cooperative Program.

In 1963 he transferred to the Loveland Division as a development engineer in the digital voltmeter group. Since coming to Loveland, Harold has worked on the Model 3460A and the development of the HO4-3460A. Since completion of these projects he has been project engineer for the Model 3450A with primary responsibility for the logic design of that instrument. He is presently the production engineering supervisor on the HP Model 9100A Calculator.

In 1965 he completed the requirements for and received the MSEE degree at Colorado State University on the HP Honors Cooperative Program. Harold is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Tau engineering honorary fraternity groups. **Jerry Harmon** (left) joined HP in Loveland in 1962 after receiving his BSEE degree from Colorado State University. He continued his studies at CSU on the HP Honors Cooperative Program and was awarded an MSEE degree in 1966.

Jerry has been project leader on the true rms ac-dc converter for the Model 3450A Multi-function Meter. Prior to that time he worked on the ac-to-dc converter, circuitry for the Model 741A/B ac-dc differential voltmeter/dc standard. He is presently working in Loveland's integrated circuits section.

Jerry is a member of Phi Kappa Pi, Sigma Tau, and Eta Kappa Nu engineering fraternities. **Bill Kay** (center) has been involved in the design and development of digital voltmeters since he joined HP Palo Alto in 1962. Initially, he worked on the HP Model 3460A Precision Digital Voltmeter and transferred to HP Loveland with that instrument in 1964. At Loveland he first became the project leader for the HP Model 3450A and then was given the overall group responsibility for the high resolution, precision digital meter program. At the present time he is a production engineering manager at the Loveland plant.

Bill received his undergraduate degree from the University of Missouri in 1962, then, as a participant in the HP Honors Cooperative Program, he attended Stanford University. He was awarded an MSEE degree in 1964.

establishes $V_{Ref} - \varepsilon$ across R and also generates a current through R_x of $I = \frac{V_{Ref} - \varepsilon}{R}$. The current that flows in the input loop, I_1, can usually be ignored since the input impedance of the amplifier in this configuration is extremely high.

For both these cases, if V_{out} is measured by a dc technique to determine R_x, the current through R_x must be precisely known. This means that V_{Ref} and R must be precise, and that the error signal ε of the amplifier must approach zero. By comparison, the Model 3450A does not use a precision voltage source nor a precision amplifier since it does not require a precision current to make high accuracy measurements.

From Fig. 14, $I = \frac{V_{Ref} - \varepsilon}{R}$ where the gain of the amplifier is large. The voltage generated across the unknown resistor is then given by $V_{RX} = IR_X \frac{(V_{Ref} - \varepsilon)R_x}{R}$ Since the voltage across R is used as the reference voltage during the run down from T4 to ZD (see Fig. 7), $\frac{V_{RX}}{V_{ohms\ Ref}} = \frac{V_{RX}}{V_{Ref} - \varepsilon} = \frac{R_x}{R}$. Thus the accuracy of the ohms measurement does not depend upon V_{Ref} or the offset of the amplifier. All that is required is that these voltages remain stable during the very short time required for a single reading.

In a basic three wire ohms measurement, Fig. 16(a), the signal current must flow through R_x and the lead resistance (R_1) to complete its return path. As a result, the voltage consists of both the drops across R_x and R_L. If another voltage series lead is brought out from ground, its impedance is simply in parallel with R_L.

Since the Model 3450A has a 100 ohm full scale range and is therefore capable of resolving 1mΩ of resistance, the effect of lead resistance cannot be tolerated. These effects have been eliminated by using a four-wire measurement technique, Fig. 16(b). To achieve a four-wire measurement, where the voltage drop in the lead resistance does not enter as measurement error, there cannot be a common connection between the ohms converter ground and the dc system ground during the interval of time that the voltage V_x is being measured.

Limit Test

A useful function in the Model 3450A is the ability to test the numeric value of any of the six basic functions—dc, dc ratio, ac, ac ratio, ohms, and ohms ratio against two binary coded limits.

The comparison is made between the binary coded limits and the actual number in the decimal counting units on a dynamic rather than a static basis: i.e., the test is completed as the number accumulates rather than testing the limits against the final number itself. Because the counters are only required to count from zero up to their final value, simple NAND type integrated circuit logic may be used to perform the limit test.

Systems Capability

In addition to the capabilities previously described, the Model 3450A is designed for systems compatability through the use of two additional options—Digital Output and Remote Control.

Digital Output supplies to the system the normal stored data, function and range information, and also provides for printout of any combination of Hi-Go-Low information when in the Limit Test mode. In addition, a pulse is available to maintain system operation in absence of a printout.

Remote Control allows for the remote selection of function, range or ratio multiplier and provides electronic lockout of all front panel controls. In addition, the decimal locator may be selected independent of range for decade scaling without disturbing the basic range settings.

Acknowledgments

Projects like the HP Model 3450A and the HP Model 11078A True rms ac-dc Converter require real team effort. The team members included Mike Aken, Jerry Blanz, Gary Egan, Al Gookin, Barry Taylor, Lee Thompson and Phil McCollum. Mike and Al worked primarily with the analog circuitry, Gary with the logical design, Lee with the circuit and product design for the 11078A, Barry and Jerry did the product design for the Model 3450A with Phil's technical support.

We wish to thank Don Schulz for his direction and counseling, and we wish to express our appreciation to Bob Shuffler for his support.

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SPECIFICATIONS

HP Model 3450A
Multi-Function Meter

The Hewlett-Packard Model 3450A Multi-Function Meter is a five-digit integrating digital voltmeter. The basic instrument measures dc voltage and four terminal dc voltage ratios. Added measurement capability is achieved by the addition of plug-in options, all of which are easily installed.

The Model 3450A uses a dual-slope integration technique and is fully guarded, providing excellent noise immunity at 15 readings per second on all dc ranges. Ranging is automatic over all ranges on all functions. The AC option adds ac measurements from 45 Hz to 1 MHz with true rms response. Six ohms ranges including a 100 Ω range are provided with the OHMS option. Ratio capability is integral in the basic instrument. When the AC and OHMS options are installed, ac and ohms ratios can be measured. Ratio measurements are made in a truly isolated four terminal manner. The Model 3450A is contained in less than 3½ inches of rack height and requires no cooling fan.

Additionally, the LIMIT TEST option allows digital comparisons against two preselected limits. This capability is applicable to all functions with no degradation in function performance. DIGITAL OUTPUT, REMOTE CONTROL and REAR INPUT options are also available.

DISPLAY

The Model 3450A presents polarity, function and digital information on a non-glare front panel display. Maximum resolution at full scale for all functions is made possible by the 20% overranging feature. HI (red), GO (green), and LO (amber) limit test indications are also displayed on the front panel.

STANDARD FUNCTIONS

DC and DC Ratio: The basic Model 3450A includes 5 ranges of dc with 1 μV sensitivity on the 100 mV range and 4 ranges of true 4-terminal dc ratio. Measurements can be made on all 5 voltage ranges at 15 readings per second with an accuracy of 0.008% of reading. The high input resistance, $>10^{10}$ ohms for the 100 mV, 1 V, and 10 V ranges, makes it possible to measure high impedance sources without detectable loading errors. Ratio (unknown and reference input) ranges are selected automatically. Reference voltages from ±110 mV to ±110 V can be used for ratio measurements. Input impedance for the reference input is the same as for the unknown input.

OPTIONAL FUNCTIONS

AC and AC Ratio (Option 001): Four ranges of true rms ac are provided by the AC Converter. Frequency response is from 45 Hz to 1 MHz. In addition, 4 ranges of true 4-terminal ac ratio are also provided with the ac converter. The reference ac level may vary from 110 mV to 110 V.

Ohms and Ohms Ratio (Option 002): Six resistance ranges and four resistance ratio ranges are provided with the Option 002 Ohms Converter. The 100 Ω range permits resistance measurements to be made with 1 mΩ sensitivity. Maximum current for the 100 Ω range is 1 mA at 100 mV. The 4-wire measuring technique permits low resistance measurements to be made without errors due to lead resistance. Readings are made at 15/s on the five lowest ranges.

The 4-terminal ratio measurement capability (two leads for each resistor) offers the advantage of having complete isolation between the reference resistor and the resistor being measured. The reference resistor may vary from 110 ohms to 11 megohms.

LIMIT TEST (OPTION 003): The capability of making limit test measurements on any one of the six basic functions (dc, dc ratio, ac, ac ratio, ohms, and ohms ratio) is accomplished by adding the Limit Test Option. This rear panel plug-in board permits limit test measurements without affecting the speed and accuracy of the six functions described above. The value of the unknown as well as a HI, GO, or LO indication is displayed on the front panel. Both indications are available in BCD form at the digital output.

The HI-GO-LO limits are programmed through a 50-pin connector provided on the limit test accessory. Each limit includes 4 digits, an overrange digit, and polarity.

DIGITAL OUTPUT (OPTION 004) AND REMOTE CONTROL (OPTION 005):

The digital output and remote control capabilities can be ordered as options or as separate accessories to meet a specific requirement.

The digital output provides 9 columns of information which includes function, polarity, data information, and range of ratio multiplier. An end-of-reading signal is provided to serve as a print command for a digital recorder or as an advance signal in a system.

BENCH AND SYSTEMS CAPABILITY, MANUAL AND AUTO-RANGING ON ALL FUNCTIONS

The Model 3450A autoranges through all ranges of each function. The STEP pushbutton provides manual range selection. The correct ratio reference range is always selected automatically for ac ratio, dc ratio, and ohms ratio functions, and the unknown input range multiplier is selected manually or automatically.

4-TERMINAL RATIO, FLOATED AND GUARDED INPUTS, FRONT AND REAR INPUTS

The Model 3450A has capability of making true 4-terminal dc ratio, ac ratio, and ohms ratio measurements. Because of this capability, the reference signal need not share a common ground with the unknown signal. As a result, ratio measurements may be made on bridge circuits, such as strain gauge transducers, etc. Thus, the 4-terminal technique eliminates requirements for highly regulated bridge power supplies. Guarding and integration provide excellent effective common mode and ac normal mode rejection characteristics.

PRICE:

HP 3450A (Includes DC and DC RATIO)	$3150
HP H50-3450A, optimum noise rejection for 50 Hz line frequency	$3210
Option 01 AC Converter (adds AC, AC RATIO)	$1250
Option 02 OHMS Converter (adds OHMS, OHMS RATIO)	$400
Option 03 LIMIT TEST (adds Limit Test capability)	$350
Option 04 DIGITAL OUTPUT (adds BCD output, 1-2-4-8 code)	$175
Option 05 REMOTE CONTROL (adds Remote Control capability)	$225
Option 06 REAR INPUT TERMINALS (adds Front/Rear selector switch and isolated rear terminals)	$50

MANUFACTURING DIVISION: LOVELAND DIVISION
P.O. Box 301
815 Fourteenth Street S.W.
Loveland, Colorado 80537

Fig. 1. *Model 2060A Digital Logic Module Test System can give most production logic modules a thorough functional test in less than 30 seconds. It is programmed in AuTest, a special simplified language. Once programmed, it can be used by unskilled operators.*

A Computer-Controlled System for Testing Digital Logic Modules

This high-speed system can do production testing quickly, thoroughly, and economically. Its principle of operation —comparing unknown modules with a known-good reference module— makes it easy to program and operate, and easy to adapt for testing different modules.

By William P. Cargile

MANUFACTURERS OF DIGITAL EQUIPMENT have to deal with some formidable numbers in production testing digital logic modules and printed-circuit boards. A complete check of the logical functioning of a module which has N binary elements may require 2^N separate steps, one for each of the 2^N possible combinations of high and low logic states of the elements. Since N can range up to several hundred, 2^N can be very large indeed, and it can take a long time to test a complex logic module. It can also be very costly.

At Hewlett-Packard, we first encountered this problem when we started making computers. We decided the answer was higher speed—an automatic test system. The system we built to solve this in-house problem has now evolved into the Model 2060A Digital Logic Module Test System (Fig. 1). Controlled by an HP 2116B Computer which is programmed in a special simplified language, AuTest, the system checks logic modules thoroughly and efficiently, and prints an error message when it finds a faulty module. The system is inherently flexible. It can test a broad range of logic modules of different types and degrees of complexity, and it is easily changed to accommodate different modules; often only a change of program is needed. It has two modes of operation, a 'run' mode for sorting good and bad modules from a production run, and a 'conversational' mode for debugging faulty modules. In its run mode it can be used by an unskilled operator.

Pretesting each logic module with this type of system before the modules are installed in instruments has reduced the test time and the cost of testing by as much as 70% for some of our instruments. At the same time, we have been able to increase the scope and number of tests performed on each module, thereby improving reliability and decreasing warranty costs. Operating at rates up to 10,000 tests per second per pin, the 2060A System can completely test most logic modules in less than 30 seconds, at a cost of less than one dollar each.

Functional Testing

The 2060A System tests modules functionally. That is, it applies sequences of logic inputs that simulate the inputs the module will receive in service. At each step in the sequence it checks all of the module's output pins for the correct responses. The system doesn't test dynamic or switching characteristics, since these are more easily tested on separate components than on fabricated modules.

Logic modules usually contain storage elements (e.g., flip-flops). This makes each logical state of the module depend on previous states. For this reason, the 2060A System maintains all logical stimuli constant from step to step over the entire logical test sequence, except, of course, those inputs that are programmed to change. The system generates logic levels in analog form and not by closing contacts, because random contact bouncing might

be mistaken for signal pulses by sequential logic circuits, and this would result in unpredictable and anomalous logical states in the module.

Comparison Reduces Programming and Storage

In some computer-controlled logic module test systems, the correct logical responses of the module must be specified in the test program and stored in the computer's memory. The number of program steps and memory locations needed for this may be as large as the number of distinct sequential logical states of the module (2^N for a module with N binary storage elements) times the number of logic outputs, plus other output states which are simply combinatorial functions of the logic inputs (i.e., derived by logic gates instead of storage elements). For all but the simplest modules, this number is so large that functional testing is uneconomical; it takes too many man-hours of programming time to generate test data and too much memory to store them.

The 2060A System uses a comparison technique which avoids these programming and storage problems (see Fig. 2). It derives the expected responses of the module being tested from an identical reference module which is known to be working properly. The system exercises the reference module and the module of unknown quality simultaneously, with identical but electrically isolated signals. After each change of inputs, all corresponding pins of the two modules are compared within a tolerance specified in the test program. Any logical disagreement is printed on the Teletypewriter. The comparison method reduces the programming effort to simply specifying logical sequences of inputs. Expected responses needn't be specified or stored.

Unlike most testers and test systems, the 2060A System can test many types of integrated-circuit and discrete-component logic without special adaptation. High and low logic levels, positive and negative current limits, and test tolerances are generated according to test program instructions. Thus the 2060A System can be set up to test DTL, CTL, TTL, RTL, ECL and most other types of logic simply by specifying the appropriate logic parameters in the test program. The system can be equipped to generate up to four separate sets of logic parameters simultaneously, for testing different types of logic on the same module.

The Hardware

Much of the 2060A System's flexibility comes from its general-purpose HP 2116B Computer. All of the computer's standard plug-in input/output options can be used with the system. An I/O extender for the computer can also be included if more input/output capacity is needed.

Included in the basic system are a Teletypewriter for program listing and operator communication, and a paper tape reader for input of test programs. Optional are a disc memory for bulk storage of test programs, a real-time scaler for time accounting, a high-speed punch for output of revised test programs, and a data acquisition subsystem for verification of reference modules and for low-speed, high-resolution dc measurements (see Fig. 2).

The system can have as few as two and as many as 32 driver/comparator registers, each of which contains eight driver/comparator circuits. Each driver/comparator circuit provides inputs or loads, and compares outputs, for one pair of corresponding pins, one on the reference module and one on the module being tested. Thus the basic system can test modules which have as many as 16 pins, and an extended system can test modules which have as many as 256 pins.

Dc reference levels for the driver/comparator circuits and dc power for the modules are generated by programmable dc power supplies which are resistance programmed by relay-register cards plugged into the computer. Since the power-supply outputs are not changed during a functional test sequence, resistance programming — uncomplicated, inexpensive, and slow — is adequate. Additional power supplies and relay registers are easily installed in the system.

The driver/comparator registers and power supplies are connected to the modules being tested via a module adapter which holds removable socket trays. Many trays are available to accommodate modules with different connectors.

Driver/Comparator Registers

The driver/comparator registers are the interface between the modules and the system. They are designed for maximum flexibility to make the system useful for testing a wide variety of circuits. There are two types of driver/comparators. One is a low-impedance driver/comparator which is compatible with most discrete circuits, with RTL, DTL, TTL, CTL, and ECL integrated circuits, and with other integrated circuits which have logic levels between −6 V and +6 V and current parameters between −50 mA and +50 mA. The other driver/comparator is a high-impedance type compatible with MOS circuits and with high-level discrete circuits. It can provide voltages between −18 V and +18 V and currents between −15 mA and +15 mA.

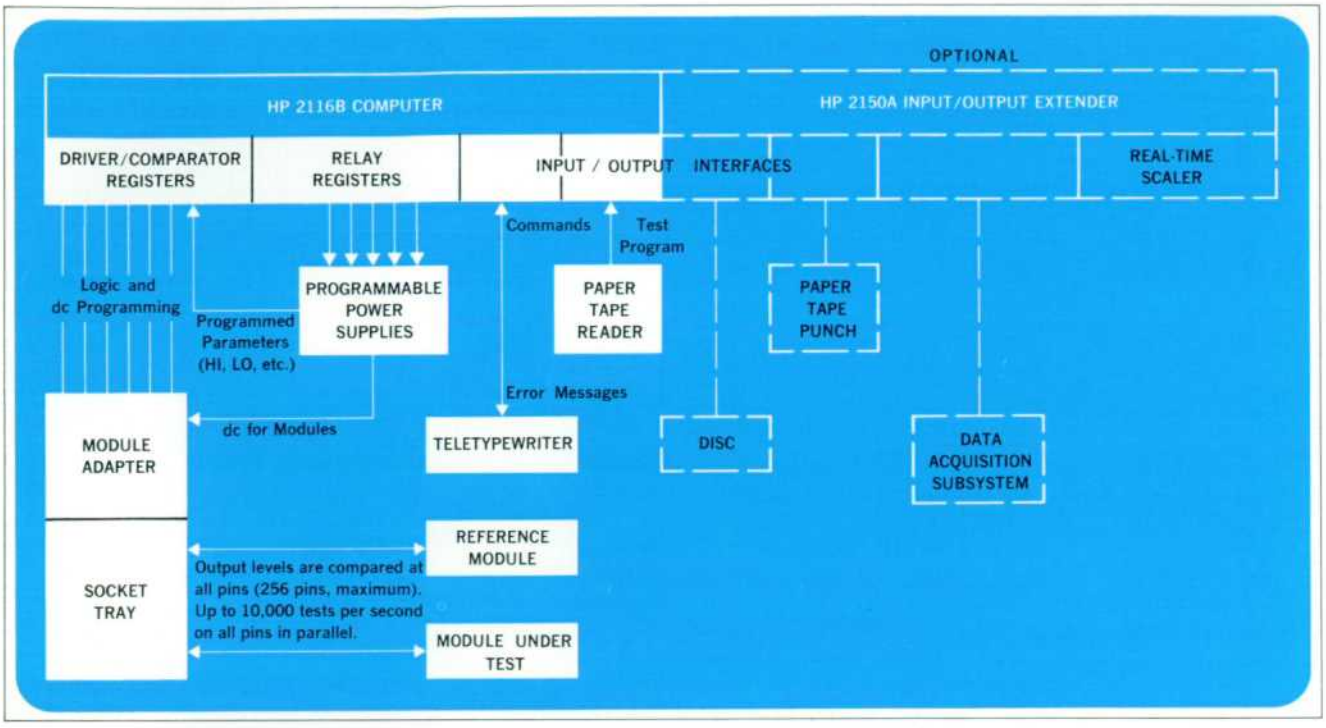

Fig. 2. *The 2060A System exercises the module being tested and a reference module with identical inputs. At each step in the test program, the system compares the signals on all corresponding pins of the two modules and prints an error message if they differ. The comparison method simplifies programming because the programmer only has to specify inputs, not the expected outputs. Logic parameters are generated by programmed power supplies under control of the test program; thus the system can test many types of logic without hardware changes. When expanded capacity is needed, standard hardware can be added easily.*

Fig. 3 is a block diagram of a driver/comparator register. Each register contains eight driver pairs, eight comparators, buffer storage for the logic signals and comparator results, and overload detectors that cause all power to be removed from the modules if the outputs of either module cannot be tolerated by the system.

Since two modules (the reference module and the module being tested) must be exercised simultaneously and their outputs compared, there are two drivers for each logic signal. They are electrically independent except for a common input. Their outputs are routed to corresponding pins on the two modules. The comparator is connected between the two outputs.

The programmable parameters of the driver circuits are

HI — *the more positive of the two logic levels*

LO — *the more negative of the two logic levels*

P — *positive constant-current limit (source)*

N — *negative constant-current limit (sink)*

These must be specified in the test program. The comparator has a programmable threshold with parameters +T and −T, which are comparison tolerances specified in the test program. Programmed parameters are the same for all eight driver/comparators in each register.

The driver circuits can drive module inputs, act as loads on module outputs, or do both simultaneously. The system distinguishes inputs from outputs only in that the logic levels for drivers acting as loads on module outputs are normally set to the appropriate state and not subsequently altered by the test program. Drivers providing module inputs are switched between logic states as required to exercise the modules. To illustrate this dual operation, Fig. 4 shows the terminal characteristics of a driver programmed to operate with TTL inputs and outputs. Also shown are the terminal characteristics of the TTL circuits and resulting operating points. Terminal characteristics of the driver circuits are established by dc voltages from the programmed power supplies.

The Software — AuTest

Module test programs for the 2060A Digital Logic Module Test System are written in AuTest, a special language designed to be easily understood by engineering people. Most digital logic technicians can learn the basic

programming rules in a day or less.

All 2060A module test programs consist of four parts — identifier, connector, and power statements, and a sequence of test statements. The first three parts perform housekeeping functions that name the program, name the module connector pins, establish 'HI' and 'LO' voltage levels, set positive and negative current limits, and specify positive and negative tolerances for all tests.

The IDENTIFIER statement names the program (usually by the model number of the printed circuit module to be tested) and the type of connection to the system (Module Adapter). For program name 2000 and Module Adapter (MA) 1901, the statement would be:

IDENTIFIER, 2000, MA 1901

The CONNECTOR statement lists all of the module connector pins for the test program. Where there are different types of logic on the same module, the pins are separated into banks according to the test conditions required for each type of logic. This statement *names* the pins. Usually, the pins would be given the same names that are used on circuit schematics and logic diagrams. To assign the labels A, B, and AB to the three pins of bank 1, and the labels D, E, and 27 to the three pins of bank 2, we would write:

CONNECTOR, BANK 1(A, B, AB),/
BANK 2(D, E, 27)

The slash at the end of the first line specifies that the statement is continued on the next line.

The POWER statement specifies the high (H) and low (L) logic levels, the positive (P) and negative (N) current limits, the positive (+T) and negative (—T) comparison tolerances, and the power supply voltages (PS1, PS2, etc.). A complete power statement would be written as follows:

1 POWER, BANK 1(H = 3.0 V, L =/
—3.0 V, P = 7.5 MA, N = 25 MA,/
+T = .75 V, —T = .75 V),/
PS 1 = 4.5 V, PS 2 = —3.0 V

If there were two or more banks, the test parameters for all banks would be specified in the same POWER statement.

If there are two or more POWER statements, the entire test program will be repeated for each POWER state-

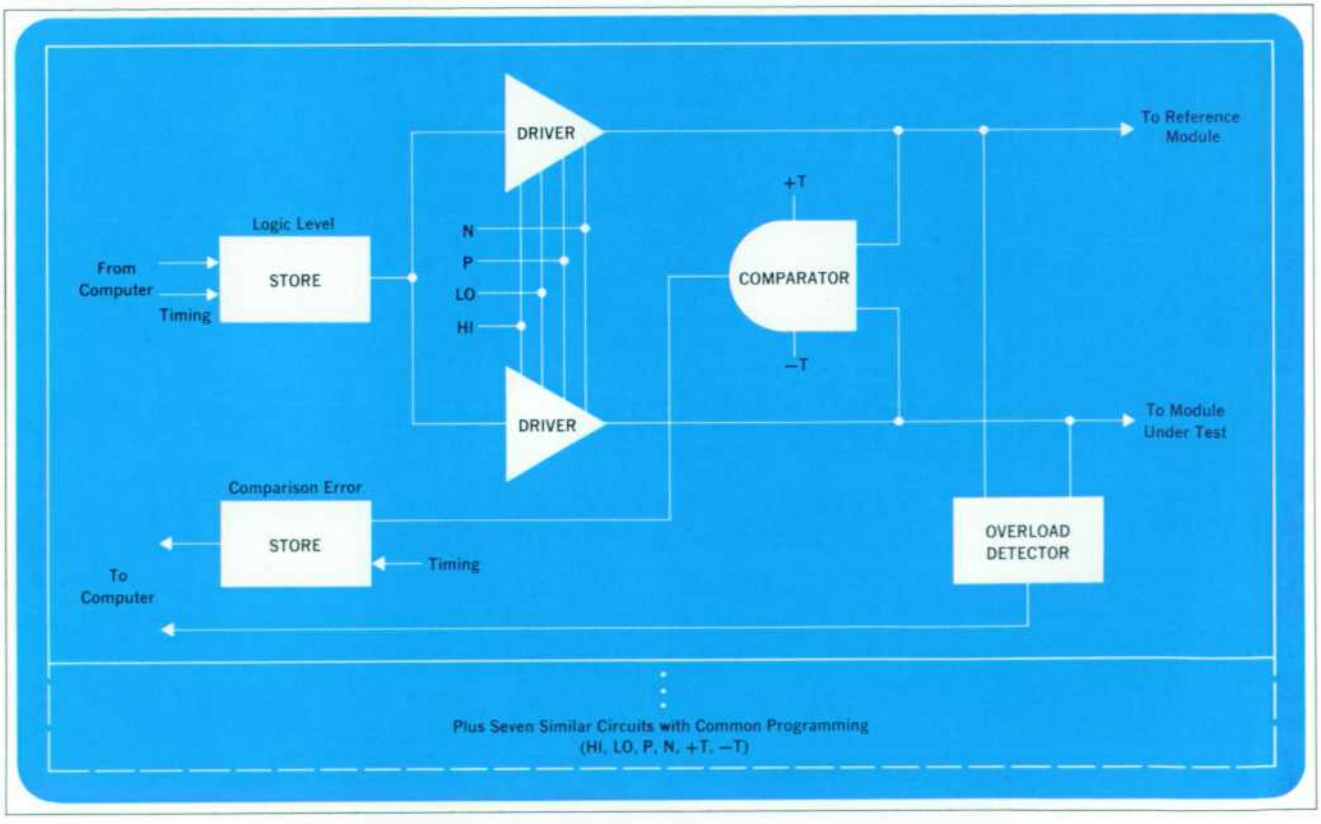

Fig. 3. *The driver/comparator registers are the interface between the modules and the system. They have six programmable parameters: low and high logic levels, source and sink current limits, and plus and minus comparison tolerances.*

ment. Using several POWER statements, the module can be tested under several worst-case conditions, one condition at a time. If a fault occurs, the system will print an error message which includes the number of the power statement that was active when the fault occurred.

The TEST statements can now be written. The first TEST statement should specify initial states for all module signal pins — for example,

2 TEST, L( ), H(A, B, AB, D)

The empty parentheses following L cause all module pins to be set to the low level. Thereafter, the high (H) instruction sets pins A, B, AB, and D to the high level.

The remaining TEST statements exercise the various logic inputs to verify that the responses of the module being tested agree with responses of the reference module. Because all previously specified logic levels are stored by the 2060A System it is only necessary to program the *changes* of input level required for each test. If needed to satisfy module timing requirements, a programmed delay (D) instruction can be inserted between changes of logic level, or preceding comparison.

After all the input combinations required to thoroughly check the module's functioning have been programmed, the test program is terminated by the word END, preceded by a label number.

Only the first character of a statement or an instruction within a statement is required. Thus I or ID can be used for IDENTIFIER, C or CONN can be used for CONNECTOR, P or PWR can be used for POWER, T can be used for TEST, H for HIGH, and so on.

Comments can be inserted in any statement by typing an asterisk (*) at the end of the statement followed by the comment. Comments can explain the purpose of the statements or give other information to a person reading the program. Comments can be continued to the next line by typing a slash (/) at the end of the current line.

Permutations Easily Programmed

The AuTest language provides special help to the test program writer in the form of the DO statement. This statement sets up a 'do' loop that causes actions called for by another statement (or group of statements) to be repeated a specified number of times. When combined with a PERMUTE instruction in a TEST statement, the DO statement can produce up to 65,536 (2^{16}) tests on 16 module connector pins. For example, to exercise all possible high-low combinations to an 8-line code translator with input pins 8, 9, 10, 11, 12, 13, 14, and 15, the programmer can simply write:

```
7 DO, 10, P = 8
10 TEST, PERMUTE/
     (8, 9, 10, 11, 12,/
     13, 14, 15)
```

Thus two program statements do the work of 2^8.

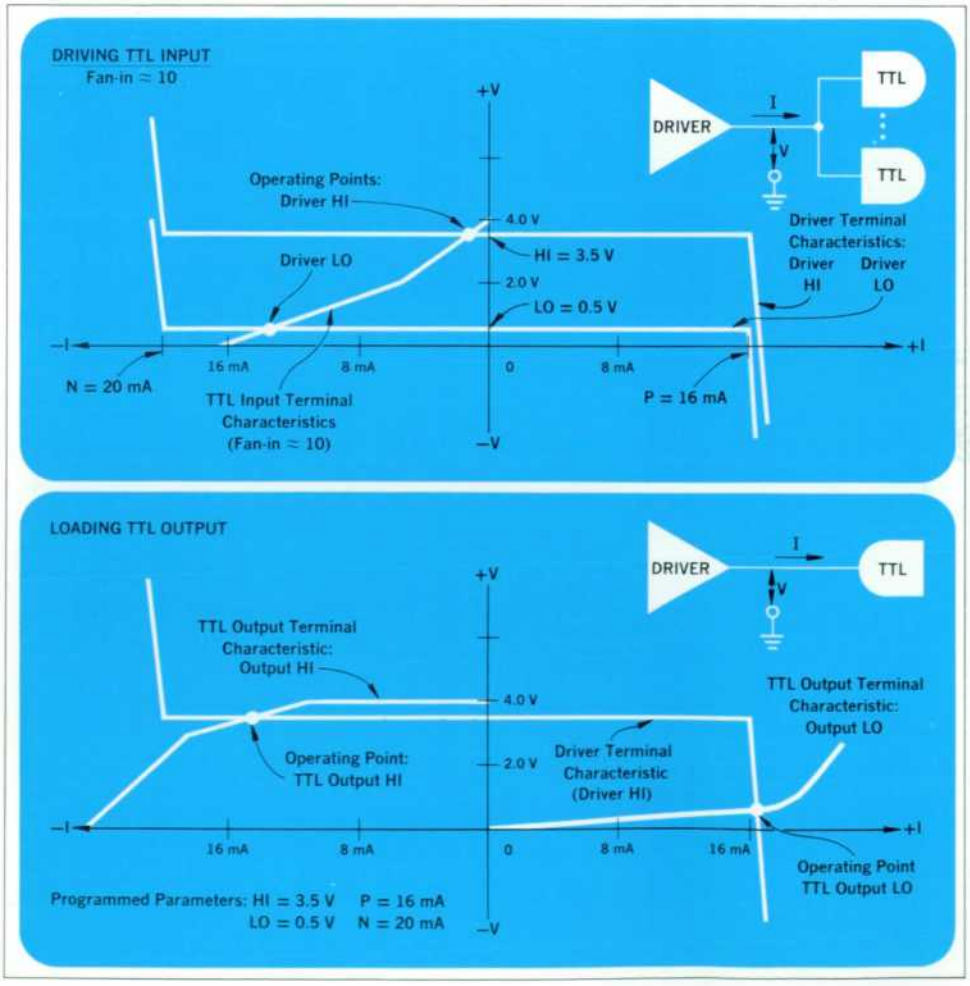

Fig. 4. *The driver circuits can act as input generators, as loads, or as both simultaneously. Thus the system doesn't care whether a particular pin is an input pin or an output pin; the difference is important only in the test program. Here is how a driver circuit works with TTL logic.*

2060A System Commands

Command*	Purpose
NEW	Prepares system to accept a new test program.
TAPE	Read-in of test program by Punched Tape Reader.
KEY	Read-in of test program from Teletypewriter keyboard.
DISC	Read-in of test program, specified by number, from optional Disc Storage Unit. Example: DISC, 2116-6002.
RUN	Starts testing of module.
ERUN	Starts module testing, with request for return to 'conversational' mode following printout of a test fault.
STOP	Stops test program at statement identified by label number, returning System to 'conversational' mode; complete command consists of STOP, followed by label number.
PRINT	Causes printout of currently programmed states (HIGH or LOW) of specified module connector pins. Command consists of PRINT (or PR), followed by list of pins separated by commas; PRINT, followed by line feed causes printout of all connector pin states.
TEST	Establishes conditions specified following the word TEST. Command is like the TEST statement except that there is no label number, TE is required, there is no comparison, permute instruction cannot be used.
CONTINUE	Restarts test program beginning with the next statement to be performed.
INSERT	Inserts one or more labelled statements into the test program.

Command*	Purpose
DELETE	Deletes one or more labelled statements from the test program.
POWER	Permits modification of a parameter or series of parameters in an existing test program power statement.
ABORT	Turns off all power to test and reference modules.
FINISH	Orderly shutdown of System at the end of a day's testing activity.
TIME	Causes printout of total time, test time, and execute time accumulated by System Timer option.
RTIME	Causes resetting to zero of time accumulated by System Timer option.
LIST	Causes printout of current test program on Teletypewriter, from the beginning or starting with a statement whose label number is specified. Example: LIST, 201. The list is an essential starting point for revision of test programs.
PLIST	Causes listing of current test program on paper tape with leader and trailer, for preparing master and duplicate tapes of revised test programs.
SAVE	Causes current test program to be stored by the optional Disc Storage Unit.
CATALOG	Causes Teletypewriter printout of the numbers of test programs in disc storage, followed by the approximate number (rounded to thousands) of words of disc storage capacity remaining.
PURGE	Deletes test program, specified by number, from disc storage. Example: PURGE, 2116-6002.

*Only the first two characters of system commands are required (NE for NEW, CO for CONTINUE, PO for POWER, IN for INSERT, etc.).

Up to three DO statements can be grouped to form a 'nest' of 'do' loops capable of testing the most complicated logical relationships that are likely to be found on any digital logic module. In the example above, statement 7 will cause all statements between 7 and 10 to be repeated for each permutation of the eight binary inputs. Therefore, if for each code combination in the previous example a set of code-dependent responses to inputs C, D, F, and H have to be checked, the program writer could set up two DO loops, one 'nested' in the other as follows:

7 DO, 10, P = 8
8 DO, 9, P = 4
9 TEST, PERMUTE, (C, D, F, H)
10 TEST, PERMUTE (8, 9, 10, 11, 12, 13, 14, 15)

Thus four program statements do the work of 2^{12}.

When a fault occurs during execution of a 'do' loop, the error message tells where in the 'do' sequence the fault occurred.

Help in Troubleshooting

In addition to its basic test and permute capabilities, the AuTest vocabulary includes other statements which can be used to simplify troubleshooting of faulty modules. These are the HALT, WRITE, GO and IF statements.

The HALT statement stops execution of the test program at a specific point. This permits the operator to change jumper connections or switch settings on the module during checkout, or to make in-circuit signal checks if module faults are encountered.

The WRITE statement provides a means for printing comments up to 50 characters long during the execution of the test program. For example, to set up a WRITE-HALT combination to instruct the operator to change jumpers on the test and reference modules, the programmer can write:

126 WRITE, MOVE JUMPERS FROM/
    A TO B, THEN CONTINUE
127 HALT

The operator would read this instruction, then move the jumpers and type CONTINUE.

The GO statement can be temporarily inserted in the test program to assist in debugging a module. This statement causes transfer of control to another statement whose label number is specified. By specifying the label number of a statement that *follows* the GO statement, intervening program statements can be skipped. By specifying the label number of a statement that *precedes* the GO statement, intervening statements can be repeated endlessly to generate signals for oscilloscope display.

The IF statement is like the GO statement in that it causes transfer of control to another statement. The IF statement differs from the GO statement in that it is conditional, becoming effective if a module fault is encountered during execution of the preceding test statement. Because it is conditional, the IF statement can be a permanent part of the module test program. It can be used in combination with GO, WRITE, and HALT statements to give troubleshooting guidance when module faults are encountered.

Other Features

The system automatically checks test programs as they are read in. When a program has to be revised, additional statements can be inserted or existing statements deleted without renumbering other statements. Once read into the system, a program is stored until deleted.

When it is not actually executing a test program, the 2060A System is in a 'conversational' mode, receptive to commands typed on an input keyboard. The commands are listed in the table on page 19.

Acknowledgments

Early in the 2060A project, Stephen C. Vallender took over as project manager and chief of software development. Much of the system's power and flexibility is due to his efforts and those of Thomas G. Ellestad of the software development group. William Miller was responsible for system checkout and project coordination. Anthony M. Tomarchio deserves special credit for the layout of the driver/comparator printed-circuit boards.

William P. Cargile

Bill Cargile studied digital systems at Princeton University, graduating in 1964 with a BSEE degree. He joined HP the same year. Since then he has developed data acquisition systems, a data multiplexer, computer input/output interfaces, and other computer hardware, as well as the 2060A Digital Logic Module Test System. He has two patents pending. Now project manager for the HP 2114A Computer, Bill is working towards his MS degree in electrical engineering and computer science at Stanford University.

SPECIFICATIONS

HP Model 2060A
Digital Logic Module Test System

SYSTEM CAPACITY

NUMBER OF MODULE CONNECTOR PINS
Basic capacity of 16 pins may be expanded in 8-pin increments to a maximum of 256 pins.

NUMBER OF BANKS
Basic capacity of one bank (set of module connector pins subject to a common set of logic parameters) can be expanded to a maximum of four banks.

TEST SPEED

MAXIMUM SPEED
10,000 tests per second per pin with no delays programmed.

AVAILABLE DELAYS
8.0 μs to 9.999 seconds, programmable in 3.2 μs increments.

DC POWER TO MODULES

The supplies listed can be provided in any combination in the system's initial configuration—and the 'mix' or total number of supplies can be changed at any time.

AVAILABLE VOLTAGE-CURRENT COMBINTIONS
0 to ±7.5 V at 5A, programmable in 0.05 V increments.
0 to ±20 V at 3A, programmable in 0.1 V increments.
0 to ±40 V at 1.5A, programmable in 0.2 V increments.

OUTPUT VOLTAGE ACCURACY
Within 0.025 V ±3% of programmed voltage.

LOGIC PARAMETERS

With Low Impedance Driver-Comparator

HIGH LOGIC LEVEL
More positive than Low, programmable in 0.1 V increments from −5.9 V to +6 V.

LOW LOGIC LEVEL
More negative than High, programmable in 0.1 V increments from +5.9 V to −6 V.

LOGIC LEVEL ACCURACY
Within 0.2 V ±5% of programmed level.

POSITIVE & NEGATIVE CURRENT LIMITS ($\pm I_{LIM}$)
Programmable in 1 mA increments from 2 mA to 50 mA.

CURRENT LIMIT ACCURACY
Within 1 mA ±5% of programmed limit.

SLEWING RATE (APPROXIMATE)
100 V/μs or (4 × I_{LIM})V/μs if smaller.

APPROXIMATE OVERLOAD DISCONNECT VOLTAGE
±7.5 V or more at any module connector pin triggers turn-off of power to protect Driver-Comparators and modules.

INTERNAL LOAD
10kΩ to ground at each I/O pin.

With High Impedance Driver-Comparator

HIGH LOGIC LEVEL
More positive than Low, programmable in 0.2 V increments from −17.8 V to +18 V.

LOW LOGIC LEVEL
More negative than High, programmable in 0.2 V increments from +17.8 V to −18 V.

LOGIC LEVEL ACCURACY
Within 0.5 V ±5% of programmed level.

POSITIVE & NEGATIVE CURRENT LIMITS ($\pm I_{LIM}$)
Programmable in 0.1 mA increments from 0.2 mA to 15 mA.

CURRENT LIMIT ACCURACY
Within 0.1 mA ±5% of programmed limit.

SLEWING RATE (APPROXIMATE)
40 V/μs or (4 × I_{LIM})V/μs if smaller.

APPROXIMATE OVERLOAD DISCONNECT VOLTAGE
±20 V or more at any module connector pin triggers turn-off of power to protect Driver-Comparators and modules.

INTERNAL LOAD
50 kΩ to ground at each I/O pin.

COMPARISON PARAMETERS

POSITIVE and NEGATIVE TOLERANCES
Programmable in 0.05 V increments from ±0.05 V to ±5 V.

TOLERANCE ACCURACY
With Low Impedance Driver-Comparator: Within 0.05 V ±5% of programmed tolerance.
With High Impedance Driver-Comparator: Within 0.1 V ±5% of programmed tolerance.

SYSTEM CONFIGURATION

BASIC SYSTEM
General-purpose computer acts as system controller, providing 8,192-word memory for test system software and test programs and 16 I/O slots for Teletypewriter, High-Speed Tape Reader, Relay Output Register, and Driver-Comparator Register cards.
300 character-per-second punched tape reader assures fast read-in of test programs.
Heavy duty teletypewriter serves as the communication link between the operator and the system.
Quick-change adapter connects test and reference modules to the system.
Two Driver-Comparator Registers each drive and check eight module connector pins.
Relay Output Registers program power supplies to establish logic parameters for one group of module connector pins.
Programmed power supplies provide logic parameters for one group of module connector pins.

SYSTEM EXPANSION

I/O Extender adds 32 I/O slots for additional Driver-Comparator and Relay Output Registers.
Up to 32 Driver-Comparator Registers for testing modules with up to 256 connector pins.
Additional Relay Output Registers and power supplies for expanding the system to provide up to four different sets of logic parameters simultaneously.
Additional adapters for checking different types of modules.
Additional Teletypewriter for off-line preparation of test program tapes.
Oscilloscope and voltmeter for isolating module faults.
120 character-per-second tape punch for fast preparation of revised master and duplicate test program tapes (Teletypewriter operates at 10 characters per second.)
System time option for logging total system operating time, total test time, and total test program execution time.
Disc Memory for convenient storage and fast change of test programs (saves reading in program tapes).
Data Acquisition Subsystem (scanner and digital voltmeter for measurement and printout of absolute voltages) where periodic self test capability is required.

SOFTWARE

Every 2060A System comes with a ready-to-use AuTest software package that generates desired test conditions and test sequences from module test programs written entirely in English and decimal numbers. Software accommodates all expansions and options.

PRICE: Basic 2060A System, **$80,000.00.**

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