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Atlanta Fiber System Experiment:

Practical 45-Mb/s Regenerator for Lightwave Transmission

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A 45-Mb/s optical regenerator using an avalanche photodiode and a GaAlAs injection laser has been designed for a field environment. Its design and performance are described here. Feedback control of the optical transducers permits operation over a temperature range of 0 to 60°C. The regenerator has simple power requirements, and optical connectors permit easy installation. Its input sensitivity and output power makes useful regenerator spacings possible with currently available optical fiber. The large AGC range permits a wide range of regenerator spacings. A novel phase-locked loop design achieves a wide pull-in range for the timing recovery circuitry.

I. INTRODUCTION

An optical regenerator* is essentially a digital regenerator with optoelectronic transducers at the input and output. The transducers used here are an avalanche photodiode and a GaAlAs injection laser. The regenerator includes the usual features of amplification, filtering, automatic gain control, retiming, and regeneration. Some features peculiar to a design for a lightwave transmission system are very high gain and wide dynamic range. Also, the characteristics of the transducers must be stabilized with feedback.

The optical regenerator described here is the prototype of a design for a field environment. The intended transmission medium is low-loss graded-index fiber.[1,16] The regenerator was initially used in the Atlanta Experiment, a study of a lightwave transmission system in an environment simulating field conditions.[2]

* A regenerator is a one-way repeater.

The feasibility of an optical regenerator operating at a data rate of 45 Mb/s has already been shown.[3] The objective here is a practical regenerator with simple power requirements, operation over a temperature range from 0° to 60°C, wide dynamic range, practical optical connectors, and a design that could be manufactured by present methods.

The selected data rate was 44.736 Mb/s, the DS3 level of the Bell System digital hierarchy. This rate makes use of the wide bandwidth of the fiber without incurring significant penalty from fiber dispersion. The signal format is binary nonreturn-to-zero* with scrambling to insure adequate balance and timing information.

The optical regenerator was constructed in three separate modules, as shown in Fig. 1. This design relaxed the requirements on size and isolation in order to focus effort on the requirements mentioned above. It also allowed the modules to be used for terminal regenerators. The functions performed in each module are shown in Fig. 2. The receiver module accepts an optical signal as low as −55 dBm at its optical connector and produces a 1-V p-p electrical output signal. The decider module extracts timing and regenerates the signal. The transmitter module converts the regenerated electrical signal to a regulated optical signal and couples a minimum of −3 dBm of average power into an optical connector.

Notice that the optical connectors[4] on the receiver and transmitter are designed to engage when electrical connection is made to the module. Electrical test points are brought to the face of each module.

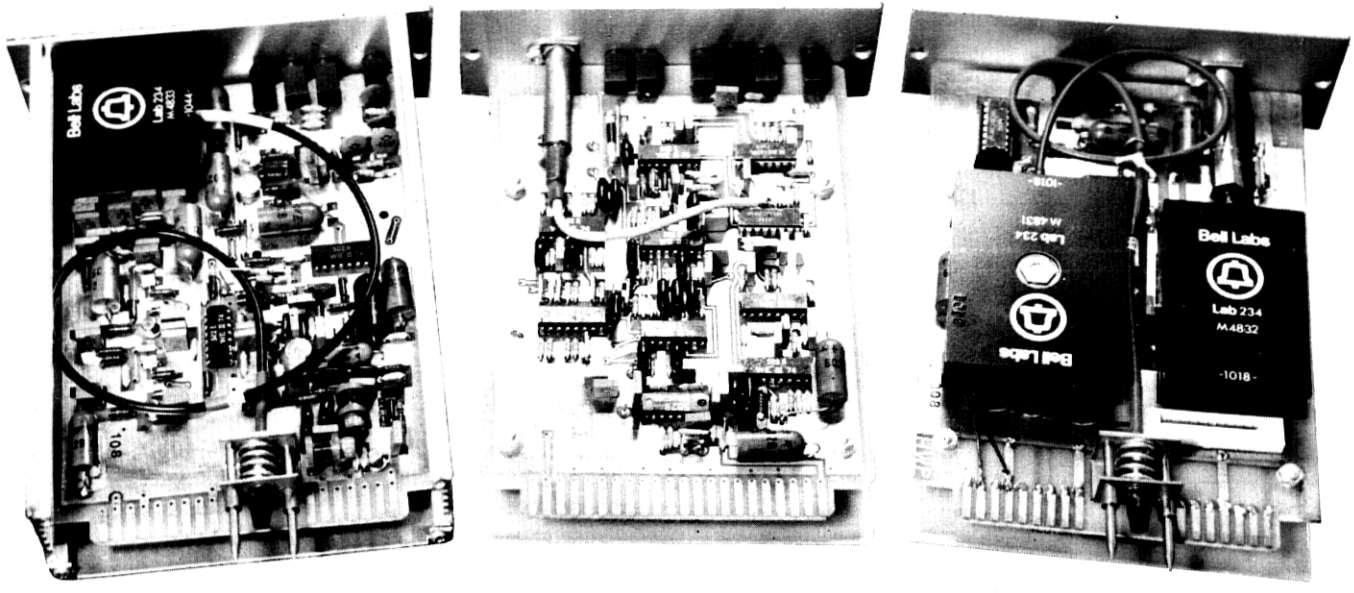
The remainder of the paper describes the operation of the three modules. The regenerator performance reported is based on the measurement of 15 regenerators.

II. RECEIVER

The receiver module comprises the linear channel of the regenerator. It converts the received optical signal to an electrical signal and maintains a constant output by automatic gain control (AGC). The dispersion of the glass fiber medium is small enough that the receiver does not need to equalize for it. However, filtering is done to limit the noise. The circuit in Fig. 3 shows the functions performed in the receiver.

Special care was needed in the layout, shielding, and bypassing for this module. (Most of the bypassing is not shown in Fig. 3 to simplify the drawing.) Signal currents differing in level by 90 dB are present in the circuit.

* Light on corresponds to a logical "one"; light nominally off is a logical "zero."



RECEIVER MODULE DECIDER MODULE TRANSMITTER MODULE

Fig. 1 — Optical regenerator. Each module is 6.5 × 4.5 × 1.5 in.

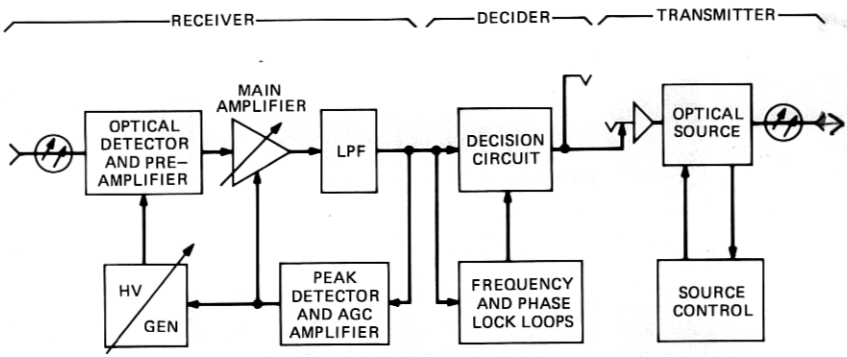


Fig. 2 — Optical regenerator.

2.1 Photodetection

The optical signal is detected by an avalanche photodiode (APD) capable of providing current gain in the range from 6 to 120. The dependence of the gain on the bias voltage is shown in Fig. 4. The bias, supplied by the dc-to-dc converter, can be varied from −150 to −420 volts by the p-n-p transistor loading down the converter's output. Zener diodes limit both the maximum and minimum voltages applied to the APD. The voltage limitation prevents excessive burst noise or damage that can occur at high voltages. It also avoids the slow APD response at low voltages.

The small current from the APD is amplified by a transimpedance preamplifier located in the same shielded package with the APD. The noise figure is not so low as that of a high-impedance preamplifier,[5,6] but the sacrifice in sensitivity is only 1 dB. The advantages of a transimpedance preamplifier are greater dynamic range and no equalization required.[7] Further details of the ADP and preamplifier performance are given by the designers and builders of the detector package in Ref. 8.

A useful measure of the received optical power level is the detected power $\eta\overline{P}$. This is the product of the average power $\overline{P}$ available at the optical connector and the combined efficiency η of the connector, pigtail, and APD.* The detected power $\eta\overline{P}$ is conveniently obtained by measuring the APD current for a known gain. For light of wavelength 825 nm, the perfect conversion to primary photocurrent would be 0.67 ampere per watt of optical power.

For a given error rate, an optimum APD gain will minimize the required optical power $\eta\overline{P}$. The optimum gain for 10^{-9} error rate was determined experimentally to be 80, and the receiver is aligned to realize this condition. The required $\eta\overline{P}$ is about −55 dBm.

The measured curve of error rate versus $\eta\overline{P}$ for a typical regenerator is shown in Fig. 5. For this range of low $\eta\overline{P}$, the APD gain was adjusted

* The efficiency η was measured to be about −1.5 dB.

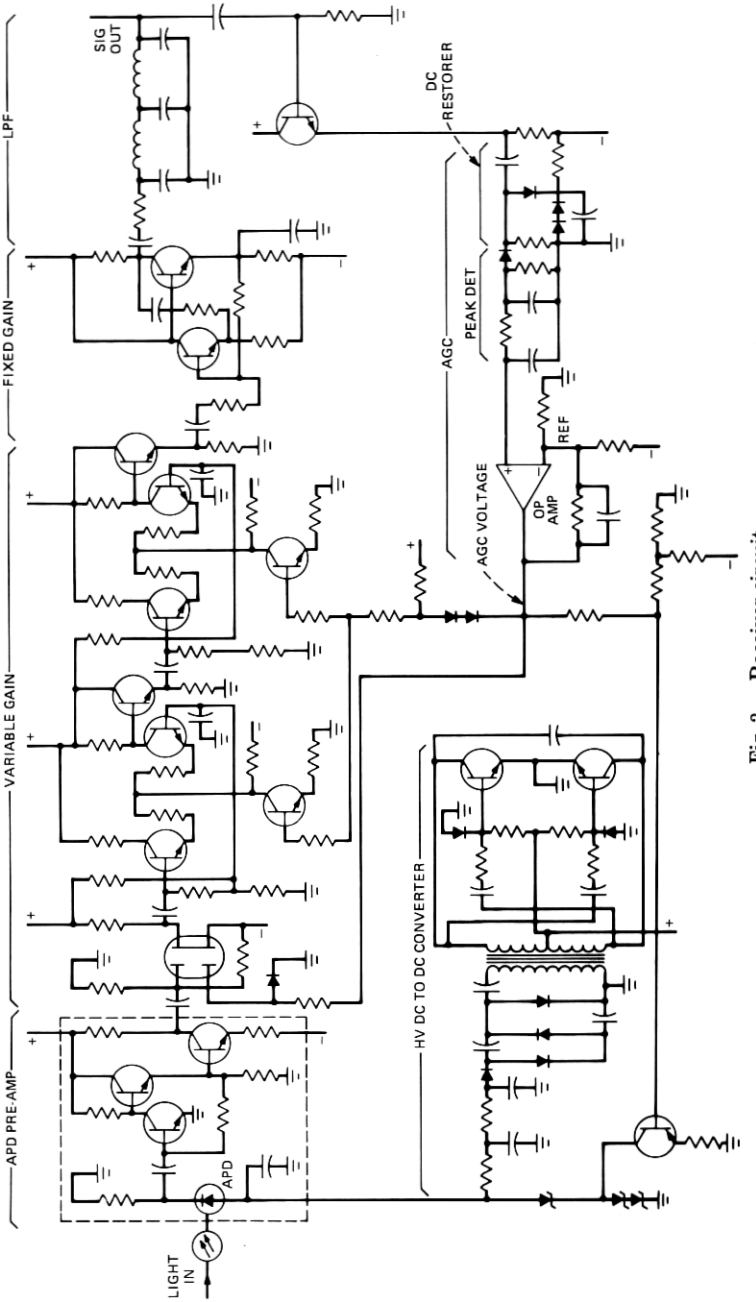


Fig. 3 — Receiver circuit.

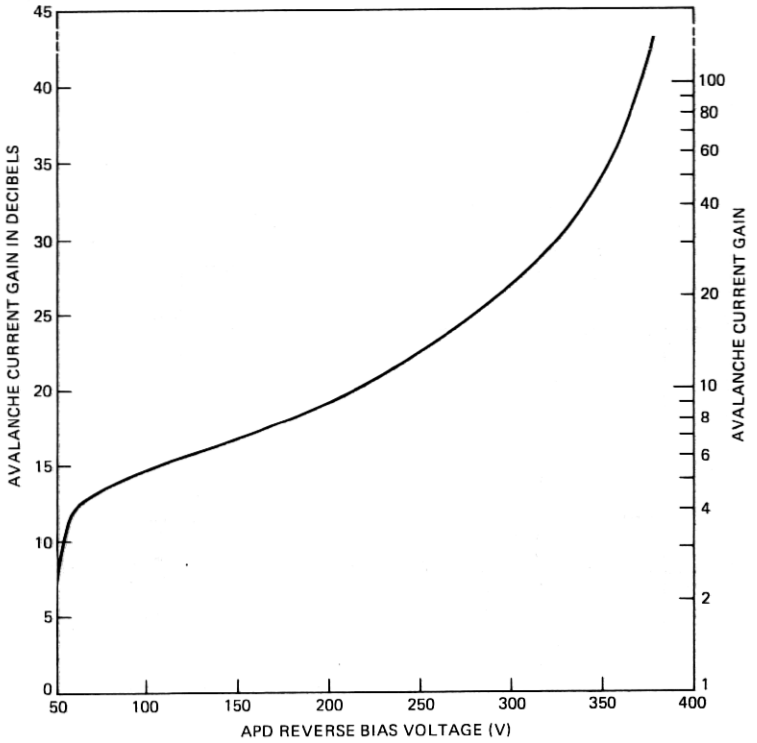


Fig. 4 — Avalanche photodiode gain characteristic.

by the AGC to maintain a constant output signal level. The performance of the regenerator is considered to be useful to an error rate of 10^{-6}, corresponding to a detected power $\eta\overline{P}$ of about −57 dBm and an APD gain of 120. (Burst noise can begin to occur at gains greater than 120.)

2.2 Main amplifier

The main amplifier consists of a variable-gain amplifier, a fixed-gain power amplifier, and a low-pass filter to limit noise.

The first stage of the variable-gain amplifier is a dual-gate FET. This device accepts a large signal input without distortion and achieves a gain variation of 20 dB. Each of the following two stages is an emitter-coupled pair with a gain variation of 14 dB. The fixed-gain amplifier provides a 2-V p-p signal to the low-pass filter. The signal at the output of the filter is maintained at 1-V p-p by the AGC.

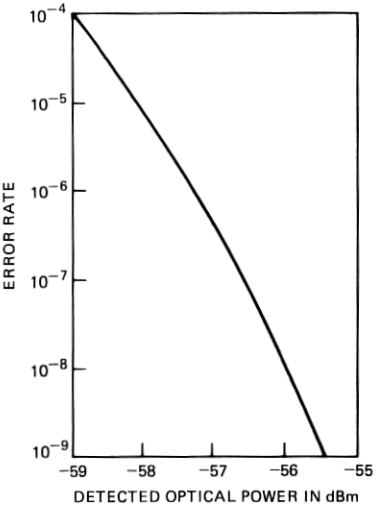


Fig. 5 — Error rate versus detected optical power.

2.3 Automatic gain control

The level of the output signal is monitored by a peak detector and compared against a reference by a comparator with a gain of 125. The peak detector includes a low-pass filter with a cutoff frequency of 0.12 Hz. The "AGC voltage" at the output of the comparator controls gain of both the APD (by varying the bias voltage) and the main amplifier.

Table I lists these gains and their ranges; 26 dB range for the APD and 48 dB for the main amplifier. Thus, the total AGC range is 74 dB. Note this is twice the 37-dB range indicated for the corresponding detected power $\eta\overline{P}$, since the APD is a square-law detector. The ranges indicated are the maximum for linear operation. $\eta\overline{P}$ can be extended 5 dB higher without incurring significant closing of the "eye."

If the APD and the main amplifier are in the active parts of their AGC ranges simultaneously, interaction and oscillation are possible. Therefore, the AGC is designed so their ranges do not overlap. For low detected power ($\eta\overline{P} < -44$ dBm) the APD gain is varied, and the main amplifier gain is at maximum (see Fig. 6). This maximum gain is accurately set, and the AGC acts to stabilize the APD gain over temperature as well as to accommodate changes in the detected power.

Table I — Receiver gains and levels

	Min.	Max.	Range
Detected power $\eta\overline{P}$	−57 dBm	−20 dBm	37 dB
APD current gain	6 (15.6 dB)	120 (41.6 dB)	26 dB
APD output (average)	0.16 μA	40 μA	
Preamp transimpedance	14 kΩ		
Preamp output	4.5 mV p-p	1120 mV p-p	
Main amplifier gain	−1 dB	47 dB	48 dB
Receiver output	1.0 V p-p		

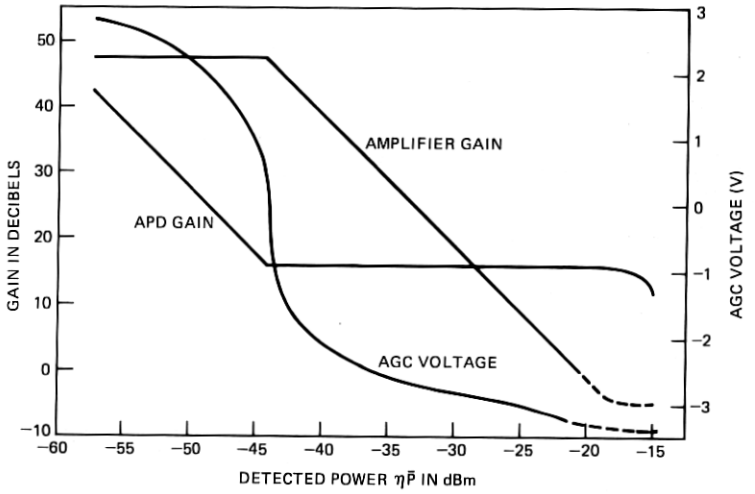


Fig. 6 — Receiver automatic gain control.

For $\eta\bar{P} > -44$ dBm, the main amplifier gain is varied, and the APD is at minimum gain. The value of the AGC voltage over the range is also shown in Fig. 6. The change in gain with AGC voltage is greatest at the extremes—about 30 dB/V, corresponding to an open-loop gain of 430 and a closed-loop bandwidth of 52 Hz.

2.4 Linear channel response

The low-pass filter at the output of the receiver shapes the frequency response of the linear channel to limit noise without introducing much intersymbol interference in the 44.7-Mb/s signal. An optimum design minimizes the detected power required for a given error rate. The filter used here introduces a complex pole pair at $24 \pm j38$ MHz and at $76 \pm j12$ MHz, and a real pole at 58 MHz. Roll-off due to parasitics in the linear channel can be modeled by two additional poles—one at 46 MHz and one at 54 MHz. This filter gives performance within 1 dB of the optimum design.[9]

The measured high-frequency roll-off of the linear channel is shown in Fig. 7. From this, the effective noise bandwidth is calculated to be 33.7 MHz. The low-frequency roll-off due to coupling capacitors is shown in Fig. 8. Cutoff is at about 650 Hz.

A single detected light pulse at the input can be modeled by a trapezoid with rise and fall times of 3 ns. The time response of the linear channel to this pulse was calculated by fast Fourier transform from the measured frequency response (see Fig. 9). Note that the time response is a little too narrow, reflecting the fact that the low-pass filter design is not the optimum. The measured eye pattern is shown in Fig. 10.

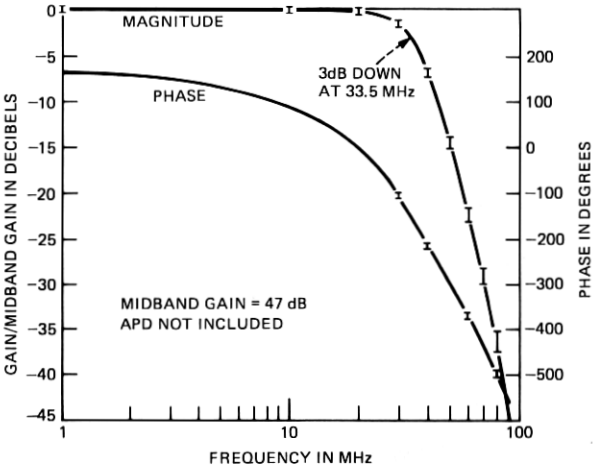


Fig. 7 — Receiver high-frequency electrical gain characteristic.

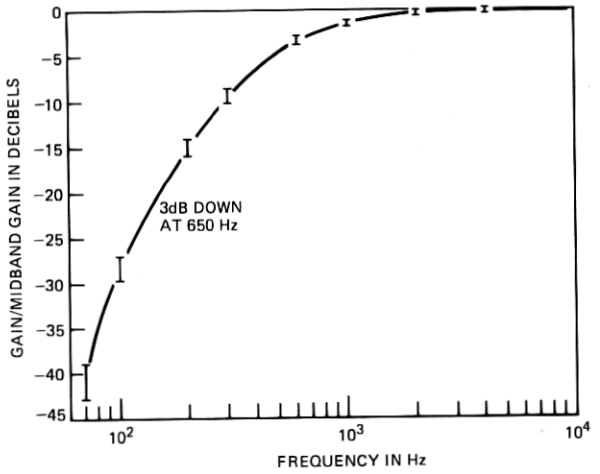


Fig. 8 — Receiver low-frequency electrical gain characteristic.

III. DECIDER

The decider module includes a decision circuit that samples the signal from the receiver and generates a logic-level output signal. The timing of sampling and of logic transitions is controlled by a clock recovered from the receiver output. A narrowband phase-locked loop is used to recover the timing. A circuit diagram of the decider is shown in Fig. 11.

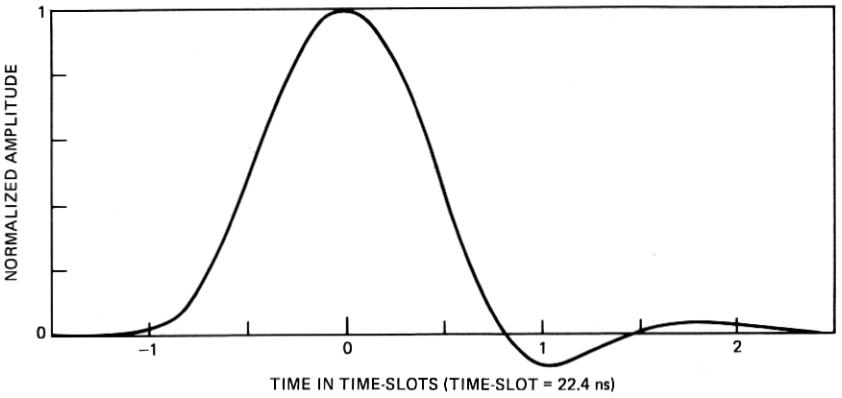


Fig. 9 — Nominal linear channel pulse response.

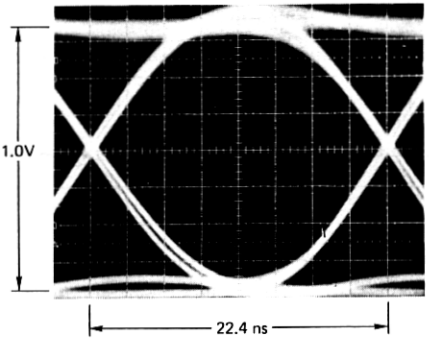


Fig. 10 — Typical eye pattern (receiver output).

3.1 Decision circuit

The decision circuit compares the SIGNAL IN with a threshold and decides, at sampling times determined by the recovered clock, whether the signal is "high" or "low." In a lightwave system, the signal is not symmetric; the high (light on) state has more noise associated with it than the low (light off) state.[6] For this reason, the optimum threshold is not at the center of the "eye" (0 V with ac coupling), but closer to the low state. A typical plot of error rate versus threshold is shown in Fig. 12. For the 1-V p-p eye, the optimum threshold averages about −70 mV.

Error rate is plotted as a function of the sampling time in Fig. 13. For timing within ±1.3 ns (±20.5 degrees), about the optimum, the error rate is not even doubled. The measured timing variation from circuit to circuit at room temperature is ±18 degrees. The stability of a timing recovery circuit over a range of 65°C is ±2.5 degrees with temperature compensation. This compensation (not shown in Fig. 10) consists of a thermistor in the load of the PLL phase comparator. (Without compensation, the variation would be ±10 degrees over a temperature range of 65°C.)

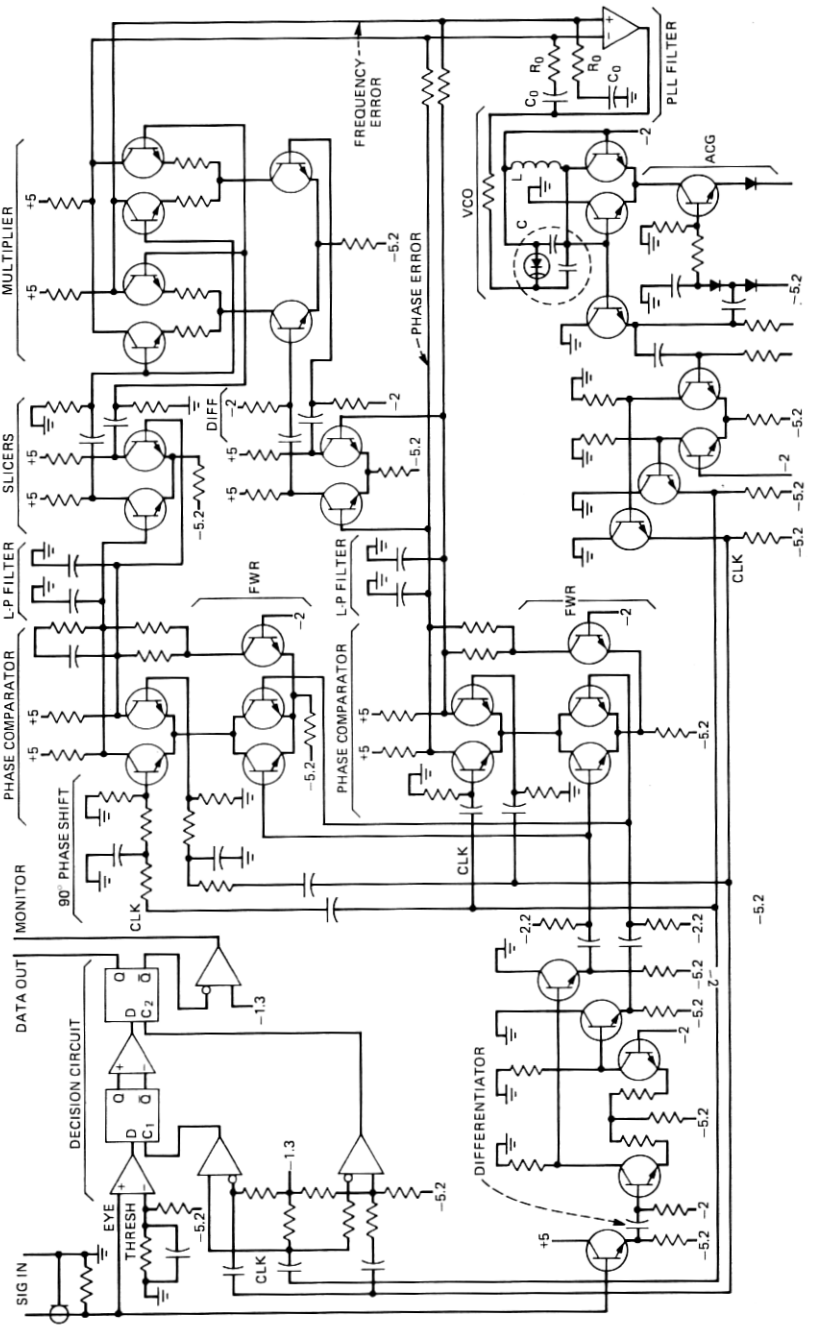


Fig. 11 — Decider circuit.

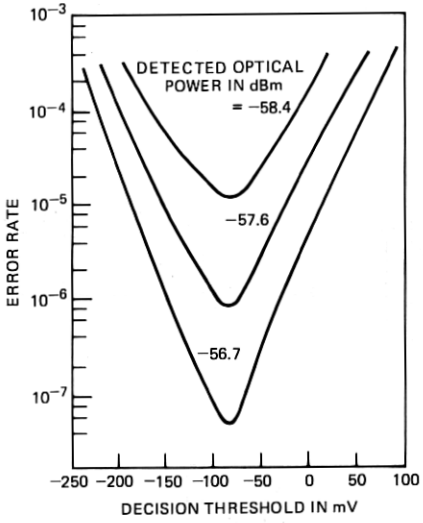


Fig. 12—Error rate versus decision threshold. Logic "1" = +500 mV; logic "0" = −500 mV.

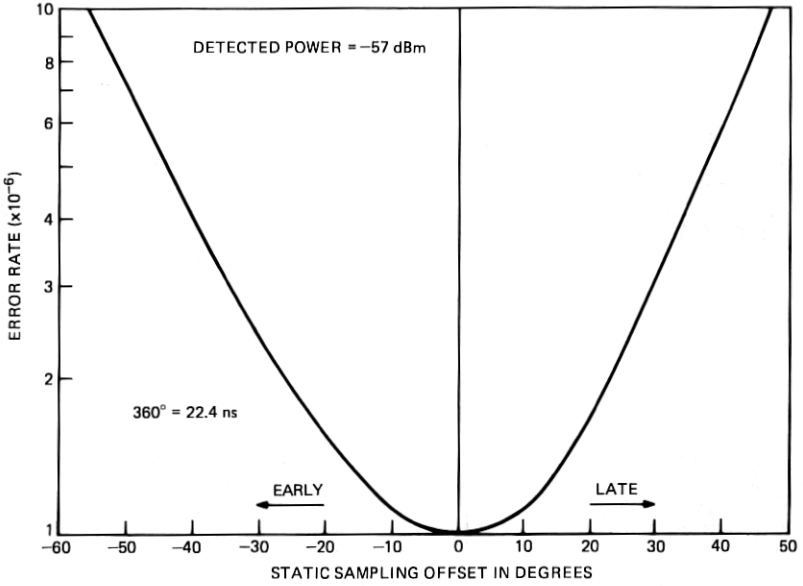


Fig. 13 — Error rate dependence on sampling time.

The decision circuit is a commercial integrated circuit MC1650 connected as a master-slave D-type flip-flop. As shown in Fig. 14, the first stage samples the SIGNAL IN when C_1 goes low, timed to be at the center of the eye. The second stage resamples to prevent feedthrough while C_1 is high. If the eye is sufficiently open to eliminate decision errors, the

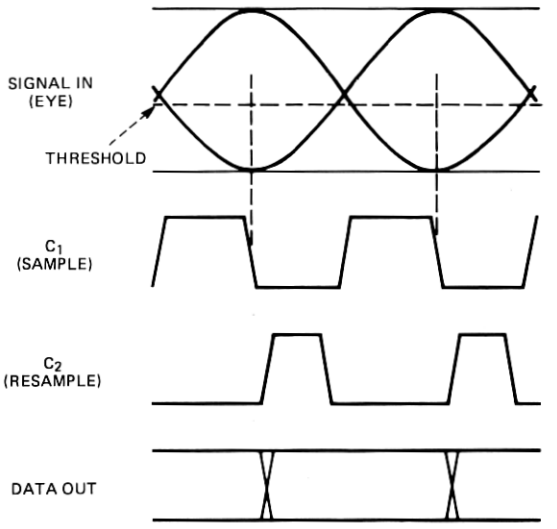


Fig. 14 — Decision circuit waveforms.

DATA OUT will be a logic-level version of the lightwave signal originally transmitted.

3.2 Timing recovery

The information for timing recovery is in the transitions of the SIGNAL IN (see Fig. 15). After some preprocessing of the signal, a local oscillator is locked to the transitions by a second-order phase-locked loop (PLL). The PLL, with a 3-dB bandwidth 1/1200 of the baud, limits the amount of timing jitter in the recovered clock. The pull-in range of the PLL is extended by a frequency comparator, permitting use of a low-tolerance (and inexpensive) oscillator.

3.2.1 Signal preprocessing

It is possible for low-frequency components of SIGNAL IN to cause timing jitter. Therefore the signal is high-pass filtered by a 60-MHz pole (approximating a differentiator); the information of the high-speed transitions is retained. See Fig. 15 for waveforms.

The signal is then processed by a full-wave rectifier (with dead zone) to produce a line in the frequency spectrum at the baud. The output of the full-wave rectifier is a series of current pulses corresponding to the transitions of SIGNAL IN.

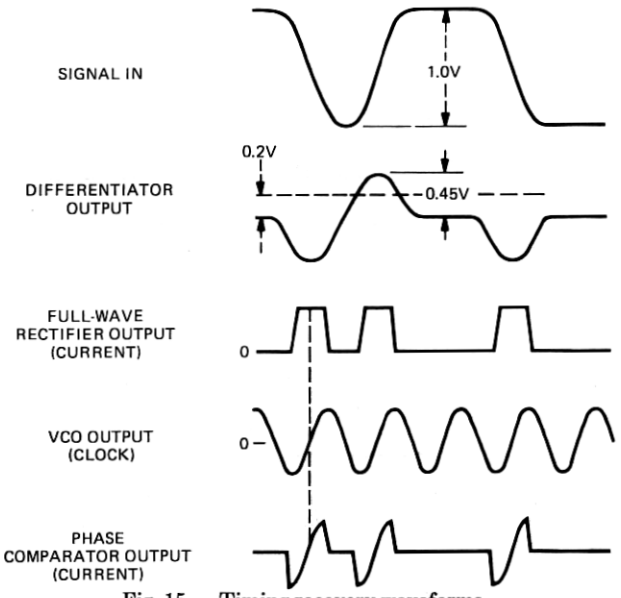


Fig. 15 — Timing recovery waveforms.

3.2.2 Phase-locked loop

The PLL comprises a phase comparator, a low-pass filter, and a voltage-controlled oscillator (VCO). Its input is the series of current pulses from the full-wave rectifier, and its output is the clock used by the decision circuit for sampling.

The phase comparator multiplies the clock by the PLL input, developing an average current proportional to their phase difference (for differences less than about 60 degrees). When the relative phase is zero, as shown in Fig. 15, the average output current is zero. The maximum average differential output of about 35 μA corresponds to a relative phase of 90 degrees.

The transfer function of the filter is $(1 + sC_0R_0)/sC_0$, where $C_0R_0 =$ 1 ms. Since the gain of the filter at dc is very great, offset of the center frequency of the VCO has a negligible contribution to the static phase offset of the clock.

An undesired differential offset current as large as 7 μA can appear at the input to the filter, causing up to 12 degrees static offset. It also causes the VCO frequency to drift when the PLL input signal is removed. If the input signal is interrupted for too long, the frequency drifts beyond the seize range of the PLL, and recovery time will be long. To assure seizure, the interrupt time must satisfy

$$\tau_i \leq R_0C_0\, I_{pc}/I_0 = 5 \text{ ms},$$

where I_{pc} is the current corresponding to a phase difference of 90 degrees,

and I_0 is the maximum offset current. When this is satisfied, measured recovery times are about 20 μs.

The voltage-controlled oscillator (VCO) has a center frequency of about 44.7 MHz. Its frequency can be varied over a range of ±10 percent according to the bias voltage applied to a varactor diode by the PLL filter. The VCO includes an AGC to maintain a 1.2-V p-p output.

The VCO is inexpensive because high stability is not required. As the power supply voltages vary over a range of ±10 percent, the VCO frequency varies by ±2 percent. As the temperature varies over a range of 65°C, the VCO frequency varies by ±1 percent. For nominal conditions, the frequency stays within ±2 percent from circuit to circuit. Therefore, the worst-case offset of the VCO over all conditions is ±5 percent. This is well within the control range of ±10 percent.

The nominal, closed-loop, 3-dB bandwidth f_0 of the PLL is 37 kHz. The noise bandwidth is $(\pi/2)\, f_0$. Due to variations in the gains of the phase comparator and VCO, f_0 was as low as 21 kHz and as high as 70 kHz for different circuits. The open-loop zero at 160 Hz introduced by the PLL filter causes up to 0.06-dB peaking in the closed-loop response.[10,11]

Since the phase comparator has a sinusoidal characteristic, the seize frequency f_s of the PLL equals its f_0 bandwidth.[12] The pull-in range of the unaided PLL is dependent on the offset current and can be as small as 55 kHz, or only 0.12 percent of the band.[12] This will not cover the ±10-percent control range of the VCO and the ±5 percent tolerance of the VCO; a pull-in range of at least ±15 percent is needed.

3.2.3 Frequency comparator

The pull-in range of the timing recovery circuit is extended to ±20 percent by a frequency comparator. The scheme was suggested by Bellisio[13] and is similar to an earlier proposal by Richman.[12] The additional circuitry needed consists of the second phase comparator, the low-pass filter, the slicers, and the multiplier shown at the top of Fig. 11.

The clock delivered to the second phase comparator is delayed 90 degrees from that delivered to the one in the PLL. When the PLL is out of lock, there is a beat note at the output of each phase comparator, and the two beat notes are 90 degrees out of phase. Which one is ahead in phase depends on the sign of the clock frequency error. The beat notes are squared up by slicers, and one of the square waves is differentiated to produce alternating positive and negative pulses. The product of the pulses with the other square wave is a train of either positive or negative pulses, depending on the sign of the frequency error. These current pulses are summed with the phase-error current at the input to the PLL filter and cause the PLL to pull in to its seize range. With the PLL in its seize range, the pulses cease and the PLL behaves as if there were no auxiliary pull-in circuitry.

The pull-in rate is proportional to the frequency comparator's average output current, which is plotted as a function of frequency difference in Fig. 16. The curve is linear near the origin. As the period of the difference frequency approaches the width of the current pulses, the curve falls off from the ideal, but it retains the right sign to beyond a frequency difference of ±20 percent.

The pull-in time is dependent on the difference between the initial VCO frequency and the baud. Figure 17 shows measured pull-in times for a typical circuit. Pull-in from a 10-percent frequency difference takes less than 50 ms.

3.2.4 Timing jitter

A regenerator retimes the phase of the data it transmits, but it can also introduce some jitter in the phase. Noise causes random jitter, and data dependence of the timing recovery circuit causes systematic jitter.

In a line of regenerators, this jitter accumulates and may become a problem for the terminal circuits. Each regenerator adds a certain amount of random and systematic jitter, characterized by the jitter power densities $\Phi_R(f)$ and $\Phi_S(f)$, respectively. (The unit of the "power" density is degrees^2/Hz.) The spectra can be considered, for all practical purposes, to be flat and equal to $\Phi_R(0)$ and $\Phi_S(0)$.

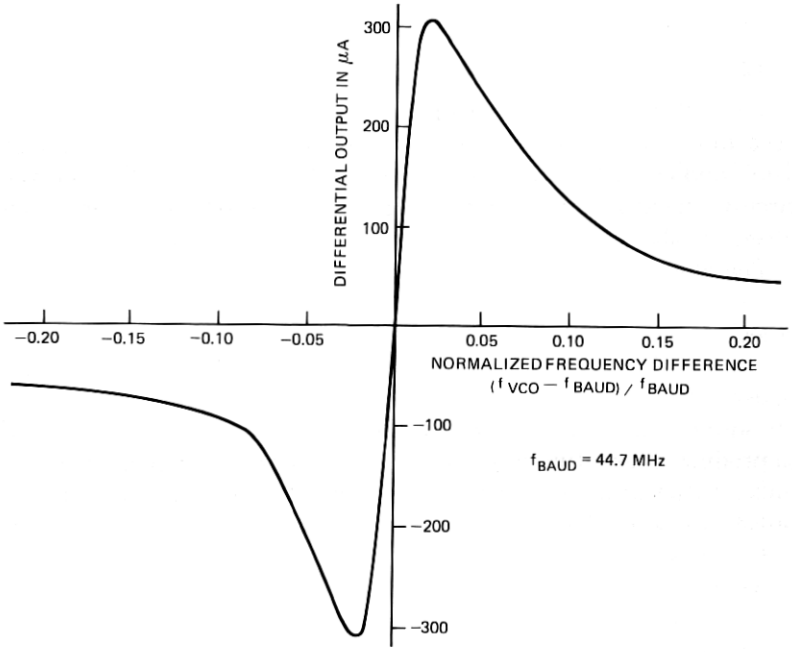


Fig. 16 — Typical frequency comparator characteristic.

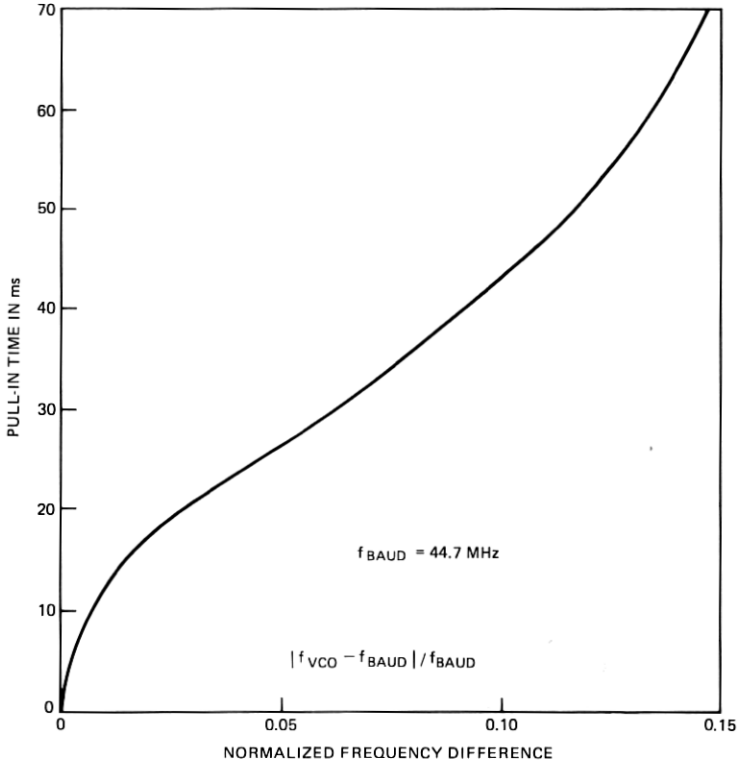


Fig. 17 — Typical pull-in times with aid of frequency comparator.

The accumulated jitter was measured for a line of 14 regenerators.[2,14] From this data the worst-case $\Phi_S(0)$ was calculated to be 33 degrees^2/MHz. This would correspond to 19 degrees rms of accumulated jitter for a line of 50 regenerators. The effect of $\Phi_R(0)$ was negligible.

IV. TRANSMITTER

The transmitter module accepts an ECL data signal and provides the data as an optical output from a fiber pigtail. The light source is a GaAlAs injection laser with an emission wavelength of 825 nm. Circuitry is included to monitor the laser output level and regulate it over time and temperature. A more complete description of the transmitter module is given by its designers and builders in Ref. 15.

A circuit diagram of the transmitter is shown in Fig. 18. When a positive-going pulse is present at DATA IN, the driver circuit applies a current pulse of about 35 mA to the laser, bringing it from below to above the lasing threshold. The pulses ride on top of a prebias current which improves switching speed and avoids chattering or oscillation of the light output.

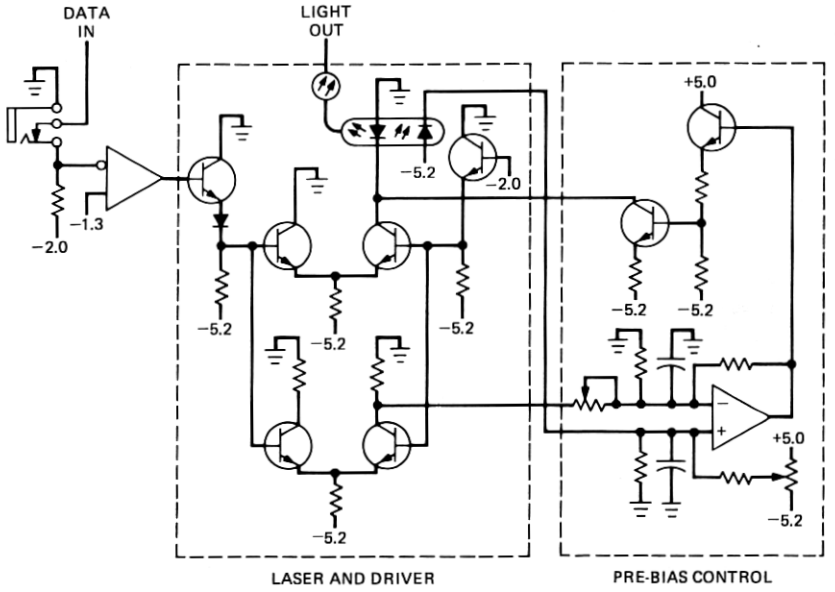


Fig. 18 — Transmitter circuit.

Through a feedback circuit, the prebias current is automatically established at a value required to maintain the light output of the laser constant. This circuit eliminates the changes in light output that would occur from changes in the threshold due to temperature and aging. As part of this control circuit, a pin photodiode senses the light output from the back face of the laser. The pin output correlates closely with the average light collected by the fiber pigtail at the other face of the lasing cavity. By deriving a reference from the DATA IN signal, the control is insensitive to the "ones" and "zeros" density in the data. At 25°C, the prebias current is typically about 100 mA, and at 50°C it is about 115 mA.

The varying density of "ones" in the data causes short-term heating and cooling of the laser. As a result, the laser output level varies at a rate faster than the response of the feedback control. Lasers are used that have a pattern dependence of the peak output power below 8 percent peak-to-peak.

For a balanced data signal, the average optical power available from the fiber pigtail is at least −3 dBm. The output power corresponding to a "one" is about 15 times that for a "zero."

The driver, laser, pin diode, and reference are contained in one package with cooling fins. The temperature of the package runs about 5°C above ambient. The remainder of the control circuit is contained in a second package.

A coaxial jack with normal-through contact provides an access point where the line signal can be interrupted and a test signal injected.

V. POWERING

The regenerator is powered by +5.0 V and −5.2 V with a typical power consumption of 3.1 W. For high supply voltages and the laser near end of life (high prebias), the power is estimated to be 3.9 W—0.9 in the receiver, 0.8 in the decider, and 2.2 in the transmitter. The supply voltages can vary by ±5 percent without affecting regenerator operation. In a subsequent regenerator modification, filtering was improved so that 100 mV p-p transients on the power line could be tolerated.

VI. CONCLUSION

The 45-Mb/s regenerator described here represents a practical design for a field environment. Feedback control of the avalanche photodiode gain and of the laser output level enable operation over a temperature range of 0 to 60°C. The regenerator has simple power requirements. Its input sensitivity and output power make useful regenerator spacings possible with currently available optical fiber. The wide AGC range permits the design to handle a wide range of regenerator spacings. The wide capture range of the timing circuit makes an expensive crystal unnecessary. The physical design is rugged and permits easy optical and electrical connection. Future efforts will reduce the three-module design to one module.

VII. ACKNOWLEDGMENTS

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