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Transaction Networks, Telephones, and Terminals:

Communication Network and Equipment

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Implementation of the Transaction Network required development of new equipment and integration of existing equipment to create a message switch and a communication network that interfaces with the switch by means of polled, dial, and synchronous access. Particular emphasis was placed on the reliability and maintainability of the system.

I. MESSAGE SWITCH COMMON EQUIPMENT

The central element of the Transaction Network is the message switch. Besides providing termination for polled, dial, and synchronous communication facilities, the message switch controls and routes traffic, performs the billing and administration function, and controls maintenance of the network.[1,2]

The configuration of the common equipment is shown in Fig. 1. The arrangement was designed with particular emphasis on reliability and maintainability. Much of the equipment is also used in systems other than the Transaction Network.

1.1 Processor

The Auxiliary 3A Processor is an enhanced version of the same processor used in the No. 2B and No. 3 ESS systems.[3] The principal enhancements consist of the addition of parallel input-output channels, direct memory access capability, and microprogrammed instructions that are useful in applications other than line switching.

The processor is a duplicated unit, containing two 3A central controls and two semiconductor memories. In the initial Transaction Network installations, 256K words are required in each memory, each word consisting of 18 bits including two parity bits. At any time, one processor

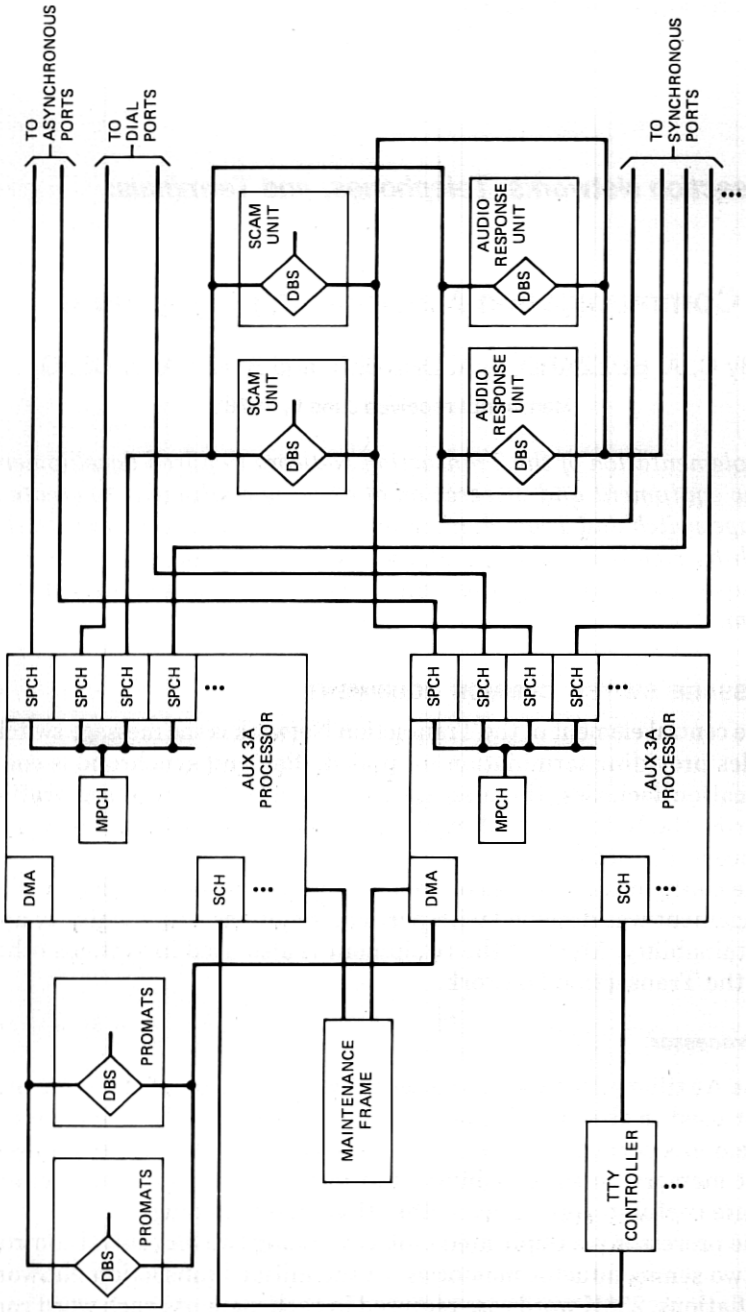


Fig. 1—Message switch common equipment.

and memory are active. The standby memory is continually updated so that the standby processor may be switched on line, with minimum disruption of service, in case of a fault in the active system, including an input-output port.

A maintenance frame associated with the duplicated processor includes a system status panel, two cartridge tape units used for loading programs, a teletypewriter, two teletypewriter control units which may serve several remote teletypewriters as well as the local one, and relays for activating office alarms. All these peripherals are connected to the processor via serial channels.

Parallel channels are used between the processor and the various communication ports to effect fast data transfer. Each processor contains a main parallel channel which couples to several subparallel channels. At each peripheral device, a duplex bus selector (DBS) is connected to a parallel channel from each processor. Under processor control, the DBS switches communication from the device to the active channel. The DBS insures that no single processor or channel failure will render the device inoperative, and also prevents any device failure from disabling the channel. Each pair of subparallel channels can support a chain of 16 DBSs and their associated devices.

1.2 Magnetic Tape System

The Transaction Network message switch contains two Programmable Magnetic Tape System (PROMATS) frames for recording of billing information. Information is recorded in 9-track, 1600 b/in. phase-encoded format.

Each PROMATS includes two programmable controller PROCON microprocessors for control and error detection. Direct memory access at the processor permits very fast bulk transfer of information. Each PROMATS frame is connected to each processor's direct memory access circuitry by means of a DBS.

1.3 Switch Control and Monitor

The Switch Control and Monitor (SCAM) provides a means for the processor to exercise control over the communication channels and to monitor the network configuration in real time. It also provides the processor with the capability of monitoring the condition of the communication hardware. In this function, it operates the switching relays which are used to busy-out dial ports, to connect dial ports to a test circuit, to switch in spare synchronous ports, to loop around synchronous ports, and to perform other miscellaneous control functions. A contact from each relay operated by the SCAM is also in turn monitored by the SCAM to check its own operation. Other monitor points are used to permit the processor to check all office power supplies and to scan numerous office alarm outputs.

The SCAM includes two control units, one of which is operative at any time. Each unit is connected to the duplicated processor by a DBS. Either unit may disable the other unit. It is also possible to disassociate switching relays from the SCAM units and leave them in a known condition, so that one control unit can perform diagnostic tests on the other without affecting operation on any communication port.

II. POLLED ACCESS

Polled terminals communicate with the message switch over dedicated facilities using 1200-b/s, serial, asynchronous, frequency-shift keying in each direction. Communication is half duplex. A remote switch, known as the Data Station Selector (DSS), permits one of many terminals to be connected to the message switch in response to a poll issued by the message switch. At the message switch, the Asynchronous Line Adapter (ALA) couples the transmission facility to the processor and implements the polling routine. A typical polled access arrangement is shown in Fig. 2.

The TN local distribution network is designed to be a cost-effective solution to problems inherent in bridged multipoint services that have been used to implement inquiry response communication systems in the past. Unlike bridged multipoint, the DSS provides isolation between loops. This facilitates maintenance and contributes to low transmission error rates. Costs are kept low by using two-wire facilities between each terminal and the DSS.

2.1 Asynchronous Line Adapter

Each ALA includes a frequency-shift modulator and demodulator coupled via a 4-wire transmission facility to a DSS. The ALA is capable of full duplex operation, although this capability is not used in initial Transaction Network Service.

The ALA may buffer up to 64 characters received from the processor, prior to transmission. During the conversion to serial format, start, stop, and parity bits are added to produce standard 10-bit asynchronous ASCII characters. Received characters from the demodulator are in the same format. After stripping of extraneous bits, checking, and conversion to parallel form, up to 64 characters may be stored in the ALA prior to being read into the processor.

When no information is being transmitted or received, the ALA autonomously implements the polling procedure without intervention from the processor. The list of station addresses is kept in the transmit buffer, which is configured as a recirculating register during polling. Each station is sequentially and repetitively polled until a station answers or the processor intervenes. After each poll is transmitted, the ALA remains silent for a period of time between 27 and 50 ms to wait for a possible

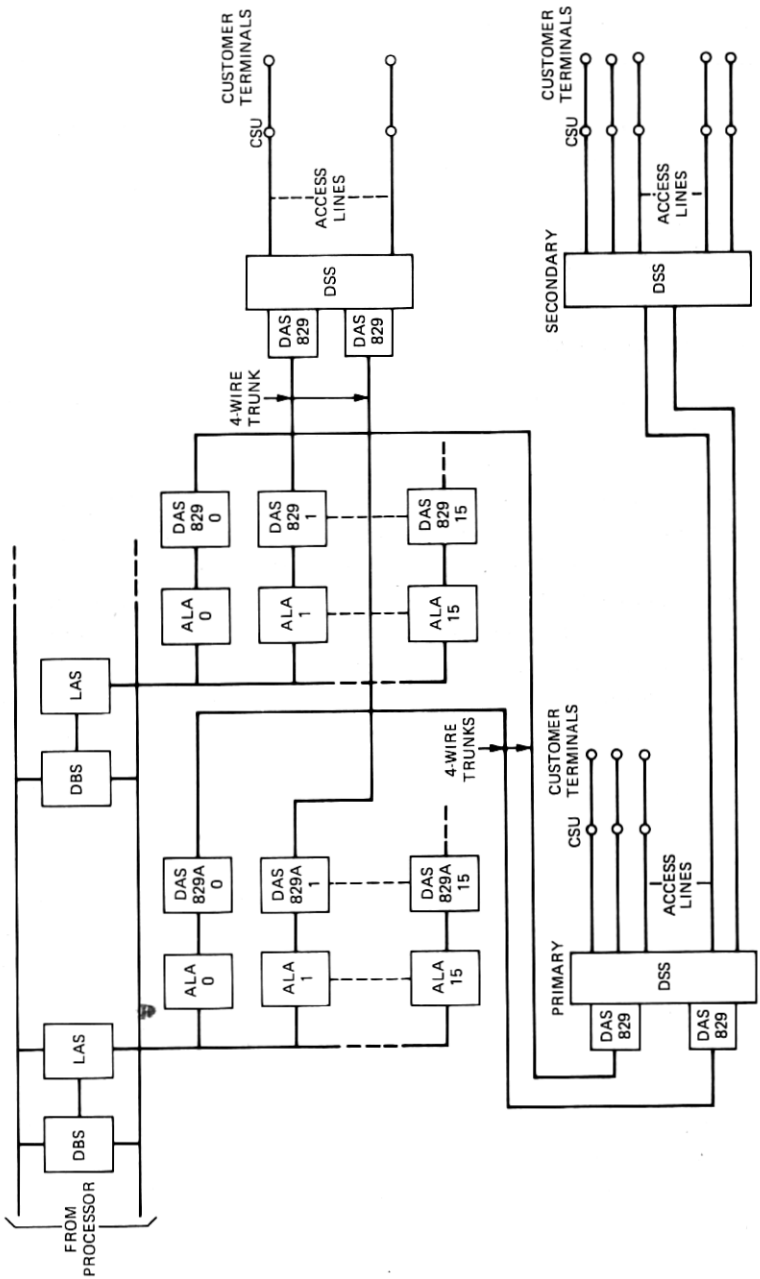


Fig. 2—Polled access configuration.

message before beginning the next poll. This period of time is set during installation by means of a group of switches. It allows for the maximum round-trip propagation delay through the DSS to the furthest station, in addition to other delays. When polling is interrupted by a message from a polled station or by a response message from the processor to a station, the polling list in the ALA is erased. The list must be reloaded by the processor before polling is resumed.

To keep costs low, a line adapter selector is used to perform some common functions for up to 16 ALAs and to interface this group of ALAs to a single duplex bus selector.

2.2 Data Station Selector

As shown in Fig. 2, the Data Station Selector (DSS) is interfaced to the message switch by means of a pair of trunks terminated in 829-type data auxiliary sets. Like the polled terminals which it serves, the Data Station Selector communicates with the message switch using 1200-b/s, serial asynchronous frequency-shift-keyed data signals. A modem contained within the DSS demodulates address (polling) signals from the message switch and passes these to the DSS control logic. As received at the DSS, addresses are the binary equivalent of the line numbers (0 through 62). The DSS control logic decodes the poll address and connects the corresponding terminal to the Asynchronous Line Adapter. The selected station is polled when it receives a burst of marking carrier (followed by a slow carrier turnoff) transmitted from the message switch. If the polled station replies to the poll with an inquiry, the DSS control logic is inhibited from decoding the response address. When a reply message is delivered from the message switch to a terminal through the DSS, the DSS is first instructed to make the proper connection and a BAL (Blind Alert) character (ASCII"?") is included in the reply message. The BAL character is interpreted by the DSS to mean that information which follows is intended as a reply to the terminal and is not to be interpreted as an address.

The DSS contains features which make possible one-person station installation and facility lineup. Direct current is normally present on the loop between the DSS and the customer terminal. Continuity is maintained through the 150A Channel Service Unit at the station location. When the craftsperson operates a screw switch in the Channel Service Unit, loop current is interrupted. This interruption is detected at the DSS, which then puts a 1000-Hz lineup tone onto the loop. The craftsperson may then adjust attenuator pads within the Channel Service Unit without any assistance at the DSS location.

The DSS is a duplicated unit. Each half is connected via a separate 4-wire facility to a separate ALA. These two ALAs are connected to different line adapter selectors, duplex bus selectors, and power supplies. In normal operation, half the stations associated with a DSS are assigned to each ALA. When an ALA or transmission facility must be taken out of service, its station list is added to that of the other ALA associated with that DSS. This permits continued operation to all terminals with somewhat slower service.

The line adapter selector generates and checks parity on all information transfers to and from the processor. The ALA includes other checking features. The processor may interrogate the status of these circuits to analyze trouble conditions.

Test characters may be generated by the processor and have them looped back at any one of several points, for transmission to the processor for trouble isolation. Loopback points exist at the input to the duplex bus selector, at the input to the line adapter selector, and at two points internal to the ALA. In addition, the modulator output may be connected to the demodulator input, with the transmission facility disconnected. All loopbacks are enabled under processor control.

When commanded by the processor, the line adapter selector can check the operation of the control and timing circuits in any one of its associated ALAs by measuring and reporting the time required for completion of a single poll.

The DSS has a test port which, when addressed in the same manner as a station, causes a test message to be returned to the message switch. This procedure provides an overall test of the ALA, the transmission facility, and most parts of the DSS. The DSS, as previously mentioned, maintains direct current on the loops to each Channel Service Unit. If the sealing current is interrupted for any reason, that fact is noted by the DSS and an indication of the faulty loop is provided to the message switch as part of the test message. The test message contains one bit for each of the 63 addressable ports. The DSS also contains circuitry which enables it to detect an abnormally high transmitted signal from a customer terminal. The line address of the loop carrying the overload signal is remembered by the DSS and returned to the message switch in the test message. The test message also contains information on the status of the DSS power supplies. To facilitate trouble isolation in the transmission path between the message switch and the DSS and between the two sections of the DSS, the two trunks may be interchanged. This is accomplished from the message switch by the transmission of a special command to the DSS.

The transmission facilities between the message switch and the DSS are terminated in 829-type data auxiliary sets at both ends. Besides

providing access, these sets permit loopback testing of the transmission facility from a centralized transmission test location.

III. DIAL ACCESS

The message switch may be accessed over the normal dial network by Transaction telephones using ordinary *TOUCH-TONE*® dialing with 12 button pads. Communication from the message switch to the station may be in the form of audio response, keyed tones, 150-b/s, serial, asynchronous frequency-shift keying, or a combination of these.

The dial access configuration is shown in Fig. 3. Each incoming line at the message switch terminates at a standard 407A data set.[4] A Dial Line Adapter (DLA) interfaces each data set to the processor. The frequency-shift modulator is part of the DLA. Those ports which require audio response are coupled to the Audio Response Unit (ARU), which delivers spoken words under processor control. Ports with and without audio response capability are arranged in separate hunting groups in order to conserve ARU ports.

3.1 Dial Line Adapter

The DLA controls the answering, disconnect, and other control features of its associated data set based on commands received from the processor. *TOUCH-TONE* characters detected by the data set are passed on to the processor in 2-out-of-8 format. The DLA times the interval between these characters. If no character is received for a period of approximately 13 seconds, the processor is notified so that it may initiate a disconnect.

Characters to be transmitted are presented by the processor to the DLA, which constructs serial asynchronous FSK characters to be transmitted through the voice answerback input channel of the 407A data set. The format is the same 10-bit ASCII as in polled access. The DLA may also cause the data set to send keyed 2025-Hz tones by operating its tone answerback lead for the proper period of time. When required, the ARU is also coupled through the DLA to the voice answerback input of the data set.

The same *DESIGN LINE** adapter selector that is used for the ALA is used to connect up to 16 DLAs to a single duplex bus selector and to perform common functions for them.

3.2 Audio Response Unit

The TN Audio Response Unit (ARU) design is based on a semiconductor random access memory containing up to 6.8 Mb of digitized

* Trademark of American Telephone and Telegraph Company.

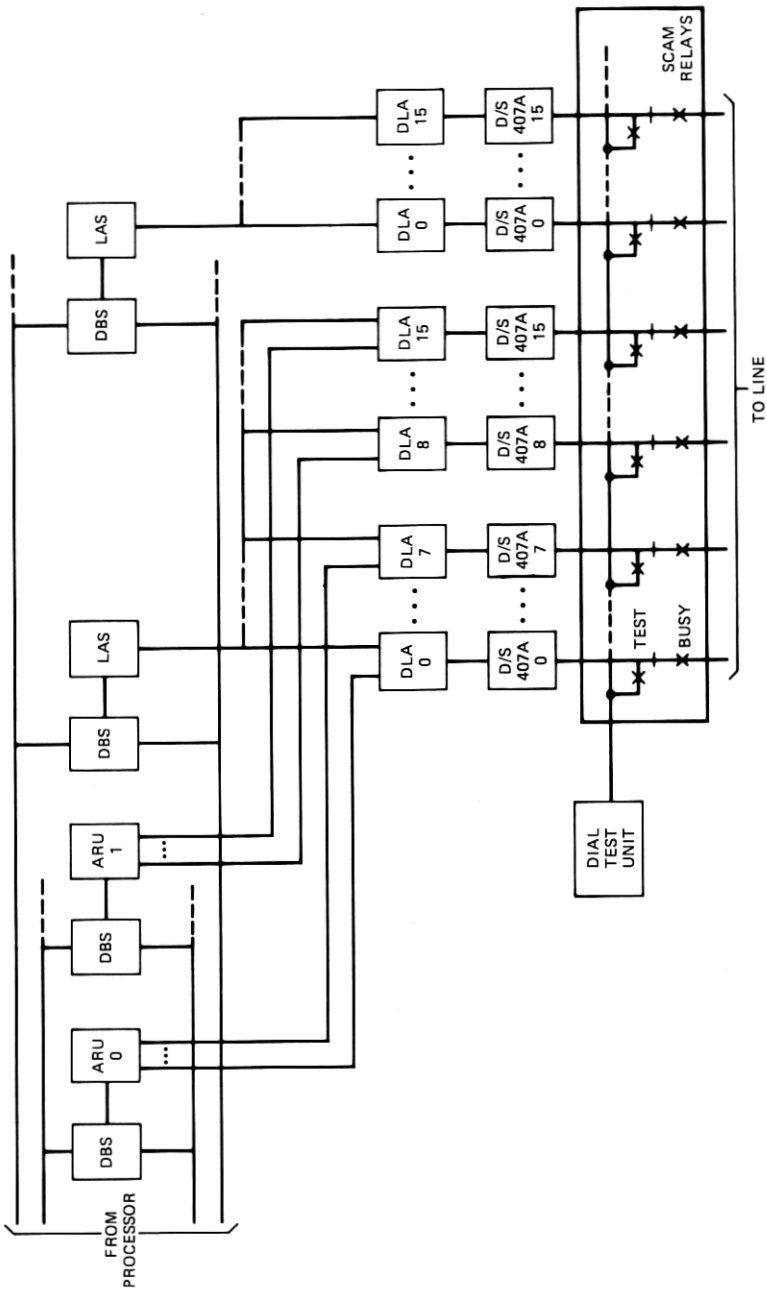


Fig. 3—Dial access configuration.

speech. The digitized speech is obtained from analog recordings of the words to be spoken which are converted to digital form at 24 kb/s using an adaptive delta modulation technique developed for subscriber loop carrier. Stored digitized speech segments are retrieved from the memory and pieced together to form phrases and sentences under control of the 3A Processor.

Each ARU speech memory can contain up to 560 spoken words and deliver as many as 76 simultaneous and independent audio responses. The ARU is an output peripheral for the auxiliary 3A Processor and is controlled by high-speed data signals sent to and from the processor on a subparallel channel. The ARU contains a duplex bus selector. Information is delivered across the DBS interface to cause the ARU to deliver an audio response to a telephone, to load the ARU speech memory with digitized speech stored on a 3A cartridge tape, or to return maintenance information from the ARU to the processor.

The ARU produces a voice response by piecing together speech segments which are approximately 170 ms long. The 3A Processor operates the ARU by delivering a list of those speech segments required to create the desired response. One 16-bit computer word must be delivered to the ARU each 170 ms for each equipped port. A buffer is provided that allows the processor to deliver these words at any time within the interval. If the processor fails to deliver the required data, the ARU will substitute silence.

The audio response delivered to a calling telephone is determined by the Customer Service Center computer. The customer has available a list of English phrases from which he can compose messages. Each phrase is specified by a triplet of ASCII characters sent to the message switch in the text portion of a response message. The 3A contains a translation table which permits it to generate the list of speech segments required to produce the desired audio output.

The vocabulary for a particular Transaction Network message switch is contained on a magnetic tape cartridge which can be read by the 3A Processor. As the tape is read, the digitized speech is delivered across the DBS interface and stored in the ARU speech memory. In the event of a power failure, the contents of the speech memory will be lost, and the ARU must be reloaded from the tape. Checks are made after a load is completed to ensure that it has been properly accomplished. Ten minutes are required to completely load an ARU. In TN applications, a pair of ARUs is provided. One ARU may be providing service while the other is being loaded.

The ARU construction is highly modular. Audio responses are produced through a port circuit pack, and each ARU must contain at least one such circuit pack which serves two ports. Port capacity may be expanded by adding additional circuit packs up to a maximum of 38; thus, each ARU can serve from 2 to 76 ports. Anywhere from 1 to 104 memory

plane circuit packs may be ordered for the speech memory, providing vocabulary storage ranging from 2 to 560 spoken words.

The three major components of the ARU circuit are the digital speech memory, the array of port circuits, and the time division switch and bus arrangement that interconnects these two. In addition, control, timing, and maintenance functions are provided. These components are interconnected as shown in Fig. 4. Digitized speech is cyclically read from the speech memory and placed on a bus, where it is available to the port circuits. The port circuits select the proper bits from the bus as specified by information received from the processor through the buffer.

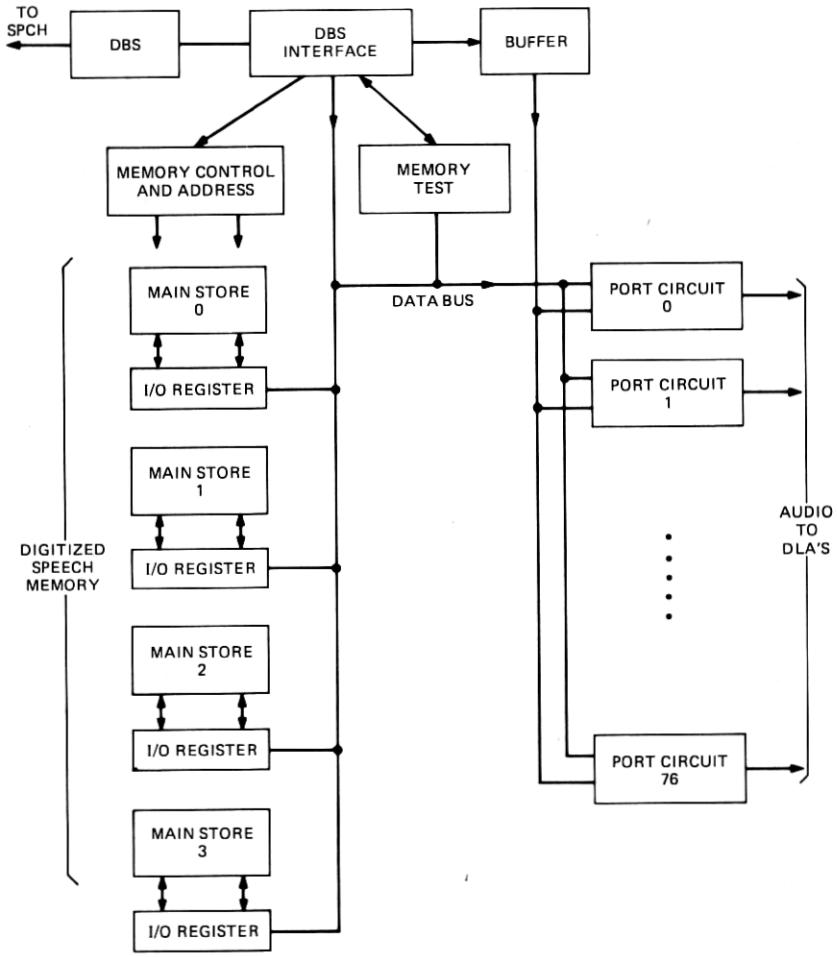


Fig. 4—Audio response unit.

3.3 Dial access maintenance features

The DLA and the line adapter selector include several checking circuits to detect troubles. They also contain status registers which may be interrogated by the processor to analyze abnormal conditions.

The processor can set up a loopback at the input to the duplex bus selector, to the line adapter selector, or to the DLA through which characters generated by the processor can be sent back to it. A dial test unit located in the SCAM provides an overall test of the dial port, including the 407A data set. Under processor control, the SCAM can connect the line side of any one data set to the dial test unit and simultaneously make the incoming line look busy. A ringing generator is used to check the answering functions of the data set. Frequency-shift-keyed characters transmitted by the port are converted to *TOUCH-TONE* signals and transmitted back to the 407A, providing another loopback point. In addition, the dial test unit checks the amplitude and duration of the keyed answertone and the disconnect feature of the data set.

The 407A may also be checked manually in the standard manner, either locally or with a remote data test center.

Any dial ports that have been determined to be faulty are placed out of service by making the incoming line appear busy. This out-of-service feature is provided in both the DLA and the SCAM. To minimize possible degradation of service, lines from each hunting group are distributed among ports using different line adapter selectors, duplex bus selectors, and power supplies.

Like the LAS and DLA, maintenance of the ARU is under control of the 3A Processor. Two signals are provided from each ARU power sequencer to the SCAM, and a considerable amount of maintenance information is routinely transferred from the ARU to the processor through the subparallel channel interface. The message switch software will bring in a minor alarm if more than a few errors are detected in the digital speech memory. Each quarter of the speech memory can be viewed as an array of 52 columns, each containing 32K bits. The first column contains a parity bit, and each row of the memory is checked for correct parity as it is read. The parity error alarm threshold is programmable. Each column of the memory should contain a known number of ones which are counted by the test circuitry on each memory cycle and the eight least significant bits of the resulting check sum are returned to the processor for verification. If the memory degradation is serious enough to be audible or if another problem is detected which requires the removal of an ARU from service, a major alarm occurs. If both ARUs are removed, a critical alarm is generated.

The ARU has been designed with a minimum of test access points and nearly all maintenance activities are carried out automatically. Two diagnostic software packages are available for the ARU. One diagnostic

contains all those tests which may be conducted without disturbing the contents of the ARU speech memory. The second diagnostic assumes that it is necessary or desirable to reload the contents of the speech memory and contains additional tests based on special patterns specifically loaded into the speech memory for test purposes. In this case, the ARU is reloaded with digitized speech at the conclusion of these tests.

The ARU also contains a short FSK test sequence which may be delivered to any port under processor control. In conjunction with the SCAM and Dial Test Unit, the processor may cause this FSK sequence to be looped through the Dial Line Adapter and its correct interpretation verified by the processor.

IV. SYNCHRONOUS ACCESS

Communication between the message switch and data processing centers is implemented using either standard data sets and 4-wire private line analog facilities, or digital data system channels. Synchronous serial communication with full duplex capability at 2400, 4800, or 9600 bits per second is provided by the 201C, 208A, or 209A data set, respectively, or the appropriate 500A data service unit.

At the message switch, the Synchronous Line Adapter (SLA) acts as the interface between the processor and a data set. Figure 5 illustrates the architecture of the synchronous access arrangement at the message switch. Each SLA is coupled to the duplicated processor by a duplex bus selector.

4.1 Synchronous Line Adapter

To provide flexibility in communicating with different types of data processing centers, the SLA has been designed such that many of its operations can be changed according to instructions received from the message switch processor. This approach permits a single hardware design to meet several applications.

A principal function is conversion between the parallel format of the processor and the serial format at the data set. The processor programs the SLA to transmit and receive character lengths of 5, 6, 7, or 8 bits including even, odd, or no parity. The same format applies in both directions. First-in, first-out buffers of 64-character length are provided in the SLA in each direction to reduce the frequency at which the processor must deliver or accept strings of characters.

The processor programs the SLA to generate an interrupt after a given number of characters have been transmitted since the last interrupt. An interrupt is also generated when the transmit buffer becomes empty. These interrupts may be disabled under processor control. The fill character that is to be transmitted after the buffer is empty is also programmed into the SLA.

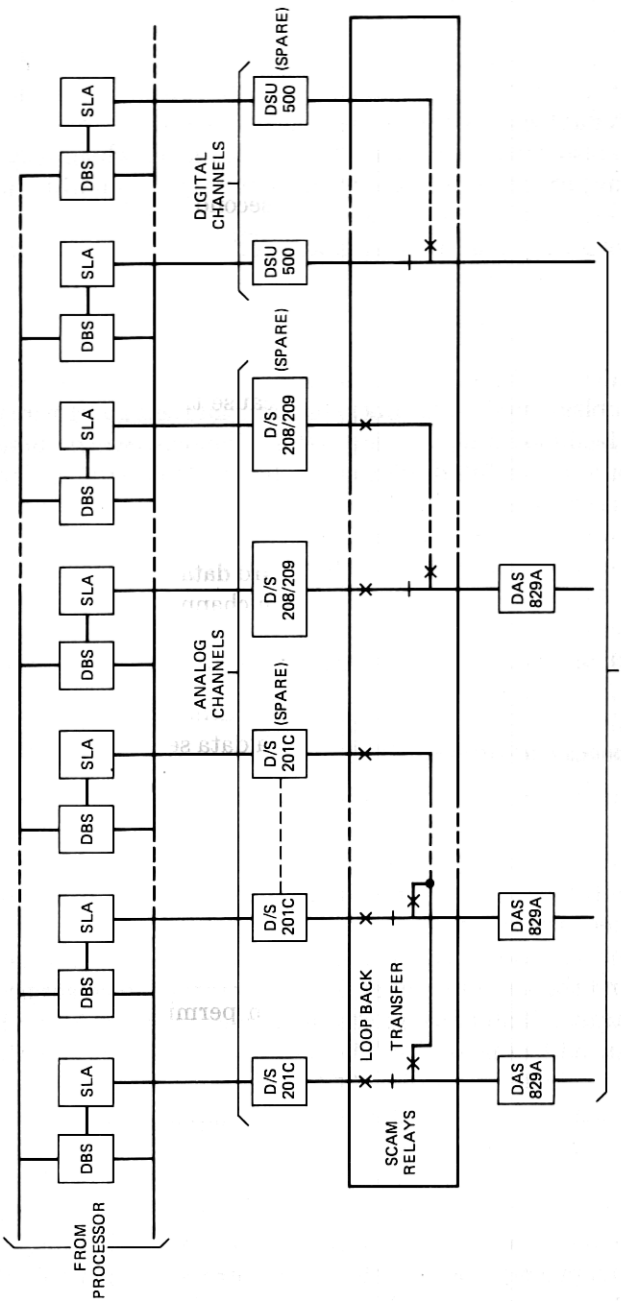


Fig. 5—Synchronous access configuration.

Similarly, the SLA is programmed to interrupt after a given number of characters has been received. An interrupt is also generated when the associated data set detects loss of carrier. In addition, up to 256 special characters may be programmed into the SLA such that an interrupt will be generated whenever any of those special characters is received. The receive interrupts may also be disabled.

Another instruction to the SLA determines the particular synchronization character that is to be recognized to establish received character synchronization. The SLA is also instructed on whether or not synchronization characters are to be passed on to the processor along with other received data.

The SLA derives all its internal clocking from the clock supplied by the data set. Its operation is therefore insensitive to data rate.

4.2 Maintenance features

All testing of synchronous access equipment at the message switch is performed under control of the processor. Tests may be manually initiated by means of teletypewriter input to the processor. Tests may also be automatically initiated by the processor periodically or whenever a trouble condition is indicated.

Malfunctions are localized by having test characters generated by the processor, looped back at a loopback point determined by the processor, and sent back to the processor. Loopback points exist at the input to the Duplex Bus Selector and at the input and output of the SLA. An additional loopback point for including the operation of analog data sets is available through operation of a SCAM relay. This loopback causes the transmitted output of a data set to be connected to the input of that data set through an attenuator.

The SLA includes parity checking and other circuits to detect troubles. The processor may interrogate the status of any of the SLA circuits to detect and analyze troubles.

For analog channels, data sets and associated transmission facilities may be tested manually from remote test centers. The 829 data auxiliary sets provide access jacks and tone-activated loopback.

One spare SLA and associated data set is provided for each type of data set used. The spare port may be substituted for any one of its associated ports by operation of a SCAM relay. All diagnostic features remain operable for the out-of-service synchronous port, as they do for the spare at all times.

V. PHYSICAL DESIGN

The functional units of the Transaction network are interconnected very simply. The physical design addresses the integration of two basically different types of hardware, ESS and data, into one system.

5.1 Message switch hardware

The basic physical design of the message switch hardware makes use of 1A technology, which was initially developed in No. 4 ESS. The 3A Processor and maintenance frames were in manufacture at the Western Electric Northern Illinois Works when design of the new hardware was started. Since this equipment employed 1A technology, its choice provided a uniform office configuration and allowed the entire system to be manufactured and tested at the North Illinois Works without new tooling or unique testing facilities. Machine aids to design and documentation and high-volume production equipment thus became available to meet a demanding schedule.

5.1.1 Circuit packs

Circuit packs are FB and FC coded packs, approximately 4 × 7 in., using 946B and 946C connectors, respectively. The 946B provides 41 pinouts, of which 36 may be used for signal levels, 2 for power, and 3 for ground. The 946C provides for 82 pinouts with 76 usable for signal leads.

The circuit packs themselves are 4- and 6-layer multilayer boards arranged to mount a maximum of 42 sixteen-pin dual-in-line packages in a 6 by 7 array. When larger devices are used, the array is disrupted slightly. Machine wire-wrapped models were initially built and tested, and then artwork was generated completely automatically for the multilayer boards.

5.1.2 Units

The assembly of circuit packs, apparatus mountings, backplane, mounting plate, and wiring is called a unit. The unit is the most important functional building block in the message switch.

Unit design uses 1A technology also. 80C apparatus mountings are used to contain the circuit packs—a maximum of 14 circuit packs can be mounted, on ½-in. centers, in each mounting. Three mountings can be mounted on each 4- by 26-in. mounting plate used to attach a unit to the frame. The units are front-removable from the frame to allow for easier maintenance.

The 946-type connector of the circuit pack plugs into a 947-type connector of the unit. The 947 connectors are mounted directly to the unit, and a 4-layer backplane is reflow-soldered onto the connectors. The backplanes are nominally 0.100-in. thick, 4-in. high, and vary in width depending upon the number of connectors that are required. Signal ground and +5V are distributed to each of the 947 connectors from this backplane. In this manner, a low-impedance power-ground plane is approximated.

The backplane system thus formed is a grid of 0.025-in. square pins

on 0.125-in. centers. Signal leads are 30-gauge wires automatically wrapped by Gardiner Denver machines at Western Electric Northern Illinois Works. The machine aids used in the design and manufacture of these units minimize the variability among units.

The unit usually includes the Duplex Bus Selector (DBS). The interface between the peripheral circuits and the DBS is 5V TTL, which allows a lead length of no more than about 24 in. Figure 6 shows a typical unit, with the DBS integrated within. This particular unit also contains 48V to 5V and 48V to ±12V converters. This has also been done in other units when space permits. The tick marks in the illustration represent circuit packs of a fully equipped unit. In this case, an ALA unit has DBS, LAS (Line Adapter Selector), three power units, and from 1 to 16 ALA circuits, each consisting of three circuit packs.

5.1.3 Frame design

The units are front mounted in 1A equipment frames which are 7 ft tall overall, providing 76 in. of mounting space, and are nominally 2 ft, 2 in. wide. Much of the equipment mounted in the frames requires 18 in. depth, and so for uniformity all message switch frames are 18 in. deep.

Since the units are highly connectorized, the frames may be considered to be convenient mounting arrangements for various combinations of units. Other units may also be incorporated into these frames as required.

Most frames have one configuration; the frames are filled with equipment and apparatus as the system grows. The synchronous line adapter (SLA) frame has more flexibility, because synchronous communication can be any of three speeds and either analog or digital. Each speed and format requires different hardware to interface the synchro-

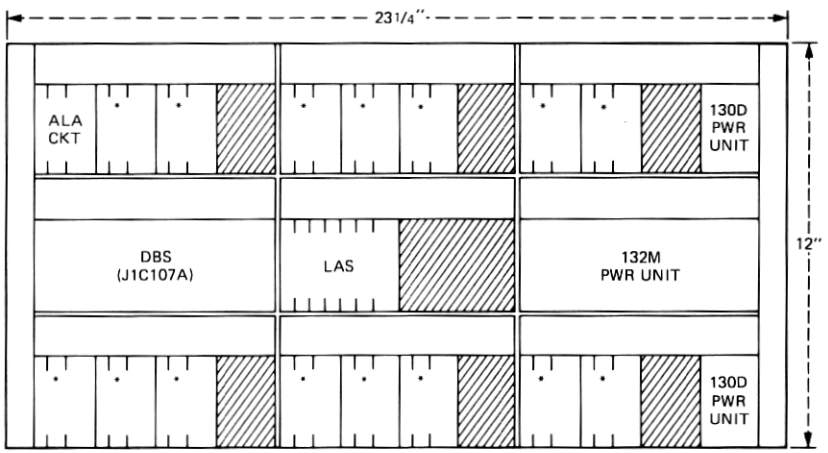


Fig. 6—Asynchronous line adapter unit.

nous line adapter. The five resulting SLA frame configurations are shown in Fig. 7. Here, DS is Data Set, DAS is Data Auxiliary Set, and DSU is Data Service Unit. The numbers to the left of the frames are distances from the floor, in inches. As can be seen in the figure, all frames are identical up to location 26. Similarly, above that location the alternative unit always appears at the same location, regardless of configuration, e.g., if a 46A1 data mounting is required at all, it will start at location 38.

The five resulting SLA frame configurations are actually quite similar, being different only in the types and combinations of data sets and DSUs incorporated.

5.1.4 Cabling and interconnection

Interconnection from one unit to another is accomplished by cable assemblies terminated at each end by 942- or 943-type connectors. This family of connectors provides 10 or 20 box contacts in a plastic housing attached to a small printed-circuit "paddleboard." The connector is used to mate with one quadrant of wire-wrap pins on the 947 connector while allowing the use of wire-wrap connections underneath. Flat flexible cable is used in some applications, but multipair switchboard cable is used in most. Provisions are made for resistor termination of the cable, if required, on the paddleboard.

Connections from data sets use KS connectors which match them, and connection to the distribution frames use KSed Blue Ribbon* connectors and standard central office cabling.

5.1.5 Office layout

A typical message switch has about 20 frames of equipment. Figure 8 shows a typical maximum size message switch. The control complex frames, containing the auxiliary 3A Processor System, has a fixed configuration required by interconnection limitations. The data bus to the processor has a maximum length, and as a result ALA frames must be adjacent to one another and so must DLA frames. The office layout of Fig. 8 produces a compact, well-organized system. If office space requires, other layouts subject to the above requirements are permitted.

Since the message switch is expected to be installed in an existing building and will utilize the type of power plant specified for ESS, the cable duct, lighting, and other metal work are those used in new ESS installations.

* Registered trademark of Amphenol, Inc.

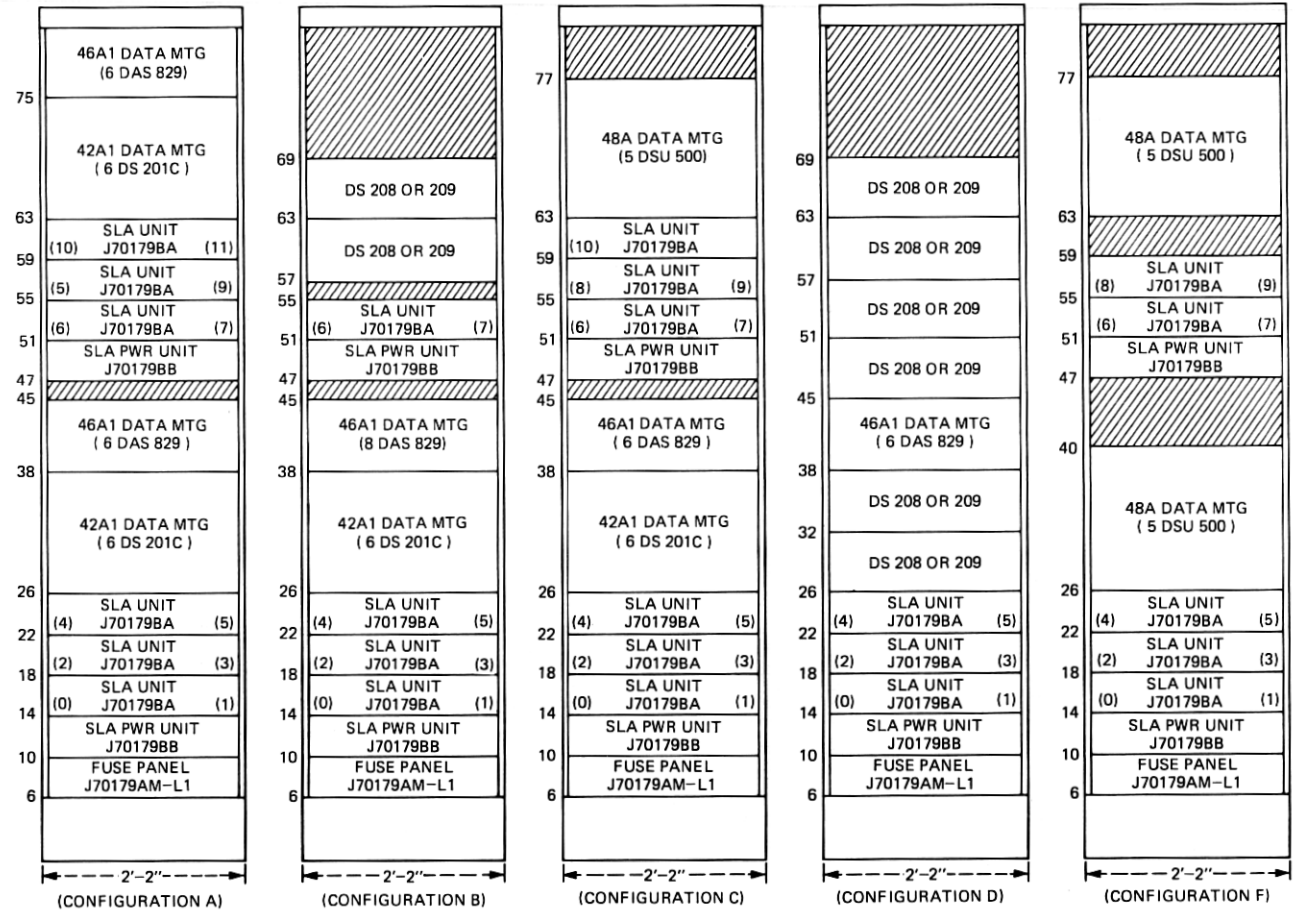
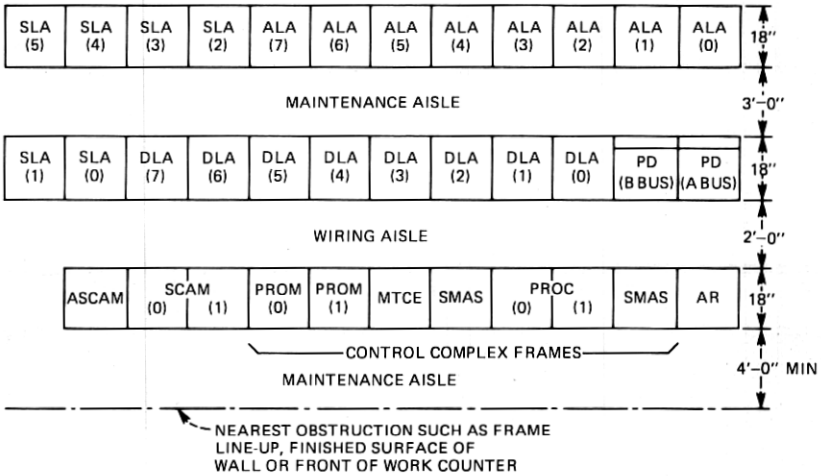


Fig. 7—Synchronous line adapter frame.



LEGEND:
ALA – ASYNCHRONOUS LINE ADAPTER
DLA – DIAL LINE ADAPTER
SLA – SYNCHRONOUS LINE ADAPTER
PD – POWER DISTRIBUTION
*ASCAM – AUXILLIARY SWITCH CONTROL AND MONITOR
SCAM – SWITCH CONTROL AND MONITOR
PROM – PROMATS – PROGRAMMABLE MAGNETIC TAPE SYSTEM
MTCS – MAINTENANCE
SMAS – SUPPLEMENTARY MAIN STORE
PROC – PROCESSOR
AR – AUDIO RESPONSE

*NOT GENERALLY REQUIRED

Fig. 8—Typical floor plan layout with PD frames.

5.2 Data Station Selector

The 1A Data Station Selector (DSS) is designed to be mounted in a variety of environments: ESS or other type central offices or on customer premises.

As indicated in Fig. 9, it connects up to 61 polled Transaction terminals to two asynchronous circuits of the message switch. As a relatively small and self-contained entity, it also incorporates testing access and facilities termination (e.g., Data Auxiliary Set). A relatively large amount of analog circuitry is involved, and data set style packaging was chosen instead of 1A technology (see Fig. 9).

The DSS is a single shelf unit 23 in. wide, which requires 10 in. vertical frame space. It can be mounted in 12-in. deep frames wherever space is available. For customer premises application, a KS-20018 series cabinet is used and a 110V ac and −48V dc converter is required.

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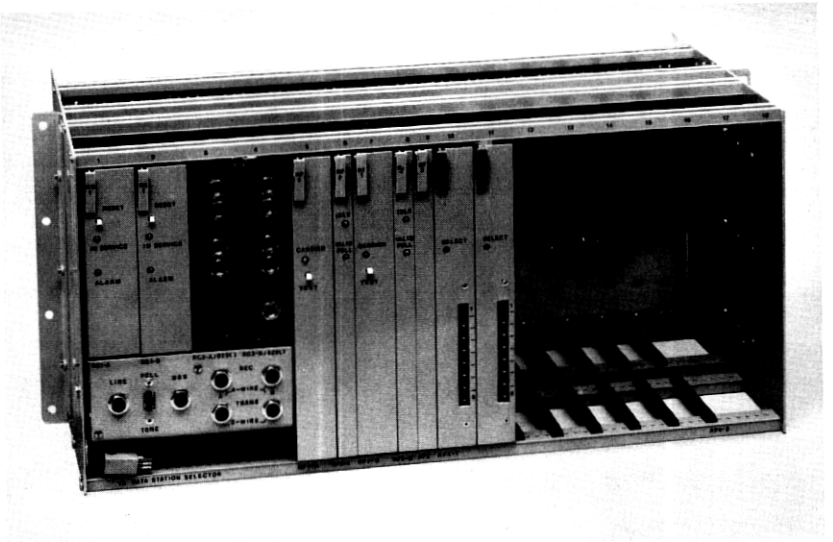

Fig. 9—1A Data Station Selector.

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