Contributors to This Issue

C. F. Ault, B.E.E.E., 1950, University of Southern California; M.S.E.E., 1955, Stevens Institute of Technology; Bell Laboratories, 1955—. Mr. Ault has been continuously involved in memory development. He has worked on the development of memory for processors, including the barrier grid store, the flying spot store, and the permanent magnet twistor. He presently supervises work on mass memory subsystems for ESS processors. Member, IEEE, Eta Kappa Nu, Tau Beta Pi.

J. O. Becker, B.S.M.E., 1960, M.S.M.E., 1961, and Ph.D., 1964, University of Illinois; Bell Laboratories, 1969—. Mr. Becker has been concerned with the thermal performance of the 1A Processor and associated technology. Since 1970, he has been supervisor of a group responsible for the physical design of memory for the 1A Processor. Member, Pi Tau Sigma, Tau Beta Pi, Sigma Xi.

P. W. Bowman, B.S.A.M.P., 1968, and B.S.E.E., 1968, University of Wisconsin-Madison; M.S., 1969, University of California-Berkeley; Bell Laboratories 1968—. Mr. Bowman has worked on specification and diagnostic design for the 1A Processor auxiliary data system. He designed a performance and evaluation system to be employed at the field trial for the High Capacity Mobile Telephone System. Since 1974, he has had responsibility for the 1A Processor diagnostics. At present, he is involved in the design and development of a voice storage system.

J. H. Brewster, B.S.E.E., 1960, Yale University; M.S.E.E., 1962, New York University; Bell Laboratories, 1960—1976. Mr. Brewster has worked on maintenance and operational software for No. 1 ESS. He has also supervised work on the design of man-machine interface and input/output subsystems for the 1A Processor. Mr. Brewster is now with American Bell International, Inc.

A. H. Budlong, B.N.S., 1946, B.E.E., 1948, and M.S. (Physics), 1950, Marquette University; Member of teaching staff of Department of

Physics 1948—1952, Marquette University; Bell Laboratories, 1952—. Mr. Budlong has engaged in exploratory development of electronic switching circuits. He has also worked on the development of the No. 1 ESS electronic telephone switching system in the areas of trunk and service circuits and automatic message recording equipment, in the design of high-speed scanners and signal distribution, and is currently in charge of a group designing high-speed communication buses and power facilities for a high-speed processor for electronic telephone switching systems. Member, Sigma Pi Sigma, Pi Mu Epsilon.

J. G. Chevalier, B.E.E., 1951, Ohio State University; Bell Laboratories, 1956—. Mr. Chevalier has worked on printed-wiring processes and applications for military projects, connector design, studies of contact finishes, and the design and packaging of electronic equipment for No. 1 ESS. His current project is the physical design of equipment and interconnection techniques for the 1A Processor. He is currently supervisor of the Interconnections Group in the Processor Development Laboratory.

G. F. Clement, B.S.E.E., 1940, New York University; M.A. (Physics), 1947, Columbia University; Bell Laboratories, 1934—. Mr. Clement has worked on electronic field studies and solid solutions. During World War II he worked on the Manhattan Project and the application of analog computers to military systems. He has worked on military missile systems, the UNICOM system maintenance, and No. 1. ESS AUTOVON. In 1968, he became head of a department responsible for No. 1 ESS maintenance and 1A Processor recovery. He is currently head of a department responsible for Step-by-Step and No. 1 Crossbar design and support. Member, Iota Alpha, Eta Kappa Nu.

B. G. De Lugish, B.S.E.E., 1965, M.S.E.E., 1968, and Ph.D., 1970, University of Illinois-Urbana; Bell Laboratories, 1965—. Mr. De Lugish has been engaged in hardware development for the 1A Processor. He has worked with processor architecture and the design of processors for electronic switching systems. Member, IEEE, Tau Beta Pi, Sigma Tau, Eta Kappa Nu.

M. R. Dubman, A.B., 1957, Princeton University; M.S., 1959, Massachusetts Institute of Technology; Ph.D., 1970, University of Califor-

nia-Los Angeles; Bell Laboratories, 1970—. From 1959 to 1970, Mr. Dubman was engaged in the development of data analysis techniques used in testing of Saturn/Apollo rocket engines for North American Rockwell. At Bell Laboratories, he has been concerned with the development of error analysis methods for the 1A Processor.

R. K. Eisenhart, B.S.M.E., 1957, Pennsylvania State University; M.E.E., 1959, New York University; Bell Laboratories, 1957—. Mr. Eisenhart has worked on the development of the photographic processor for the flying-spot store of the Morris electronic switching system. He has supervised the development of apparatus and equipment used in No. 1 ESS. In 1966, he was appointed head of a department responsible for the development of packaging technology for electronic switching systems and for the physical design of the 1A Processor.

J. H. Forster, B.A., 1944 and M.A., 1946, University of British Columbia; Ph.D., 1953, Purdue University; Bell Laboratories, 1953—. Mr. Forster has worked on transistor development and reliability and in semiconductor surface studies. He has supervised the development of computer and microwave diodes and integrated circuits. Since 1963, he has headed departments engaged in various aspects of silicon and hybrid integrated-circuit development, including bipolar logic circuits for 1A Processor, No. 4 ESS, and many other Bell System applications. Member IEEE, Sigma Pi Sigma, Sigmi Xi.

A. W. Fulton, B.S.E.E., 1966, University of Arizona; M.S.E.E., 1967, and Ph.D. 1971, Stanford University; Bell Laboratories, 1966—. Mr. Fulton has worked on the development of technology, circuits, and file-memory systems for electronic switching systems. In 1972, he was appointed supervisor of a file-store memory development group. He is presently supervisor of a group involved in the development and application of integrated circuits for switching systems. Member, Tau Beta Pi, Sigma Xi.

P. S. Fuss, B.S.E.E., 1956, University of Michigan; M.E.E., 1960, New York University; Bell Laboratories, 1958—1977. Mr. Fuss has worked on circuit and system development on various missile guidance and antisubmarine warfare systems. In 1969, he was appointed head of a department responsible for the development of a digital signal processor

system for an advanced ASW program. He was head of the Large Processor Design Department which is responsible for the design of large switching control processors and their associated operating system software. He is currently Director of Product Development, Teletype Corporation. Member, IEEE, Tau Beta Pi, Eta Kappa Nu.

F. M. Goetz, B.E.E., 1953, Manhattan College; M.S. (Math), 1960, New York University; Bell Laboratories, 1953—. Mr. Goetz has worked on logic design, software development, and system design for electromechanical and electronic switching systems. Since 1962, he has been a supervisor responsible for various aspects of electronic switching system maintenance. At present, he is responsible for small processor system design and maintenance. Member, IEEE, Eta Kappa Nu.

T. S. Greenwood, B.S.E.E., 1951, Northeastern University; M.S.E.E., 1953, Massachusetts Institute of Technology; Bell Laboratories, 1953—. Mr. Greenwood has been continuously involved in development of electronic switching system processors. His early work involved the development of memory for processors, including the barrier grid store, the flying spot store, and the permanent magnet twistor. He has worked on the development of both maintenance and operational programs for No. 1 ESS. He currently heads a department responsible for the development of the 1A Processor hardware. Member, IEEE, ACM, AAAS.

R. J. Griffith, B.S.E.E., 1963, Iowa State University; M.S.E.E., 1965, Ph.D., 1969, Columbia University; Bell Laboratories, 1963—. Mr. Griffith has worked on the design of information processing techniques in systems used by the U.S. Navy. Since 1974, he has been concerned with development and evaluation of software for the 1A Processor.

R. E. Haglund, B.S.E.E., 1960, M.S.E.E., 1963, and PhD., 1969, Iowa State University; Bell Laboratories, 1969—. Mr. Haglund was a member of the original 1A Processor file-store design group and presently is engaged in file-store design utilizing new memory technologies. Member, IEEE, Eta Kappa Nu, Sigma Xi.

W. L. Harrod, B.S.M.E., 1962, Texas Tech University; M.S.E.M., 1964, Rutgers University; M.S.M.S., 1971, and Ph.D., 1975, North-

western University; Bell Laboratories, 1962—. Mr. Harrod has worked on the physical design of hardware for government and military switching systems and on the development of technology for applying thin-film and silicon integrated circuits in electronic switching systems. Since 1968, he has been supervisor of a group responsible for design, development, and characterization of new hardware for integrated-circuit packaging in ESS. His current responsibilities also include the physical design of advanced file memory systems. Member, Tau Beta Pi.

H. A. Hilsinger, B.S.E.E., 1954, Newark College of Engineering; M.S.E.E., 1959, New York University; Bell Laboratories, 1954—. Mr. Hilsinger's early work included military missile projects. Since 1961, he has supervised groups associated with the physical design and construction program for electronic switching systems.

R. F. Kranzmann, B.E.E., 1969, Union College; M.E.E., 1962, New York University; Bell Laboratories, 1960—. Mr. Kranzmann has worked on the design and development of call-processing software for military and government communication systems (UNICOM and AUTOVON). From 1969 through 1971, he supervised a group responsible for maintenance planning and diagnostic software design for No. 1 ESS peripheral units. More recently Mr. Kranzmann has had responsibility for diagnostic software design for several 1A Processor subsystems and for design of both on-line and off-line software to implement trouble-location procedures for the 1A Processor.

R. C. Lee, B.S.E.E., 1948, University of Michigan; M.S.E.E., 1957, Polytechnic Institute of Brooklyn; Bell Laboratories, 1948—. Mr. Lee has been involved with the development of switching systems including Crossbar Tandem, 101 ESS, No. 1 ESS, and the 1A Processor. He is currently supervisor of a group responsible for 1A Processor fault-recovery programs.

K. D. Mozingo, B.S.E.E., 1963, North Carolina State University; M.S.E.E., 1964, University of Michigan; Bell Laboratories, 1963—. Mr. Mozingo has been involved in software and system test development for switching systems (No. 1 ESS, No. 1 ESS ADF, 1A Processor). He is presently a supervisor in the Processor Applications and Software De-

partment of the Processor Development Laboratory. Mr. Mozingo's group is responsible for the diagnostic control and trouble-location programs in the 1A Processor. Member, Phi Kappa Phi, Theta Tau, Eta Kappa Nu.

S. M. Neville, B.S.E.E., 1959, University of Oklahoma; M.E.E., 1961, New York University; Bell Laboratories, 1959—. Mr. Neville has worked on circuit, logic, and system design for the No. 1 ESS processor and 1A Processor. He presently is supervisor of the Processor Design Group in the Processor Development Laboratory. Member, IEEE, Sigma Tau, Tau Beta Pi, Eta Kappa Nu.

J. S. Nowak, Bell Laboratories, 1955—. Mr. Nowak has worked in the system planning area of the Morris experimental electronic central office. He later supervised a group developing system requirements and designing maintenance programs for No. 1 ESS. He presently heads a department responsible for the planning, design, and introduction of a high-capacity No. 1A Electronic Switching System.

J. L. Quinn, B.S.E., 1959, Stevens Institute of Technology; M.S.E.E., 1961, New York University; Bell Laboratories, 1959—. Mr. Quinn has worked on the design and testing of the No. 1 ESS. Since 1965, he has been supervisor of groups concerned with ESS system testing and development of maintenance programs. At present, he is responsible for the 1A Processor. Member, IEEE, Eta Kappa Nu.

W. A. Read, A.B., 1960, Bowdoin College; M.S.E.E., 1962, Columbia University; Bell Laboratories, 1964—. Mr. Read was initially involved in the design of logic circuits for No. 101 and No. 2 ESS. Subsequently, he has been engaged in the design and development of memories for the No. 1 ESS and the 1A Processor. Member, IEEE.

M. W. Rolund, B.E.E., 1961, Cooper Union; M.S.E.E., 1963, New York University; Bell Laboratories, 1961—. Mr. Rolund is supervisor of a group engaged in circuit and system design of magnetic and semiconductor memories for No. 1 ESS and the 1A Processor. Member, IEEE, Tau Beta Pi.

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R. E. Staehler, B.S.E.E., 1947, The College of the City of New York; M.S.E.E., 1948, Polytechnic Institute of Brooklyn; Bell Laboratories, 1948—. Mr. Staehler's early work was on No. 5 Crossbar, toll signaling systems, and trainers for guided missile systems. In 1953, he worked on the development of electronic switching systems, specifically, the processor memory for the experimental central office in Morris, Illinois, and the processor logic and call memory for No. 1 ESS. He was appointed Director of the Electronic Switching Projects Laboratory in 1964 with responsibility for special applications for No. 1 ESS to military and data networks, including No. 1 ESS AUTOVON. In 1968, he was appointed Director of the Electronic Systems Design Laboratory with responsibility for development of the 1A Processor. In 1976, he was appointed Director of the Operator Services Laboratory with responsibility for extending the automation of operator services. Member, IEEE, Eta Kappa Nu, Tau Beta Pi, Sigma Xi.

C. F. Starnes, B.S.E.E., 1964, Oregon State University; M.S.E.E., 1965, Oregon State University; Bell Laboratories, 1965—. Mr. Starnes has worked on integrated-circuit design, test-facilities development and electromagnetic compatability. He is a supervisor in the Field System Department, responsible for the development of system acceptance tests, generic program retrofit, and system hardware growth.

E. H. Stredde, B.S.E.E., 1966, and M.S.E.E., 1967, University of Illinois; Bell Laboratories, 1967—. Mr. Stredde has worked on No. 1 ESS software development for pheripheral fault recovery, trunk maintenance, and software integrity verification, and transient memory initialization. He has alwo worked on 1A Processor software design of system-recovery programs and is currently working on software design of international call-processing features for No. 4 ESS. Member, Eta Kappa Nu, Tau Beta Pi.

G. A. Van Dine, B.S.E.E., 1956, Purdue University; Bell Laboratories, 1956—. Mr. Van Dine initially worked on digital circuit designs for NIKE Missile Systems, and subsequently for delay line storage systems and magnetic tape stores on the UNICOM and No. 1 ESS ADF Systems. He later worked on cathode ray tube display system techniques. Since 1967, he has supervised the development of computer-driven test facilities for 1A Processor frames, and the utility system used for monitoring and control of the 1A Processor in the system laboratory environment. He subsequently supervised a group responsible for No. 4 ESS reliability studies.

R. J. Watters, B.M.E., 1948, Cornell University; Bell Laboratories, 1948—. Mr. Watters has worked on the design of several military systems. In 1965, he was appointed head of a department responsible for the design of maintenance for the No. 1 ESS AUTOVON system. Since 1968, he has had the responsibility for design of diagnostic programs for the 1A Processor. He currently is Head of the Processor Application and Software Department which has the software responsibility for the 3A Processor. Member, Association of Computing Machinery, Tau Beta Pi.

P. W. Wendland, B.S.E.E., 1965, and M.S.E.E., 1966, Cornell University; Bell Laboratories, 1966—. Mr. Wendland has been involved in subsystem and system testing of the 1A Processor. He presently supervises a group responsible for design of 1A Processor man-machine interface circuits and teletypewriter data link circuits.