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1A Processor:

Organization and Objectives

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This paper presents an overview of the 1A Processor in terms of objectives, design philosophy, major features, and applications in the Bell System. It also serves as an introduction to the detailed technical papers that follow.

I. INTRODUCTION

A steady and rapid increase has occurred in urban and toll traffic and service features during the past decade. This has highlighted the need for large, high-traffic capacity electronic switching systems for local, tandem, and toll applications in the Bell System. The 1A Processor[1-3] has been developed to meet this high-processing capacity need. It is a stored program processor having a basic instruction execution speed of 700 ns, a memory access speed of 1400 ns, direct-memory access to bulk memory and data links, and a peripheral bus system and associated controls for interfacing to the switching networks. The technology is based upon beam-leaded integrated circuits that are used for most logic functions. A common processor was designed for use in a variety of applications to minimize the expenditure of both development and manufacturing resources.

The 1A Processor provides a number of improvements over its Bell System predecessors. It executes instructions faster, provides more program and call storage capacity, and permits more rapid program and translation changes. It also employs an improved order structure that

uses less storage and leads to more efficient program development. In addition to space, power, and cost reductions, it provides improved trouble detection and repair, shorter installation intervals, and increased dependability. The maintenance programs and fault-recognition programs are an integral part of the processor. It has stand-alone capability that permits use in a variety of applications.

The intent here is to outline the objectives, design philosophy, major features, and applications of the 1A Processor and to provide an introduction to the more detailed technical papers that follow.

II. OBJECTIVES

2.1 Capacity

Capacity objectives for the 1A Processor were set to meet the processing needs of electronic switching systems, which must handle about 500,000 busy-hour calls in a toll environment.

2.2 Flexible network interface

Another objective in the design of the processor was a flexible network interface that permits control of either the space-division network used in No. 1 ESS that requires central pulse distribution enabling or the time-division network used in No. 4 ESS that uses coded enabling.

2.3 Dependability

Bell System electronic switching systems must provide dependable telephone service 24 hours a day during the life of the system. Converting this requirement to a specific design objective, a service interruption which results in a total loss of service, should average less than 3 minutes per year per office.

Since total loss of service can be caused by facilities other than the processor, the processor has been allocated only two-thirds of the downtime; that is, 1A Processor service interruptions that result in a total loss of service should be less than 2 minutes per year per office.

2.4 Self-sufficiency

The processor was designed with the capability of stand-alone operation. In other words, it consists of a self-sufficient hardware-software package that permits self-testing without any auxiliary equipment.

2.5 Program compatibility

Another important goal was the ability to retrofit the processor into capacity-limited operational No. 1 ESS offices. To achieve compatibility, the No. 1 ESS instruction set was included as a subset of the 1A Processor instruction set. This allows well-tested No. 1 ESS call-processing pro-

grams to be semiautomatically computer-translated for operation on the 1A Processor.

2.6 Environmental

The processor was designed to operate over a wide temperature and humidity range. Specifically, the worst-case range is from 0°C to 50°C and from 20 percent to 80 percent relative humidity.

2.7 Economy

The processor was designed to be economically competitive with its predecessors, while still adhering to the preceding objectives. To minimize development and manufacturing costs, a low-cost standardized technology based on integrated circuit building blocks was used, and computer aids were concurrently developed to accelerate all aspects of hardware and software development, manufacture, and test.

2.8 Other objectives

Many other objectives were established for the 1A Processor. For example, the processor should require minimum floor space, energy consumption, and installation time, while maintaining enough of a structural similarity to the No. 1 ESS processor and standardized input/output message format to minimize additional training required for experienced ESS craftspersons.

III. DESIGN PHILOSOPHY

3.1 Standardized technology[4]

The ultrahigh performance requirements of the 1A Processor require maximum use of integrated-circuit and thin-film techniques. The packaging methods used in the first generation of electronic switching systems are not adequate for such complex and advanced circuitry. As a result, a fundamental premise in the design of the 1A Processor was recognition of the need for a new and innovative packaging approach. To meet this need, a standardized packaging system called 1A technology was developed.

1A technology consists of a set of standardized high-performance devices and packaging techniques that provide miniaturization, high-speed performance, low-energy consumption, ultrareliability, low-cost manufacture, and ease of installation and maintenance. These elements form the basic building blocks for the processor. Application guidelines stress design standardization and full connectorization of packs, units, and frames. Connectorization permits rapid assembly of complete pro-

cessors for comprehensive factory testing, rapid disassembly for shipping, and rapid reassembly of a pretested processor on site. It also provides for rapid repair and maintenance. The guidelines also specify a standardized, fixed floor plan, which is applicable to local, tandem, and toll offices and provides graceful store growth. The net result is a reduced engineering and cabling effort and a shortened telephone company order to service interval.

1A technology is designed for use in a broad spectrum of other digital units or processors. It is used in the space-division networks of No. 1 ESS, No. 2 ESS, and No. 3 ESS; the processor of No. 2B and No. 3 ESS; and the time-division network of No. 4 ESS.

3.2 Improved development methods

In the formative stage of the project, it was evident that methods used in the development of the first generation of the electronic switching system family were inadequate for the development of the new generation. This was due to the complexities of integrated circuit technology as well as the increased size of the software package. Hence, a decision was made to designate the attainment of improved development techniques as a specific goal and to form organizations chartered to achieve this goal. The thrust for new techniques was designated as the development of development methods.[5] The main objectives were improved quality, enhanced diagnosability, assured manufacturability, reduced cost, shortened intervals, and more efficient utilization of the members of the development team.

As a result, Bell Laboratories has developed a complete computer-based data-management facility that permits design specifications to be introduced into a massive data base and enables their subsequent use by complex application programs (see Fig. 1).

The design verification, physical design, documentation, and manufacturing application programs have been essential to the development of the hardware and software of not only the 1A Processor, but also the networks of No. 1 ESS, No. 2 ESS, No. 3 ESS, and No. 4 ESS, and the processor of No. 2B ESS and No. 3 ESS.

The application programs include both automatic and interactive capabilities. The latter permits the designer to interrupt, query, and make changes as an application program is run.

Use of a general-purpose computer with virtual memory simplified the storage of massive quantities of data and made feasible the simulation of large-scale systems containing tens of thousands of gates. For example, simulation of the 50,000-gate central control eliminated many clerical encoding and logic errors at a time when the only existing central

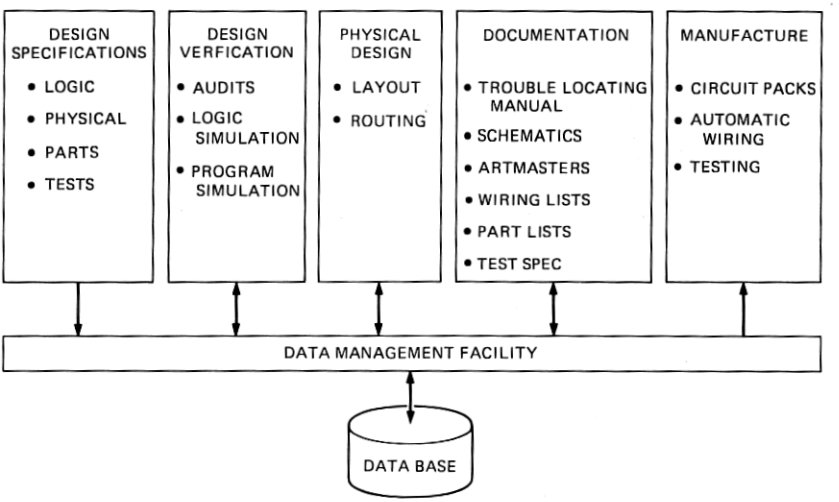


Fig. 1—Computer-aided design.

control was "logically built" in the memory bank of a general-purpose computer.

Interactive simulators were also used to validate new system or program strategies, to design programs, and to debug programs that have been designed. Simulation was found to be an effective debugging tool for all types of programs including fault recovery and diagnostic programs.

The need for a sophisticated laboratory software testing tool triggered the design of a comprehensive utility test system. The hardware consists of over 80,000 gates and 16,000 words of memory. It provides an electrical and time buffer between the processor and a utility minicomputer. The system, the minicomputer in conjunction with its resident utility program, provides direct and conditional control over any processor-resident program as well as monitor, trace, load, and dump capabilities.

3.3 Integrated development, manufacture, and test[6]

The need to automatically convert a staggering volume of design information was recognized as an integrated part of the development methods. To meet this need, application programs were designed to extract manufacturing information from the data base in the general-purpose computer. This information is used by Western Electric to generate artmasters for the plated-interconnection patterns on both circuit packs and printed-wire backplanes, and to produce machine-readable data to control wiring machines for automatic wiring of those connections, which are not contained on the printed-wire backplanes.

Bell Laboratories and Western Electric engineers collaborated on the development of computer-controlled test facilities. The test sequences are verified using the design data base and are used to program minicomputers that control a variety of test stations that test everything including interconnection patterns, circuit packs, backplanes, frames, and complete processors. The processor test sequences from the data base are also used for installation and performance testing in the field.

Still another set of application programs use the design data base to generate documentation such as schematic diagrams and wiring lists.

IV. PROCESSOR ORGANIZATION

4.1 Hardware[7,8]

As shown in Fig. 2, the general architecture of the 1A Processor is similar to the No. 1 ESS processor[9], except for the provision of a direct-memory-access feature for auxiliary units. This is accomplished over an auxiliary unit bus on the central control. Thus, data can be transferred between program and call stores, and file stores, tape units, and external data links with minimal interference with other processor activities. This feature is essential to the achievement of the modern services planned

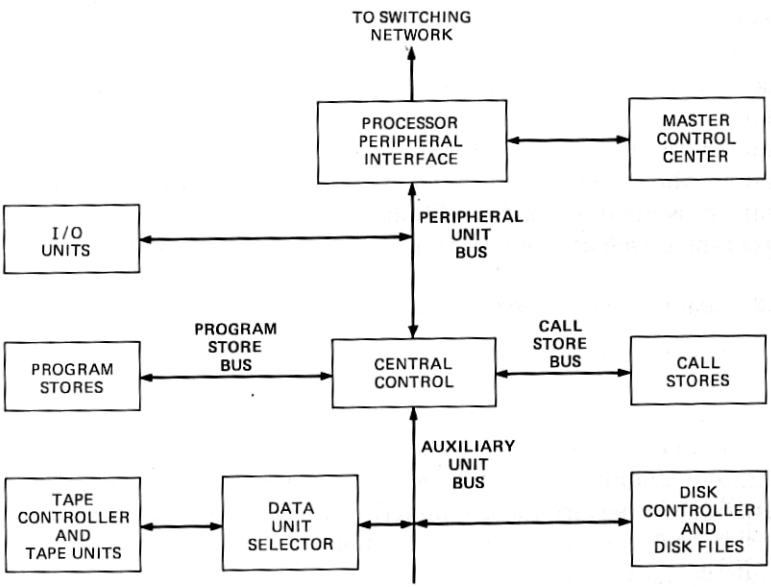


Fig. 2—1A Processor block diagram.

for electronic switching systems without impacting heavily on the call-processing capacity of the system.

The direct-memory-access feature also permits a varied spectrum of maintenance programs to be retained on lower-cost file stores with programs paged into high-speed random-access stores only as needed. Substantial reduction in high-speed memory can thus be realized. Furthermore, many maintenance features, which were not included in earlier generation electronic switching systems because of a high-cost penalty, are now economically provided in the 1A Processor.

High-speed, low-power DTTL logic integrated circuit devices are used for all logic circuits. The beam leads of the chips are thermocompression bonded to a ceramic substrate. The complete ceramic is mounted on a supporting aluminum plate and bonded to a male-connector assembly.

Program and call stores contain two magnetic core modules and are capable of storing 65,536 words of 26 bits (24 data bits plus 2 parity bits). File stores contain four magnetic disks and are capable of storing a total of 64 megabits. A sufficient number of each type of store is provided to meet the needs of each of the contemplated processor applications.

In the 1A Processor, all subsystems have redundant units and are connected to the basic system via redundant bus systems. Thus, it is possible to operate at full capacity with faults in some units.

The central control units are fully duplicated; they normally operate in step and compare results.

The program store community consists of a prime set plus two additional (or "roving spare") stores. If one of the prime stores fails, the program that is contained in that store is transferred from the duplicated copy of the system program contained in the file store to one of the "rover spares."

The call-store community consists of a prime set plus a full on-line duplicate set for only those stores that contain transient call data. For those stores that contain translation data, one of the duplicated stores containing transient call data is preempted and loaded with the necessary translation data from the duplicated copy in the file store.

Remaining critical units in the processor are duplicated while less critical units are not duplicated.

4.2 Maintenance software[10]

Error-detection is the basis for automatic detection and resolution of problems without service interruption. This is achieved through matching of duplicated units, parity checks on communications (both address and data) over all buses, interval self-checking in hardware units

(control pulsing, timing, internal data transfer), and system sanity timers.

A failure reported by any one of these error-detection schemes triggers a program interrupt, and control is transferred to a fault-recovery program. This program verifies that a fault is present, identifies the most probable subsystem or unit, and then removes the faulty unit from service by reconfiguring the system to maintain call-processing capability. The intent is also to retain as much redundancy as possible in the remaining hardware units in the working configuration.

Special programs, called restart programs, set a diagnostic-request flag and save any data that will aid in identifying trouble symptoms. Upon completion of these actions, system operation is continued by returning control to the interrupted program.

Maintenance experience with earlier generation electronic switching system processors clearly highlighted a need for rapid repair through the use of a comprehensive set of diagnostic tests. To meet this need, a number of diagnostic practices, which differed significantly from those employed in the sixties, were introduced. These practices included organization of the development team to emphasize early and continuing diagnostic planning and execution, use of a common standard macro-oriented test design language, and application of a complementary fault-simulation process involving the merging of logical simulation in a general-purpose computer with physical simulation in an operational system laboratory.

The resulting diagnostic programs differ from those used in previous electronic switching systems in that they are also used, as noted earlier, for computer-controlled hardware testing in the manufacturing plant and during installation on the telephone company site.

Hardware or software errors can cause mutilation of the program or data base. Special programs for mutilation detection provide for a progressive verification of integrity. If the mutilation is minor, audit programs analyze the affected data base and correct any errors on a time-shared basis with normal call-processing programs. If the mutilation is severe, the call-processing program is stopped until the mutilation programs are regenerated by transferring the backup information from file memory.

4.3 Administrative software

To provide a number of the required 1A Processor capabilities, an extensive set of administrative programs was developed and is included in the processor software package. (These perform many of the functions normally included in an operating system, but since program control is not included, it would not be correct to use that term here.)

These programs serve many functions, such as: transferring data between the call and program stores and the auxiliary units such as the file store, tape store, and input/output terminals; transferring programs into the program store from the file store; controlling (on a predetermined priority basis) the execution of deferred programs in a time-shared mode with call-processing programs, gathering all system-detected trouble symptoms and recording them in the file store for later analysis (these data include audit errors, interrupt reports, fault recovery actions, and diagnostic failure results); executing utility features permitting on-site analysis; temporarily allocating and loading stores for special programs; and providing an on-line complete and partial update capability.

V. APPLICATIONS

5.1 Large toll offices—No. 4 ESS[12]

On January 17, 1976, the first 1A Processor for toll applications was cut into service as the common control for the No. 4 ESS toll switching office in Chicago (see Fig. 3). No. 4 ESS uses a solid-state time-division network and can switch up to 550,000 peak busy-hour calls from 107,000 trunks. It is described in a future special issue on No. 4 ESS. The second No. 4 ESS was cut into service in Kansas City on July 3, 1976.

Two more No. 4 ESS offices are expected to become operational in 1976.

5.2 Metropolitan local offices—No. 1A ESS[13]

On October 15, 1976, the first 1A Processor for local applications cut into service as the common control for the No. 1A ESS local switching office in Chicago (see Fig. 4).

No. 1A ESS uses a remreed space-division network and can handle up to 240,000 peak busy-hour calls and about 100,000 line terminations. No. 1 ESS call-processing programs are semiautomatically computer-translated to operate on the 1A Processor. The 1A Processor occupies less than one-half the space of the No. 1 ESS processor.

5.3 Retrofit into No. 1 ESS offices

Plans call for the 1A Processor to replace the No. 1 ESS processor in capacity-limited working offices (the first retrofit is scheduled for 1978). The new processor will provide more than twice the present call-processing capacity of a No. 1 ESS.

VI. PERFORMANCE

6.1 Laboratory

Prior to field service, extensive laboratory testing was conducted during which over 100,000 processor hours were logged. This testing

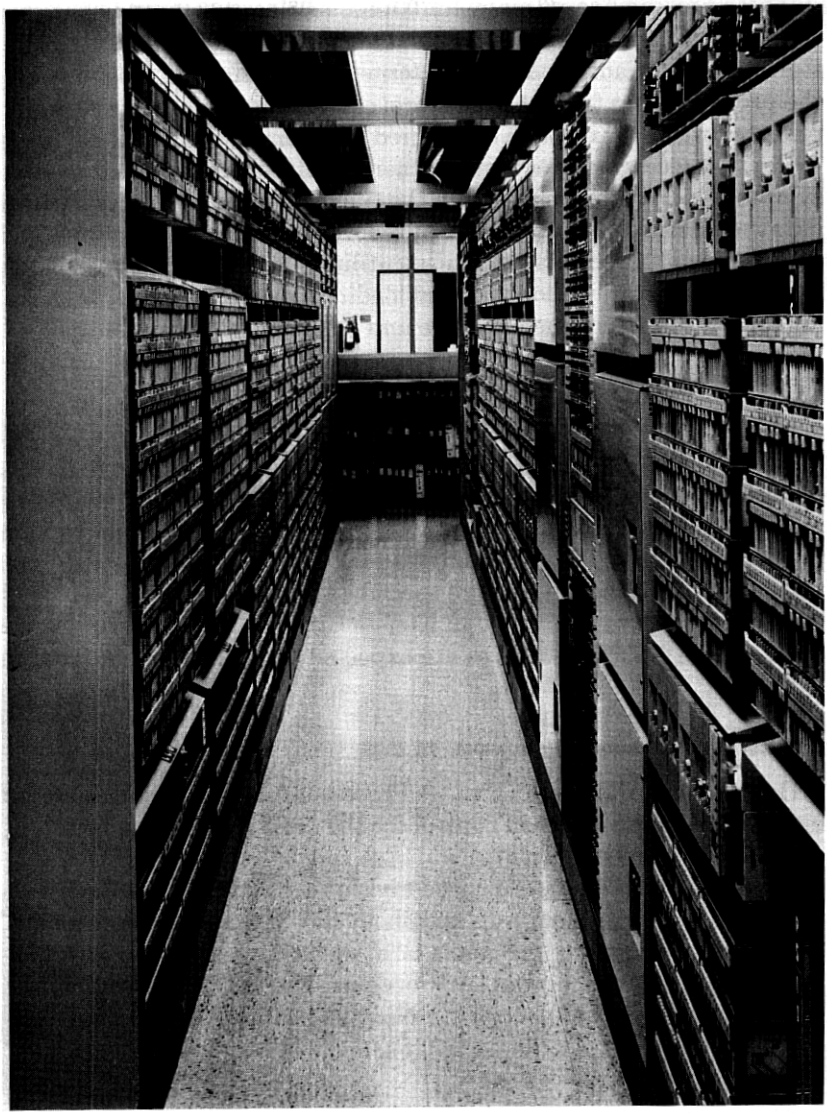


Fig. 3—1A processor in No. 4 ESS (Chicago toll office).

indicates that the design objective of hardware component reliability, automatic isolation of faulty units without service interruption, rapid repair, and automatic recovery from program and data mutilation are being met. More detail is presented in the associated papers.

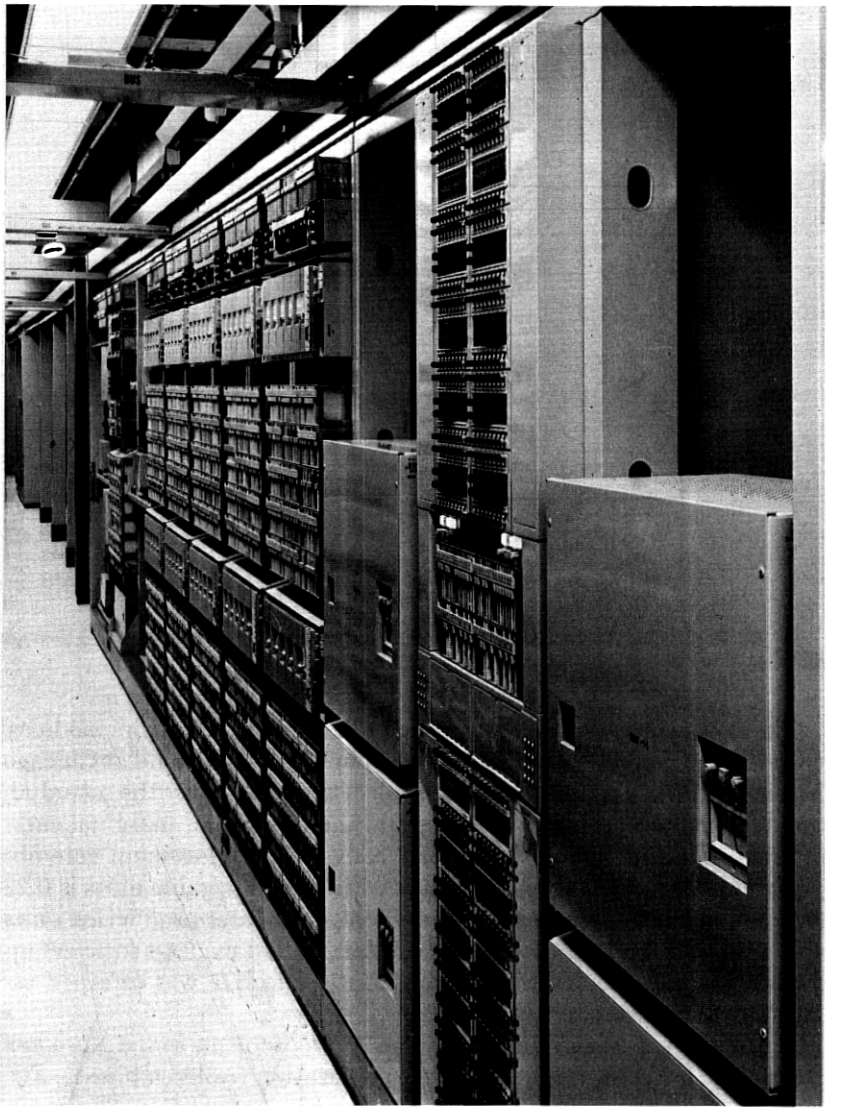


Fig. 4—1A Processor in No. 1A ESS (Chicago local office).

6.2 Field

Field performance of the 1A Processor in both No. 4 ESS and No. 1A ESS has been excellent. This is best illustrated by key operational data gathered from the first two offices put into service.

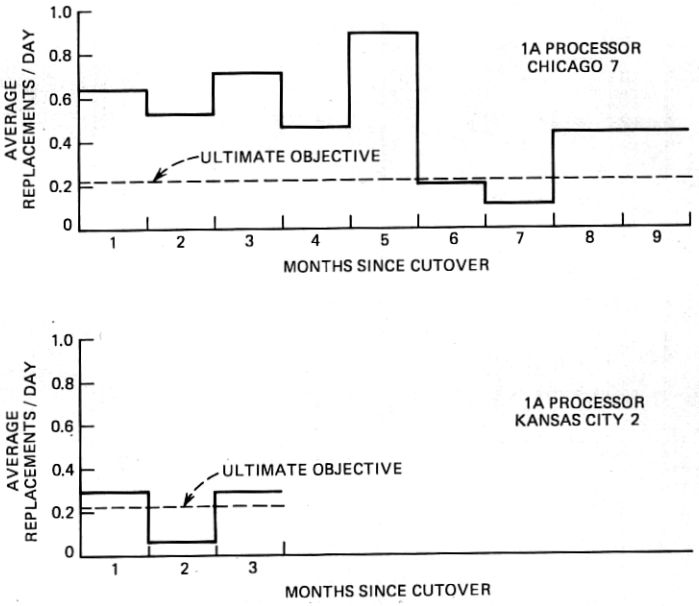


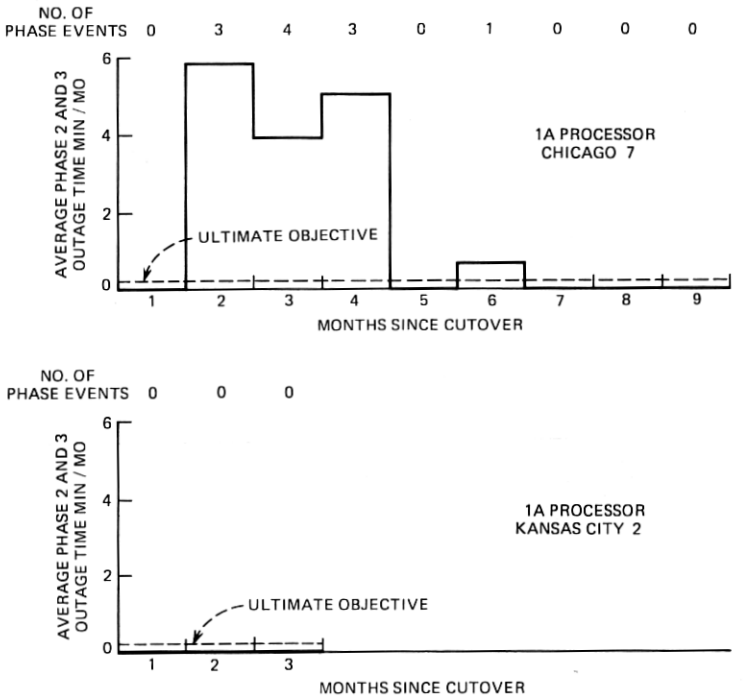
Fig. 5—Replacement rate for pluggable units in the 1A processors in No. 4 ESS through October 1, 1976.

The replacement rate for pluggable units (circuit packs, core modules, power modules) in both offices is shown in Fig. 5. The trend at Chicago 7 shows a marked reduction in the replacement rate after the introduction of some design improvements and the removal of marginal early production units. The ultimate or steady-state replacement rate objective for the 1A Processor complex with 7000 pluggable units is 0.22 unit per day. The data from Kansas City 2 (with later production units and where design improvements were introduced prior to cutover) indicate that the ultimate replacement rate objective was attained essentially at cutover.

Hardware, software, or memory mutilation problems in the No. 4 ESS can result in the need for system reinitialization (called a phase). Fig.

TYPE OF PHASE	DURATION (SECONDS)	EFFECT OF PHASE
1	1	NO SERVICE EFFECT
2	27	TRANSIENT CALLS LOST
3	40	TRANSIENT CALLS LOST
4	40	ALL CALLS LOST

Fig. 6—No. 4 ESS reinitialization phase structure.



NOTE: NO PHASE 4 OR TOTAL SYSTEM OUTAGE TIME CAUSED BY 1A PROCESSOR IN CHICAGO 7 AND KANSAS CITY 2

Fig. 7—Phase events and outage time in No. 4 ESS caused by 1A Processor through October 1, 1976.

6 shows the No. 4 ESS reinitialization phase structure. Note that a phase 1 has no system effect. Phases 2 and 3 result in the retention of established calls, but the loss of transient calls. Phase 4 results in a total system outage with a loss of all calls.

Fig. 7 shows both the number of phase 2 and 3 events as well as the average phase outage time by month caused by the 1A Processor for both No. 4 ESS offices. The outage time represents the duration of the phase, during which established calls were retained, but no new calls were established. The trend at Chicago 7 shows a rapid reduction in the frequency and outage time for phase 2 and 3 events as the causes of the phases were determined and corrected. The ultimate or steady-state total 1A Processor phase outage time objective is 0.16 minute per month or 2 minutes per year. Note that at Kansas City 2 there have been no 1A Processor phase events or outages.

As noted in Fig. 7, no phase 4 or total system outage has been caused

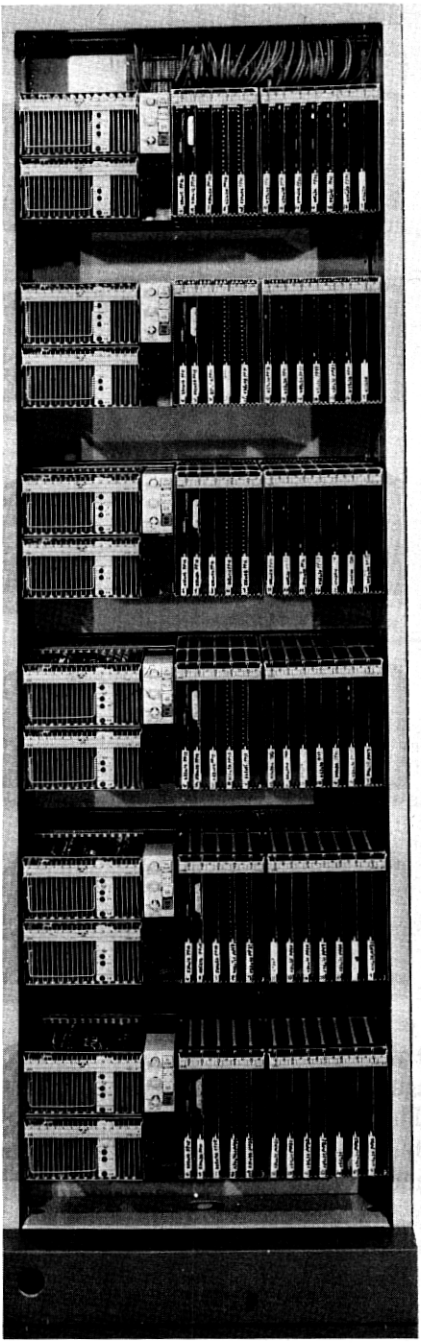


Fig. 8—Program and call stores using 4 K MOS integrated-circuit devices.

by the 1A Processor in either Chicago 7 or Kansas City 2.

VII. CONCLUSION

After logging more than a total of 8000 in-service hours, 150,000 laboratory and field hours, 4 million unit hours, 350 million ceramic integrated-circuit pack hours, and 10 billion semiconductor integrated-circuit hours on the 1A Processor, overall performance indicates that the design objectives are being realized.

Nevertheless, constant attention is being given to possible areas of improvement. 1A technology was designed so that larger scales of integration could be smoothly introduced into the 1A Processor. Furthermore, as with the No. 1 ESS processor, as technological advances occur, it is expected that subsystems can be redesigned and smoothly introduced into the 1A Processor. A specific example is a program and call store using 4 K MOS integrated-circuit chips in place of magnetic cores. These stores require less space and power than the magnetic core stores currently used in the 1A Processor. As shown in Fig. 8, six stores (over 10 megabits) can be mounted in one 2-foot, 2-inch bay. The integrated circuit program and call store is currently being manufactured by Western Electric with shipment expected in early 1977. These continuing refinements of the 1A Processor should provide additional improvements in performance as well as additional economic advantages.

VIII. ACKNOWLEDGMENT

The design of the 1A Processor required the cooperative efforts of hundreds of people in Bell Laboratories, Western Electric, and A.T. & T. The author wishes to acknowledge the contributions of all the team members whose work is summarized herein.

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