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***Remreed Switching Networks for No. 1 and No. 1A ESS:***

# Remreed Network Electronic Control

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*The new remreed network was designed to reduce the cost and the size of the No. 1 ESS network. It uses a new self-latching sealed contact and a new switch-package design. This new package includes components directly related to the control of the switch. Remreed network control, the subject of this paper, is all electronic. It uses a mixture of silicon integrated circuits and discrete circuits to accomplish its control functions.*

*The network topology and modularity has not been changed. The design was undertaken with the goal of complete compatibility with all existing system programs, including fault-recognition and diagnostic programs. This has permitted the addition of remreed networks to existing No. 1 ESS offices with no program changes or modification of ferreed networks. The resulting remreed-ferreed mix is operated and maintained by the same software.*

*The new network offers reduced manufacturing costs, simplified installation, improved reliability and maintainability, and a 3:1 to 4:1 space reduction.*

## I. INTRODUCTION

A new technology has evolved in designing and assembling central office equipment. This new technology has reduced the cost and size of a No. 1 ESS office. The remreed controller uses low-level, high-speed, integrated-circuit logic for all its information-processing functions. Higher-voltage integrated and discrete circuits interface with PNPN transistors in the network control path. Standard 24-V central office battery is the primary source of power. It is converted locally to low voltage levels to provide power for the integrated circuits.

Automatic machine wiring is used to interconnect circuit packs and construct wired backplanes. Other interconnections are made using connectorized cables and flat ribbons. Flexible circuits are used in switch packages and will also be used in grids and concentrators. The remreed network has become fully connectorized.

A dramatic size reduction has been achieved. One fully equipped trunk link network can now be assembled in one shippable unit compared to eight separate frames required for one ferreed trunk link network.

The new network controller has been designed and organized to be compatible with all existing No. 1 ESS programs. This requirement determines how much network fabric is assigned to one controller. It determines the method a controller must use in reporting its normal and diagnostic functions and also the sequence of events that must take place during an operating cycle.

## II. ELECTRICAL DESIGN

### *2.1 Basic features*

The remreed network is made up of four different switching circuits. These are the 2:1 line-switching circuit which uses 12A concentrator grids, the 4:1 line-switching circuit which uses 13A concentrator grids, and the trunk- and junctor-switching circuits that use 11A and 10A grids, respectively.[1] These four circuits are all different in size and organization, but basic control functions are common.

Figure 1a illustrates a remreed crosspoint.[2,3] The figure shows the reed contacts and two pairs of differently wound windings. One pair is associated with a vertical control path and the second pair is part of the horizontal control path. The reeds will close and latch if a current pulse passes through the vertical and horizontal control winding simultaneously. Pulsing through either the vertical or horizontal windings alone magnetizes the reeds opposing and, thus, releases the contact.

The remreed crosspoint has the same destructive mark feature as the ferreed crosspoint. The choice of 64-31 turns of 29-gauge wire is an electrical and physical compromise. The crosspoint will be in an all-electronic-control environment. From an electrical control standpoint, it is desirable to have a large number of turns of heavy-gauge wire to minimize both current and voltage. The opposite is true from a physical design standpoint. The chosen number of turns and wire gauge is therefore a compromise. The impedance of the pulse path is dominated by the ohmic resistance of control windings. A typical path through a grid has about 23 ohms resistance and requires 96 V of driving potential.

The flux through the ferreed contact during operate pulsing is opposite to the holding flux. Each time a closed ferreed contact is pulsed, the flux through the contact will reverse. The flux will go through zero and cause the contact to open momentarily. The reversal of flux does not take place in the remreed crosspoint. The contact

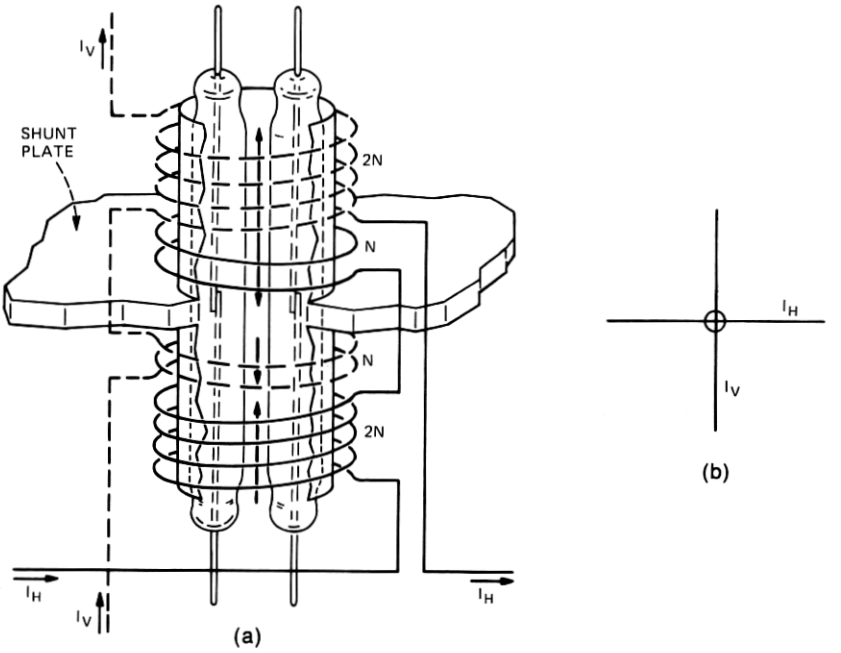



Fig. 1—(a) Remreed crosspoint. (b) Schematic symbol.

members contain the magnetomotive force for latching and, during reoperate of a closed contact, the flux density will change but the direction of the flux will remain the same and the contact will remain closed. This modulated flux density will cause magnetostrictive elongations of the reeds. This motion produces scrubbing of the contact surfaces which can cause cold welding. The retractile forces available may not be enough to overcome the bonds and the contact will stick. Therefore, a standard remreed operating cycle will initially deliver a prerelease pulse to ensure that the crosspoint is open prior to the operate pulse.

A 4-A, 1-ms-wide prerelease pulse will be steered along the vertical column of control windings to release the contacts that the subsequent operate pulse will close. This prerelease action is performed simultaneously in both stages of a concentrator or grid. The operate pulse has an amplitude of 4 A and a width at the base of about 4 ms. Figure 2 illustrates the events.

### *2.2 Basic control functions*

A remreed switch package is assembled by forming a matrix of crosspoints. The vertical control windings are interconnected to form

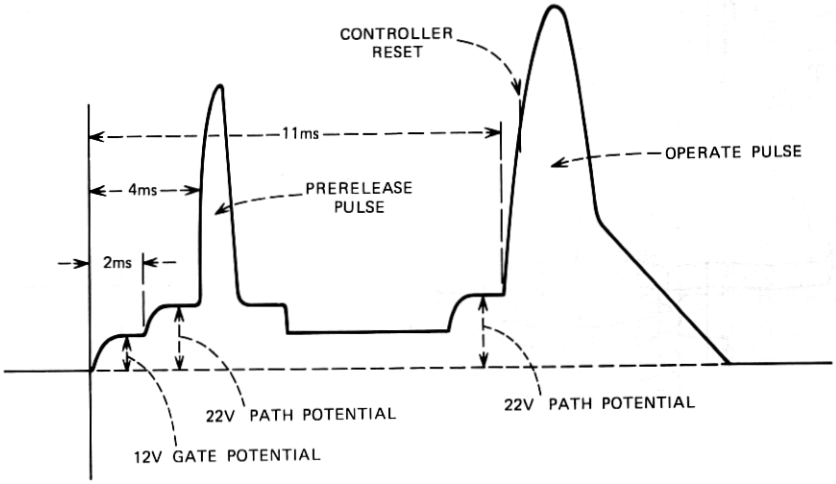



Fig. 2—Voltage at positive pulser terminal.

columns and the horizontal windings are interconnected to form rows. The reed contacts are interconnected to form a contact matrix that corresponds to the control-pulse-path matrix. Such an interconnected matrix is referred to as a switch. More than one switch may be assembled in one switch package. Switch packages are interconnected to form larger arrays called either concentrators or grids. The concentrators and grids have the same dimensions and topology as in the present ferreed network.[4]

PNPN transistors are used in pulse-path arrays and also external to the arrays to select a unique pulsing path. Both concentrators and grids are two-stage arrays. Stage 0 contains input switches and stage 1 contains the output switches. PNPN transistors used to select an input or output switch are located inside the switch package. All vertical columns and horizontal rows contain series-connected diodes that are also part of the switch package.

A unique pulse path is established by selectively "turning-on" PNPN transistors. A path normally consists of an input level, input switch, output switch, and output level. Some pulse paths through a concentrator or grid are partial paths. The remove-cutoff and restore-cutoff functions are examples of orders requiring partial paths through a concentrator. Operate no-test and remove no-test are examples of partial paths through a junctor grid.

A PNPN transistor and some associated control components are used in all stages of selection. These components are located inside switch

packages and on external circuit packs. Figure 3 illustrates the PNPN transistor and its control components.

This group of components is used in every stage of selection. It provides means for detecting any component failure. Any number of these groups of components may be connected in series for multistage path selection. In this description the N-emitter will be referred to as the cathode and the P-emitter as the anode. The two diodes connected to the base provided access to the PNPN-transistor from two sources. In this case two controllers may have access to this transistor. The PNPN transistor chosen requires a minimum gate current of 5 mA and it has a maximum latch current of 16 mA.

The 430-ohm resistor provides terminations for the gate current. The diode in series with the cathode permits the formation of merging pulse-path nodes. The cathode may drive expansion nodes where each driven member of the node contains a diode.

A PNPN transistor is selected when a positive potential (+12 V) is applied to one of the gate diodes and the associated cathode resistor is terminated to circuit ground. The cathode resistor is terminated to ground through one or more saturated transistors. This gate-drive and cathode-terminating scheme permits using the PNPN transistor as a selection device in a two-dimensional selection matrix. Gates are interconnected along one dimension and cathode resistors are interconnected along the second dimension.

The gate-current path is perpendicular to the pulsing or holding path as shown in Figs. 3 and 4. This combination of PNPN transistors and associated components is used in all concentrators and grids for selecting a unique path. This scheme permits cascading any number of these combinations in series without the familiar voltage ladder problem. In

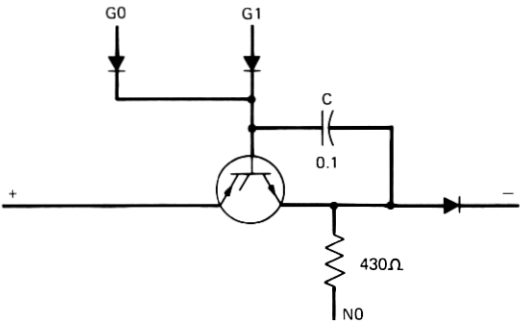
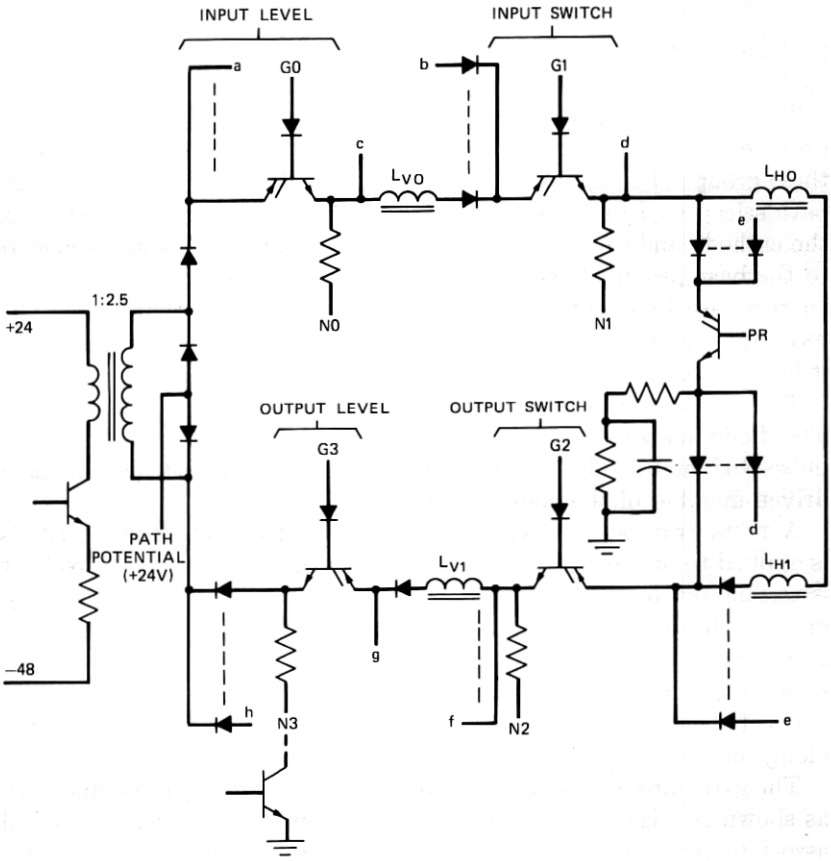



Fig. 3—PNPN transistor and associated control components.




a – TO OTHER INPUT LEVELS IN THE SAME GRID
b – TO OTHER INPUT LEVELS OF THE SAME INPUT SWITCH
c – TO CORRESPONDING INPUT LEVEL OF OTHER INPUT SWITCHES
d – TO OTHER OUTPUT SWITCHES IN THE SAME GRID
e – TO OTHER INPUT SWITCHES IN THE SAME GRID
f – TO OTHER OUTPUT LEVELS IN SAME OUTPUT SWITCH
g – TO CORRESPONDING OUTPUT LEVEL OF OTHER OUTPUT SWITCHES

Fig. 4—Basic pulse path.

addition, this scheme provides the means for detecting component failures or physical problems such as shorted conductors or open paths.

### *2.3 Gate drive and group check*

Each select group is driven by a current-limited voltage source. Each controller has six such voltage sources. The voltage applied to the gate of any PNPN transistor is limited to 12 V and the voltage source is designed to deliver a maximum of 34 mA. Figure 5 illustrates the circuit. The voltage source is turned on at the beginning of each

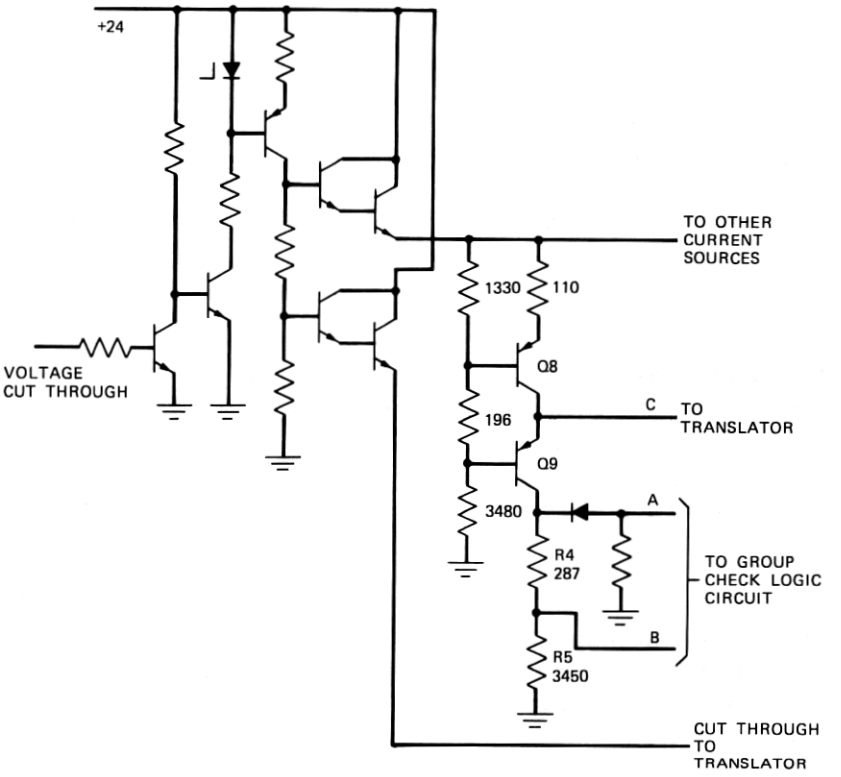



Fig. 5—Current-limited voltage source.

network cycle and turned off during the operate pulse. Only one PNPN transistor in each select group should be activated. This will draw 24 mA from each voltage source over the C lead and the remaining 10 mA flow through resistors R4 and R5. An excessive demand of current on any of the C leads will cause a "more-than" failure. A translator failure or addressing error that will attempt to select more than one PNPN transistor in any select group will demand more current from the gate driver than is available. A component failure in the pulse-path fabric, such as shorted components or shorts between components, will cause the same controller failure.

Similarly, a failure or error that fails to select any device in a select group will cause a "less-than" failure. There will be no demand for current on the C lead and all the current will go through R4 and R5. A connection logic circuit monitors the A and B leads in each group for failure states. It will indicate the type of failure and indicate the select group that has the failure. Strobing for group-check failure takes place about 2 ms into the network cycle. At this time all gate currents

should have reached their final value. If a failure is detected, the network cycle is aborted.

When the group-check test passes, it indicates that the address received is valid, the translators are giving valid outputs, and all transistors, diodes, and PNPN transistors involved in selecting a pulse path are functioning properly. As previously mentioned, the control path or gate-current path of a PNPN in this scheme is perpendicular to the pulse path, and the group check does not, therefore, indicate continuity in the chosen pulse path. A separate path check will sense for continuity between stages of the pulse path.

#### *2.4 Path check and pulsing sequence*

Figure 4 shows four select points interconnected to form a four-stage pulse path. This method of forming and selecting a unique pulse path is basic to all remreed circuits. Gate potential (+12 V) has been applied to all four PNPN transistors and gate current flows through the four cathode resistors. Since the voltage source for all gates is the same, gate current cannot flow forward into the succeeding stage. The forward voltage drop of the pulse-path diode and PNPN transistor prevents current from flowing between stages.

Checking for a pulse path starts after a successful group check. A +24-V path potential is applied to both the positive and negative terminal of the pulser circuit. The path-check circuit is part of the pulser circuit. The path potential will propagate forward through each selected stage, and path current will flow to ground through each of the cathode terminating resistors. The higher level of the path potential will back-bias the gate diodes and shut off the gate current.

Each PNPN transistor in the path changes from a gated state to an avalanched and forward-conducting state. The path-sensing circuitry in the pulser circuit will trigger at a path current of 120 mA and initiate the pulsing sequence. The path potential maintains the negative pulser terminal at +24 V. The pulser circuit is a constant-current pulser. Voltages along the path are determined by the impedances and voltage drops across PNPN transistors and diodes. Figure 2 illustrates the voltage waveforms at the positive terminal of the pulse and the sequence of events during an operating cycle.

The first event in the pulsing sequence is the prerelease pulse. The desired operate path remains selected; gate potential, path potential, and cathode-resistor terminations remain active. A 0.5-ms pulse is given to the gate of a prerelease PNPN transistor. This PNPN transistor (PR), shown in Fig. 4, shorts half the chosen operate path.

The prerelease current flows only along the vertical control windings of both stages and releases all closed contacts in those two verticals.

This release path shuts off after the 1-ms pulse. The R-C network in the cathode shuts the path off. In addition, the path potential is temporarily removed. The path potential is later reconnected. The initial operate path is again turned on and the operate-pulse sequence starts. The controller remains in its active state during the initial rise of the operate current. As the current goes through half its peak value, the controller will reset. Gate and path potential and cathode resistor terminations are removed. The pulse path becomes a semifloating path. The source of the path potential supplies the current that flows to ground through the cathode resistors during prerelease and the initial part of the operate pulse.

The control point in Fig. 3 shows a 0.1 $\mu$F capacitor connected between gate and cathode. All PNPN transistors in the pulse path have this capacitor. In the switch packages and in the assembled concentrator and grids, tip-ring conductors are carefully balanced to achieve crosstalk and impulse noise requirements.[5] This careful balance solves the problem of pulse-path-to-transmission-path impulse noise. The reverse is not true. The pulse path is an unbalanced segmented single conductor. It is susceptible to impulse noise coupling from the transmission path. The gate-to-cathode capacitor reduces the dynamic sensitivity of the PNPN transistor to any type of impulse noise.

### *2.5 Frames and circuits*

A ferreed line-switching circuit is mounted in a double-bay frame. A ferreed trunk-switching circuit is also mounted in a double-bay frame. The system refers to these circuits as frames in its input and output message nomenclature. A remreed line-switching circuit occupies less than half a single-bay frame and a remreed trunk-switching circuit occupies less than one-quarter of a single-bay frame. The system message nomenclature is in this sense not compatible with the remreed physical design.[6] The office craftsperson needs to make a mental translation of frame into circuits and bay into mounting plate.

The remreed network frame has one peripheral bus circuit per bay. This circuit converts the system ac bus to a dc bus within the bay. All circuits in the bay connect to the common bay bus. In the trunk-link network the number of peripheral cable receivers has been reduced by a factor of four. Similarly, each bay has one diagnostic bus-access circuit.

In the remreed network, the concentrators and grids are the smallest functional and physical units of the switching fabric. In a fabric sense, these are functionally identical to their ferreed counterparts. These units are the smallest replaceable fabric unit in the field. A 6-foot, 6-inch, double-bay frame contains a fully equipped and

factory tested 1:1 test link network. It contains a factory wired and tested connectorized B-link cable. It is the largest shippable network unit.

Remreed network topology and control partitioning is the same as in the ferreed network. Functional names and abbreviations in the remreed network controller design are the same as those used for similar functions in the ferreed controller.

One important objective of the new network design has been compatibility with the existing system programs and general system structure. All operating instructions are received over the peripheral bus. This bus is fixed both in number of information bits and in the coded format of the information. The number of bits on the bus and the information format was initially determined by the ferreed network electromechanical pulse-path-selection scheme. The information format is different for the different network circuits. The information is folded to achieve efficiency in the use of relay contacts in the ferreed pulse-path selectors.

#### 2.6 Power

Standard central office +24-V and −48-V power is used. Each bay terminates duplicated feeders of the two voltages into 32,000-$\mu$F filters. Each controller converts some +24-V power to +3.0 V using a dc-to-dc converter. This provides a single-point power source for all low-level integrated and discrete circuits within a controller. Each switching circuit dissipates about 50 W. The −48 V power is used primarily as a source of pulsing power.

## III. REMREED CONCENTRATORS AND GRIDS

This section examines the four types of network circuits and describes the use of the basic control principles introduced earlier in the article.

#### 3.1 The 2:1 concentrator

A 12A concentrator is a 2:1 concentrator. It has 32 inputs and 16 outputs. It is assembled from three switch packages, two 3C packages and one 2A package. These are interconnected either by a machine-wired backplane or a double-sided, flexible-circuit backplane. The 3C stage 0 switch package contains four 4-by-4 switch arrays and a pair of cutoff contacts* associated with each input level. In addition, the package contains a new reduced-size line ferrod for each input level.[7]

* The cutoff contacts are the same as any other fabric contact. Only the control windings are different to provide for individual crosspoint control.

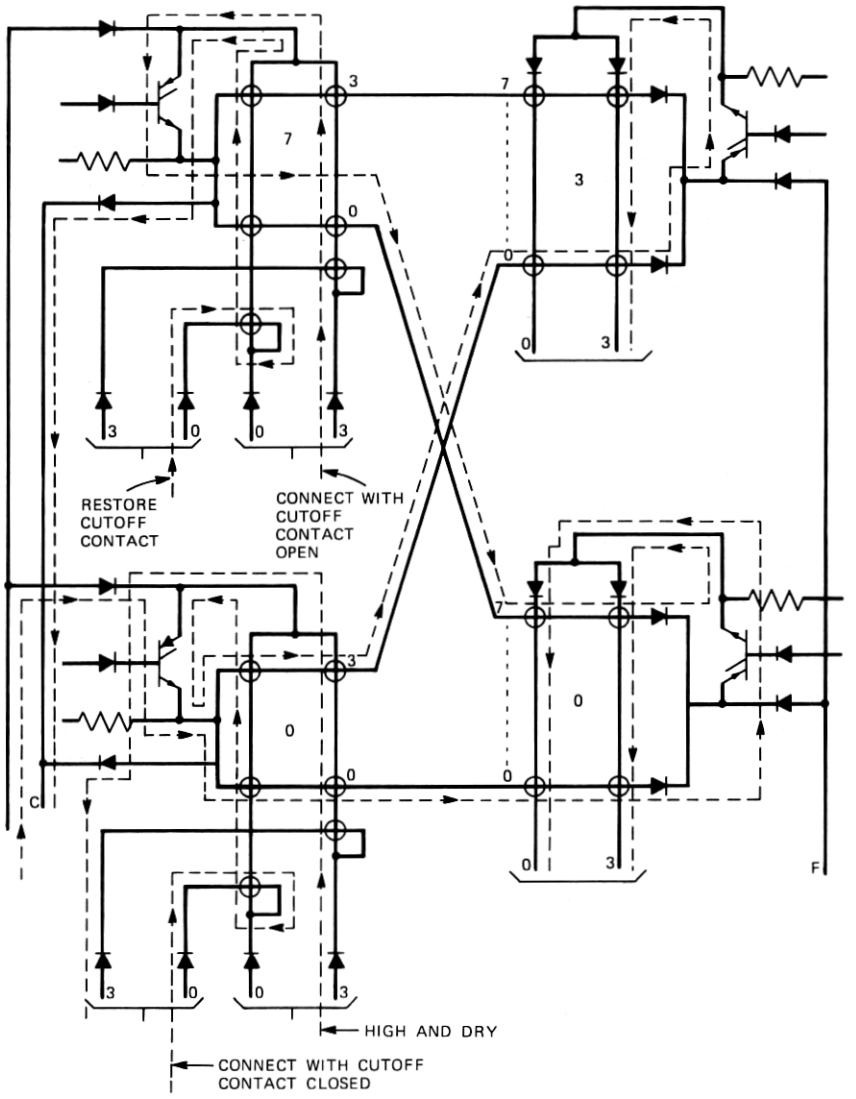



Fig. 6—12A concentrator.

Figure 6 illustrates the control path for a 2:1 concentrator. The PNPN transistors and other control components are part of the switch package. Four 16-conductor connectorized cables are connected to the rear of the concentrator to provide for all network control access. Same numbered input and output levels are interconnected and level selection is performed external to the concentrator.

Figure 6 illustrates typical paths the operate-current pulse will follow as a function of the order. The order group is a select group that determines the kind of path to be established. The other select groups determine the location of the path. Input level, input switch, output switch, and output level are path-select groups. The control of the cutoff contacts is determined by which group of input-level-control windings is chosen. With reference to Fig. 6, the right-hand group of inputs will cause the cutoff contacts to open. If the selected input level is in the left group, the cutoff contacts will close.

The prerelease path in a concentrator consists of two parallel paths. One path enters the selected input level in the right group and follows the vertical control winding of the selected input switch and exits over output C. The second prerelease path enters the selected output switch over input F and follows the vertical control windings that correspond to the selected output level.

The connect-with-FCG (OR2) prerelease path consists of only the output switch vertical control winding path. This order does not require closing the stage 0 crosspoints and the stage 0 prerelease path is not used. The operate pulse in this order opens a crosspoint in stage 0.

### 3.2 The 4:1 concentrator

Figure 7 illustrates the 13A concentrator. This 4:1 concentrator has 64 inputs and 16 outputs. The input switch is a limited-access switch. Each input level has access to four of the eight outputs. The 13A concentrator is assembled from four 4C switch packages and one 2B switch package. The switch packages are interconnected either by machine-wired or flexible-circuit backplanes. Each of the 4C switch packages contains one 16-by-4-out-of-8 switch, 16 cutoff switches, and their associated line ferrods. The switch is controlled as two separate 16-by-4 switches. Figure 7 shows two PNPN transistors associated with each input switch. One PNPN selects the even-numbered outputs and the other selects the odd-numbered outputs. The four physical input switches are controlled as eight electrical switches. Control path and prerelease paths are the same as for the 2:1 concentrator. All same-numbered input and output levels are interconnected. One set of 16 input-level-control paths are used with all orders that require the cutoff to open. The other set, the left-hand group in Fig. 7, is used to close the associated cutoff contacts.

### 3.3 Trunk and junctor grids

Figure 8 illustrates the control path of the familiar 64-by-64 octal trunk grid. The grid is assembled from four 1A and four 1C switch

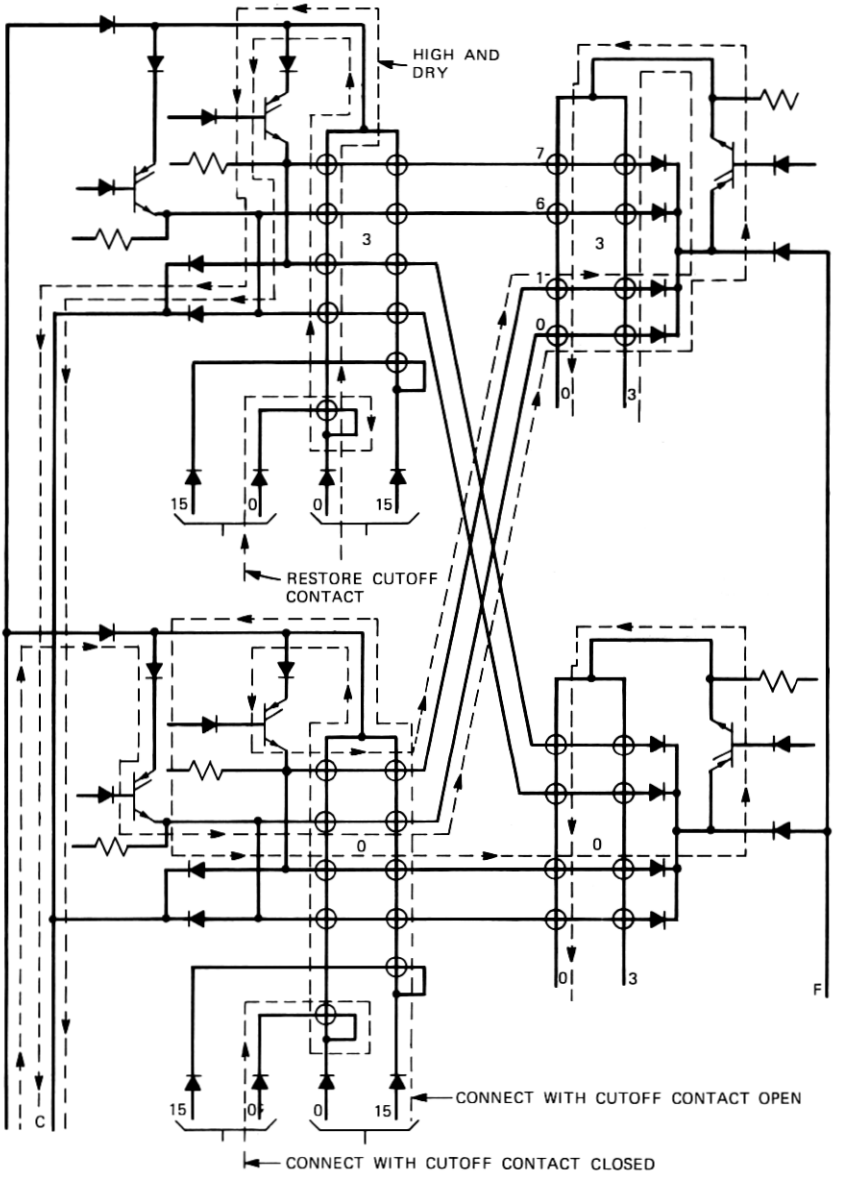



Fig. 7—13A concentrator.

packages. The switches are interconnected by either a machine-wired or flexible-circuit backplane. The interconnected unit is apparatus coded as the 11A grid. Four connectorized 16-conductor cables attach to a connector location in the backplane. These cables provide all the

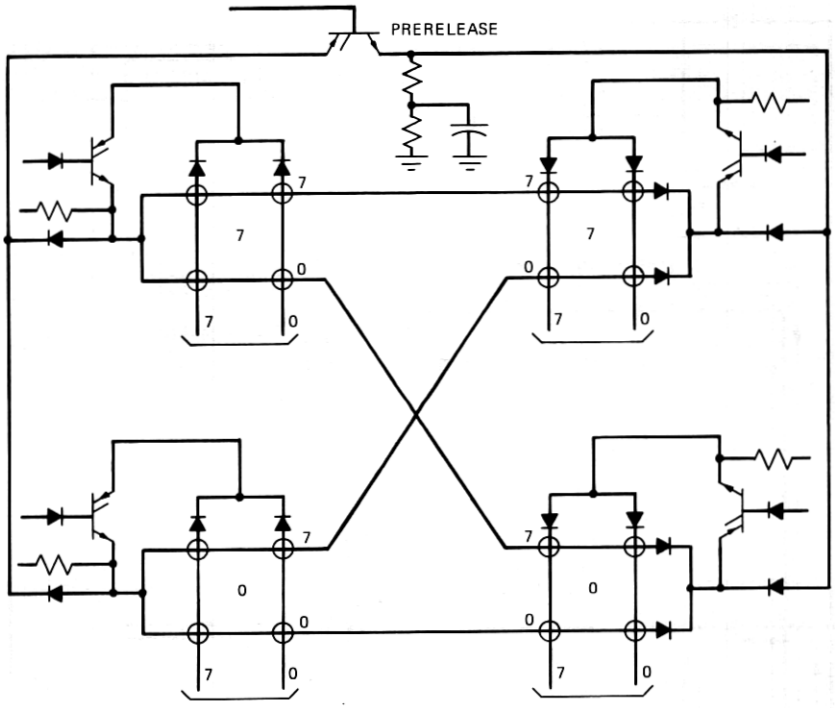



Fig. 8—11A trunk grid.

control connections for the grid. A unique pulse path through the grid is established by selecting one of the eight input and one of the eight output switches. Input and output levels are selected externally to the grid.

The prerelease path utilizes the PR PNPN transistor. This path effectively short-circuits the interconnected horizontal control winding of both stages. The prerelease pulse current will enter the grid along the stage 0 vertical control winding determined by the selected input level and switch, and it will exit the grid along the vertical control windings of stage 1 determined by the selected output level and switch. Most of the prerelease pulse current will follow the external short-circuiting PR path. Only "connect" instructions can be executed in this grid.

The 10A grid contains two additional switch packages. These packages each contain four 1-by-8 crosspoint arrays. The crosspoint control windings are connected to provide for individual control. The contacts and control windings are otherwise the same as all other fabric crosspoints. Figure 9 shows these F-contact or test-vertical access-control windings connected in series with each of the output-level-control

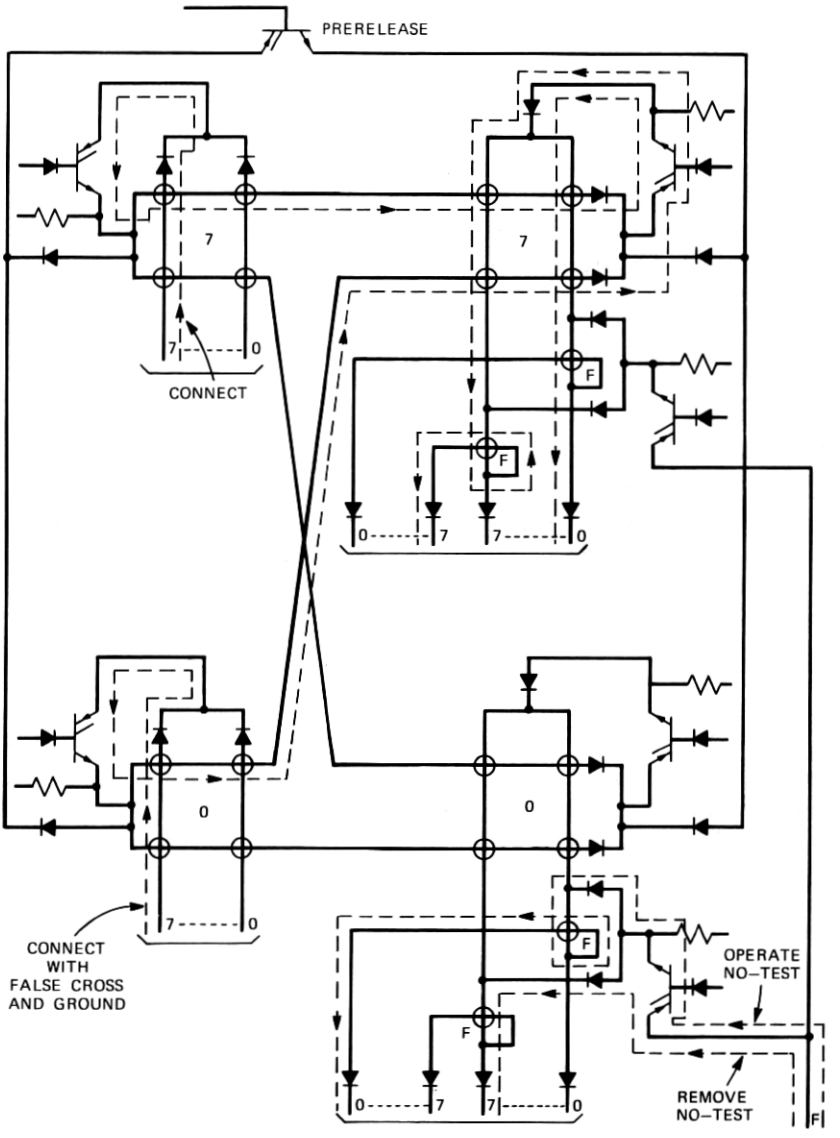



Fig. 9—10A junctor grid.

windings of the grid. When the operate pulse is applied to the terminal designated F, the access contacts can be controlled individually.

A path through a junctor grid can either close or open the F contacts associated with the chosen output level. The two eight-output level-control groups determine the state of the associated test-vertical

crosspoint. In Fig. 9, the F-contact will open if the operate-pulse current exits the grid on a level that belongs to the right-hand group and close it if it exits on a level in the left-hand group.

The prerelease path is the same as in the 11A grid. In addition, the prerelease pulse is forced to exit on an output level that is a member of the release group.

The output switch and the corresponding F-switch PNPN transistor have their gate diodes interconnected. All output switch PNPNs have their cathode resistors interconnected and, similarly, the F-switch PNPN cathode resistors are interconnected. External termination to ground of one of these two resistor groups will cause the selection of either an output switch or an F-switch.

## IV. REMREED NETWORK CONTROL

### *4.1 Introduction*

The different types of network circuits differ mainly in their internal organization and the network fabric they control. This results in differences in the information processing. The basic scheme, control components, and apparatus are the same for all circuits. The general partitioning of functions and sequence of events are the same as in the ferreed controller. The actions or reactions of the remreed controller must be similar to those of the ferreed controller in order to make the remreed switching circuits compatible with existing diagnostic programs, as well as with call-processing programs. Functional names have been maintained. The few items that are not directly compatible with existing programs are primarily physical. Some sensing and monitor functions that are unique to the ferreed electromechanical controller have been added to the remreed controller as artificial monitor points to maintain program compatibility.

The cycle time (20 ms) in the ferreed controller is primarily determined by the operate time, chatter characteristics, and release times of the wire-spring relays. In the remreed electronic controller, the minimum cycle time is dictated by the remreed crosspoint. The need to prerelease and the need to maintain operate current for 3 ms to ensure contact closure and latch consume 5 ms of cycle time. Addressing, testing of the selected path, and circuit restoration consume another 5 ms. An electronic remreed controller could reduce the network cycle time to 10 ms.

A remreed controller performs two types of checks before transmitting its operate-current pulse into a concentrator or grid. The group-check circuitry determines if the state of the translator is valid or not. A nonvalid combination of bits on the peripheral bus or some faults in the buffer register or translator will cause the controller to stop

processing the information. The PNPN transistors and diodes in the pulse-path fabric are part of the translator. Component failures and other pulse-path faults will be detected by the group check. In comparison, the ferreed controller terminates in relay windings and is disjunctive from the contacts that form the pulse path. Shorts in the ferreed pulse path are not detectable by the ferreed controller as they are in the remreed network. While group check protects against double pulse-path connections, the controller path check tests for pulse-path continuity and protects against pulse-path opens.

Each controller connects to the central control over the familiar F, S, and T monitor points, used to report failures to the system fault-recognition programs.

The two 38-pair peripheral unit-address busses connect the central processor with each network bay. The peripheral bus-receiver circuit is the interface between the system bus and the local bay bus. The peripheral bus-receiver circuit is an independent circuit in each network bay. It converts the balanced ac system bus to an unbalanced information bus shared by all circuits in the same bay. Similarly, one diagnostic bus-access circuit is provided per bay.

#### *4.2 Circuit organization and information format*

Both line-switching circuits and the trunk- and junctor-switching circuits are organized to match the peripheral bus-information format. The existing format was prepared to be efficient for the ferreed electromechanical control.

The 36 information bits on the bus are pretranslated into several 1-out-of-4 groups. The different circuits use different group sizes. A line-switching circuit has 16 concentrators. Concentrators 0 through 7 are associated primarily with controller 0, and concentrators 8 through 15 are associated primarily with controller 1. The terms "home" and "mate" are used to indicate control configuration. Concentrators 0 through 7 are home concentrators for controller 0 and mate to controller 1. Each controller contains enough circuit redundancy to control all 16 concentrators in case the mate controller is out of service.

Figures 10 and 11 illustrate in a block diagram the eight 2:1 and eight 4:1 concentrators associated with a controller. The diagrams show P- leads that are gate-driver leads and SN- leads that are cathode-resistor nodes. The peripheral bus path information for the line-switching circuits is all in multiple 1-out-of-4 format. Four bits are used to identify one out of four input switches in a switch group. Another four bits are used to identify a concentrator pair and a third group of four bits identifies the switch group in the pair. This selects the input-switch PNPN transistor by providing simultaneous gate-drive and

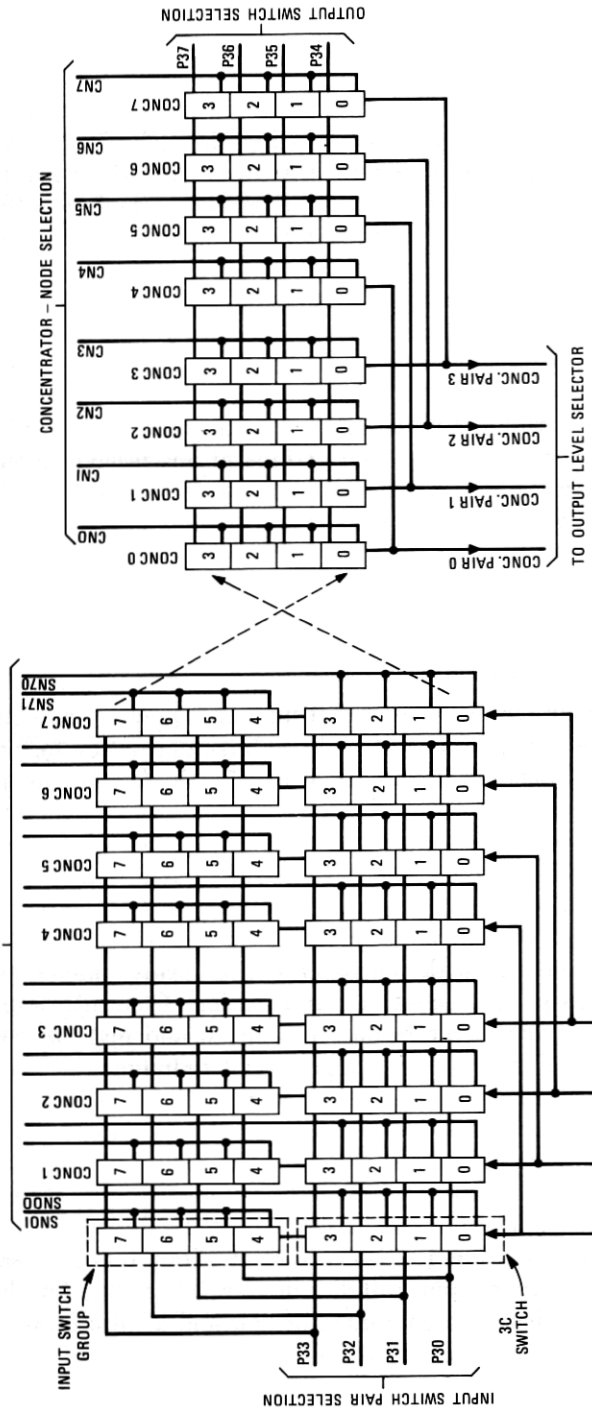



Fig. 10—12A concentrators, concentrator pairs, and input-switch groups.

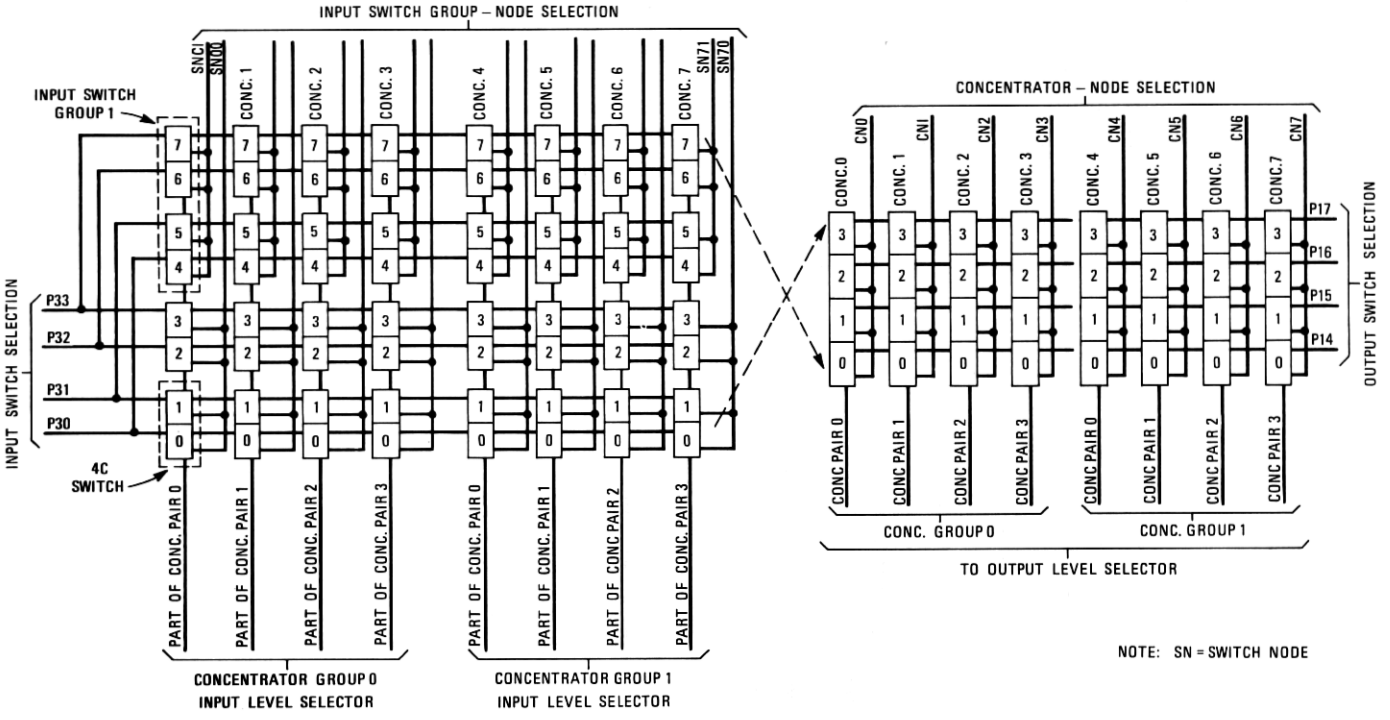



Fig. 11—13A concentrators, concentrator group, concentrator pair, and input-switch group.

cathode-resistor termination. The same information is used to identify the concentrator-node termination (CN-) and an additional four bits identifies the output switch. Selection of input level and output level each require four bits and this selection is illustrated in Fig. 6.

The 4:1 line concentrator has 16 input levels compared to 4 inputs in the 2:1 concentrator. This requires an additional four bits. In the electromechanical ferreed pulse-path selection, the peripheral bus-path information had to be folded to minimize the need for relay contacts. Figure 11 shows the eight remreed concentrators grouped into two concentrator groups; the peripheral bus-path information is folded between the two groups. This means that part of the bus information has a different meaning from another part in relation to the concentrator group selected.

The peripheral bus information for the trunk- and junctor-switching circuits has a multiple 1-out-of-2 and 1-out-of-4 format. This information is translated by the controller into multiple groups of 1-out-of-8 information.

### *4.3 Register, translator, and buffer circuit*

Figure 12 illustrates the register and translator used in the trunk- and junctor-switching circuits. The circuit connects directly to the two local dc bay busses. A 1-out-of-2 and 1-out-of-4 bit combination is registered and translated to a 1-out-of-8 output by a pair of parallel-connected translators. One translator is designated H for home and the other is designated M for mate. This circuit portion is assembled

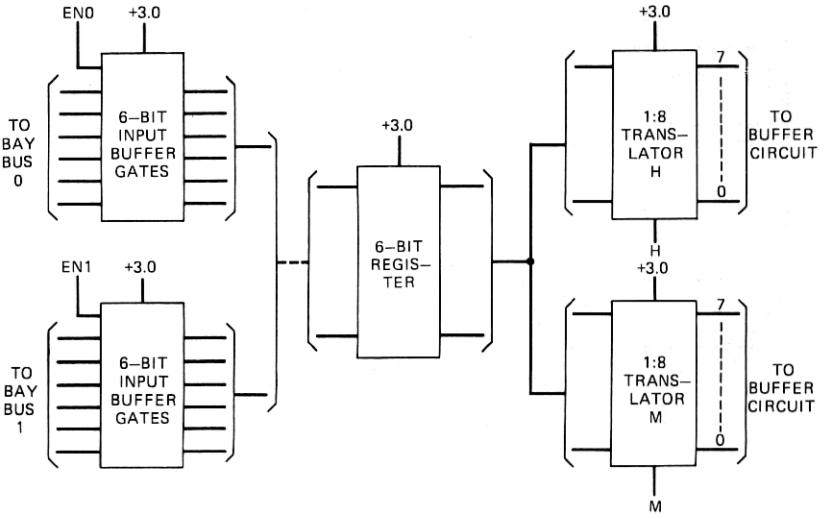



Fig. 12—Register and translator circuit.

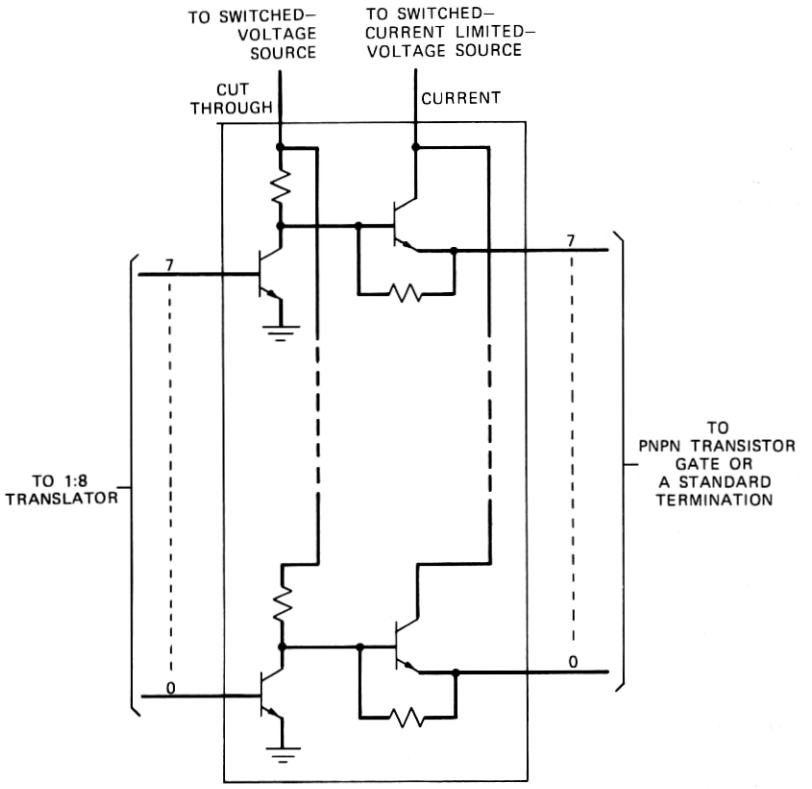



Fig. 13—Buffer circuit.

from integrated-circuit chips. The same ceramic circuit pack contains the output buffer interface shown in Fig. 13. This interface is assembled from junction-isolated-monolithic (JIM) chips that will handle the 12-V gate-driver potential. This interface circuit is connected to an external switched-voltage source which is the group-check circuit. The current in the collector lead designated C is monitored by the group-check circuit, which will report a failure whenever the current demand deviates significantly from the expected value. Cause of such failure can be invalid information on the bus, malfunction of the translator, or a component failure. Failure of pulse-path components in concentrators or grids or physical failures such as opens or shorts are detected as group-check failures.

Four such 1-out-of-8 groups are required to select a path through a grid and each of these groups is monitored by the group-check circuit. These groups select input level, input switch, output switch, and output level.

In the line-switching circuits, the 1-out-of-4 information groups are registered without any initial translation. The information is gated directly to the PNPN transistor gates in the concentrators and to discrete transistor translator circuits that terminate the cathode-resistor nodes.

#### *4.4 Sequence control*

One code of ceramic circuit pack is common to all remreed switching circuits. It contains the controller low-level logic and digital portion of the group-check circuit. It contains 38 integrated-circuit chips and about 900 crossovers. It interfaces with connecting discrete circuit packs where the low-level logic has to convert into 24-V signal levels. External discrete circuits perform differentiations and integration where timing functions are needed. Figure 14a shows this circuit as a functional block diagram.

All inputs are high (+1.0 V) in their idle states. The circuit receives its enable signals from the peripheral bus circuit and enables the register and translator circuit to read information from either bus 0 or 1. It generates and stores the F, S, and VCT signals. VCT stands for voltage cut-through. This is the signal that will start the gating sequence. The circuit further administers the special functions such as: connect with FCG, restore verify loop start, and ground start and operate no-test.

The digital portion of the group-check circuit is shown in Fig. 14b. It connects to the A and B monitor leads associated with the group-check current source. Six such A and B pairs, one pair for each monitor group, are monitored. Two milliseconds after cut-through and the application of gate drive, a strobing signal designated GW reads the state of these monitor pairs. A more-than or less-than failure will cause the GC1 or GC0 flip-flop to become set (GC stands for group check). Both types of failures may occur among the six groups. The group-check logic contains a 6-bit register. Each bit is assigned to a monitor group. The GC1–GC0 pair of flip-flops indicate the type of failure while the other six indicate the location of the failure. The content of this register can be gated onto the diagnostic bus if STG is set. STG stands for "short to ground." It is a special test function in the ferreed controller. In the ferreed network, the STG tests for shorts to ground in the pulse path formed by the wire-spring-relay contacts. STG has no similar meaning in the remreed pulse path. A short in the remreed pulse path will cause group-check failure. However, STG action must be maintained to satisfy the diagnostic program. Therefore, the diagnostic STG action has been made an artificial function that will generate the expected state on the diagnostic bus when the remreed

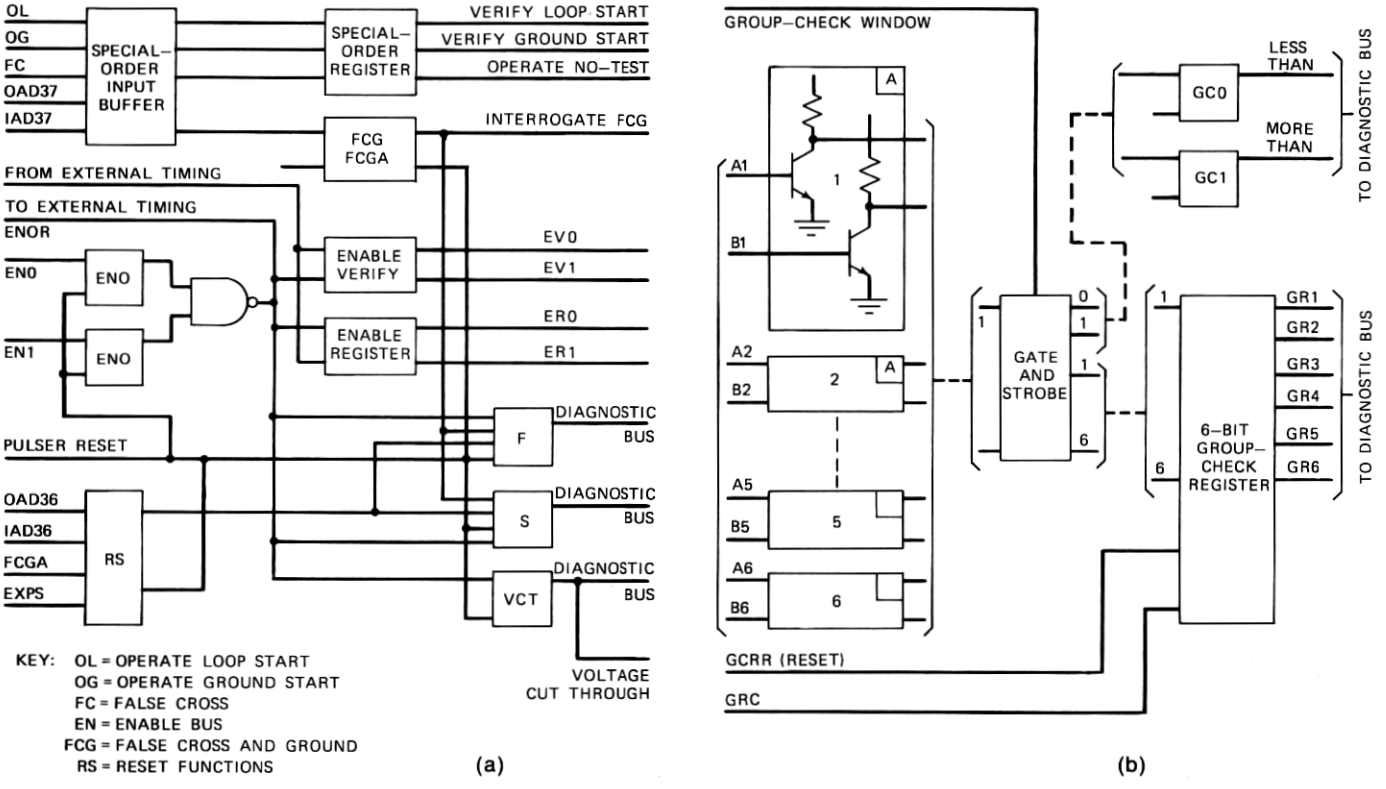



Fig. 14(a)—Control diagram. Fig. 14(b)—Group-check register.

controller receives a set STG instruction. The set STG has been expanded to also mean: gate the six failure-location bits onto the diagnostic bus. While this is of no use to the present generic diagnostic program, installation test programs have been modified to take advantage of this feature, which aids in locating faults.

All other controller functions are similar to the ferreed controller logic. This one ceramic circuit pack contains the same logic functions as 14 discrete ferreed controller circuit packs.

### 4.5 Pulser-driver sequence

The pulser-driver sequence starts after strobing for group check is complete. Figure 15 illustrates in a block diagram the actions and sequences that follow VCT. Strobing for group check takes place 2 ms after VCT and the application of all PNPN transistor gate drives and cathode-resistor node terminations. This sequence circuit supplies the path potential and the connecting pulser circuit senses the path cur-

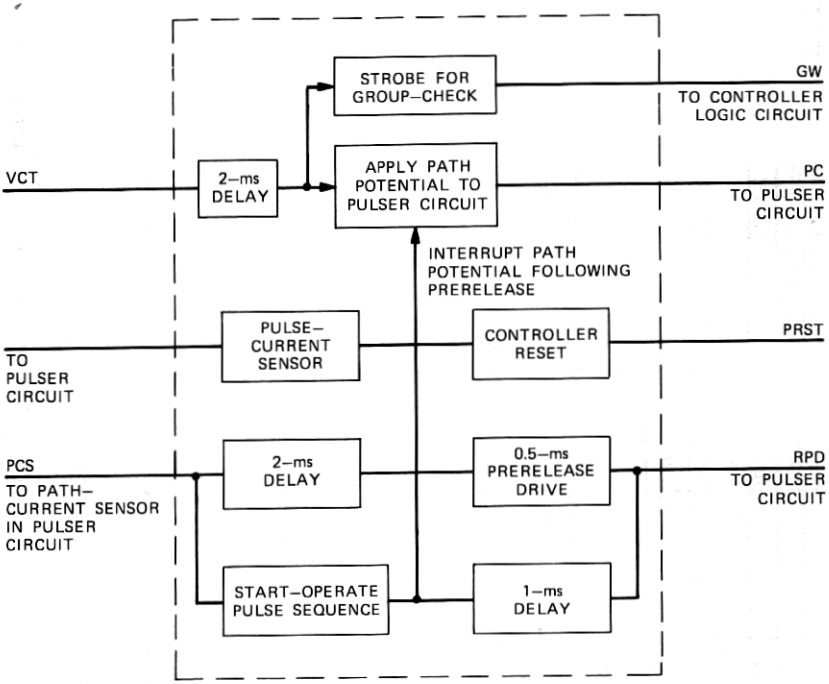



Fig. 15—Pulser-driver sequence.

rent. If the path-current sensor detects the pulse-path continuity, the pulse-current-sensor (PCS) input will go high and initiate the prerelease-and-operate pulsing sequence. The controller sequence will stop if the pulser fails to detect a path. The path potential is interrupted for about 1 ms following the prerelease pulse. This is to ensure that the prerelease path has been released prior to the start of the operate pulse. The release-pulse-driver (RPD) signal is used to drive the prerelease pulse in the connecting pulser circuit. The same RPD signal is also used to temporarily remove some of the cathode-resistor terminations during the prerelease pulse. This avoids draining off some of the active pulse current into cathode-terminating resistors.

#### *4.6 Pulser circuit*

The pulser circuit provides the power in the prerelease-and-operate pulse. The frame filter stores the energy. Each bay filter serves as many as eight controllers and each intra-bay +24- and −48-V power feeder is supported by a 32,000-mF filter. The remreed network requires only one-fourth as many feeders of half the gauge as does the ferreed network. The energy per pulse is the same in both networks. The pulser circuit and associated path-sensing circuit is shown in Fig. 16. The circuit is a constant current-pulsing source. Voltages of +24- and −48-V are used as the primary driving potential. The pulser is coupled to the pulse path by means of a 1:2.5 step-up transformer. This voltage step-up provides for the pulsing voltage across pulse-path semiconductors and an ohmic resistance of up to 24 ohms. Furthermore, the transformer provides compensation for the primary voltage losses. These losses include ohmic drops in power feeders, power relay contacts, fuses, and connectors, and can become significant, since the primary peak currents are nominally 12 A.

The pulser circuit action starts as the input path current (PC) reaches +24 V. This applies path potential to both output terminals of the pulser. The circuit expects to see a forward termination to ground through the terminated cathode resistor of selected PNPN transistors. A forward path current of 120 mA will cause current to flow into the PCS terminal of the sequence circuit through transistor Q6. This current is initially limited by the high input impedance of the sequence circuit. Relay CT (cut-through) will not operate at this time.

The detection of 120 mA of path current starts the prerelease-and-operate-pulse sequence. The path potential and current shut off the gate current to all PNPN transistors in the path and the path is held on by the path current. The negative terminal of the pulser remains at the path potential (+24 V). This gives the pulse path a reference termination that is at a voltage higher than any gate potentials. This

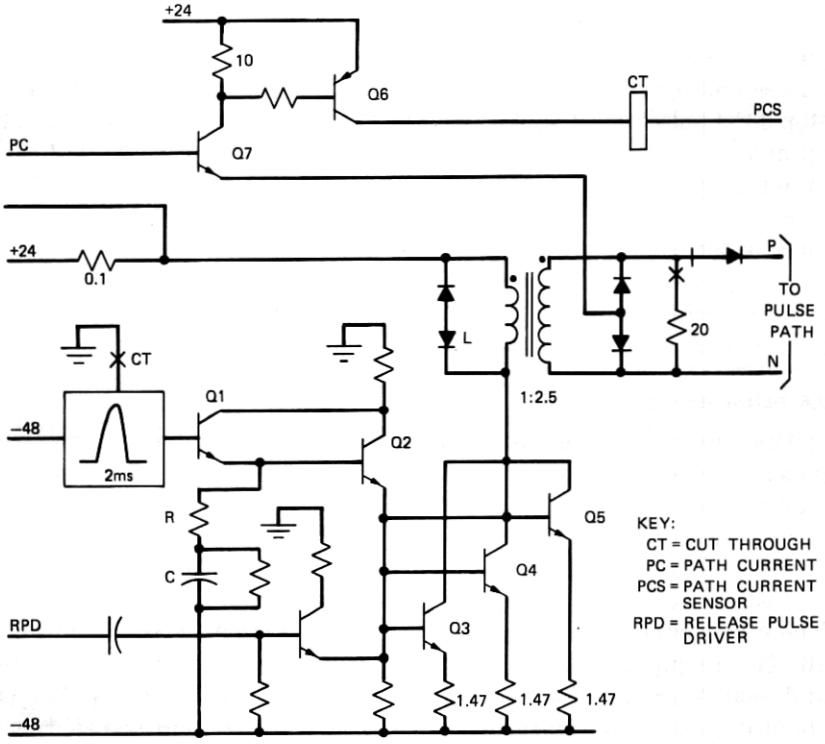



Fig. 16—Pulser circuit.

reference path potential ensures that other gated PNPN transistors in the pulse-path fabric will not be "pulled on." The operate pulsing sequence follows the prerelease and interruption of the path potential. The path potential is reapplied and the pulser sequence circuit changes the impedance on the PCS terminal from 10 kilohms to 1000 ohms. This permits the current in the PCS lead to increase and operate relay CT. The CT relay contact will cause a half-wave-sinusoidal voltage wave to be applied to the base of the Q1–Q2 Darlington pair. The sinusoid measures 2.0 ms at the base. The Darlington pair drives three current sources connected in parallel. The RC network associated with emitter of Q1 will modify the trailing edge of the half sinusoid and cause an almost straight-line decay of the operate pulse as indicated in Fig. 2. This gives the operate pulse the required width, minimizes the eddy-current losses, and provides holding and damping forces on the closed contact.

The pulse-current amplitude is regulated to provide 4.2 A at maximum and minimum battery. The maximum expected pulse-path im-

pedance is 24 ohms in series with 1.2 mH. The pulse-path voltage is not affected by the inductance since the pulsing power is all in a frequency band below 1000 Hz.

#### *4.7 Input- and output-level selection*

Input level, output level, prerelease, and order-group-pulse steering is performed externally to the concentrators and grids. PNPN transistors and their associated standard control components (Fig. 3) are mounted on circuit packs. Figure 17 illustrates the selection scheme used in the 2:1 line-switching circuit. The scheme is the same in the 4:1 line-switching circuit except that the input-level dimension is four times as large.

The selector illustrated in Fig. 17 works directly with the 12A concentrator shown in Fig. 6. The input levels are numbered from 0 to 7. The four lower-numbered levels are used with all orders that require the cutoff contacts to be opened. The four higher-numbered levels are used with all orders that require the cutoff contacts to close. In this example, the concentrator pair 0 is used and consists of concentrators 0 to 4. These circuits are dedicated to the concentrators and can be accessed by both controllers. The cathode-resistor nodes have been given a designation that contains one or more digits. The digits correspond to the order number that will cause the node to be terminated to ground.

These groups of four PNPN transistors are preceded by an order-group pulse-steering stage. PNPN transistors OR1 and OR4 steer the pulse to all input-level-select groups that will cause the cutoff contacts to open. Transistors OR5 and OR7 connect to groups that will close the cutoff contacts. OR2 does not require an input-level selection and only orders 1, 2, and 5 require an output level to be selected.

For orders 1 and 5, the prerelease path consists of two parallel paths. Half of the pulse current will enter the release cutoff path, follow the selected input-level vertical-control windings, and exit through OR47 PNPN transistor. OR4 is made active during the prerelease interval. The second half of the prerelease pulse enters the concentrator at the anode of the selected output switch through PNPN PR1 and exits the concentrator along the vertical in the output switch associated with the selected output level.

For all orders that require the cutoff contacts to close, the input-pulse-steering path is modified to add the release path in parallel. The resistor in series with the operate path will ensure that most of the prerelease current will follow the cutoff release path to the concentrator.

The line-switching circuits use this split prerelease path scheme rather than the horizontal shunt path used in the trunk- and junctor-

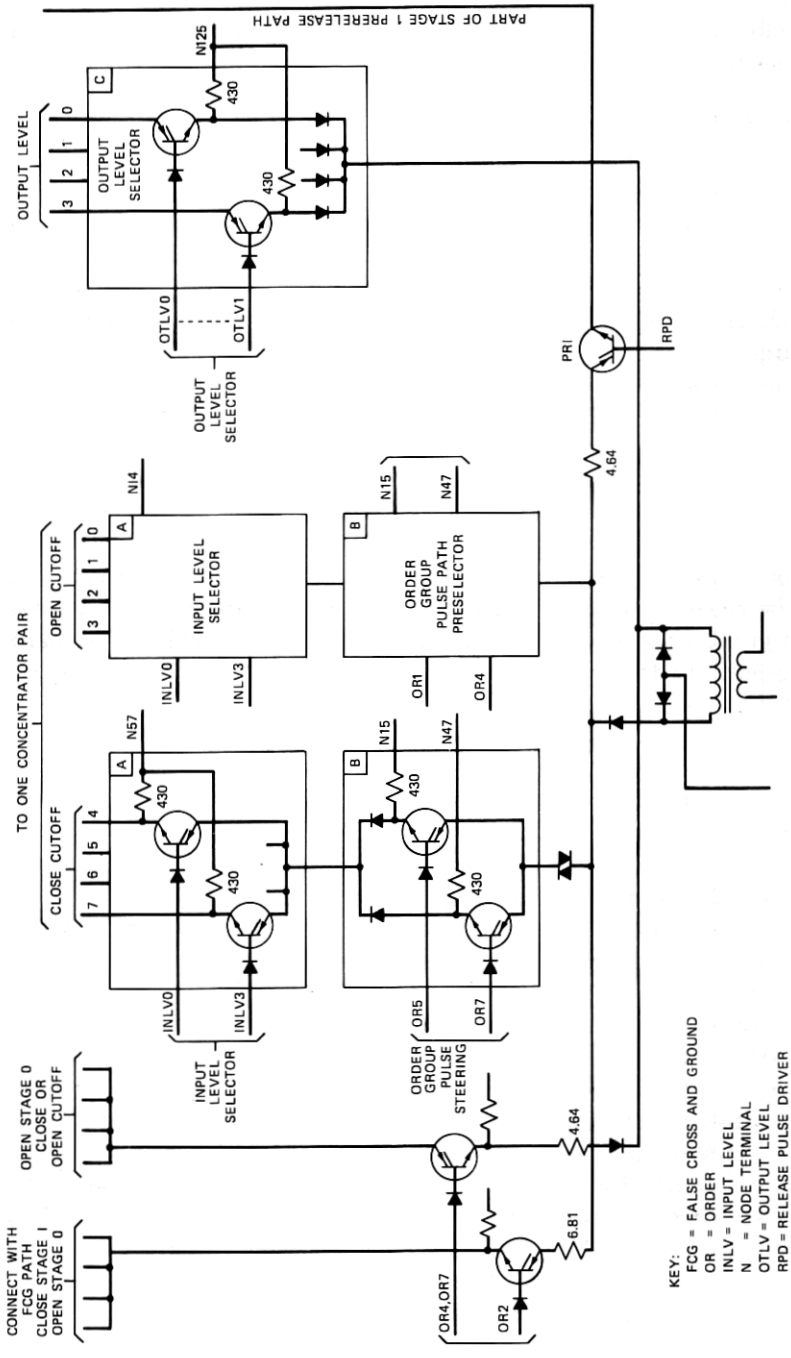



Fig. 17—Line-switching circuit: input-output path selection for 2:1 concentrators.

switching circuits. The horizontal-pulse-path impedance in the concentrators is too low to make a horizontal shunt practical.

### *4.8 Test-vertical functions*

Figure 18 illustrates the familiar test-vertical-access function. A test vertical is common to a pair of 10A grids. A pair of 5D switch packages in each 10A grid provides access to all junctor terminals. The access contacts can be controlled as part of a path through the grid or individually. The loop-start-restore and ground-start-restore verify functions use reed relay contacts to apply the two resistive terminations.

The false-cross-and-ground test is used during call processing to test the integrity of each network path prior to the application of talking battery. Battery and ground are applied in the reverse sense (battery on tip, ground on ring) on the test-vertical pair which are connected to the network path through the contacts of the 5D switch.

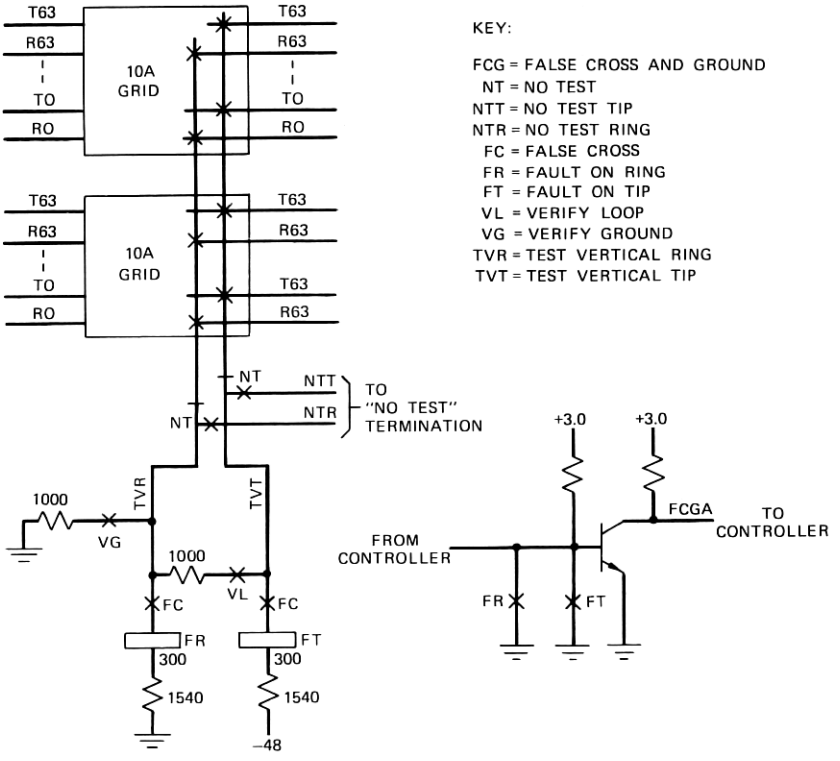



Fig. 18—Test-vertical access for one pair of grids.

A pair of relays, FR and FT, wired in series with the test vertical are used to detect the current which flows in the event of a cross to an active path or a ground in the path under test. The FCG test fails when either relay operates.

## V. SUMMARY

The remreed network and its electronic control is a merger of both old and new electrical and physical technologies. The physical partitioning has been made to agree with a logical partitioning of the controller functions. The remreed network controller was designed from standard, available, Bell System devices. No special chip or device was designed specifically for this project. This permitted the design, construction, evaluation, and introduction into the field to be made in a very short time. With all control functions defined, the door has now been left wide open for on-going cost-reduction efforts. This is taking place both at the device and IC level. The initial choice of a pulse-path fabric diode has been replaced by a diode designed specifically for this use at one-quarter the cost. The PNPN transistor has been given a new encapsulation to reduce its cost. The relatively complicated and expensive 36-chip ceramic circuit pack used in the register and translator circuit has been redesigned using a new integrated-circuit technology. This new equivalent circuit pack contains four chips mounted on a one-quarter size piece of ceramic at one-third the cost. Other functions that presently are performed using discrete devices are candidates for eventual replacement by integrated circuits, which will result in considerable reduction in material cost.

## VI. ACKNOWLEDGMENTS

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