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Digital Data System:

Digital Multiplexers

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The two-stage multiplexing hierarchy developed for the Digital Data System is described. Included in this hierarchy are three synchronous time-division multiplexers and a new 64-kb/s cross-connect arrangement that offer both flexibility and simplified administrative procedures. Maintenance for the multiplexers is provided on an in-service monitoring basis and includes automatic switching of a "hot" spare in the event a fault is detected.

I. INTRODUCTION

The Digital Data System employs all digital facilities for both short-haul transmission within a digital serving area and long-haul transmission to interconnect digital serving areas. Except for the local loop which serves individual customers,[1] the T1 carrier system is used exclusively within a digital serving area, while several alternatives are available for the long-haul digital channel. To obtain efficient utilization of these facilities, a two-stage data-multiplexing hierarchy is employed. As illustrated in Fig. 1, each customer's loop is terminated in an office channel unit (OCU) that matches the loop's data rate, e.g., 56, 9.6, 4.8, and 2.4 kb/s. The output of a 56-kb/s OCU feeds directly into a port of the second-stage multiplexer. The other three, which are collectively termed subrate data rates, are gathered in groups of 5, 10, or 20 in the first-stage multiplexer. Each first-stage, or subrate, multiplexer, in turn, feeds a port of the second-stage multiplexer.

Synchronization information is contained within the multiplexed output signal of a first-stage multiplexer. This permits it to operate independently of the second-stage multiplexer. The result is that any port of one second-stage multiplexer may be cross-connected to any spare port of another whether the signal source is a subrate multiplexer or an OCU. To further simplify the cross-connect process, all

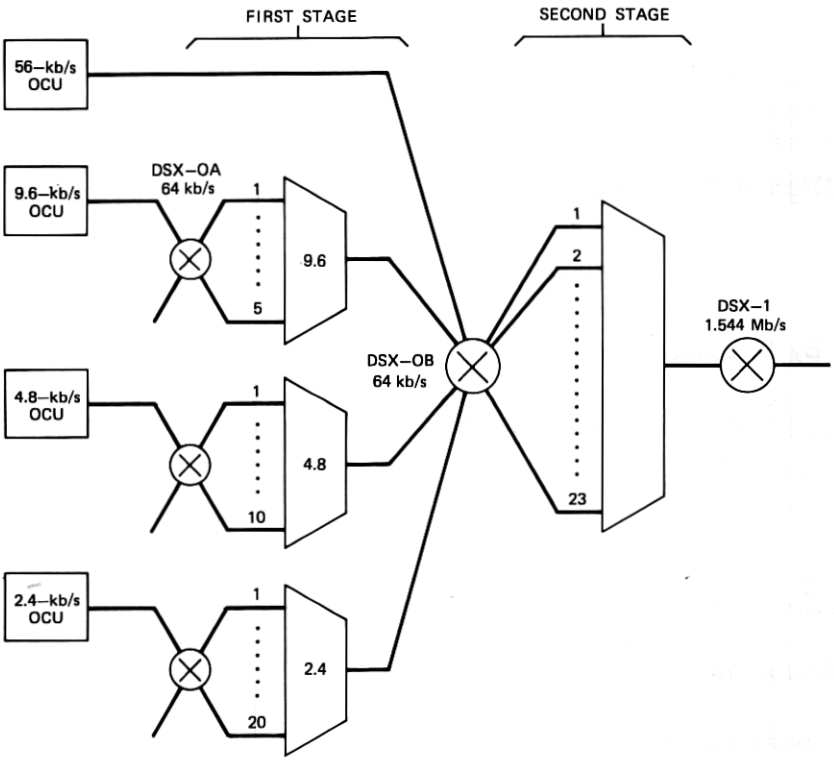


Fig. 1—Two-stage multiplex hierarchy.

signals passing between office channel units and multiplexers do so at 64 kb/s. This arrangement, called a "universal cross-connect" and designated DSX-0, offers wide flexibility and simplified administrative procedures. The signal passing through DSX-0 is called DS-0. The second-stage multiplexer is designed to interface with a T1 carrier system or equivalent digital transmission facilities through a standard cross-connect identified as DSX-1. The signal passing through this cross-connect is designated DS-1.

The failure of a multiplexer, particularly a second-stage multiplexer that may carry as many as 460 individual customer channels, could be catastrophic. To minimize the likelihood of this event, a "hot" spare can be automatically switched into service in the event a malfunction is detected.

II. UNIVERSAL CROSS-CONNECT—DS-0 SIGNAL FORMAT

The Digital Data System employs several different types of transmission equipment that must be interconnected within a central office.

Among these are multiplexers, office channel units (OCUs) for all four data speeds, multipoint junction units (MJUs), and various pieces of testing equipment. To allow a maximum of possible interconnecting arrangements with no tailoring of the equipment to the data rate requires a signal format that is universal to all four customer data rates.

As illustrated in Fig. 2, the format for all intraoffice transmission is organized on an eight-bit byte structure. The eighth bit in each data byte is not made available for the transmission of customer data but is reserved for network control purposes and to assure that the data channel is transparent to the customer's data format. This bit, under control of the OCU, is set to a logical 1 whenever the customer's data terminal is in the transmitting mode and 0 otherwise. Coding the eighth bit in this manner provides the means to transmit control information in the data channel. Any byte in which the eighth bit is a 0 is called a control byte. To meet the requirements of the T1 repeatered line, in particular, items (*i*) and (*ii*) of Section 4.1, it is necessary to make one or more of the other seven bits in a control byte a logical 1. Bit position 1, as described in Section 3.1, is used as a subrate synchronizing channel; therefore, only bits 2 through 7 are available providing a maximum of 63 control codes. Network integrity is pro-

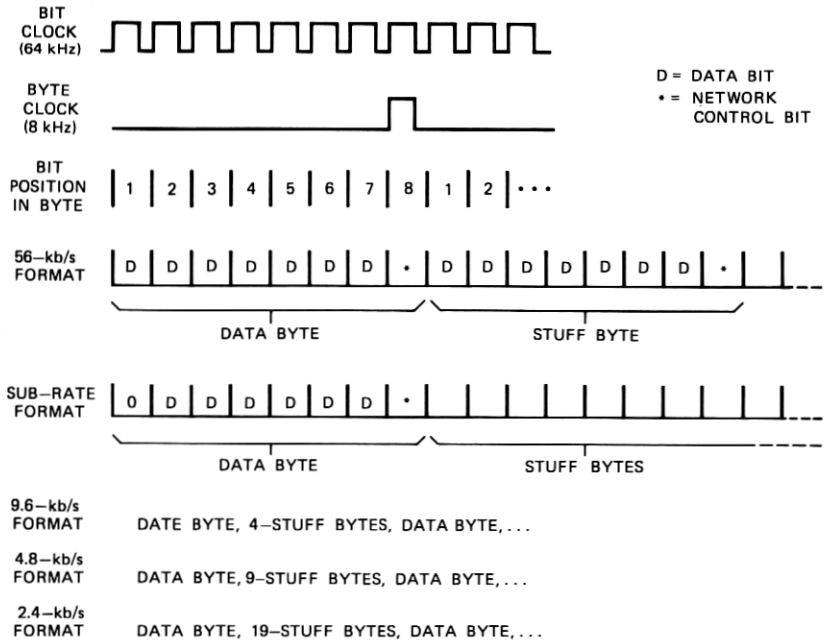


Fig. 2—DS-0 signal format.

tected since the ability to affect the state of the eighth bit is reserved for DDS central office equipment.

The DS-0 signaling rate is 64 kb/s for all data rates; therefore, each byte is 125 μs long. Office channel units for all four data rates translate the customer's data stream into this byte format, second-stage multiplexers accept this byte format for multiplexing onto a T1 line, and all other office equipment operate with the 64-kb/s byte format at their inputs and outputs.

2.1 Data channel capacity

The manner in which the multiplexers operate is to assign all the bits in a given byte to the same data source. Since the eighth bit in each data byte is assigned a network control function, seven bits are available in each byte for the transmission of data. Hence, the maximum data rate is 56 kb/s. Subrate channels are derived by sharing the same 64-kb/s channel among several sources. However, only bits 2 through 7 are assigned to customer data. Since six bits per byte are used, the maximum data capacity per channel is 48 kb/s. If a byte is assigned to a given data source once every five frames, that data source can transmit at 9.6 kb/s. Conversely, one 64-kb/s channel can be used to transmit signals from 5 data sources, each operating at 9.6 kb/s, or from 10 sources, each operating at 4.8 kb/s, or from 20 data sources, each operating at 2.4 kb/s. To distinguish among the 5, 10, or 20 subrate channels that share the same 64-kb/s channel, a synchronizing pattern of length 5, 10, or 20 is inserted into the first bit position of each byte. This is discussed in detail in Section 3.1

Because the 64-kb/s cross-connect data rate is faster than the customer's data rate, the latter must be increased. This is accomplished by repeating the bytes 5 times in succession for 9.6-kb/s data, 10 times for 4.8-kb/s data, and 20 times for 2.4-kb/s data. The repetition interval for each speed is exactly equal to the duration of six-bit intervals at the customer's data rate. For example, at the 9.6-kb/s data rate, six bit intervals equal 625 μs (6 ÷ 9600 seconds). Five byte intervals at 64 kb/s also equal 625 μs (5 × 125 μs).

The DS-0 format enables considerable flexibility in the design of the overall DDS network. It allows a subrate multiplexer of a single design to be easily adapted for all three subrate speeds, it enables one basic design for the MJU to be used at all speeds, and it provides a maintenance scheme common to all four data rates.

2.2 Timing signal constraints

The DDS is a synchronous transmission system, i.e., timing information is required with every data stream. To eliminate the need to trans-

mit timing information between pieces of central office equipment or to derive it from the data signal, a single source of 8-kHz and 64-kHz reference timing signals exists in each office. All transmitting circuits transmit data to the DSX-0 and all receiving circuits sample data from the DSX-0 at instants defined by the same office clock. The 64-kHz and 8-kHz reference signals are distributed from a central clock source to all equipment in an office. Data are transmitted into the cross-connect on positive clock transitions and data sampling occurs on negative clock transitions of the 64-kHz clock.

The delay in transmitting the clock from the office timing supply to various pieces of equipment and the delay involved in transmitting data between equipment are both significant fractions of the 64-kHz clock period. The difference in the clock delay between the timing supply and two pieces of equipment may be as large as 3.0 μs, and the data transmission delay may be up to 5.0 μs. In addition, there may be up to a 0.5-μs delay in distributing a clock signal within a bay of equipment. The time interval between the write (or transmit) transition and the read (or sample) clock transition of the 64-kHz clock must be greater than the sum of these maximum time delays, e.g., greater than 9.0 μs. To accomplish this, the 64-kHz clock has a $\frac{5}{8}$ duty cycle, i.e., it consists of a positive-going pulse 9.8 μs in duration every 15.67 μs.

The 8-kHz office clock is distributed to all equipment to define the interval between 8-bit bytes. This clock has a duty cycle of 5/64 (9.8 μs every 125 μs). As illustrated in Fig. 3, the 9.8-μs pulse in the 8-kHz clock coincides with every 8th bit of the 64-kHz clock. The two reference timing signals are distributed in the form of a composite signal described in a companion article on DDS network synchronization.[3]

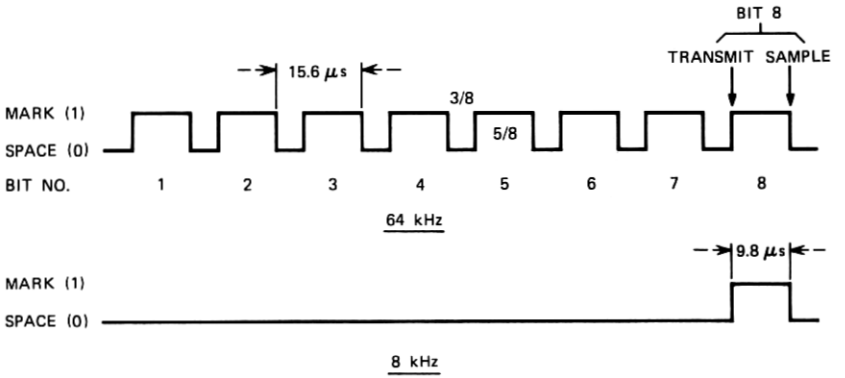


Fig. 3—Reference timing signals for universal cross-connect.

2.3 Electrical characteristics of DS-0 signals

Data are transmitted between DDS central office transmission equipment (e.g., T1DM, OCU, MJU, etc.) in a nonreturn-to-zero bipolar format. Balanced, shielded, twisted-wire pairs are used that are transformer-coupled at each end to reduce the effect of electromagnetically induced noise currents on the operation of active circuits. The need for an inexpensive line driver and terminator plus the requirement for the dc-free signal led to the adoption of a bipolar format. Time delay requirements stated in Section 2.2 limit the length of the cross-connect interconnecting wires to 1500 feet. Attenuation requirements limit the wire-pair loop resistance to 77 ohms.

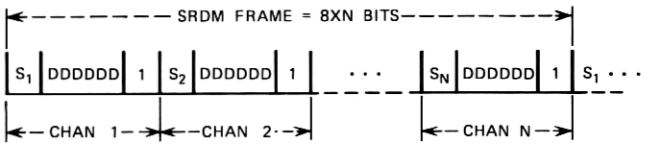
III. FIRST-STAGE MULTIPLEXER

In the Digital Data System, the first-stage multiplexer is designated the subrate data multiplexer (SRDM). It provides efficient packing of the lower rate channels by combining several subrate data channels operating at 2.4, 4.8, or 9.6 kb/s into a single 64-kb/s channel. Functionally, there are three different forms of a subrate data multiplexer, one for each of the three customer data rates. A 2.4-kb/s SRDM can multiplex up to twenty 2.4-kb/s channels onto a 64-kb/s line; a 4.8-kb/s SRDM can combine up to ten channels of that speed onto a 64-kb/s line, and a 9.6-kb/s SRDM can multiplex up to five such channels onto a 64-kb/s line. One SRDM-multiplexed data stream occupies one 64-kb/s channel of a second-stage multiplexer.

A direct result of the DS-0 format described in Section II is that an SRDM input port can accept a signal whose bit rate is lower than that of the SRDM. For example, a 4.8-kb/s SRDM can have among its inputs any number of 2.4-kb/s channels in addition to 4.8-kb/s channels as long as the total number of channels multiplexed is not more than 10. The 2.4-kb/s channel will be scanned every 10 bytes and will appear twice in the multiplexed stream. At the output of the far-end demultiplexer, the 2.4-kb/s channel will then appear with each byte repeated 20 times. Similarly, a 9.6-kb/s SRDM can multiplex any combination of five subrate signals, regardless of whether their speed is 2.4, 4.8, or 9.6 kb/s. In this way, if a given route must handle, say, only three customers, one at each of the three subrate speeds, then only one 9.6-kb/s SRDM is required.

3.1 Frame structure

The multiplexed frame format of each SRDM consists of 5 (or 10 or 20) bytes, one from each channel. The first bit of each channel's byte is always a logical 0 when received from an OCU or another SRDM. The SRDM multiplexer inserts a sequential pattern into this bit position



FRAME RATE = $\frac{8000}{N}$ PER SECOND

BIT RATE = 64 kb/s

SRDM DATA RATE	N $S_1S_2S_3S_4S_5S_6S_7S_8S_9S_{10}S_{11}S_{12}S_{13}S_{14}S_{15}S_{16}S_{17}S_{18}S_{19}S_{20}$
9.6 kb/s	5 0 1 1 0 0
4.8 kb/s	10 0 1 1 0 0 1 0 1 0 0
2.4 kb/s	20 0 1 1 0 0 1 0 1 0 0 1 1 1 0 0 0 0 1 0 0

Fig. 4—Line format for first-stage data multiplexer.

to form a framing channel. The length of the framing sequence is equal to the maximum number of channels of the SRDM. These sequences are shown in Fig. 4. The five-bit framing pattern used in the 9.6-kb/s SRDM is seen to be a subset of that employed in the 4.8-kb/s SRDM which, in turn, is a subset of that employed in the 2.4-kb/s SRDM. At the demultiplexer output, a 0 is inserted in bit position 1 of each channel.

3.2 Synchronization algorithm

While in sync, the minimum interval to enter the out-of-sync state is approximately 0.5 ms. A searching interval follows which requires three consecutive correct framing bits for a 9.6-kb/s SRDM (four for 4.8 kb/s, five for 2.4 kb/s) for resynchronization. An additional 1.5-ms verifying interval is required, during which correct framing bits are received to ensure that the SRDM is properly in sync.

3.3 Functional block diagram

A functional block diagram of an SRDM is shown in Fig. 5. Data from each of the five channels on a port circuit pack are first multiplexed on that board; data from each of the port circuit packs (if more than one is required) are then combined with the framing pattern on the common logic board and transmitted as a 64-kb/s multiplexed stream. The incoming 64-kb/s multiplexed stream passes through a reframe circuit on the common logic board and is then distributed to the appropriate port circuit packs. The common logic generates an address to each port circuit pack so that the latter can properly distribute its received data to the five channels served by it. When each channel

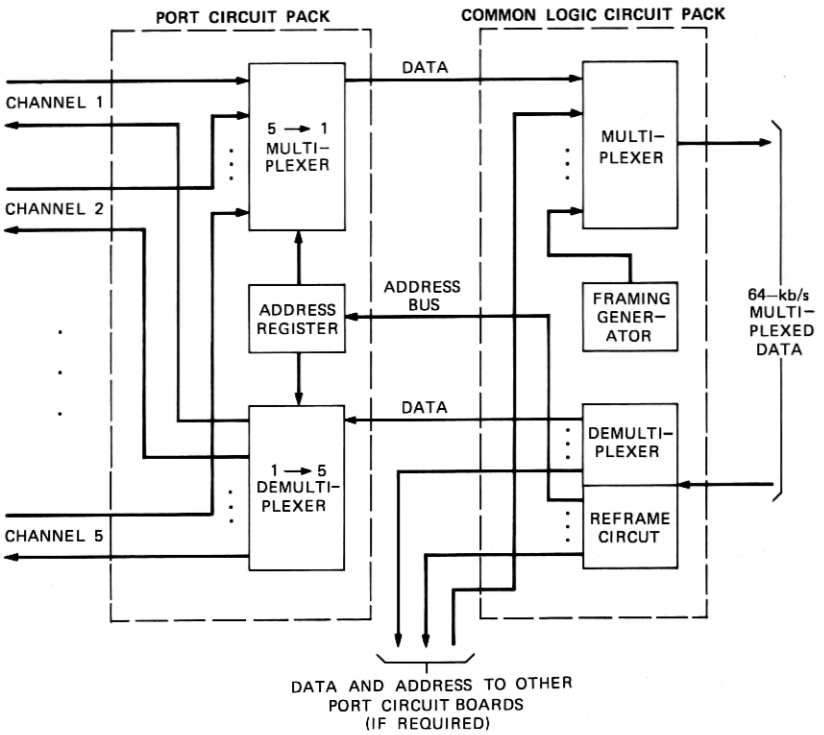


Fig. 5—Subrate data multiplexer, functional block diagram.

circuit receives its byte at the 64-kb/s rate, it is transmitted at the 64-kb/s rate into the cross-connect and is also stored in a recirculating register. The latter provides the means for repeating the byte a total of 5, 10, or 20 times until a new byte is received from the incoming multiplexed stream.

3.4 Integral subrate multiplexer

A special arrangement for a 9.6-kb/s SRDM exists.[1] It is contained on one circuit pack and is called the five-channel integral subrate multiplexer (ISMX). This unit performs the same function as the 9.6-kb/s SRDM but is packaged to mount in an OCU assembly. Up to five channels at any subrate speed can be multiplexed for transmission over a second-stage multiplexer channel without the need for wiring the output of each OCU to an SRDM bay. Unlike the SRDM, the ISMX has no provisions for monitoring, alarms, or automatic replacement.

IV. SECOND-STAGE MULTIPLEXER

Two second-stage multiplexers are available in the Digital Data System. One, designated the T1 data multiplexer (T1DM), is intended

for high-usage routes within a digital serving area as well as for operation over long-haul digital facilities. It provides up to 23 data channels and is equipped with extensive performance monitoring, maintenance, and restoration features. The other is designated the T1WB4 data-voice multiplexer (T1WB4). It provides up to 12 data channels and is designed to share a T1 repeatered line with a D3 or D1D voice channel bank over lower usage data routes within a digital service area, or may be used alone if voice sharing is not desired. The T1WB4's more economical design offers somewhat reduced maintenance and restoration features.

4.1 Multiplexer requirements

Basic to the design of the second-stage multiplexers is the need to operate with a T1 repeatered line. Three restrictions are, therefore, immediately evident: (*i*) not more than 15 consecutive 0's may be transmitted,* (*ii*) the average pulse density shall be not less than one pulse out of eight, and (*iii*) the transmission rate must be consistent with the clock recovery circuit found in T1 repeaters, i.e., 1.544 Mb/s. To avoid possible conflict with existing or future T1 carrier maintenance routines, the 193-bit frame employed for voice transmission is retained, as is the coding of the 193rd bit. In addition to these are the requirements of the Digital Data System, namely, to provide data channels that are transparent to all customer data at the four synchronous data rates, to associate with each data channel a signaling channel that can be used to pass network control information, and to operate with a source of timing that is common to all DDS central office equipment.

4.2 DS-1 signal format

The requirements stated in Section 4.1 lead to the multiplexer format illustrated in Fig. 6. The 193-bit frame is divided into 24 eight-bit bytes plus one additional bit designated the F-bit. A byte represents a 64-kb/s channel. When T1DMs are used, all the bytes, except the 24th are data channels. When a T1WB4 is used, the 24 bytes may carry data or digitized voice.

4.2.1 T1DM signal format

The T1DM must operate over both long- and short-haul facilities. In anticipation of possible repeated losses of synchronization because of radio fades or other short-term outages, the synchronizing algorithm is designed primarily to protect against aliasing or false reframing. To accomplish this, six bits of the 24th byte are used in conjunction with

* A zero is the absence of a pulse on the transmission facility.

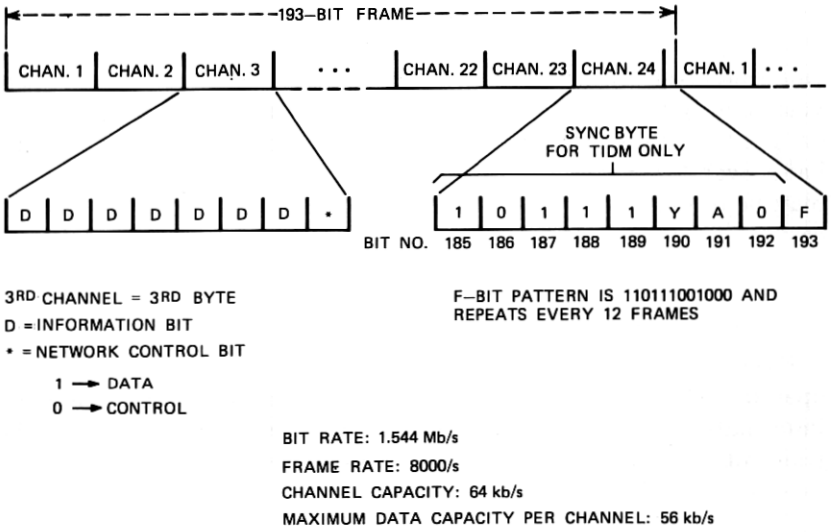


Fig. 6—DS-1 signal format.

the 193rd or F-bit. As illustrated in Fig. 6, the former appear as a fixed pattern while the latter follows the 12-frame pattern employed in the D1D, D2, and D3 channel banks. Bits 190 and 191 are employed for housekeeping purposes by the T1DM. The remaining 23 bytes are assigned as data channels.

4.2.2 T1WB4 signal format

The T1WB4 may share a T1 facility with digital voice channel banks within a digital serving area. To ease the administration of the shared facility as well as maximize its use for voice, the T1WB4 employs only the F-bit for frame synchronization, making all 24 bytes available to carry traffic. While up to 12 of these can be assigned to carry data, there is no restriction as to which bytes carry data and which carry voice.

4.3 T1 data multiplexer

The T1DM combines twenty-three 64-kb/s data channels and a synchronization pattern into a 1.544-Mb/s time-division multiplexed bit stream and converts this to a 50-percent bipolar format[2] (DS-1 signal) for transmission on a T1 repeatered line. It also provides the appropriate demultiplexing functions to convert the received DS-1 signal into twenty-three 64-kb/s channels.

Figure 7 is a simplified block diagram of a T1DM. Each port possesses a four-wire interface with the DSX-0 cross-connect consisting of a bi-

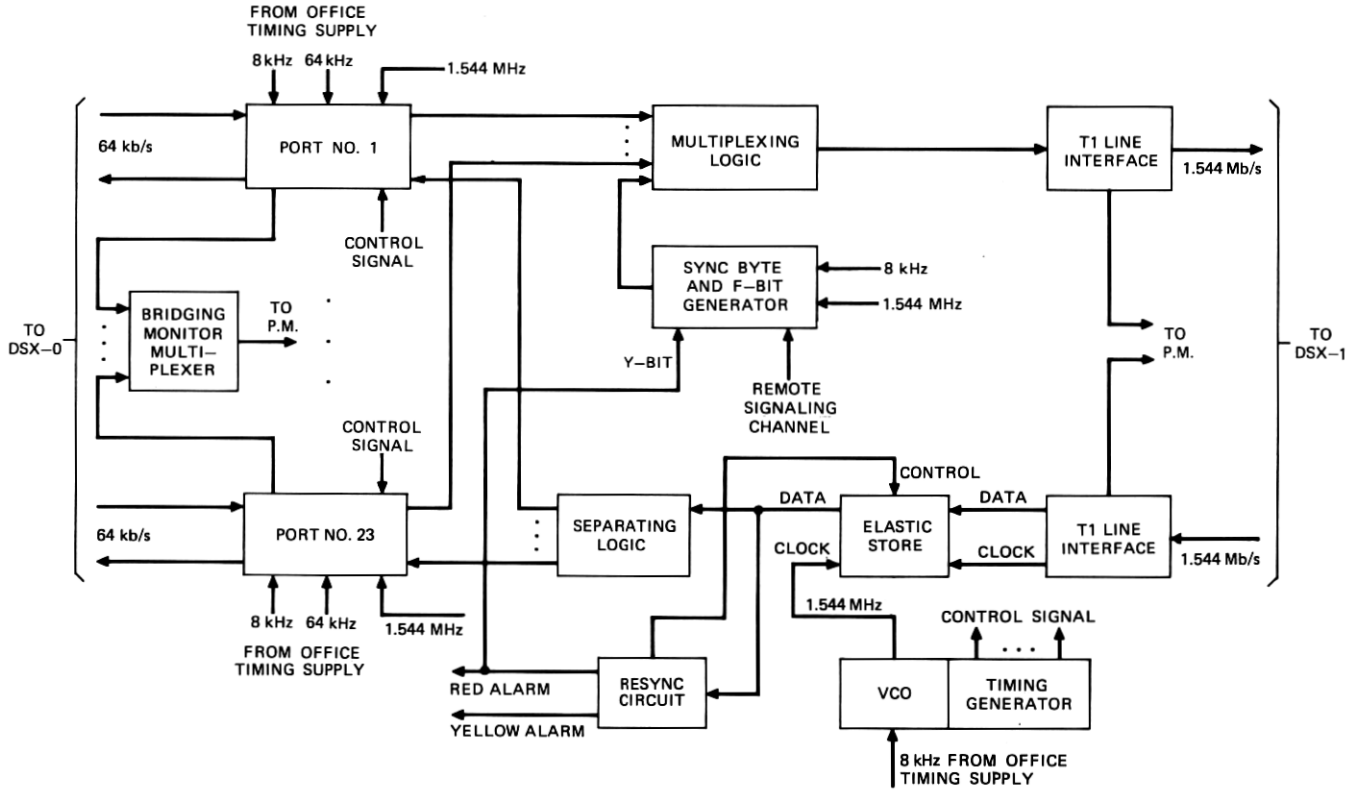


Fig. 7—Block diagram of TIDM.

polar line driver and terminator. The electrical chacteristics of the drivers and terminators are discussed in Section 2.3. Data are clocked into all ports simultaneously under control of the 64-kHz reference signal from the office timing supply. The 8-kHz reference identifies the completion of a byte. Each port contains a pair of 8-bit registers and some control logic. The first register accumulates eight bits of data at 64 kb/s and then serially transfers this byte to the second register under control of an eight-pulse clock burst at 1.544 Mb/s. The byte resides in this register until it is read out at 1.544 Mb/s during the appropriate time slot for each port in the T1 frame. Common circuitry combines these bursts of data, one from each port, and adds on the nine-bit synchronization pattern to complete the 193-bit frame. The transmitting converter converts the logic-level 1.544-Mb/s multiplexed stream into a 50-percent duty cycle return-to-zero bipolar signal for transmission over a T1 line.

After being transformed from a bipolar to a logic level signal in the receiving converter, the incoming DS-1 signal passes through a 256-bit elastic store. The basic purpose of the elastic store is to enable the output 64-kb/s data of the T1DM demultiplexer to be time-aligned with the office 8-kHz and 64-kHz reference signals and to be jitter-free. To accomplish this requires that the phase of the office reference timing signals and the incoming frame be uniquely related. Unless it is provided for, this relation would be arbitrary since the DS-1 signal originates in another central office. One hundred ninety-three bits of the elastic store's capacity is required to align all the data bytes with the office 8-kHz byte reference regardless of the fixed time delay between the sending and receiving central offices. The remaining capacity of 63 bits is available to absorb time variations in the office-to-office delay caused by temperature changes in cable, path changes in radio links owing to atmospheric conditions, etc. The elastic store is basically a 256-bit shift register with a fixed read-in point at the beginning of the register and a readout location that can be varied in one-bit increments anywhere along the register. A 256-state binary up/down counter counts up 1 for every clock pulse from the incoming T1 line interface representing a bit being read into the store, and counts down 1 for every clock pulse of the locally generated 1.544-MHz clock that reads a bit out of the store. The output of this counter provides the address for reading data out of the elastic store. Small differences between the input and local 1.544-MHz clocks will cause the fill of the elastic store to slowly change, but the capacity is sufficiently large to handle all expected variations. If an overflow or underflow (slip) does occur, the fill of the store will immediately be shifted exactly 193 bits in the opposite direction resulting in a deletion or addition of 193 bits in the received DS-1 signal; this is done so the T1DM can maintain

synchronization with the incoming DS-1 signal minimizing customer outages in the event of a slip. The 1.544-MHz clock used to read data out of the elastic store is an exact multiple of the office 8-kHz clock and is generated by a voltage-controlled oscillator within the T1DM.

The data that is read out of the elastic store is sent through demultiplexing logic to the port circuits where it is read into one 8-bit register per port at 1.544 Mb/s. The data are then serially transferred to another register at the same speed where it resides until read out into the DSX-0 cross-connect at 64 kb/s. Recall that the input port circuit also required two 8-bit shift registers. Because the input and output 64-kb/s data signals are aligned with the office 8-kHz and 64-kHz references, the multiplexing and demultiplexing halves of the port circuit can each share the same two registers. For each register, one data byte is read in while the other is read out.

4.3.1 Frame synchronization

The output of the elastic store feeds a resynchronization circuit which examines the incoming data stream to locate the seven-bit framing pattern in the 193-bit frame. Six of these are the fixed pattern located in the 24th or sync byte (see Fig. 6). The seventh or F-bit is a 12-bit sequence requiring 12 frames to complete its cycle. While in sync, four out of 12 framing bytes each with one or more of the seven framing bits in error are required to cause the T1DM to assume that synchronization has been lost. The minimum time to enter the out-of-sync state for random signals is 0.5 ms. Once the signal is out of sync, a searching period follows. During this interval, the resynchronization circuit looks for the six framing bits in the sync byte; the F-bit is ignored because its status in previous frames is required to correctly predict its next state. The maximum average time to reframe is about 0.5 ms. Once the six-bit framing pattern has been located, four consecutive frames with correct framing patterns are required to verify that synchronization has been attained. The verifying interval requires 0.5 ms.

During the reframing procedure, the resynchronization circuit controls the delay in the elastic store to force the frame of the incoming data stream to be properly phased with the office byte clock. This is accomplished after the first good framing byte is detected by directing the elastic store to halt its read-out of data until the incoming sync byte is properly aligned with the office 8-kHz clock.

4.3.2 Control codes

The T1DM generates several DDS control words. To comply with the one's density requirement of the T1 repeatered line, the T1DM multiplexer translates any incoming byte that contains only 0's into the

pattern 00011000. This is employed within the network to identify a channel as being unassigned, since no OCU can transmit all 0's towards a T1DM. An all-0's channel may have a 1 inserted into the first bit position by a subrate data multiplexer as part of its framing pattern. Although the resulting pattern, 10000000, does not violate the T1 line constraint, trouble isolation would be made more difficult because the channel in question would not have a fixed unassigned code repeating every frame. Therefore, only bit positions 2 through 8 are examined in the T1DM and the pattern 10000000 is translated into 10011000.

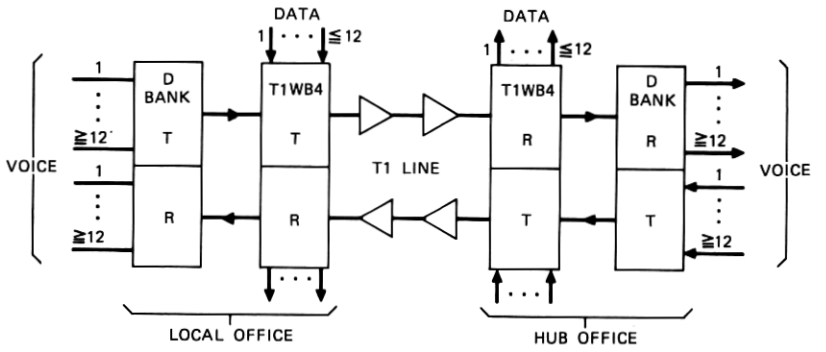
The T1DM demultiplexer has two out-of-sync states. If less than 300 ms has elapsed, the incoming bit stream, which may be random data or all 0's, is distributed to the individual ports; if the out-of-sync state persists for 300 ms or more, the T1DM will transmit the control code word 00011010 out of all ports for as long as the out-of-frame condition persists. The latter state is identified locally as a "red alarm." The red alarm condition is transmitted to the far end via the "Y" bit (bit 190 in the frame), where it is received as a "yellow alarm," meaning that the other end's incoming T1 line has probably failed.

4.4 T1WB4 data-voice multiplexer

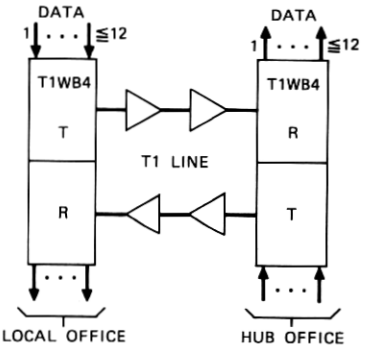
The T1WB4 has three modes of operation, shown in Fig. 8. The primary mode, Fig. 8a, is to combine digital data signals with PCM voice from a D3 or D1D channel bank for transmission over T1 carrier facilities. In this mode of operation, the T1WB4 acts as a "three-port" multiplexer. It inserts data into unassigned PCM voice channel positions and transmits the combined data-voice signal in a standard format suitable for T1 repeatered lines. The T1WB4 can insert up to twelve 64-kb/s data signals on the T1 line with any or all of the remaining channel positions used for PCM voice. A second mode of operation is the independent data mode shown in Fig. 8b. The third mode of operation is the chained data mode shown in Fig. 8c. This allows data in offices along a route to be added onto the T1 facility without using back-to-back terminals. This mode of operation is made possible by the inherent three-port nature of the T1WB4. Sharing a T1 facility with voice is not permitted in the chained mode.

4.4.1 Functional description

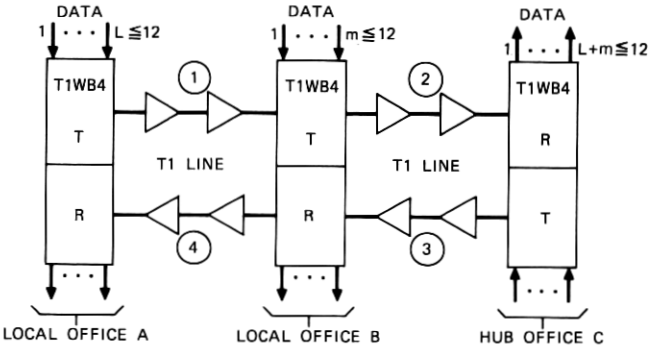
Figure 9 is a block diagram of the T1WB4. The first stage of the transmitter is a receiving converter which accepts a standard 1.544-Mb/s bipolar signal from the channel bank, recovers timing, and converts the PCM voice to logic level signals. The recovered clock is used to drive the counter, the F-bit frame-synchronizing circuits, and the



(a) COMBINED DATA–VOICE OPERATION



(b) INDEPENDENT DATA OPERATION



(c) CHAINED DATA OPERATION

Fig. 8—T1WB4 data-voice multiplexer, modes of operation.

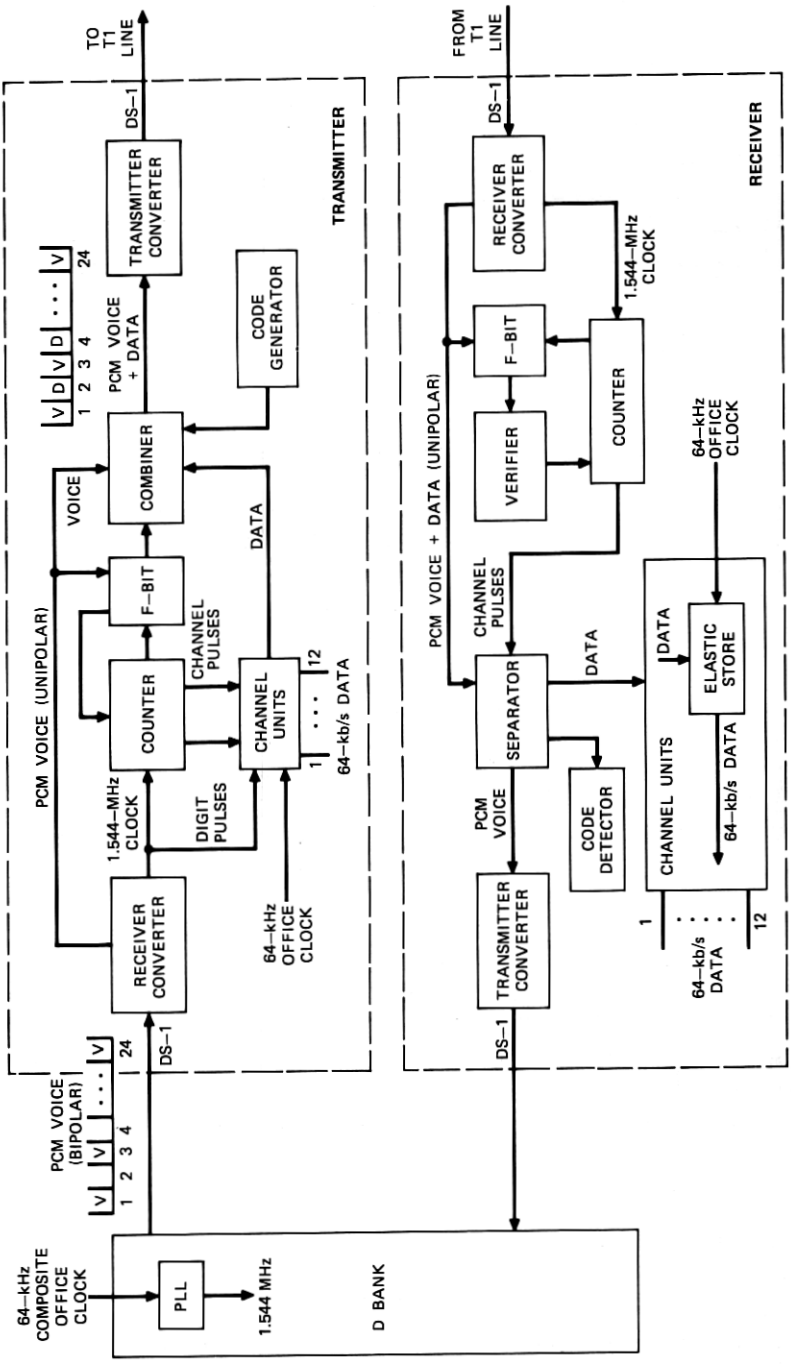


Fig. 9—T1WB4 data-voice multiplexer, simplified functional block diagram.

channel units. Under control of the 64-kHz reference signal from the office timing supply, 64-kb/s data signals are read into all the channel units simultaneously. The data are then sequentially read from each channel unit onto the high-speed bus by the recovered 1.544-MHz clock and combined with the logic-level voice bytes. Following the 24th byte, a single F-bit is generated to complete the 193-bit frame. The multiplexed logic-level signal is then converted via the transmitting converter to the 50-percent duty cycle bipolar format associated with T1 line signals. The receiver functions in a similar manner, but in reverse. The bipolar format of the received DS-1 signal is converted to logic level signals, and the data bytes are separated from the voice bytes and read sequentially into the channel unit receivers. Under control of the 64-kHz reference signal, all 12 data channels are then read out simultaneously at 64 kb/s. The recovered voice bytes are transmitted, as a DS-1 signal, to the D-bank receiver by the T1WB4s transmitting converter.

Per-channel elastic storage is used in the T1WB4 to minimize system start-up cost. The elastic store used in each channel unit transmitter and receiver consists, basically, of two eight-bit shift registers that alternately write in every other frame of data bytes. This approach yields an equivalent elastic storage capability of 96 bits ($\frac{1}{2}$ T1 frame), which is more than adequate to account for line jitter, delay variations in the T1 facility, and the phase offsets resulting from mistuning of phase-locked loops.

4.4.2 Generation and detection of synchronization pattern

Synchronization is achieved by monitoring the F-bit. As noted in Fig. 6, it follows a 12-bit sequence and therefore repeats every 12 frames. The F-bit circuitry is designed to search for the sequence 1, 0, 1, 0, $\cdots$, which occurs every other frame. To guard against the possibility that the T1WB4 transmitter or receiver might falsely frame on a customer data pattern, the verifier circuit examines the remaining six interlaced bits (1, 1, 1, 0, 0, 0) in the 12-bit sequence. A simultaneous match of both sequences is required to satsify the reframing algorithm.

A minimum of three bits out of five checked in the main framing sequence must be in error for the T1WB4 to enter the out-of-sync state. In this state, the sync detector searches matches for the alternating 1, 0, $\cdots$ sequence. Nine successive matches plus verification of the interlace sequence are required for the T1WB4 to enter the in-sync state. The T1WB4 will, on the average, recover sync in about 20 ms.

Two distinct, out-of-sync states are possible depending upon the interval that the T1WB4 is out of sync. If less than 400 ms has elapsed,

random data are transmitted from each of the 12 data-channel units. If the T1WB4 is out of sync for 400 ms or more, the out-of-sync code described in Section 4.3.2 is transmitted from all data-channel units.

4.4.3 Zero suppression

Circuitry is provided in the T1WB4 which will replace an all-0's byte with the unassigned channel code (see Section 4.3.2). As with the T1DM, only bit positions 2 through 8 are examined for the all-0's condition in a data byte. This approach cannot be used for voice bytes, because a 1 followed by seven 0's is a legitimate voice code. Hence, the T1WB4 0-suppression circuitry must perform the dual function of examining the last seven bits of each data byte and all eight bits of each voice byte. If eight 0's are detected in a voice byte, the same 0-suppression code word is substituted.

4.4.4 Operation with D-channel banks

In the combined data-voice mode, there is need to maintain data service continuity in the event a D-bank fails. To accomplish this, when the near-end D-bank fails, the associated T1WB4 discards the DS-1 signal from the failed D-bank and establishes its own properly framed signal. This assures good data transmission between T1WB4s. However, this good signal, if passed on to the far-end D-bank receiver would not activate the latter's "red alarm." For this reason, when the near-end T1WB4 transmitter breaks away from its associated D-bank, it inserts a special code (digit 3 missing) in all nondata channels. This code, when detected in the far-end T1WB4 receiver, causes framing to be deleted from the DS-1 signal sent on to the far-end D-bank receiver. This forces the far-end D-bank out of frame and initiates a red alarm. The far-end D-bank transmitter in turn sends a "yellow alarm" code (digit 2 missing in all bytes) toward the failed (near-end) bank. To maintain data service, this yellow alarm code is preempted in the data channels by the far-end T1WB4 transmitter. The near-end T1WB4 receiver detects the yellow alarm code in all the nondata channels and inserts the yellow alarm code in all channels toward the near-end D-bank receiver.

4.4.5 Timing

The T1WB4 timing plan must provide for two functions, namely, the synchronization of the T1WB4 and its associated facilities and the provision, for economic reasons, of an integrated local timing supply to extend the DDS synchronization network to small local offices.

4.4.5.1 Synchronization of T1WB4 and associated facilities. Both the transmitting clock of the D-bank and that of the associated T1WB4 are

synchronized to the DDS timing network. In hub offices, this is accomplished by utilizing an external timing source, e.g., the composite clock signal available from the DDS office timing supply.[3] D-banks in hub offices are provided with an interface unit (IU) designed specifically for this application. Loop timing of the D-bank transmitters is employed in local offices. This permits flexible location of the D-banks associated with T1WB4s in local offices, even to the extent of permitting D-banks in remote offices.

In the combined data-voice mode, T1WB4 transmitters in both hub and local offices derive 1.544-Mb/s transmitting clock from the DS-1 signal received from their associated D-banks. In the independent mode of operation, the hub office T1WB4 is synchronized to an 8-kHz signal derived from the composite clock. In the local office, the recovered 1.544-MHz clock from the T1WB4 receiver's input T1 line signal is used to generate an 8-kHz signal. The latter is used to synchronize a 1.544-MHz clock which is then used by the T1WB4 transmitter. Thus, the T1WB4 transmitter is always synchronized, directly or indirectly, to the hub office timing supply.

4.4.5.2 Integrated local timing supply. Section 2.1 points out the need to supply 8-kHz and 64-kHz signals from a common timing source to all DDS equipment. In small local offices, that source is contained within the T1WB4 and is designated the integrated local timing supply (ILTS).

The general structure of the ILTS is shown in Fig. 10. Its input is an 8-kHz clock recovered by the regular T1WB4 receiver from the incoming T1 line signal. A 1.544-MHz oscillator in the ILTS is synchronized to this input. The latter is used as the transmitting clock in

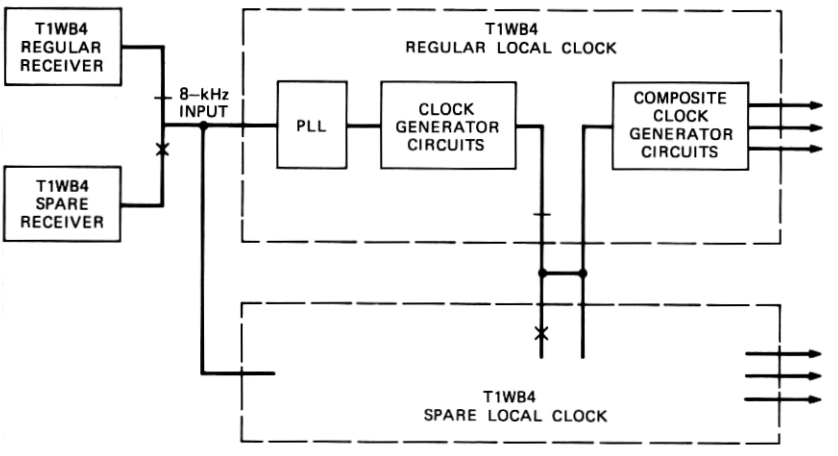


Fig. 10—General structure of integrated local timing supply.

the absence of D-banks and as the input to additional clock-generating circuits in the ILTS. The clock-generating circuits produce 8- and 64-kHz signals that are combined in the composite clock-generating circuit. Three composite clock signals are provided for distribution to DDS equipment associated with the T1WB4.

Two significant features of the ILTS are its ability to bridge short-term outages on the T1 facility (holdover) and its reliability. The ILTS provides the holdover feature by incorporating an oscillator with a moderately accurate free-running frequency and an inexpensive form of frequency memory. This results in a holdover capability of approximately 2 seconds. Reliability of the ILTS is obtained through redundancy.

V. MAINTENANCE

All the data multiplexers (except the ISMX) employ some form of in-service monitoring. The maintenance plan[4] for the Digital Data System is, in part, predicated on the fact that the multiplexers are not only adequately alarmed in the event of a service outage, but include a standby spare that can be used to rapidly restore service.

The data multiplexers take advantage of the digital characteristics of their input and output signals to provide a mechanism for monitoring these signals on an in-service basis. In addition, they provide automatic means to place the spare in service.

5.1 T1 data multiplexer and subrate data multiplexer

The maintenance philosophy for both the T1DM and SRDM is based primarily on the availability of a performance monitor. In the event that a T1DM performance monitor is not available (e.g., taken out of service for maintenance reasons), the T1DM is equipped with alarm and manual test features similar to those found in the D3 channel bank. The SRDM is solely dependent on its performance monitor for testing.

5.1.1 T1DM and SRDM performance monitors

The T1DM performance monitor (T1DM–PM) and the SRDM performance monitor (SPM) provide continuous surveillance of a bay of their respective multiplexers. They detect hardware failures associated with the common circuitry as well as with individual port circuits. Both performance monitors switch into service a spare multiplexer in place of the failed unit, transmit the fault information to the faulty multiplexer for display on a seven-element LED and generate signals to activate the appropriate central office alarms, i.e., minor or major. In the case of the T1DM, transmission failures on the incoming DS-1 signal are also detected and alarmed; however, switching to the spare

T1DM is inhibited. Since both performance monitors are similar in function, only the T1DM–PM is discussed. Where significant differences exist between the T1DM–PM and the SPM, they are noted.

As illustrated in Fig. 11, T1DM–PM access to each T1DMs DS-0 and DS-1 signals is provided through a multiconductor cable. To minimize the number of required conductors, the DS-0 signals from the 23 transmitting and receiving ports are concentrated within each T1DM and appear on two leads. The T1DM–PM sequences through each of the 16 DMs (including the spare) in the same manner. It first checks the multiplexing functions and then the demultiplexing functions of each unit. The multiplexing function is checked by comparing a byte from each 64-kb/s data input port with the corresponding byte, one T1 frame later, in the multiplexed DS-1 signal at the output of the selected multiplexer. The demultiplexing function is checked in a similar fashion with one exception: a byte of 1.544-Mb/s data from the output of the elastic store (rather than the incoming DS-1 signal) is compared, one frame later, with a byte from the corresponding 64-kb/s data output port. Clearly, hardware failures in the data transmission path in either the multiplexer or demultiplexer will result in an unsatisfactory comparison. If the port test fails, the identity of the port under test is stored and the monitor then steps to the next port.

The demultiplexer port test utilizes the 1.544-Mb/s output of the elastic store rather than the incoming DS-1 signal since the delay through the elastic store is unknown and any attempt to compensate for this would overly complicate the performance monitor. Instead, since the elastic store is essentially a long shift register, it is checked by verifying that the sync word can pass through unmutilated. This sync detector circuit is also used to check the transmitted sync word in the multiplexer section of the T1DM.

Aside from the lack of an elastic store test, the SPM's testing algorithm differs from that of the T1DM–PM in another significant area. Before the SPM can begin testing, it must determine the data rate of the multiplexer under test. From this, the SPM can deduce the maximum number of ports to be tested. As described in Section 3.1, three unique framing patterns are used corresponding to a 9.6-, 4.8-, and 2.4-kb/s subrate multiplexer. The SPM determines the data rate by identifying the framing pattern in the incoming multiplexed stream.

Each time that a T1DM performance monitor completes its scan of all the multiplexers, it enters a self-test mode. In this state, the performance monitor is not connected to any multiplexer; hence, the inputs to the monitor self-test circuit should indicate a port failure, a 1.544-MHz clock failure, a transmitted DS-1 sync failure, and the absence of incoming DS-1 signal. If all these events are detected, the performance monitor proceeds to the start of its scan cycle; if not, the

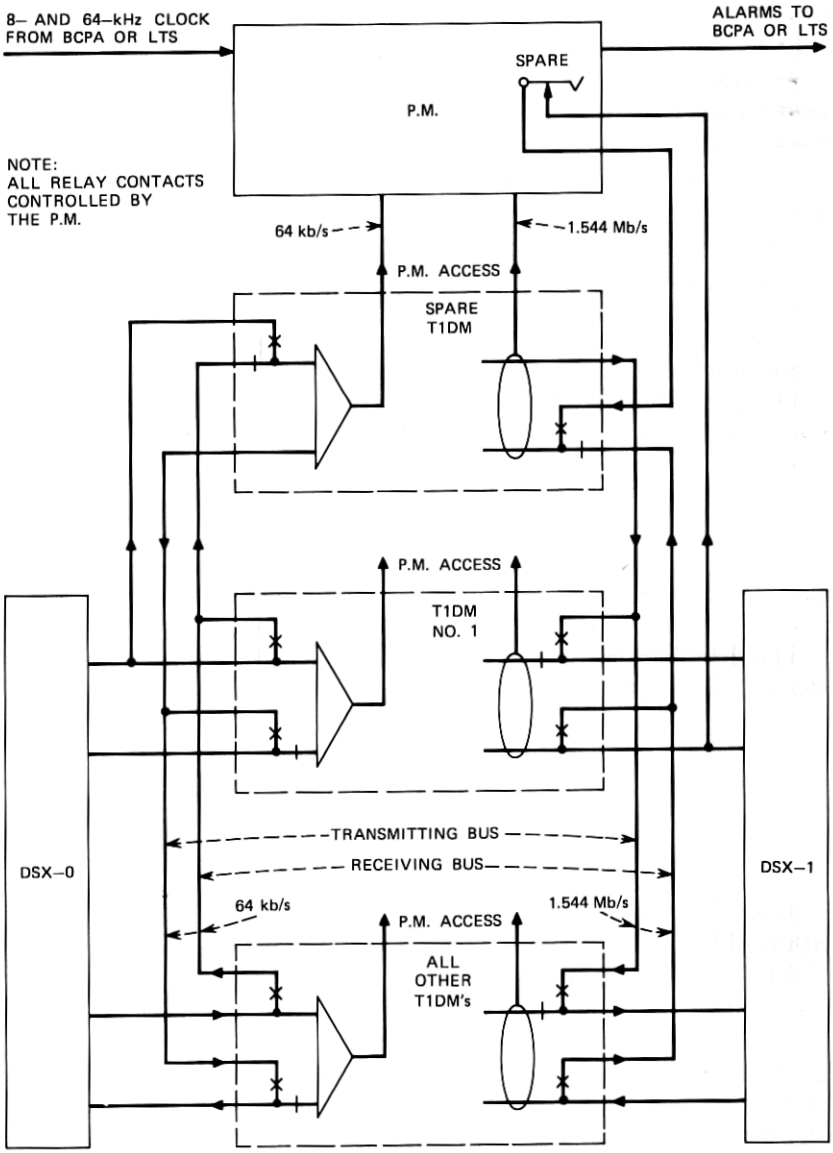


Fig. 11—T1DM performance monitor, functional block diagram.

performance monitor stops and an alarm is initiated. A less sophisticated self-test concept is employed in the SRDM-PM. The scan cycle for a fully equipped T1DM bay (16 multiplexers) is approximately one-half second, while for a SRDM bay (48 multiplexers) it is approximately five seconds.

5.1.2 Standby spare and one-for-n switching

The standby spare is physically and electrically identical to a working multiplexer in every respect. The spare T1DM is checked by the T1DM–PM in the manner described in Section 5.1.1. A source of signals is required by the performance monitor to completely specify the state of a T1DM. To obtain this, as illustrated in Fig. 11, the spare is bridged across a predesignated working multiplexer's DS-0 and DS-1 inputs. Unlike the T1DM, the spare SRDM is checked by a special data sequence generated by the SPM. Also, in the event a subrate multiplexer is found to be faulty, the data rate of the spare is adjusted by the SPM to agree with that of the faulty unit before the spare is switched into service. Thus, the spare is a tested "hot" standby unit. In the event a fault is detected in the spare, a minor alarm is initiated and the appropriate fault symbol is displayed on the spare T1DMs (or SRDMs) LED.

To permit the spare to substitute for any of the 15 other T1DMs, all 16 are bridged onto four buses. Each multiplexer contains a switch module that serves to isolate the multiplexers from the buses. Since balanced transmission pairs must be transferred from a working multiplexer to the spare, economic and reliability considerations dictates the use of relay contacts to accomplish the transfer. Although it is switched out of service automatically, returning a multiplexer to service requires a manual operation. This method offers two advantages: (*i*) it prevents an oscillatory condition from occurring because of marginal operating conditions and (*ii*) it permits coordination with customers where sensitive data services are involved.

As observed in Section 5.1.1, only a hardware failure within a multiplexer will result in a switch to the spare unit. If the spare is already in use, the failure of a second multiplexer will not result in a switch. However, immediately upon returning the first failed multiplexer to service, the spare will be switched in place of the second failed unit.

5.1.3 Alarms and visual aids

In the presence of a performance monitor, all single multiplexer failures, spare as well as working, result in a minor office alarm since customer service is not affected. Both the minor and major alarms result in bay and aisle pilot lamps being lighted. An alarm-cutoff switch provides means to silence both the minor and major audible alarms. If a multiplexer is faulty, its seven-element LED display is energized by the performance monitor. The character displayed identifies which circuit pack or packs are the most likely culprits. A complete list of these characters for the T1DM appears in Fig. 12. A

ALPHANUMERIC CHARACTER	INTERPRETATION	BAY ALARM*	
		YES	NO
123456	SINGLE PORT FAILURE ON CP DESIGNATED	X	
A	AMBIGUOUS CONDITION †		X
C	FAILURE IN CERTAIN COMMON CIRCUITS	X	
E	FAILURE IN ELASTIC STORE	X	
F	FAILURE IN MULTIPLEXER FRAME GENERATION CIRCUIT	X	
P	FAILURE IN SYNC. RECOVERY CIRCUIT	X	
J	FAILURE IN 1.544-MHz VCO IN T1DM	X	
O	RED ALARM – TRANSMISSION FAILURE ON INCOMING T1 LINE, NO SWITCHING OCCURS.	X	
o	YELLOW ALARM – TRANSMISSION FAILURE ON REMOTE T1DM'S INCOMING T1 LINE		X
H	MODE SWITCH IN NO ALM POSITION. IF T1DM PM DETECTS A TROUBLE CONDITION, APPROPRIATE CHARACTER IS DISPLAYED – NO ALARM GIVEN, NO SWITCHING OCCURS.		X
8‡	T1DM OPERATIONAL BUT NOT RETURNED TO SERVICE	X	
BLANK	NORMAL OPERATION		X

*SINGLE T1DM FAILURE RESULTS IN MINOR ALARM AND SWITCH TO SPARE; TWO OR MORE DETECTED FAILURES RESULT IN MAJOR ALARM. IF SPARE FAILS, A MINOR ALARM OCCURS, BUT NO SWITCHING WILL OCCUR.

†T1DM IS ABLE TO RECOVER FRAME SYNC, BUT PM CANNOT.

‡FLASHING

Fig. 12—T1DM alphanumeric displays when performance monitor is used.

similar set is used with the SRDM. If the performance monitor detects a failure internal to itself, it energizes its own displays.

5.1.4 Reliability considerations

The bridging method used by the T1DM–PM ensures the detection of failure of any component (transistor, integrated circuit resistor, etc.). This includes those components that are required to perform the bridging function itself as well as those in the actual data stream. Thus, a multiplexer may fail and a switch to the spare occur because of the presence of monitoring equipment within the T1DM. Also, a failure within the T1DM can cause an unnecessary switch to the spare T1DM. Both these failure modes produce momentary interruptions in service.

A more serious condition is that of service loss resulting from faulty performance monitor operation. While estimates based on *single component* failures indicate that the likelihood is slight that any of these events could occur, they will be detected and an office alarm will be initiated if they should occur.

5.2 T1WB4 data-voice multiplexer

Consistent with its low first-cost design goal, the maintenance arrangement for the T1WB4 is significantly different from that of the T1DM. The T1WB4 provides 1:1 automatic protection switching of the common equipment. No protection of the individual channel unit circuit packs is provided.

To determine when the transmitting or receiving common-equipment circuit packs fail, monitoring circuits are provided at the output of each unit, both regular and spare. This circuitry detects both loss of frame and loss of signal at the T1WB4s DS-1 outputs. By making a comparison of the quality of the input signals to the multiplexer, as determined by the basic framing detection circuitry internal to the common equipment, and that of the output signals, as measured by the monitors, it can be determined when a common unit has failed. For example, if the framing detectors in both the regular and spare receivers indicate a valid incoming signal framing pattern and the monitor at the output of the regular, but not the spare, common receiver indicates a bad output signal framing pattern, the regular common-receiver circuit pack is determined to have failed. This two-out-of-three check using loss of frame/signal indicators provides a good measure of common-equipment operation. If a common circuit pack fails for more than 200 ms, it is automatically spared. Once the failed circuit pack is repaired, it takes about 1 second for the multiplexer to automatically switch back. The delay times are used to guard against over-responding to transient or intermittent conditions.

5.2.1 Automatic breakaway and restoral

The decision to provide 1:1 sparing of the common equipment as opposed to $1:n$ sparing was based on two factors. First, in the smaller local offices where T1WB4s would principally be used, there would most likely be only a few multiplexers present. A second factor is the need to provide automatic breakaway when D-banks fail. The monitoring scheme previously described makes it straightforward to determine when the incoming signal from a D-bank is bad. If the incoming signal to the T1WB4 transmitter fails because of loss of pulses or loss of framing for 400 ms or more, the T1WB4 will automatically break away and switch to the independent data mode of operation to maintain data service. Breakaway will also occur if the D-bank is deter-

mined, by circuitry in the T1WB4, to be asynchronous to DDS timing because of, for example, a failure of the phase lock-loop in the D-bank. To automatically restore to combined data-voice operation, once the D-bank failure has been cleared, requires that monitoring equipment be applied to the incoming line during the breakaway period. Under normal operation, the spare common equipment is used to provide redundant backup for the regular common equipment. When an incoming failure occurs and independent operation is established, the spare common equipment is used as the monitor to determine the status of the incoming signal from the D-bank. This double duty for the spare common equipment results in an inexpensive automatic restoral capability with little if any degradation in system availability since double failures are required before service is affected.

VI. SUMMARY

The Digital Data System provides customer data channels operating synchronously at 2.4, 4.8, 9.6, and 56 kb/s. A two-stage multiplexing hierarchy that obtains efficient utilization of the long-haul 1.544-Mb/s facility has been described. The first stage gathers the three lower data rates in groups of 5, 10, or 20. Each first-stage multiplexer feeds a port of a second-stage multiplexer which is designed to interface with the DSX-1 cross-connect. Up to 460 2.4-kb/s channels can be accommodated in one DS-1 signal. To minimize the likelihood of extensive service interruptions owing to hardware failures, each stage of the multiplexing hierarchy is protected with a standby spare that can be automatically switched into service.

VII. ACKNOWLEDGMENTS

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