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# RC Active Filters for the D3 Channel Bank

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*The development of the voice-frequency active filters for the D3 channel bank is described. These filters are the first single-substrate RC active filters using thin-film tantalum RC and silicon integrated-circuit technology to be produced on a large scale by Western Electric. To create complete confidence in both the design and the new technology, an extensive model building and testing program was undertaken. In addition, continuous interaction with manufacturing engineers resulted in a design that facilitated the introduction of this new technology in a large-scale manufacturing environment.*

*Significant advances were made in reducing the complexity of tuning active filters. In fact, the tuning and testing procedure has been adapted for use with a totally automated computer-controlled test set. Furthermore, a Monte Carlo statistical simulation of the manufacturing process of the filters was developed. This model includes tolerances of the manufactured components, test set errors in measuring gain and component values, resistor adjustment accuracies, and temperature and aging behavior of the components. This computer program has been an invaluable tool in determining the requirements for tuning, testing, and optimizing the final design for minimum manufacturing cost.*

## I. INTRODUCTION

Resistance-capacitance active filters are a relatively new addition to the family of frequency selective networks. Although active filters have been in existence for 20 years, they have not been widely used because passive filters have been less expensive. However, the concurrent development of silicon integrated circuits, tantalum thin-film technology, and automated computer-controlled test sets have made RC active filters a practical alternative to passive filters at voice frequencies.

This paper deals with the design and development of the voice-frequency RC active filters used in the D3 channel bank.[1,2] These filters are realized in thin-film tantalum technology with beam-leaded silicon integrated-circuit operational amplifiers on one ceramic substrate.[3]

New analysis[4,5] and modeling techniques, more efficient optimization algorithms,[6] the concept of statistical design,[7] and more flexible machine aids to physical design gave the network designers powerful tools with which to attack the design process.

## II. DEVELOPMENT PROCESS

The development process involves a number of interrelated steps. Neglecting any of the steps can result in a design that either does not meet requirements or is unmanufacturable at a reasonable cost. Traditionally, the first step is a careful analysis of the filter requirements. This will determine the order of the filter and, possibly, the technology needed for the physical realization (e.g., LC, RC active, or mechanical technology). Next, the initial design is undertaken. This step requires accurate models for the components and general-purpose analysis and synthesis routines. Unfortunately, when initial designs using new technologies are breadboarded, requirements are very rarely met. In addition, the physical realization is either too large and/or the network is too costly. Thus, we must optimize the network to meet not only electrical requirements but also size, environmental, and cost restrictions. Next, sensitivity studies must be undertaken to determine both the viability of the design and whether or not manufacturing adjustments (tuning) are necessary. Since the designer cannot afford to wait 10 or 20 years to see if his design meets performance objectives in the field, a statistical simulation of the manufacturing process and field performance is useful. This simulation can analyze the effects of component and adjustment tolerances, simulate the tuning procedure and temperature and aging effects, and statistically optimize the design to give both the greatest manufacturing yield and a prediction of the end-of-life performance.

In the design of filters, early attention to the physical realization and tuning and testing for manufacture is important. Lack of attention to these details can result in an unmanufacturable design and/or a design that has excessive cost. In addition, when new technology is introduced, the designer must closely follow the initial manufacture of his design to aid the manufacturer in overcoming initial production hurdles.

## III. FILTER ENVIRONMENT AND REQUIREMENTS

The D1 and D3 channel banks[1] are the terminals for the T1 PCM repeatered line.[8,9] The T1 PCM line carries 24 telephone conversations over two cable pairs. A simplified sketch of the voice frequency end of the D3 channel bank is shown in Fig. 1. A voice-frequency analog signal from the switching equipment passes through a hybrid trans-

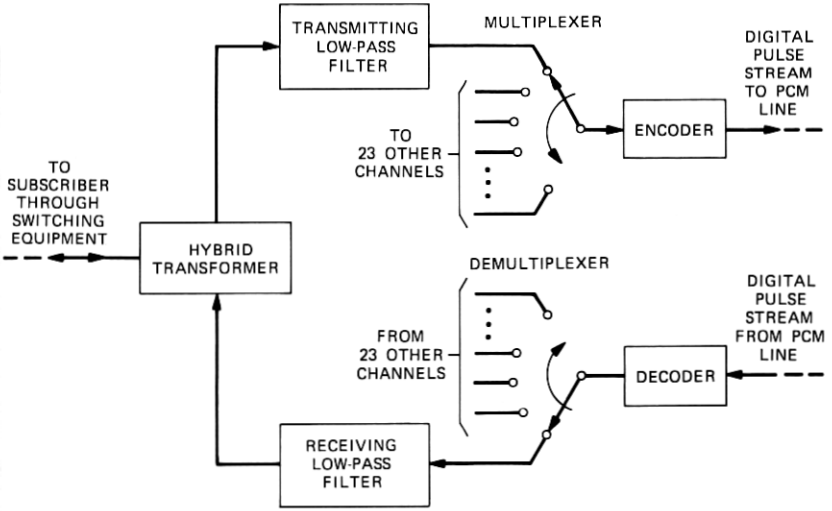


Fig. 1—Simplified model of PCM channel bank.

former. It is then amplified and bandlimited by the transmitting low-pass filter. Subsequently, it is converted into a pulse-amplitude modulated (PAM) signal by a JFET (junction field-effect transistor) switch operating at an 8-kHz rate. The PAM signals from the 24 channels are sequentially encoded into a binary bit stream (1.544 megabits/s) and sent out as PCM signals over a line. On the receiving end, the incoming PCM signals are sequentially decoded and converted to PAM signals. The analog signal for each individual channel is then recovered from the PAM signal by passing it through an interpolating receiving low-pass filter. The analog signal then passes through the hybrid transformer to the switching equipment and subsequently to the subscriber.

The transmitting band-limiting filter must present a good impedance to the hybrid transformer and negate the effect of the switched load impedance. In addition, it must pass frequencies between 200 and 3200 Hz with less than $\pm 0.09$-dB ripple and suppress frequencies above 5 kHz by at least 30 dB. At half the sampling rate of 8 kHz (or 4 kHz), there must be at least 15 dB of suppression. An RC active filter is ideal for this voice-frequency application, since the operational amplifier output will be impervious to the time-varying load, and the passband ripple performance is not degraded by inductor losses. The above requirements can be met with a fifth-order Cauer-Chebyshev filter. To obtain a low-cost, highly reliable filter conducive to high-volume manufacture, thin-film tantalum technology[3] was chosen for the physical realization.

One method of realizing a multiple-order active filter is cascading noninteracting lower-order sections. This realization consists of two stages. The first stage is a modification of a low-pass notch section (Fig. 2) developed by J. J. Friend.[10] It is a differential-input single operational-amplifier section. The second stage is a twin-T notch section[11] that has been modified by the addition of an RC network (Fig. 2) to include the pole on the negative real axis. Their respective transfer functions are

$$T_1(s) = \frac{s^2 + \omega_{z1}^2}{s^2 + \frac{\omega_{p1}}{Q_{p1}} s + \omega_{p1}^2} \tag{1}$$

and

$$T_2(s) = \frac{s^2 + \omega_{z2}^2}{\left(s^2 + \frac{\omega_{p2}}{Q_{p2}} s + \omega_{p2}^2\right)(s + \alpha)}. \tag{2}$$

The nominal performance of each section and the overall design is given in Fig. 3.[12]

The smoothing filter on the receiving side of the channel presents the designer with a difficult problem. It has a time-varying, rather than a time-invariant, generator impedance. This is caused by the JFET switch, which operates at an 8-kHz rate (125 μs) and is "on" for 3.5 μs. The switch working in conjunction with the input impedance of the network contributes an additional frequency-dependent gain characteristic to the filtering function of the network. A detailed description of the design of this filter is given in the next section.

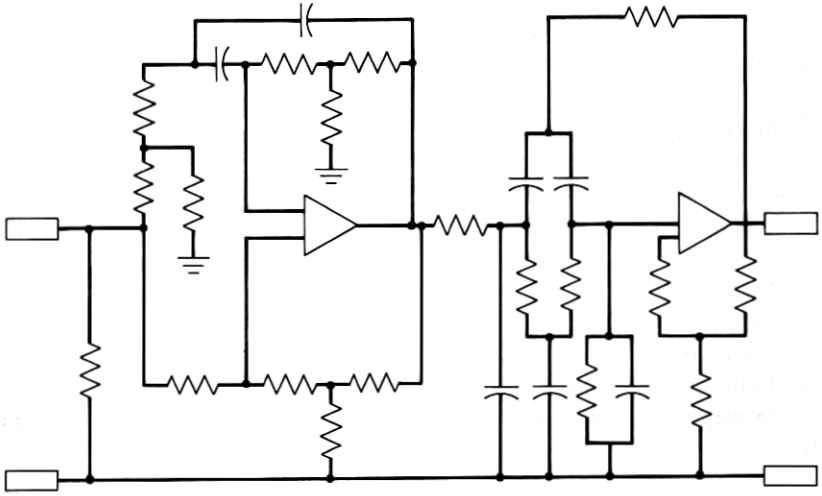

Fig. 2—Configuration of transmitting filter.

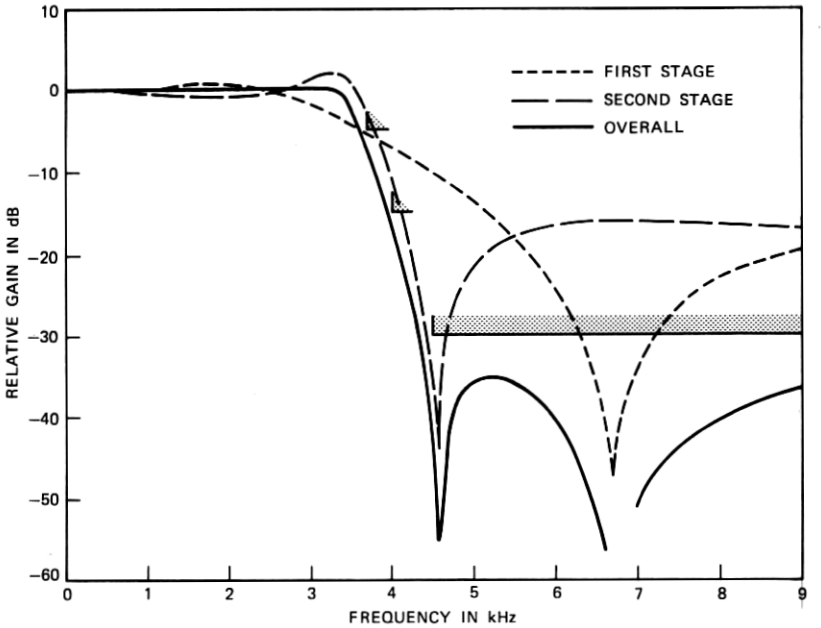


Fig. 3—Nominal performance of transmitting filter.

The design objectives of the receiving filter are as follows:*

(*i*) Passband ripple (200 Hz–3200 Hz) $\leqq \pm 0.16$ dB.
(*ii*) At 3300 Hz: 0.16 dB $\geqq$ gain $\geqq -0.60$ dB.
(*iii*) At 3400 Hz: 0 dB $\geqq$ gain $\geqq -1.20$ dB.
(*iv*) At 4000 Hz: gain $< -15$ dB.
(*v*) Above 5000 Hz: gain $< -30$ dB.
(*vi*) Gain at 1000 Hz: 4.75 dB $\pm$ 0.02 dB.

In addition, the filter must absorb the following manufacturing and environmental variations:

(*i*) Switch "on time": 3.1 $\mu$s to 3.7 $\mu$s.
(*ii*) Switch "on resistance": 50 $\Omega$ to 200 $\Omega$.
(*iii*) Temperature: 0°C to 60°C.
(*iv*) Aging: 20-year life.

## IV. INITIAL DESIGN OF THE RECEIVING FILTER

The configuration and nominal performance of the receiving filter are given in Figs. 4 and 5, respectively.[13,5] If the switch were not present, the requirements in Section III could be met by a fifth-order

* All gains and losses are relative to 1000 Hz.

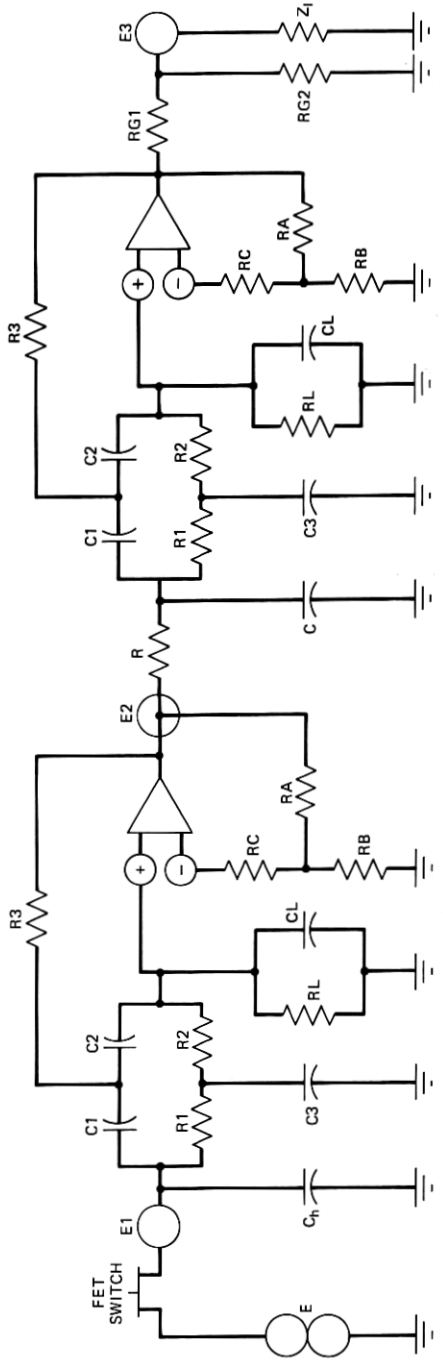


Fig. 4—Configuration of receiving filter.

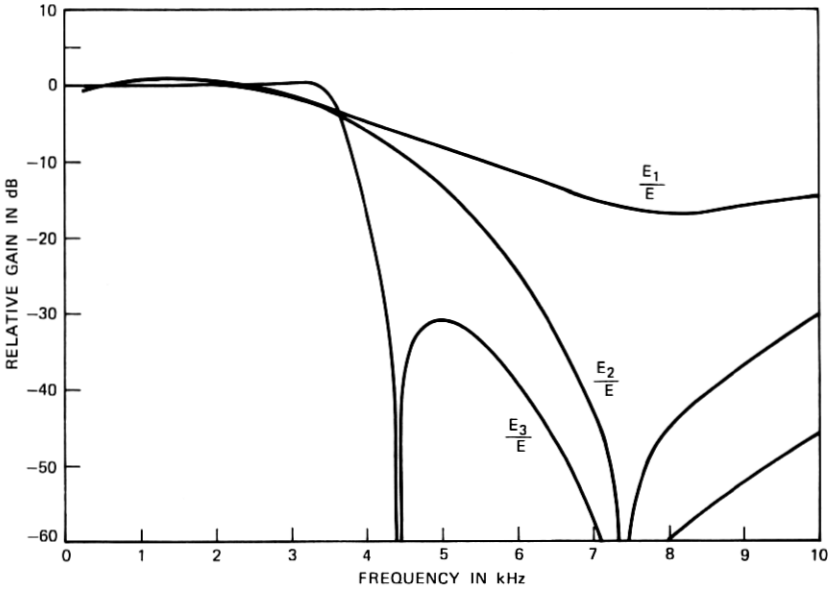


Fig. 5—Nominal performance of receiving filter.

Cauer-Chebyshev transfer function of the form

$$T(s)=\frac{V_{out}}{V_{in}}$$
$$=K\frac{(s^2+\omega_{z1}^2)(s^2+\omega_{z2}^2)}{[s^2+(\omega_{p1}/Q_{p1})s+\omega_{p1}^2][s^2+(\omega_{p2}/Q_{p2})s+\omega_{p2}^2](s+\alpha)}. \quad (3)$$

The first pole-zero pair can be realized with a second-order tuned twin-T.[14] The real pole at $s = -\alpha$ could be realized with a first-order section, although an operational amplifer can be saved by combining this pole with the second pole-zero pair to form a third-order twin-T section.

To maintain the gain level and reduce the sensitivity to switch "on time" and "on resistance" variations, the input stage must provide some "holding" function.[13] An ideal sample-and-hold network would accomplish this, but it would require an additional operational amplifier. Therefore, a holding capacitor was added to the input stage. When the switch is on (for a nominal 3.5 $\mu$s), the capacitor $C_h$ is charged. During the off time (121.5 $\mu$s), the capacitor will slowly discharge through the network if the input impedance is at a high level (>100 k$\Omega$). The switch working in conjunction with the high input impedance of the first stage acts as a lossy sample-and-hold network with a $(\sin x)/x$-type frequency-dependent gain character-

istic. This gain characteristic has minima at multiples of the 8-kHz switch rate ($E_1/E$ in Fig. 5).

To design this filter, we could first assume that no switch or holding capacitor is present. An initial network would then be developed, to which the switch-and-holding capacitor would be added. Because of the roll-off introduced by the lossy sample and hold, further optimization would be required. Using a state-variable switched-filter analysis program in conjunction with a general-purpose optimization program,[4,5] the desired frequency characteristic is obtained (Fig. 6).

The program output gives the element values of the first stage of the filter (including the holding capacitor) and the transfer function coefficients of the second stage of the filter. To realize the second stage, the element values must be described as a function of the transfer function coefficients. The transfer function for a tuned, twin-T, second-order section with a preceding RC stage can be written as

$$T(s) = K \frac{s^2 + \omega_z^2}{[s^2 + (\omega_p/q_p)s + \omega_p^2](s + \alpha)} \tag{4}$$

or

$$T(s) = K \frac{s^2 + \omega_z^2}{s^3 + A_1's^2 + A_2's + A_3'}. \tag{5}$$

If we define

$$\begin{aligned} \beta &= 1 + (RA/RB), \\ c_1 &= (2CL/C1), \\ c_2 &= (CL/C), \\ r_1 &= (2R1/RL), \\ r_2 &= R/RL, \end{aligned} \tag{6}$$

and assume the twin-T is symmetrical and tuned, the coefficients of (5) can be written as

$$K = \frac{\beta}{RC(1 + c_1 + c_2)} \tag{7}$$

$$\omega_z^2 = \frac{1}{(R1\ C1)^2} \tag{8}$$

$$A_1' = \frac{1}{(1 + c_1 + c_2)} \left[ \frac{1 + c_1}{RC} + \frac{2}{R1\ C1} \left(2 - \beta + \frac{r_1 + c_1}{2}\right) + \frac{2}{R1\ C} \left(2 - \beta + c_1 + \frac{r_1}{4}\right) \right] = \frac{\omega_p}{q_p} + \alpha \tag{9}$$

$$A_2' = \frac{1}{(1 + c_1 + c_2)} \left[ \frac{1 + r_1 + c_2}{(R1\ C1)^2} + \frac{2}{RC\ R1\ R2} \left(2 - \beta + \frac{r_1 + c_1}{2}\right) + \frac{2}{R1^2\ C1\ C} (2 - \beta + r_1) \right] = \omega_p^2 + \frac{\omega_p}{q_p} \alpha \tag{10}$$

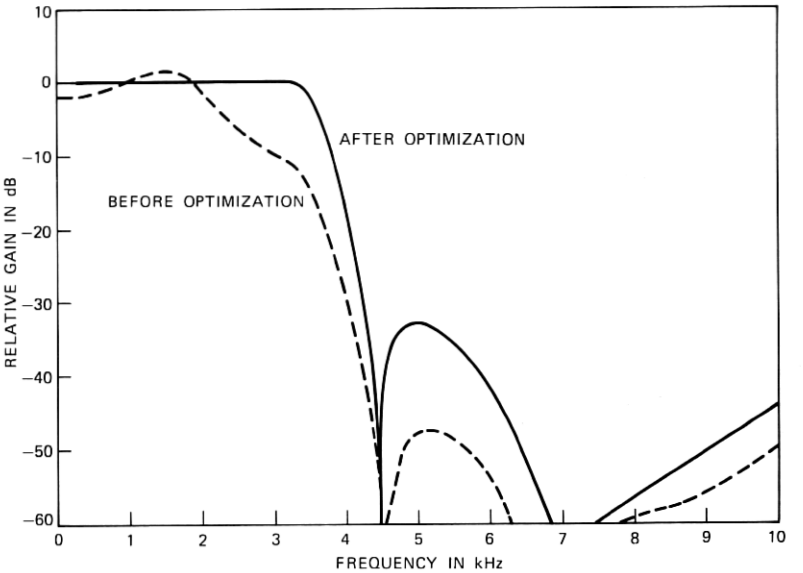


Fig. 6—Receiving filter before and after optimization.

and

$$A_3' = \frac{1}{RC}\left(\frac{1 + r_1 + r_2}{1 + c_1 + c_2}\right)\frac{1}{(R1\ C1)^2} = \omega_p^2\alpha. \tag{11}$$

Since there are more parameters (elements) than constraints (coefficients), the designer can optimize both the absolute values of the elements and the element value ratios, in addition to matching the required coefficients. An interactive computer program[15] was used to obtain the element values of the third-order twin-T.

## V. SENSITIVITY CONSIDERATIONS

An important concern in the design of filters is the degradation of the frequency response because of environmental and element value changes. Some portions of this degradation can be controlled by specifying components with tight tolerances, or by carefully tuning the filter. Others can be controlled by matching the temperature coefficients of the components used. However, there are some uncontrollable changes, e.g., aging, adjustment tolerances, and measurement tolerances. The sensitivity of the filter design to these changes will determine whether a particular technology can be used in the realization, the amount of tuning required, the margin requirements of the design, the tolerance of the components, and, subsequently, the cost of the filter.

Many approaches can be taken for analyzing the sensitivity of the filter to element changes. One is the degradation of the frequency

response caused by all elements taken one at a time. This method is very useful in determining which elements require tight tolerances and whether tuning or tracking is required. Another is the variation of the frequency response under true manufacturing and environmental variations. This would involve all components varying according to some statistical description.

As an illustration of the first type of sensitivity, Fig. 7 shows the degradation of the frequency response of the receiving filter when each capacitor is increased in value by 1 percent. Although the response degrades significantly with these capacitor variations, the degradations tend to cancel if the capacitors vary in the same direction (track). In fact, as can be seen from eqs. (5) through (11), if the second-stage capacitors track perfectly, i.e., all capacitors increase by 1 percent, the only effect on the frequency response of that stage will be a shift in frequency.

Also, from eqs. (5) through (11), it can be shown that if, in addition, the resistors vary in the opposite direction from the capacitors, then even this degradation is cancelled. Another point evident from Fig. 7 is that even $\pm 1$-percent capacitor variations would cause the response to miss the frequency requirements. Since thin-film capacitors can only be manufactured to $\pm 5$-percent tolerances, it is evident that initial tuning of the network is necessary.

Fortunately, thin-film resistors and capacitors have opposite temperature and aging characteristics. Thus, once tuned, the frequency response is quite stable. However, since the tracking is not perfect, further analysis must be undertaken.[16] This is explained in Section VII.

## VI. TUNING

Many elegant tuning procedures have been developed for hybrid integrated circuits.[17–19] Most rely on gain and/or phase measurements at a number of frequencies (one for each transfer function coefficient) and adjustment of element values in some algorithmic fashion. Usually, some form of descent algorithm, depending upon component sensitivity, with a number of iterations is used to solve this multiparameter optimization problem. Thin-film networks contain critical constraints. The capacitors cannot be adjusted and the resistor values can only be increased either by anodization[20] or laser trimming.[21]

For the above network, nine constraints must be satisfied. They are the zero frequencies of each stage, the frequency of the real pole of the second stage, the frequencies and $q$'s of the two complex poles, and the 1-kHz flat gain. In addition, the manufacturing deviations of the switch "on resistance" and the holding capacitor must be compen-

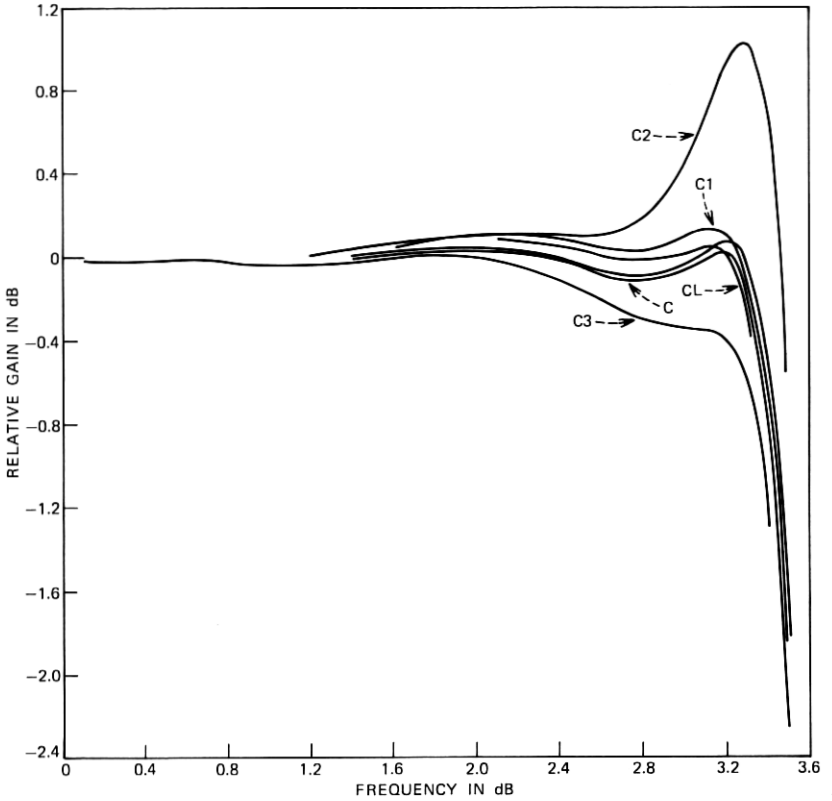


Fig. 7—Sensitivity of frequency response to capacitor changes of +1 percent.

sated for. Consultations with manufacturing engineers indicated that most iterative approaches that involved measurements of the performance at a number of frequencies were impractical from a throughput viewpoint, i.e., they took too much time.

From the manufacturing viewpoint, two points are critical: (*i*) the adjustment sequence must be fast and (*ii*) the adjusted network must meet the given frequency requirements. To accomplish both these aims, the tuning procedure shown in Fig. 8 was developed. It consists of two parts. The first is parametric; that is, it depends only upon component measurements and component adjustments. The second is functional; the gain is measured at *one* frequency for each stage, and an adjustment is made to bring the gain at that frequency to its nominal value. Finally, the voltage divider network at the output is used to trim the absolute through gain at 1 kHz to a predetermined level.

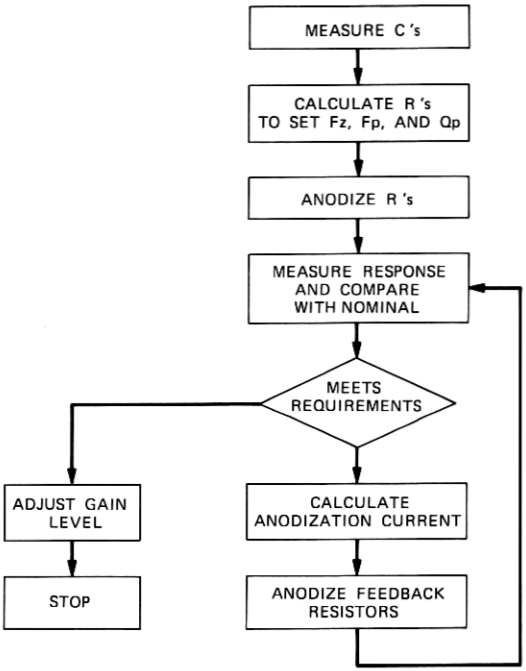


Fig. 8—Tuning procedure.

To tune the first stage of the filter, the switch-and-holding capacitor are initially neglected. The remaining part is a second-order twin-T notch filter whose transfer function is given in the appendix. Since the capacitors $C1$, $C2$, $C3$, and $CL$ cannot be adjusted, their values are measured. To obtain a null at the prescribed frequency, eqs. (22), (25), and (27) dictate that

$$\frac{1}{(C1 + C2)R3} = \frac{R1 + R2}{R1\ R2\ C3}, \tag{12}$$

$$\omega_z^2 = \frac{1}{R1\ R2\ C3\ CS}. \tag{13}$$

Since the capacitor values are known, the constraints given by (12) and (13) can be satisfied if we pick

$$R1 = R2 = \frac{1}{\omega_z(CS\ C3)^{\frac{1}{2}}} \tag{14}$$

and

$$R3 = \frac{R1}{2}\frac{C3}{C1 + C2}. \tag{15}$$

To set the pole frequency, eqs. (22) and (32) can be used. Thus,

$$\omega_p^2 = \frac{1 + (2R1/RL)}{1 + (CL/CS)}\,\omega_z^2. \tag{16}$$

Since all the variables but $RL$ of (16) are known, $RL$ can be used to set $\omega_p$. Rearranging (16),

$$RL = \frac{2R1}{[1 + (CL/CS)](\omega_p/\omega_z)^2 - 1}. \tag{17}$$

At this point, we have calculated the resistor values necessary to set the null, null frequency, and pole frequency of (28). To set the pole $q$, eq. (30) can be used. It is repeated here for convenience.

$$a_1 = \frac{\omega_p}{q_p} = \left[\frac{1-\beta}{R3\,C1} + \frac{1}{R2\,CS} + \frac{2CL}{R1\,C3\,CS} + \frac{1}{RL\,CS}\right] \Big/ \left(1 + \frac{CL}{CS}\right). \tag{18}$$

At this point, all the capacitors have been measured and $R1$, $R2$, $R3$, and $RL$ have been adjusted. Thus, the only additional adjustment that can be made is on $\beta$, which is controlled by negative feedback resistors $RA$ and $RB$. In fact,

$$\beta = 1 + \frac{RA}{RB}. \tag{19}$$

Solving (18) for $\beta$, we have

$$\beta = 1 + R3\,C1\left\{\frac{1}{CS}\left[\frac{1}{R2} + \frac{2CL}{R1\,C3} + \frac{1}{RL}\right] - \frac{\omega_p}{q_p}\left(1 + \frac{CL}{CS}\right)\right\}. \tag{20}$$

To adjust $\beta$ to coincide with that calculated by (20), $RA$ and $RB$ are adjusted.

Because we have neglected the holding capacitor and switch "on resistance," it is necessary to functionally adjust this stage. This adjustment is done at 2100 Hz, where the desired nominal gain with respect to 1000 Hz is known. Through sensitivity studies, it was found that the gain deviation from nominal at 2100 Hz was linearly dependent upon the ratio of the $\beta$ resistors, $RA$ and $RB$. Hence, either $RA$ or $RB$ is adjusted to complete the tuning of the first stage.

Since there is interaction between the real pole, the complex pole, and the transmission zero, the tuning of the second section is more complicated. With $C1$, $C2$, and $C3$ (Fig. 5) measured and the zero frequency $\omega_z$ given, the twin-T resistors $R1$, $R2$, and $R3$ can be determined. With $C$ and $CL$ measured and $\alpha$, $\omega_p$, and $q_p$ given, eqs. (9) through (11) are a nonlinear set of equations in terms of $\beta$, $R$, and $RL$. Using the nominal values of these parameters as starting guesses, the

new values which set $\alpha$, $\omega_p$, and $q_p$ to their design values are easily found.

After anodizing the resistors $R$, $R1$, $R2$, $R3$, $RL$, $RA$, and $RB$ to their calculated values, a functional adjustment is performed at 3300 Hz where the nominal gain value is known. This adjustment mops up the previous capacitor measurement and resistor adjustment errors and operational-amplifier variations. As in the first stage, the resistor ratio of the negative feedback network is touched up in a functional adjustment.

Finally, the gain at 1000 Hz must be adjusted to within $\pm 0.02$ dB. To increase the output level, $RG2$ is increased. To decrease the level, $RG1$ is increased.

## VII. TOLERANCE ANALYSIS

The network designer's work would be cut significantly if inexpensive components could be manufactured to their nominal values and have no variations with time and temperature. However, manufacturing processes are such that the designer must consider variations in the component values and characteristics from sample to sample. He could do a worst-case analysis in which he would specify tolerances that would ensure that, under all component combinations, the final manufactured network would meet specifications. In general, this would result in specifying tighter tolerances than needed and necessarily increase the cost of the network.

To get a realistic estimate of the performance of the filter as it left the manufacturing facility and a good prediction of its field performance, a statistical simulation of the manufacturing process and environmental behavior was developed. Included in this model were manufactured element variations, measurement errors, adjustment errors, temperature and aging characteristics of the components, and switch timing variations. The variables were the tolerances and distributions associated with the above errors, the adjustment procedure, and the adjustment frequencies. The figure of merit was the highest possible end-of-life yield at the lowest possible cost. Figure 9 is a flowchart for this simulation.

The simulation proceeds in the following manner. First, a set of random numbers is generated for a network. Next, the manufactured capacitor and JFET "on resistance" values are calculated. For the thin-film capacitors, the absolute tolerance and the tracking tolerances are included. The switch "on resistance" has a nominal value of 125 ohms and can vary between 50 and 200 ohms. The next step is a simulation of the tuning procedure, where the capacitors are first measured, the resistor values calculated, and the resistors adjusted.

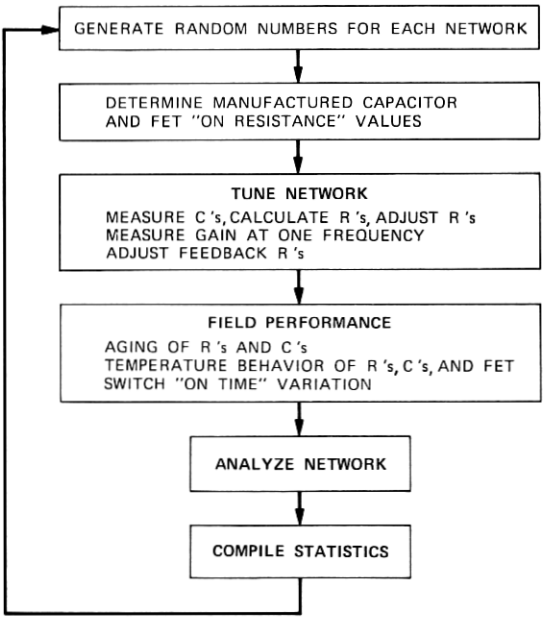


Fig. 9—Flow chart of tolerance analysis program.

For this parametric adjustment, the errors in capacitor measurement and the anodization errors for the resistors are included. During the functional touch-up adjustment, gain measurement errors are simulated. To evaluate the field performance, we use the temperature and aging characteristics of the components.

Finally the network is analyzed for the final element values that are determined by adding the temperature and aging deviations to the manufactured element values. Then the network performance is compared with the specifications at a number of frequencies, and statistics are compiled. If the requirements are not met at any one frequency, the network has failed. Next, a new network is picked, and we repeat the process.

The statistical performance of this filter is shown in Figs. 10 and 11. Only the minimum and maximum deviations at each frequency for 1000 sample networks are shown. At each frequency, there is a normal distribution of the networks' performance between the minimum and maximum deviations. At room temperature, 25°C, 94.5 percent of the samples fell within the design objectives, while at 60°C, 89.3 percent fell within. To ensure that the mathematical modeling was correct, these results were compared with the measured performance of the first 1000 filters manufactured. All those filters fell within the given

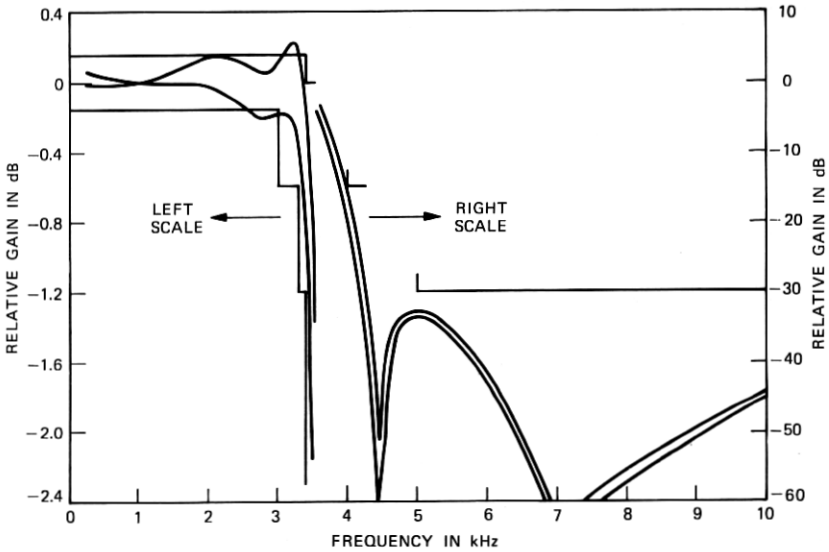


Fig. 10—Overall statistical performance of filter.

statistical bands. This type of extensive simulation is justified when we have a well-characterized technology, automated adjustment and testing, and high-volume manufacturing.

## VIII. PRODUCTION EXPERIENCE

As previously mentioned, the tolerance analysis program has aided in obtaining a practical tuning procedure. If temperature and aging variations are ignored, the program predicts the filter yield at the end of the manufacturing process. The assigned component tolerances have a significant effect on manufacturing costs; thus, a trade-off takes place between manufacturing cost and filter yield. Ideally, we would like to find the set of component tolerances that minimizes manufacturing cost. This problem has been attacked by Karafin[22] and Pinel and Roberts.[23] However, their work has been restricted to networks where: (*i*) the performance criteria (i.e., gain or loss constraints at given frequencies) is met 100 percent of the time; (*ii*) tunable elements are banned, and (*iii*) there is no correlation between the elements.

In the case of the D3 filters, it is known that the 100-percent performance criteria restriction will not produce a minimum cost network. In other words, if the yield at final test drops from 100 to 96.7 percent by increasing the tolerance on the resistors during parametric adjustment, the cost drops by more than 3.3 percent. Thus far, cost minimization has been attacked in a heuristic manner. Figure 12 shows the

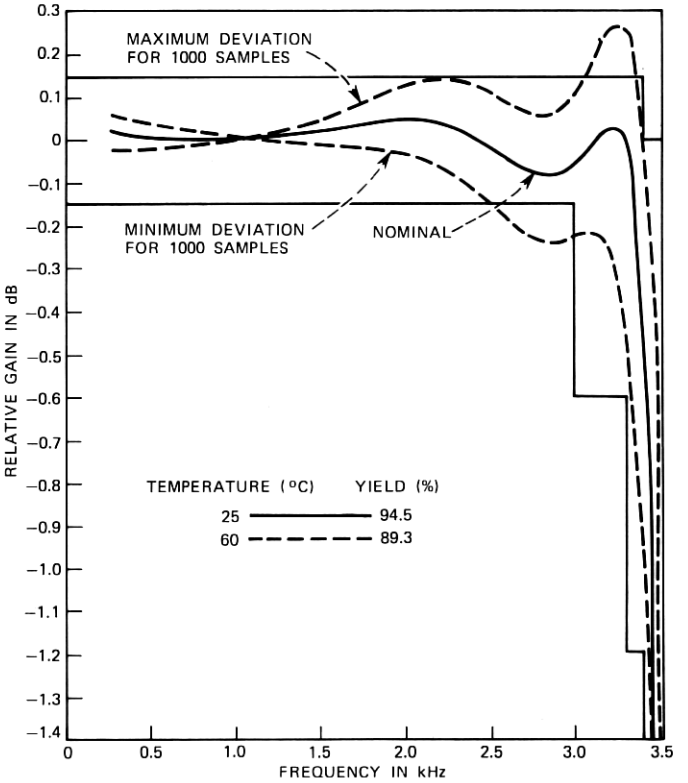


Fig. 11—Statistical performance of passband at temperature extreme.

theoretical manufacturing yields for the transmit filter at 0.1, 0.2, and 0.5-percent resistor tolerances. Current production experience indicates that widening the tolerance on certain resistors to 0.3 percent results in a lower cost, even though the overall yield decreases.

One might ask, Why not remove all tolerance restrictions on the parametric adjustments and accept any filters as long as they are functionally adjusted to meet the frequency requirements at a finite set of test points? The answer is quite simple. If all resistors were adjusted at the parametric step to, say, 0.5 percent tolerance, then only 50 percent of the filters could meet requirements after functional adjustment. Since the silicon is bonded after parametric adjustment, a much higher final yield is needed to justify the additional investment. In addition, as the tolerance is relaxed at the parametric adjustment step, more frequency tests are required at final test.

The tolerance analysis program also helped to provide a temporary solution to a capacitor tracking problem. If the ratio of certain capaci-

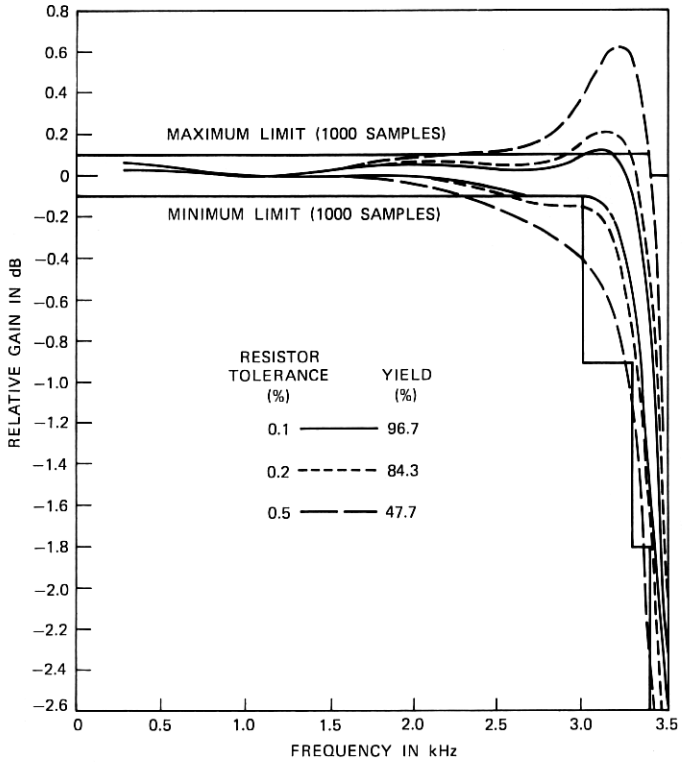


Fig. 12—Statistical performance of transmitting filter with different resistor tolerances.

tors is not within specified limits, then some resistors may have to be anodized excessive amounts—excessive because the resistors will then age poorly. However, the tracking requirement on all sets of capacitors need not be the same; thus, in a particular case, with the tolerance program, it was possible to demonstrate that the tracking requirement on a pair of capacitors could be relaxed and therefore solve a temporary production problem.

A tolerance analysis program can be used only if we have good estimates for the various tolerances that affect the manufacturing process. This was possible for the parameters that influence the frequency performance, but not possible for the dc gain requirement. The 1-kHz frequency gain is required to be adjusted to an accuracy of $\pm 0.02$ dB. This stringent requirement was chosen so that no adjustments would be necessary when D3 channel banks were installed in the field. The no-adjustment philosophy saves on installation and maintenance cost, but it does require critical tuning for the D3 filters.[24]

## IX. PHYSICAL REALIZATION

In this case, the physical realization uses single-substrate hybrid-integrated circuit (HIC) technology.[3] The resistors are tantalum nitride thin film, and the capacitors have a base electrode of $\beta$-tantalum, a dielectric of tantalum pentoxide, and a counter electrode of nichrome paladium gold. The conductor paths are also nichrome paladium gold, while the operational amplifiers and JFET switch are beam-leaded silicon integrated circuits. They are all placed on a 33-by-20 mm glazed ceramic substrate with a 34-terminal lead frame (Fig. 13).

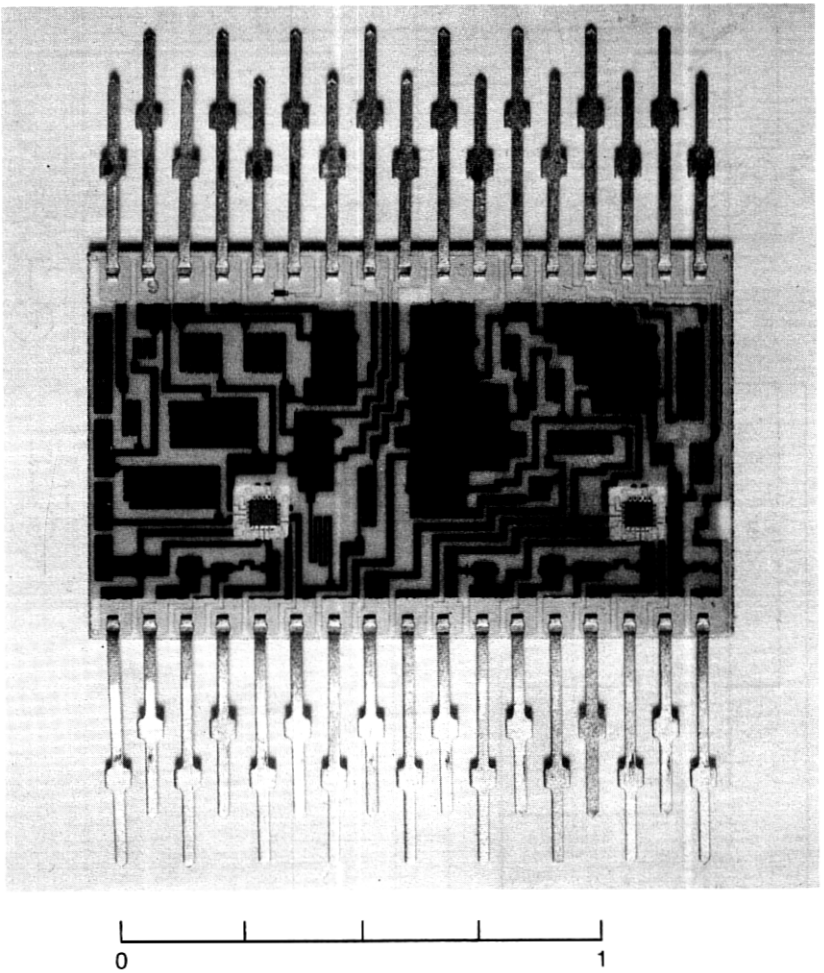


Fig. 13—Hybrid integrated circuit realization of filter.

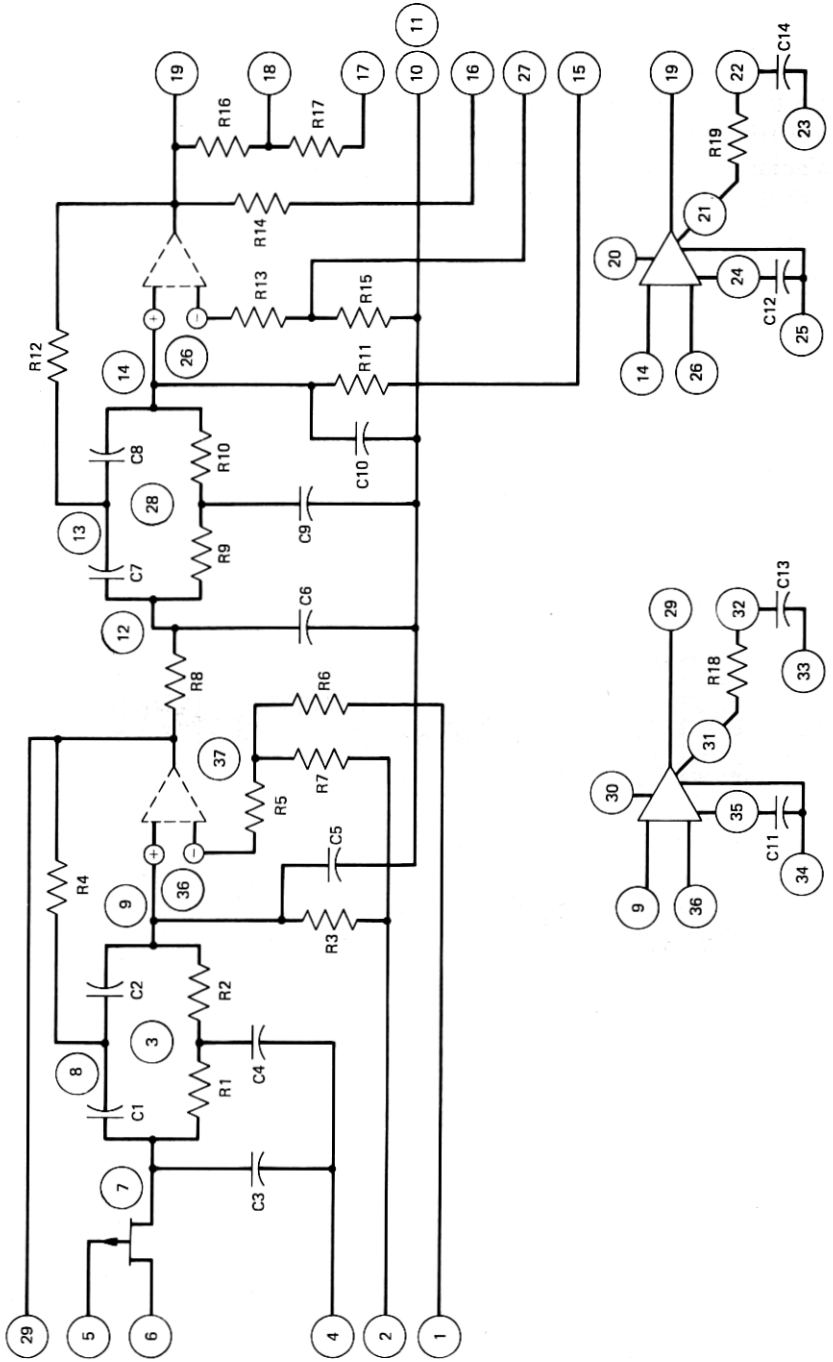


Fig. 14—Electrical layout of HIC realization.

To minimize both the tuning time and the complexity of the test fixtures, the substrate layout was constrained. Thus, all measurements are made from the sides and all adjustments from the top of the substrates. To incorporate the tuning procedure of Section VI, the layout must provide the capability of measuring all element values. Thus, all network nodes must be brought to the edge of the substrate.

Traditionally, layouts follow the flow of a network. Thus, for a network of this complexity, crossovers are generally required, as well as break points, to measure the component values. Crossover and break closures are normally processed following filter tuning. To eliminate breaks and crossovers and separate the measurement and adjustment functions, a unique circuit layout was developed. These aims were accomplished by judiciously separating common grounds and incorporating break points. These redundant points are brought to the substrate edge (Fig. 14) and are subsequently connected when the substrate is inserted into a printed wiring board. Three terminal capacitor measurements and capacitor electrode sharing were necessary to make these measurements. To realize this layout with its subsequent 11 mask levels required considerable reliance on computer-aided graphics.[25,26]

## X. ACKNOWLEDGMENTS

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## APPENDIX

### *Transfer Function of Second-Order Twin-T Section*

#### *A.1 Untuned case*

The transfer function of the untuned, unsymmetrical second-order twin-T is

$$T(s) = K\frac{(s+\tau_2)s^2 + (s+\tau_1)\omega_z^2}{(s+\tau_1)D(s) + \delta_\tau E(s)}, \tag{21}$$

with the following definitions:

$$\begin{aligned} CP &= C1 + C2, & CS &= (C1\ C2)/CP, \\ RS &= R1 + R2, & RP &= (R1\ R2)/RS, \\ \tau_1 &= 1/(R3\ CP), & \tau_2 &= 1/(RP\ C3), \\ \delta_\tau &= \tau_2 - \tau_1, & \beta &= 1 + (RA/RB), \\ c_1 &= CL/CS, & r_1 &= RS/RL. \end{aligned} \tag{22}$$

The polynomials $D(s)$ and $E(s)$ of (21) are

$$D(s) = s^2 + \left[ \frac{1-\beta}{R3\,C1} + \frac{1}{R2\,CS} + c_1\tau_2 + \frac{1}{RL\,CS} \right] \frac{s}{(1+c_1)} + \left( \frac{1+r_1}{1+c_1} \right) \omega_z^2, \quad (23)$$

$$E(s) = \left[ \frac{1}{1+c_1} s + \frac{(1-\beta)}{R3\,C1(1+c_1)} \right] s, \quad (24)$$

and

$$\omega_z^2 = \frac{1}{R1\,R2\,C3\,CS}, \quad (25)$$

$$K = \frac{\beta}{1+c_1}. \quad (26)$$

### *A.2 Tuned case*

When the twin-T is tuned,

$$\tau_1 = \tau_2, \qquad \delta_\tau = 0. \quad (27)$$

Thus, (21) reduces to

$$T(s) = K \frac{s^2 + \omega_z^2}{s^2 + a_1 s + a_2} = K \frac{s^2 + \omega_z^2}{s^2 + (\omega_p/q_p)s + \omega_p^2}. \quad (28)$$

If, in addition, a symmetric twin-T is picked, i.e.,

$$\begin{aligned} R1 &= R2 = 2R3 \\ C1 &= C2 = C3/2 \\ CL &= (C1\,c_1)/2 \\ RL &= (2R1)/r_1, \end{aligned} \quad (29)$$

then

$$a_1 = \frac{2}{R1\,C1} \left( 2 - \beta + \frac{r_1 + c_1}{2} \right) \frac{1}{1+c_1}, \quad (30)$$

$$a_2 = \left( \frac{1+r_1}{1+c_1} \right) \omega_z^2, \quad (31)$$

and

$$\omega_p = \left( \frac{1+r_1}{1+c_1} \right)^{\frac{1}{2}} \omega_z, \quad (32)$$

$$q_p = \frac{[(1+r_1)(1+c_1)]^{\frac{1}{2}}}{2[2 - \beta + (r_1 + c_1)/2]}. \quad (33)$$

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