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A Fundamental Comparison of Incomplete Charge Transfer in Charge Transfer Devices

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Using a small-signal analysis, we present a general comparison of the more important contributions to the incomplete transfer of charge in the following charge transfer devices: (i) the polyphase charge-coupled device and the IGFET bucket-brigade shift register, where individual charge transfers are single-step processes, and (ii) the two-phase charge-coupled device, the conductively connected charge-coupled device, the tetrode bucket brigade, and the stepped-oxide bucket brigade, where individual charge transfers are two-step processes. A recently proposed lumped-charge-model approximation is made in order to estimate the time dependence of the transferred charge including both drift and diffusion. In this calculation we also include the effects associated with the injection of charge from a diffused source into the IGFET channel which modify the current-voltage behavior at low currents. Using this calculation of the time dependence of the transferred charge, the various contributions to incomplete transfer, including those due to trapping in the interface states, are derived and compared for each of the charge transfer devices of interest. The results

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show that highest transfer efficiencies at low frequencies will usually be obtained from suitably designed shift resisters utilizing a two-step transfer process. This is because a two-step process tends to reduce those contributions to incomplete transfer which are due to signal-charge-modulation of the conductances and capacitances governing the charge transfer current. For example, the coefficient of incomplete charge transfer, α, for an individual transfer in a polyphase CCD is found to be 0.6, 0.85, and $1.4 \cdot 10^{-3}$ at 2, 4, and 8 MHz, respectively. By contrast, for the same physical device dimensions, α in a stepped-oxide, two-phase CCD is reduced to 0.35, 0.5, and $0.8 \cdot 10^{-3}$ at the same frequencies, nearly a factor of two reduction. The intrinsic contributions to incomplete charge transfer, which dominate the high-frequency operation, are found to be relatively insensitive to the type of device considered for the dimensions given. An α of $0.3 \cdot 10^{-1}$ at 100 MHz is typical. Among the various two-step process devices, interface-state effects are found to be comparable, $0.3 \cdot 10^{-3}$ being a typical value for this frequency-independent contribution. At low frequencies, a frequency-independent contribution to incomplete transfer in bucket-brigade transfer processes is found. The size of this contribution is about $0.15 \cdot 10^{-3}$. These results further illustrate the utility of analyzing incomplete transfer effects in terms of single-device, small-signal characteristics.

I. INTRODUCTION

Since the introduction of the charge-coupled device[1] (CCD) and the bucket-brigade shift registers,[2–4] there have been a number of proposed modifications to the basic structures in order to achieve specific performance goals.[5–10] It is the purpose of this paper to analyze the mechanisms of charge transfer in these devices and to compare the characteristics of the incomplete charge transfer in each. In this way one can evaluate the relative merits and limitations of these modified charge transfer devices (CTD's).

In a recent article, the authors[11] presented a general analysis of incomplete charge transfer in CTD's. Using a lumped model[12,13] to characterize the dynamics of the charge transfer, it was possible to calculate α, the small-signal coefficient of incomplete transfer, in terms of single-device, small-signal characteristics. It was found that three contributions to incomplete transfer are common to all charge transfer shift registers: an intrinsic transfer rate contribution, an output conductance or feedback contribution, and a storage-capacitance modulation contribution. A significant feature of that calculation was that each of these contributions could be expressed analytically in terms of

the charge transferred as a function of time. Analytic results are, of course, very convenient for comparative purposes. In addition, numerical values for α could be obtained, the accuracy of which depends only on the accuracy to which the transferred charge is known, and *not* on the much lower accuracy obtainable from the *difference* between the transferred charge for slightly different signal sizes. Although originally developed to treat the standard CCD and bucket-brigade[2–4] devices, it is possible by a straightforward generalization to analyze the more complicated device structures considered here with little additional effort.

In this paper we derive in a uniform manner the incomplete transfer properties[11] of the simple bucket brigade, the three-phase CCD, various two-phase CCD's, the conductively connected CCD, and the tetrode and stepped-oxide bucket brigades. These calculations are then used as a basis for comparison of the performance to be expected from each CTD. It will also become clear that other CTD's can be treated in a similar fashion.

Using a lumped-charge model for CTD behavior[13] based on a charge-control concept proposed by Lee and Heller,[12] we first calculate the time-dependence of the transferred charge in a CTD for both a bucket-brigade cell and a CCD cell. This derivation of necessity is somewhat approximate, but it is found to be satisfactory for the purpose of calculating the incomplete transfer properties by our method and is comparable with the other approximations necessary for any such calculation. Being simple, it emphasizes the important characteristics of the transfer event. From the time dependence of the charge transfer we determine the small-signal transfer inefficiency[11] and calculate the clock-frequency dependence of the several contributions to incomplete transfer. Finally, these theoretical results are applied to several specific CTD's and their important operating limitations are discussed.

II. TIME DEPENDENCE OF TRANSFERRED CHARGE

2.1 *Preliminary Considerations*

The starting point in determining the performance characteristics of a charge transfer device is a calculation of the time dependence of the charge transfer process. However, the nonlinearity of the problem, the requirement that several assumptions be made concerning the charge transport and trapping along a semiconductor interface, and the dependence of the solution on clock-voltage waveform and on the details of device design, all combine to make a general solution valid

for all cases an unrealistic goal. Indeed for our purposes here a highly accurate solution is not necessary. We shall, therefore, make assumptions to simplify the problem considerably.

2.2 *General Approach*

Our first assumptions are that the charge transfer in the more complicated modified structures can be treated as a series of simpler transfer steps, and that each charge-transfer step can be characterized by either a "CCD" transfer process or a "bucket-brigade" transfer process. The major difference between the two is that in the "bucket-brigade" transfer process the injection of carriers from a diffused region into a surface channel is taken into account. In the "CCD" transfer process, by contrast, the charge carriers are initially in the surface "channel" (storage well) and no injection over a barrier is necessary. We shall solve for the charge transfer as a function of time for both types of transfer processes. Such solutions will be sufficient to discuss CTD's in which the charge transfer from one storage region to the next are single-step processes. For CTD's with more complicated charge transfer mechanisms involving multiple-step processes, the charge transfer is represented as a series of single-step processes of either the "CCD" or the "bucket-brigade" type as is appropriate. In this way, sufficiently accurate results will be achieved to illustrate most of the important features of the charge transfer and to provide a basis for comparison of the several CTD schemes.

In order to carry out the above program, we must calculate the charge transfer in a "CCD" and in a "bucket-brigade" transfer process. The general approach that will be used will be the charge-control or lumped-charge model. This type of model has usually been used for time-dependent analyses of circuit problems[14–16] as well as for analysis of some CTD's such as the IGFET[17] and bipolar[18] bucket-brigade shift registers. By comparison of results from such a model with exact computer solutions,[19–21] it has been shown that the model is also applicable with surprising accuracy to the charge-coupled device.[12] We shall assume that the gradual channel approximation is valid for all the cases to be treated here. This means that the one-dimensional solution to Poisson's equation will be used throughout and that fringing electric fields will influence only a small fraction of the active device area, and will, by definition, mean that our results will not be applicable to CTD's such as the buried channel CCD,[22] except possibly in the high-frequency limit. For simplicity, it will also be assumed that we are dealing with p-channel devices with a constant carrier mobility, that depletion-

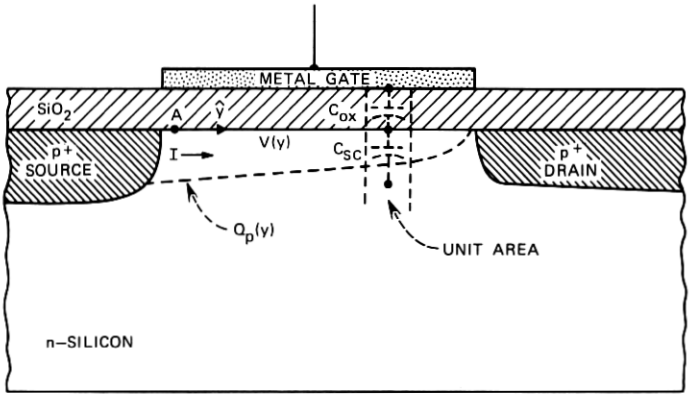

Fig. 1—IGFET gate region illustrating the symbols defined in the text.

layer capacitances are constant, voltage-independent quantities, and that the clock voltage driving the CTD's are ideal square waves.

We begin by calculating the steady-state transport under given boundary conditions for an IGFET gate. This is similar to the conventional IGFET solution except that we include carrier diffusion in addition to drift. The current-voltage relation we obtain will then be used in calculating the "CCD" and "bucket-brigade" transfer processes.

Referring to Fig. 1 and following Sze,[23] the minority carrier charge density $Q_p(y)$ is given by

$$Q_p(y) = C_i V(y) \tag{1}$$

where C_i is the capacitance per unit area of the oxide C_{ox} in parallel with the silicon space charge C_{SC}, and $V(y)$ is the silicon surface potential with reference to the surface potential value in the absence of minority carriers. A lateral electric field can only exist in the gradual channel approximation because of a gradient in Q_p, and will be represented as $-(1/C_i)(dQ_p/dy)$. Given that the current flowing at any value of y must be a constant I, and that current density J is given by

$$J = q\mu pE - qD\frac{dp}{dy} \tag{2}$$

where μ and D are the carrier mobility and diffusion constants respectively (related by the Einstein relationship), p is the hole density, and E is the electric field, one can write for the current flowing from

the source to the drain:

$$I = -\frac{Z\mu}{C_i}\left[Q_p(y) + C_i\frac{kT}{q}\right]\frac{dQ_p(y)}{dy} \tag{3}$$

where Z is the channel width. Placing the boundary condition that the surface potential V on the "drain" side of the channel is approximately zero (i.e., assume the drain voltage is sufficiently negative that we are operating in saturation) and on the "source" side is assumed equal to a voltage V_A, one obtains

$$I = \frac{\beta}{2}V_A\left(V_A + 2\frac{kT}{q}\right) \tag{4}$$

where $\beta = Z\mu C_i/L_c$ is the conventional IGFET gain factor, and L_c is the effective channel length. This expression differs from the usual saturation IGFET current expression (which ignores diffusion) only by the additive term $2kT/q$ in the last factor. Similarly we can calculate the total charge Q stored under the gate for a given voltage V_A. Representing the geometrical capacitance of the gate oxide in parallel with the underlying silicon space-charge capacitance as C_{GO},

$$Q = \tfrac{2}{3}C_{GO}V_A\left[\frac{V_A + \frac{3}{2}\frac{kT}{q}}{V_A + 2\frac{kT}{q}}\right]. \tag{5}$$

Hence, for V_A very large or very small with respect to kT/q, Q is linear in the voltage V_A. Thus an effective gate capacitance C_G can be defined which is $\frac{2}{3}$ or $\frac{1}{2}$ respectively of the geometrical capacitance. For our purposes here, this is sufficiently close to a constant value that we can assume C_G is equal to $\frac{2}{3}C_{GO}$ over the entire range of V_A of interest.

2.3 *The "CCD" Transfer Process*

In the CCD problem treated by several authors,[12,19–21,24] the transient decay of the charge stored under a single capacitor plate is calculated. With the ideal square-wave clocks assumed here, this problem is illustrated in Fig. 2. Given the charge-control or lumped-charged model assumption, the problem reduces to one of discharging a capacitor through a nonlinear resistor derived from eq. (4). In the lumped-charge model as shown above, the total charge under the plate is approximately linear in the voltage V_A (see Fig. 2). Hence, one can

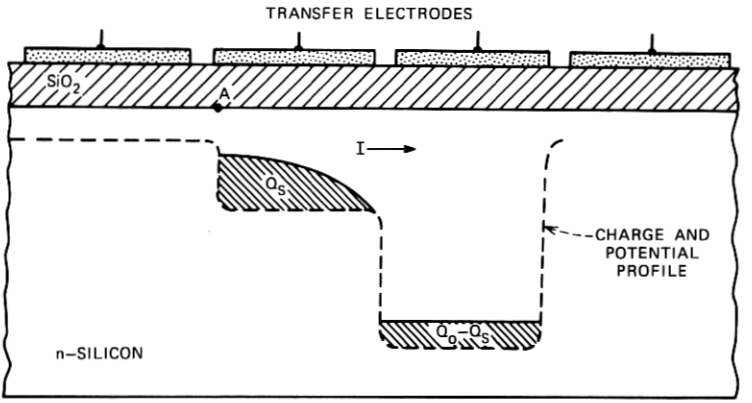

Fig. 2—Transfer of charge in a standard CCD cell with symbols defined in the text.

write from eq. (4)

$$\frac{dQ_S}{dt} = C_G \frac{dV_A}{dt} = -I = -\frac{\beta}{2} V_A \left(V_A + 2\frac{kT}{q} \right) \tag{6}$$

(L_c in β now refers to the effective length of the storage well of the CCD cell). If the initial voltage at A at the beginning of transfer was

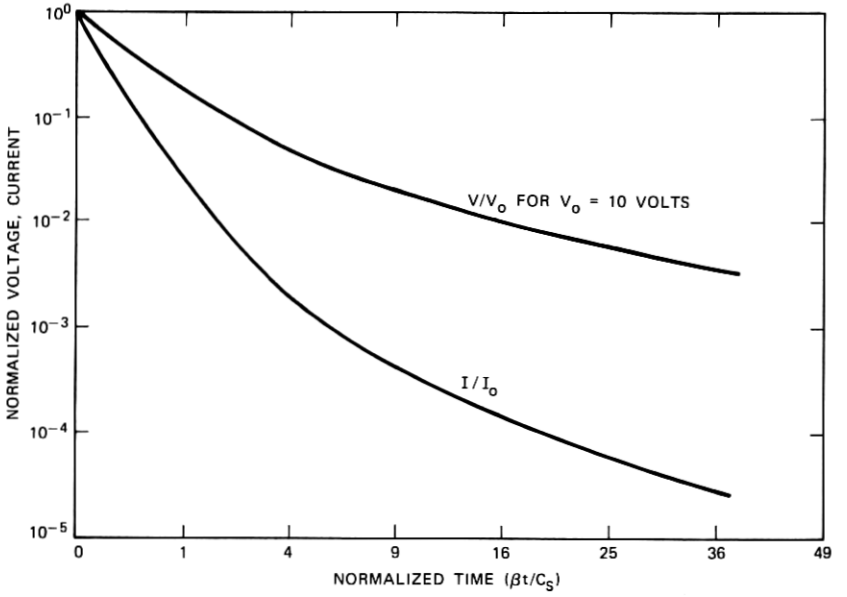

Fig. 3—Normalized voltage and current plotted as a function of normalized time for the transfer of charge from one well to the next in a standard CCD.

V_o and the voltage at time t is V, then eq. (6) gives the solution

$$\frac{V}{V_o} = \frac{\exp\left[-\frac{\beta kT}{qC_G}t\right]}{1 + \frac{qV_o}{2kT}\left[1 - \exp\left(-\frac{\beta kT}{qC_G}t\right)\right]}. \tag{7}$$

Except for the fact that V and V_o are voltages at point A rather than some appropriately defined average voltage under the plate, this result is very similar though not identical to one derived by Lee and Heller[12] and is plotted in Fig. 3 assuming a 10-volt value for V_o. Comparison of eq. (7) with the computer results of Strain and Schryer[19] also gives excellent agreement provided that the voltage V in eq. (7) is scaled to reflect the average voltage as defined by Strain and Schryer.[19]

It will be shown later that in calculating the incomplete transfer properties of CTD's the current I at time t compared to the current I_o at the initial part of the transfer is of importance. From eq. (6)

$$\frac{I}{I_o} = \frac{V}{V_o}\left[\frac{V + \frac{2kT}{q}}{V_o + \frac{2kT}{q}}\right] \tag{8}$$

and this is also plotted in Fig. 3.

2.4 *The "Bucket-Brigade" Transfer Process*

The bucket-brigade transfer problem is very similar to that of the CCD in the sense that the current during transfer is given by eq. (4) with the voltage V_A being measured at point A in the channel near the source (see Fig. 4). The important difference which requires us to treat the transfer process separately is that in the bucket brigade the minority carriers must be injected into the channel from the diffused p-regions, i.e., a large fraction of the charge is stored in the diffused regions and the p-island voltage is different in general from V_A. Representing the voltage on the source p-region as V_p, the storage capacitance associated with the p-island as C_p, and that associated with the channel as C_G, we can write analogous to eq. (6)

$$C_G\frac{dV_A}{dt} + C_p\frac{dV_p}{dt} = -\frac{\beta}{2}V_A\left(V_A + 2\frac{kT}{q}\right). \tag{9}$$

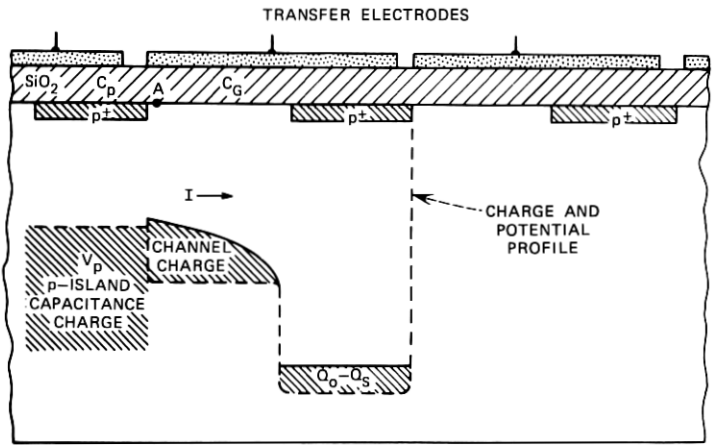

Fig. 4—Transfer of charge in a standard IGFET bucket-brigade cell with symbols defined in the text.

In order to solve this equation, a relation between the p-island voltage and V_A must be obtained. This problem has been treated somewhat differently by Barron.[25] For our purposes here, we shall simply assume that the minority carrier density at point A is related to the source p-island voltage by an expression of the form

$$C_i V_A = Q_p = Q_{po} \exp[q(V_p - V_A)/kT] \tag{10}$$

where Q_{po} is some constant [see eq. (1)]. Taking derivatives with respect to time gives

$$\frac{dV_p}{dt} = \left(1 + \frac{kT}{qV_A}\right)\frac{dV_A}{dt} \tag{11}$$

and substituting in eq. (9) we obtain

$$\frac{dV_A}{dt} = -\frac{\beta}{2C_p} V_A^2 \left[\frac{V_A + 2\dfrac{kT}{q}}{V_A\left(1 + \dfrac{C_G}{C_p}\right) + \dfrac{kT}{q}}\right]. \tag{12}$$

This expression can be solved exactly for V_A as a function of time, and such a calculation has been carried out assuming C_G negligible compared to C_p and is plotted in Fig. 5. In addition to this, however, it is of most value to note that eq. (12) reduces to the CCD transfer

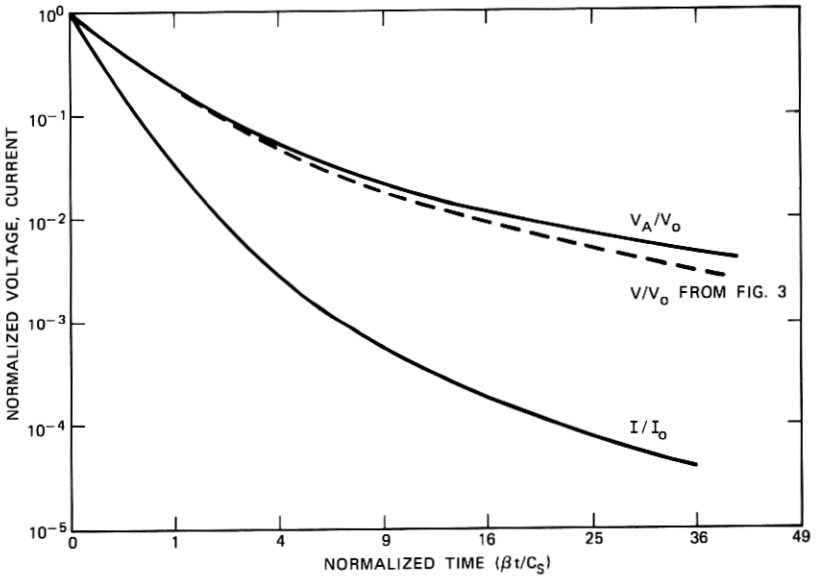

Fig. 5—Normalized voltage and current plotted as a function of normalized time for the transfer of charge from one p-region to the next in a standard IGFET bucket-brigade cell. V/V_o from Fig. 3 is shown for comparison.

result in the limit of C_p equal to zero, so that in that sense eq. (12) is a general expression for single-step charge transfer devices. Also, the last factor in eq. (12) for C_p large compared to C_G is a very slowly varying function with value on the order of one or two depending on V_A. If we assume this quantity to be unity, then the solution to eq. (12) is the previously[4] derived bucket-brigade result assuming an ideal square-law current-voltage relation

$$\frac{V_A}{V_o} = \frac{1}{1 + \dfrac{\beta V_o t}{2C_p}}. \tag{13}$$

Hence we see that for the bucket-brigade transfer process under square-wave clocks, the voltage V_A varies as reciprocal time after long times rather than exponentially as it does for the CCD transfer process. This is also illustrated by the exact solution shown in Fig. 5. Note from eq. (10) that V_p can be related to V_A through

$$V_p - V_{po} = V_A + \frac{kT}{q} \ln \frac{V_A}{V_o} \tag{14}$$

where V_{po} is a constant. Thus V_p follows V_A but differs by a term logarithmic in V_A. Since V_A varies reciprocally with time at long times, V_p ultimately has a logarithmic dependence on time as reported by Buss and Gosney.[26]

For comparison to the CCD transfer process, we have plotted V_A from Fig. 3 in Fig. 5. Also of interest is the time dependence of the transfer current, given by eq. (8) and plotted in Fig. 5.

III. TRANSFER EFFICIENCY IN CHARGE TRANSFER DEVICES

Given that one has calculated the charge left behind as a function of transfer time as in the previous section, the problem of using these results to predict the performance of an n-stage shift register remains. Under most shift register operating conditions, a circulating charge or fat zero will be used, so that a large fraction of the charge left behind after each transfer will be independent of the signal charge. Thus, a definition of transfer inefficiency as the total charge remaining divided by the total charge to be transferred will often be of little value even if we had a highly accurate solution including the net amount of charge trapped in interface states. Further, the amount of degradation in a shift register will depend on the time dependence of the particular signal being used. Since, in addition, the charge transfer process is generally nonlinear, it has been found convenient to define a differential or small-signal parameter to characterize incomplete charge transfer in CTD's; i.e., superimpose a small-signal charge on a larger background charge being continually transferred. It has been shown[27,28] that by linearizing the problem in this way, the signal degradation by an n-stage register can be readily characterized. For this reason we will focus our attention here on the small-signal incomplete transfer parameter α defined as the change in the charge left behind after transfer divided by the small change in signal charge, which was the cause of the change in charge left behind. Using derivatives

$$\alpha = \frac{dQ}{dQ_o} \tag{15}$$

where Q_o is the total charge to be transferred. ($\alpha = \alpha(t)$ since $Q = Q(t)$.) In a recent paper[11] the authors have shown that incomplete transfer in CTD's can be treated in a general way using this small-signal approach, and that α can be separated into three components: an intrinsic transfer rate term, a drain conductance or feedback term, and a storage-capacitance modulation term. Interface states introduce additional terms, but of a similar nature to these three.

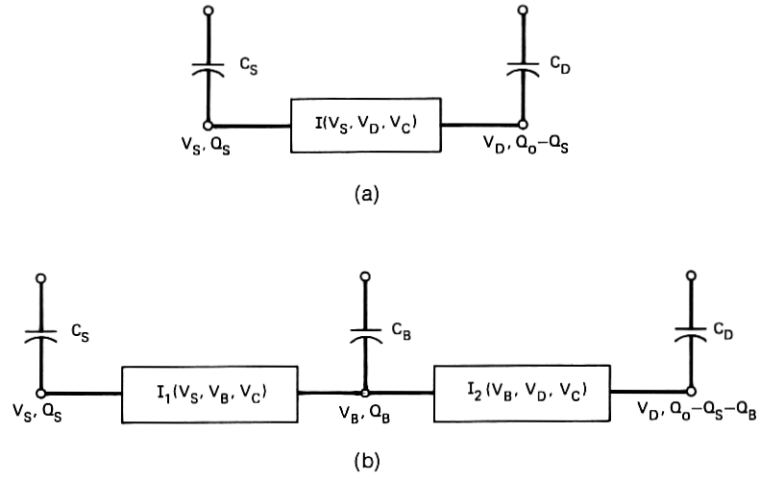

Fig. 6—(a) General representation of a single-step transfer cell of a charge transfer device. (b) General representation of a two-step transfer cell of a charge transfer device.

In this previous paper[11] we described the charge transfer process in a CTD in terms of the model shown in Fig. 6a. Although applicable for treating two-step processes, this model is really best suited for single-step processes. This being the case, it is convenient to treat a two-step process using the model shown in Fig. 6b, which is basically two single-step models in series. Even more complicated charge transfers can be treated by including additional single-step models.

The single-step process is illustrated in Fig. 6a using the same symbols as used previously. The charge from a storage capacitor C_S is transferred through some nonlinear conductance to the drain capacitor C_D as in the simple bucket brigade or the three-phase CCD. (V_C is the clock voltage.) However, in the two-step process illustrated in Fig. 6b, the charge from the storage capacitor C_S is transferred to some intermediate capacitor C_B then to the drain capacitor C_D during a single transfer period. The advantage of this is that channel-length modulation effects will be reduced, as will be described later. Examples of this kind of transfer are the two-phase CCD and the tetrode bucket brigade.

In Appendixes A and B, the various contributions to the incomplete transfer parameter α are calculated for both single-step and two-step CTD's, and in the next section, α is evaluated theoretically for several proposed CTD structures in order to provide a comparison and point

TABLE I—LIST OF ASSUMPTIONS MADE TO SIMPLIFY CTD INCOMPLETE TRANSFER CALCULATIONS

1. All devices are based on the silicon-silicon-dioxide system using n-type silicon substrates doped to a density of 10^{16} cm^{-3}.
2. The silicon dioxide thickness is 1000 Å.
3. All charge-storage regions, gates, and diffusions have a length of 10 microns.
4. Net interface state charge after transfer is constant at 2×10^{-9} coulombs per square centimeter.
5. Minority carrier mobility is constant at 200 cm^2/volt-second.
6. Fringing electric fields penetrate a distance equal to the one-dimensional space-charge width.
7. The background charge on which the signal charge is superimposed corresponds to a voltage at point A of 10 volts, and the drain-to-substrate voltage reaches a value of 10 volts at the end of transfer.
8. Clock voltages are ideal square waves.

out the important incomplete transfer mechanisms. To simplify the calculations and provide specific examples, several assumptions have been made which are listed in Table I. Calculations for conditions other than those listed in Table I can be made using the derivations in the appendix. In Table II we summarize the nature of the transfer processes involved in each type of device discussed in Section IV.

IV. INCOMPLETE TRANSFER PROPERTIES OF SEVERAL CHARGE TRANSFER DEVICES

4.1 *The Simple Bucket Brigade*

The simple bucket-brigade shift register is a two-phase CTD fabricated as illustrated in the insert in Fig. 7. In such a shift register, it has been shown[4,17] that the two dominant terms under most conditions are the drain conductance or feedback contribution, α_D, and the intrinsic transfer rate contribution, α_i. However, the analyses

TABLE II—SUMMARIES OF THE NATURE OF TRANSFER PROCESSES

Type of Device	Mode of Charge Transfer	
Single-Step Transfer Process		
Standard CCD	CCD	
Standard Bucket Brigade	BB	
Two-Step Transfer Process	First Transfer	Second Transfer
Two-Phase CCD	CCD	CCD
C4D	CCD	BB
Stepped-Oxide BB	BB	CCD
Tetrode BB	BB	BB

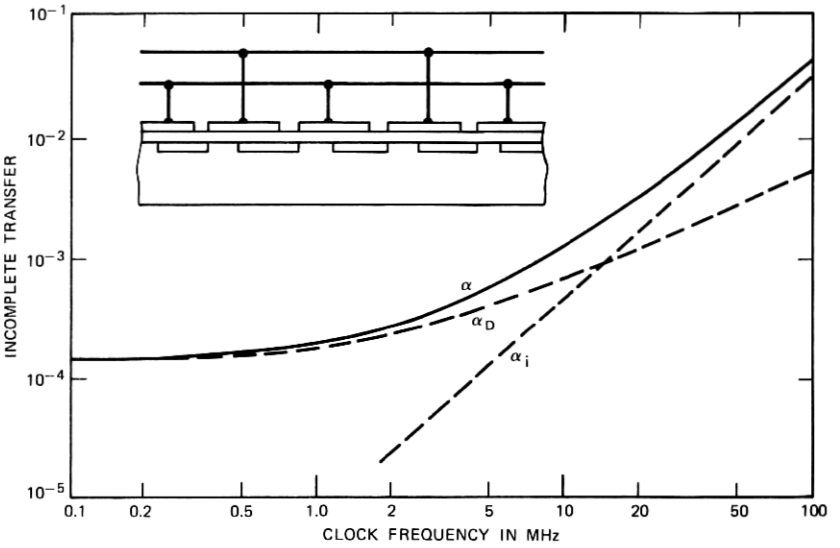

Fig. 7—Contributions to α (incomplete transfer) in the simple bucket-brigade shift register shown in the insert.

have usually assumed a simple square-law IGFET current-voltage characteristic and have ignored the fact that the carriers must be injected into the channel from the diffused regions. Recently[26] it has been pointed out that this injection requirement leads to a charge left behind which is logarithmic with time and an incomplete transfer parameter which tends to a constant value at low clock frequencies. Using the assumptions listed in Table I and assuming in addition that the drain capacitance C_D is equal to C_p, Fig. 7 shows the calculated behavior of the two contributions to α, α_i and α_D, as a function of clock frequency. The tendency for α to saturate at low frequencies is apparent in addition to the previously derived linear behavior of α_D and quadratic behavior of α_i with clock frequency at the high frequencies.

The other components of α, storage capacitance modulation and interface-state capacitance modulation, have not been shown in Fig. 7 because their values depend on the ratio of the channel capacitance to the storage capacitance. Both should be relatively small compared to the sum of α_i and α_D at all frequencies, if C_G is much smaller than C_p; so that qualitatively the bucket-brigade shift register should be well approximated by considering only α_i and α_D. However, if C_G and C_p

are of the same order as will often be the case for small-area devices, the interface-state capacitance modulation will add a frequency-independent term $\alpha_{C,SS}$ of value equal to approximately 8×10^{-4} (C_G/C_p). In that case, the interface-state term may dominate α at low frequencies.

4.2 *The Three-Phase CCD*

As originally proposed,[1] the charge-coupled device was driven by a three-phase clocking scheme as shown in the insert in Fig. 8. If it is assumed that the transfer time from one capacitor plate to the adjacent capacitor plate is one-third of a clock period, then the incomplete transfer parameter for the CCD under the restrictions of Table I is calculated to vary with clock frequency as shown in Fig. 8. In comparison to the simple bucket brigade, the three-phase CCD has a similar clock frequency behavior at high frequencies and a similar upper limit for operation. However, at lower frequencies the two modulation terms α_C and $\alpha_{C,SS}$ become dominant.[29,30] At very low frequencies, α tends to a relatively frequency-independent value due to the interface-state capacitance modulation term. Over most of the range of clock frequencies, the feedback or drain conductance term,

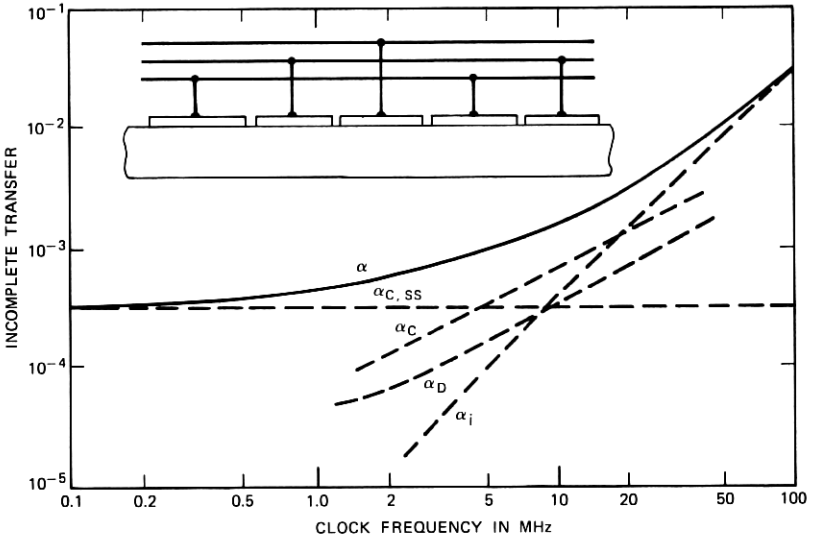

Fig. 8—Contributions to α (incomplete transfer) in the standard three-phase CCD shown in the insert.

of such importance for the bucket brigade, is nearly negligible for the three-phase CCD.

In Fig. 8 the various modulation terms have been calculated assuming that the channel-length modulation can be computed using eq. (69). Care should be used in comparing the modulation terms in Fig. 8 with those in Fig. 7. Owing to the uncertainty in the estimated modulation of the length of the channel or storage region, the magnitudes of the modulation terms should be considered to be approximate. Since α_D, α_C, and $\alpha_{C,SS}$ are each directly proportional to the length modulation, primary emphasis can be placed on their relative magnitudes and on the clock-frequency dependence of the various terms.

4.3 *The Two-Phase CCD*

Since the basic charge-coupled device has no inherent directionality like that of the bucket brigade, two-phase operation can only be achieved if some asymmetry is introduced into the CCD cell. One way to do this is to make each CCD capacitor plate consist of two regions, a transfer or barrier region which prevents carriers from moving in the wrong direction and a storage region. Ion-implanted barriers[7] and two oxide thicknesses[8,9] are two schemes which have been proposed, but two-phase operation can also be achieved by fabricating a four-phase CCD and placing a dc bias between alternate clock lines. Figure 9 illustrates these approaches to two-phase operation.

It is immediately evident from Fig. 9 that a two-phase CCD operates using a two-step transfer process. Hence, as shown in Appendix A, the operational improvement over a three-phase CCD comes primarily from making C_B small compared to C_D and by reducing the channel-length modulation. Given that the barrier length is identical to the storage capacitor length as assumed in this work, this means that best performance should be achieved either with the stepped-oxide device in Fig. 9, since the thicker oxide over the barrier region results in a smaller C_B, or with the ion-implanted device since dL_c/dV_D is reduced. In calculating the incomplete transfer for the stepped-oxide device, we will assume that the geometrical capacitance associated with the barrier and the transconductance are both one-half the values in the storage region.

Figure 10 shows the calculated incomplete transfer results for the stepped-oxide, two-phase CCD. Comparing these results to those for the three-phase CCD shown in Fig. 8, it is seen that the intrinsic transfer rate term, thus the high-frequency limitation, is about the same for both. The storage-capacitance modulation and drain con-

ductance terms are both reduced because of the small value of C_B, but the interface-state capacitance modulation term is approximately the same. Hence, operationally, some improvement is gained by using a two-phase CCD rather than a three-phase CCD.

A word of caution concerning the results for α shown in Fig. 10 is in order at this point. Some recent measurements[31] indicate that at

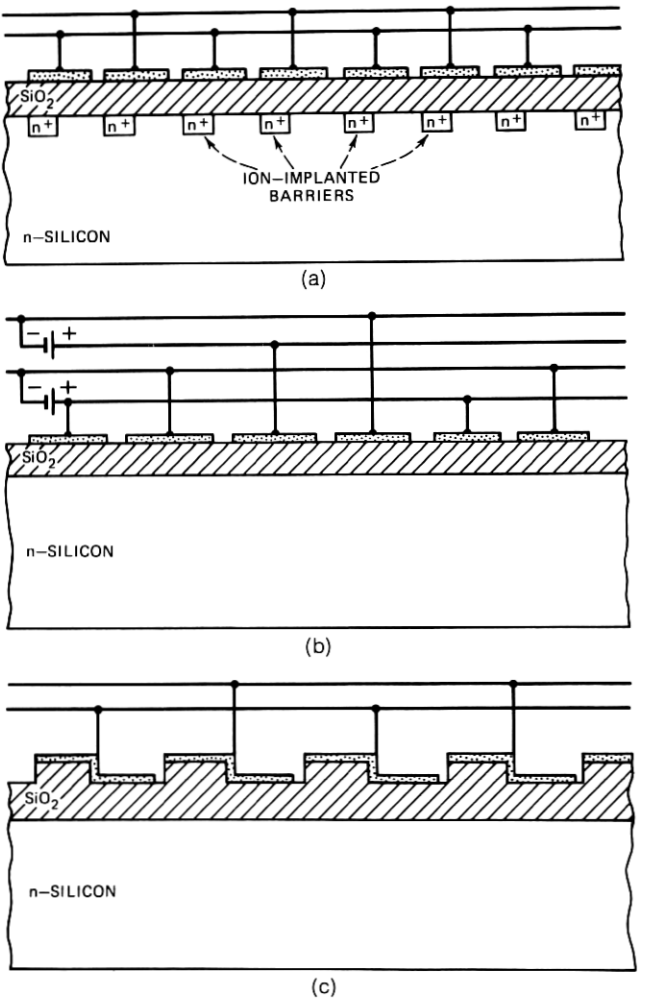

Fig. 9—Several examples of two-phase CCD device structures: (a) Ion-implanted barrier. (b) Standard four-phase run two phase. (c) Stepped-oxide.

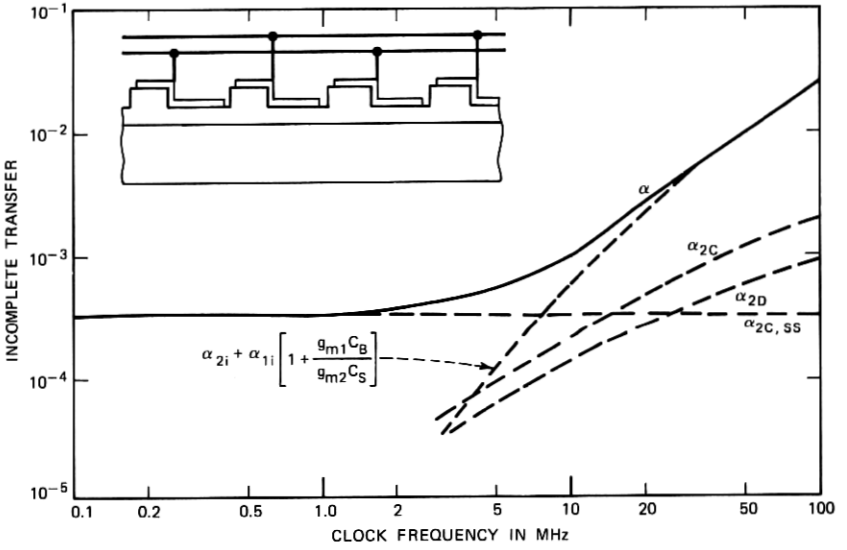

Fig. 10—Contributions to α (incomplete transfer) for the stepped-oxide, two-phase CCD.

low frequencies, α may be *in*dependent of interface-state density. However, as shown in Fig. 10, it is at low frequencies that the interface-state contribution to α is dominant, and this contribution is proportional to the density of interface states. The result shown, about $3 \cdot 10^{-4}$, is for a density of $1 \cdot 10^{10}$ states/cm^2. For $2 \cdot 10^{10}$ states 1 cm^2, one predicts $\alpha \approx 6 \cdot 10^{-4}$, which is reasonably close to the $4 \cdot 10^{-4}$ observed at this density.[32] Tentative results for other devices[31] have yielded similar low-frequency α's for interface-state densities up to $2 \cdot 10^{11}$ states/cm^2. If true, a reexamination of the contribution of interface states would be in order. However, before this is attempted, it is essential to ascertain the interface-state density not at midgap but at V_{SS} (see Appendix B) for the devices whose α's are being measured. Lateral inhomogeneities[33] may also be contributing to incomplete transfer.

4.4 *The Conductively Connected Charge-Coupled Device (C4D)*

The C4D[34] is illustrated in Fig. 11. Diffused p-regions connect the depletion region under the capacitor plates as compared to the usual CCD arrangement of closely spaced capacitor plates. An ion-implanted n^+ barrier is used to provide the directionality so that two-phase operation is achieved. From Fig. 11, it can be seen that transfer occurs

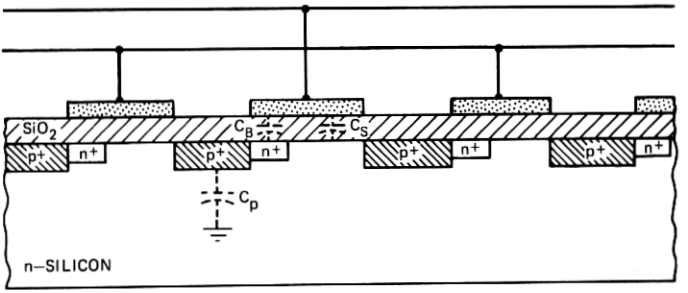

Fig. 11—Structure of the conductively connected, charge-coupled device (C4D).

by a two-step process. The charge is stored under that portion of the capacitor plate which sees the n-silicon substrate (labeled C_S in Fig. 11), and the first step of the transfer, a CCD transfer process, is from this depletion region to the adjacent diffused p-region. The second step of the transfer is from the p-region over the n^+ barrier to the next inversion region, a bucket-brigade transfer process.

In practice the p-regions will have finite capacitance to the substrate as shown dotted in Fig. 11. This has two effects. First, the p-region capacitance is in parallel with the adjacent drain capacitance C_S during transfer and charge must transfer back and forth from the p-region to C_S during clocking. Even if no charge is transferred over the barrier, a charge corresponding to the p-island capacitance multiplied by the voltage change across C_S will flow to C_S, thus assuring that the interface states in the storage region become occupied during each cycle regardless of whether charge has been transferred or not. This has been referred to as an automatic "fat zero."[7,34] However, the fat zero influences only the first step of the two-step process, and, as previously discussed (see also Appendix A), it is primarily the second step which contributes to the incomplete transfer.

The second effect of the p-region capacitance is that it adds to the intermediate capacitor C_B. Since for best operating performance we wish to minimize C_B, it seems that best results will be achieved by making the p-island capacitance as small as possible. In fact, in the limit of negligible p-island capacitance with respect to barrier capacitance, the C4D will have the same performance as a two-phase ion-implanted CCD with zero electrode spacing (see Fig. 9), and this will represent its optimum performance capabilities. However, it is the p-island capacitance when the p-region is at its most positive voltage with respect to the substrate that is of importance, and this corre-

sponds to the largest value of its capacitance. In most cases this will not be negligible compared to the drain capacitance C_S. If we consider the other extreme case, when p-island capacitance is large compared to C_S, then the C4D will perform like a simple bucket brigade but with the modulation terms multiplied by the ratio of p-island capacitance to depletion region capacitance plus p-island capacitance. Also, interface-state effects are similar to those in the ion-implanted two-phase CCD. Hence, C4D operating characteristics will lie between those of the simple bucket brigade and those of the ion-implanted two-phase CCD.

4.5 *The Stepped-Oxide and Tetrode Bucket Brigade*

The tetrode bucket brigade, first proposed by Sangster,[2,3] is shown in Fig. 12a. It was proposed[5] in order to reduce the drain conductance or

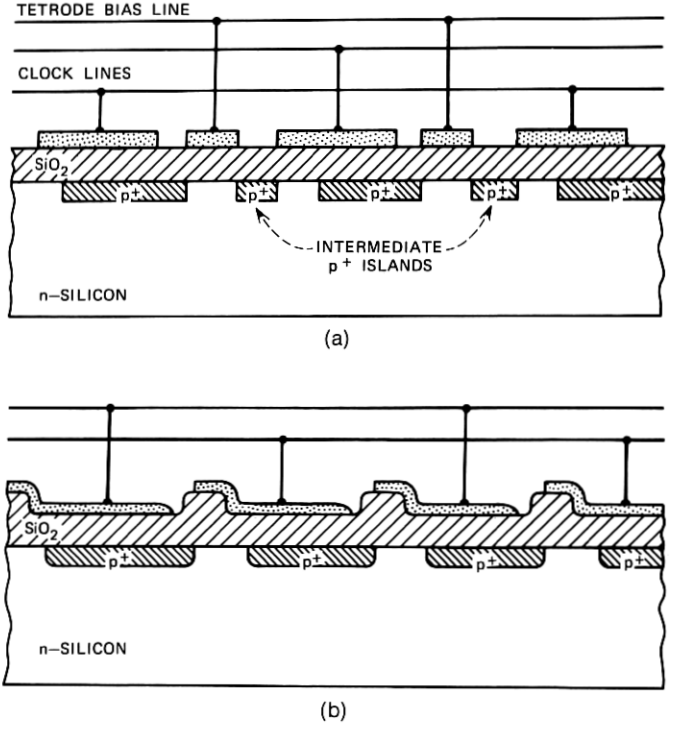

Fig. 12—(a) Structure of the tetrode bucket-brigade device. (b) Structure of the stepped-oxide bucket-brigade device.

feedback contribution to incomplete transfer, the effect known to be the dominant performance-limiting effect for bucket brigade at low frequencies. Sangster[5] pointed out that because of the finite capacitance between the intermediate p-diffusion and the substrate, the improvement in performance was not as great as was hoped, but the drain conductance term α_D was reduced by the ratio of the intermediate p-region capacitance to the storage capacitance.

Recently,[6] one of the authors (CNB) has suggested a similar scheme to reduce α_D referred to as the stepped-oxide bucket brigade and illustrated in Fig. 12b. The gate of each IGFET is separated into two regions, the region nearer the source having a higher threshold than that near the drain. In this way the charge transfer process becomes a two-step process like that of the tetrode bucket brigade, but the intermediate capacitance C_B is made up only of the effective gate capacitance associated with the low-threshold region near the drain. In this way, the first step of the charge transfer is by a "bucket-brigade" transfer process, and the second step is by a "CCD" process for the stepped-oxide bucket brigade but by another "bucket-brigade" process for the tetrode bucket brigade.

Like the other charge transfer devices treated here, the upper frequency limit for both the tetrode bucket brigade and the stepped-oxide bucket brigade will be limited by an intrinsic transfer rate term dependent on the channel lengths. Given the 10-micron assumption for all critical lengths, these two bucket-brigade registers will have the same upper frequency limit as the other CTD's. At lower frequencies, the incomplete transfer parameter should become very small depending on the ratio of C_B to C_D, and experimentally this has been found to be the case with measured values of α below 10^{-4}.[5]

V. DISCUSSION AND CONCLUSIONS

In the preceding section we discussed the coefficient of incomplete transfer, α, for CTD's in which the transfer of charge could be characterized as a single-step process or as a two-step process, and in which each step is either a "CCD" process or a "bucket-brigade" process. All devices were found to have approximately the same high-frequency limitation dominated by the intrinsic transfer rate contribution to α under the assumption that they were all of the same geometrical size. However, the middle- and low-frequency performance of the single-step devices can be improved upon by using the more complicated two-step devices. One finds in two-step devices that the source is effectively isolated from the sink so that the primary contribution to

α comes from the modulation contributions associated with the second transfer. If now the intermediate capacitance is made much less than the storage capacitance, the modulation terms are reduced by approximately the ratio of the intermediate capacitance to the storage capacitance. If this is achieved by making the storage capacitance large and keeping the intermediate capacitance fixed, better low-frequency performance will be accompanied by a lower high-frequency limit.

It was also found that the bucket-brigade transfer process leads to a frequency-independent contribution to α at low frequencies. This results from the requirement that charge must be injected from the diffused region into the channel of the IGFET. Conservation of current leads to a relation between the voltages of both sides of this barrier: V_p in the diffused region and V_A at the beginning of the channel. For long transfer periods (low clock frequency) V_A varies at $1/t$ and V_p varies as log V_A: hence, V_p varies as log t, or essentially independent of time and of clock frequency.

The analytic expressions we have obtained for the contributions to the coefficient of incomplete charge transfer α of both single-step and two-step transfer devices are quite general and provide a good qualitative and a reasonable quantitative prediction of the dependence of α upon the various device parameters. If more accurate quantitative results are desired, particular attention must be paid to channel-length modulation. This, however, is a static problem and should prove to be simpler than the dynamic problem of calculating α directly from a solution of $Q(t)$.

VI. ACKNOWLEDGMENTS

We wish to thank J. R. Brews, G. E. Smith, and R. J. Strain for helpful discussions.

APPENDIX A

Derivation of the Incomplete Transfer Parameter α

A.1 *Single-Step Process*

In a recent paper the authors[11] have shown that the incomplete transfer parameter α for a charge transfer device (ignoring for the moment the contribution of interface states) is made up of three terms

$$\alpha = \alpha_i + \alpha_D + \alpha_C$$

where α_i is the intrinsic transfer-rate contribution, α_D is the drain-conductance contribution, and α_C is the storage-capacitance modulation

term. For a single-step process, the intrinsic term is given by

$$\alpha_i = \exp\left[-\int_0^\tau \frac{g_m}{C_S}\,dt\right] \tag{16}$$

where g_m is the transconductance of the transfer mechanism joining C_S to C_D (see Fig. 6) and τ is the transfer time. As a first approximation for square-wave clocks, $g_m \approx dI/dV_S$ and $dt \approx (C_S/I)dV_S$, so eq. (16) becomes

$$\alpha_i \approx \frac{I}{I_o} \tag{17}$$

where I_o is the transfer current at the beginning of transfer.

The drain conductance term, α_D, is given by

$$\alpha_D = \frac{g_r C_S}{g_m C_D} \tag{18}$$

where g_r is the reverse transconductance of the transfer mechanism, and both g_r and g_m are evaluated at time τ. Since in eq. (4) it is only the constant β which can be dependent on drain voltage V_D, we can write

$$g_r = -\frac{\partial I}{\partial V_D} = -\frac{I}{\beta}\left(\frac{d\beta}{dV_D}\right) = I\left(\frac{1}{L_c}\frac{dL_c}{dV_D}\right) \tag{19}$$

where we have taken $\beta = Z\mu C_i/L_c$ [see eq. (4)].

According to the assumptions made here and listed in Table I, β can only vary through channel-length modulation. However, the exact form of this variation has not been theoretically established. The most common assumption is that the channel length L_G is shortened by an amount equal to the one-dimensional depletion-layer width L_D associated with the voltage on the IGFET drain diffusion. Even for an IGFET with source shorted to the substrate, this assumption is somewhat crude, and for the bucket brigade with the source p-islands reverse biased with respect to the substrate, it is expected to be even less accurate. For the CCD, an additional problem arises in that the transition fringing-field region under high lateral electric field connecting one charge storage region to the adjacent one extends under both capacitor plates so that less "channel-length modulation" will occur than for an equivalent bucket brigade.[19,20] This effect is particularly important when an ion-implanted barrier is used because, owing to the higher doping density in the barrier, channel length associated

with the barrier will change much less than the length of the adjacent storage well. An accurate treatment of this problem of calculating dL_C/dV_D is beyond the scope of this paper. However, in Appendix C we briefly outline an approximation which can be used.

Returning to eq. (19), and inserting I from Eq. (4), we have

$$g_r = \frac{\beta}{2} V_A \left(V_A + \frac{2kT}{q} \right) \frac{1}{L_c} \frac{dL_c}{dV_D}. \tag{20}$$

Similarly, from eq. (4) we can derive g_m to obtain

$$g_m = \frac{\partial I}{\partial V_S} = \beta \left(V_A + \frac{kT}{q} \right) \frac{\partial V_A}{\partial V_S}. \tag{21}$$

For a "bucket-brigade" transfer process, $\partial V_A/\partial V_S$ is $[1+(kT/qV_A)]^{-1}$ from eq. (11). It is also easy to show using eq. (11) that the effective C_S for a bucket brigade-transfer process is (see Fig. 4)

$$C_S = C_p + \frac{V_A}{V_A + \frac{kT}{q}} C_G. \tag{22}$$

Hence α_D is given by

$$\alpha_D = \frac{C_p \left(V_A + \frac{2kT}{q} \right) + C_G V_A \left[\frac{V_A + \frac{2kT}{q}}{V_A + \frac{kT}{q}} \right]}{2C_D} \cdot \frac{1}{L_c} \frac{dL_c}{dV_D}. \tag{23}$$

Given a calculation of V_A as a function of transfer time, the drain conductance contribution can be determined from eq. (23) by using the appropriate values of C_p and C_G. For a CCD transfer process, C_p is zero, and in the limit as V_A tends to zero (i.e., at long transfer times or low clock-frequency operation) α_D tends to zero linearly with V_A. For a bucket-brigade transfer process, C_p is finite and α_D will tend to a constant value in the limit of small V_A.

The capacitance modulation term, α_C, has been shown[11] to be

$$\alpha_C = Q_S \left(\frac{1}{C_S} \frac{dC_S}{dQ_o} \right) \tag{24}$$

where Q_S is the transferable charge remaining on C_S at time τ. Usually, however, C_S is made up of several contributions only one of which is

modulated by Q_o. In this case if the particular capacitance is C_{Si} with a transferable charge Q_{Si} remaining on it,

$$\alpha_C = \frac{Q_{Si}}{C_D}\left(\frac{1}{C_{Si}}\frac{dC_{Si}}{dV_D}\right). \tag{25}$$

In all the CTD's of interest here it is the gate capacitance C_G which is modulated due to the channel-length modulation effect. Since this capacitance is linear in channel length, we obtain

$$\alpha_C = \frac{C_G V_A}{C_D}\left(\frac{1}{L_C}\frac{dL_C}{dV_D}\right). \tag{26}$$

The one extra contribution to incomplete transfer which will be considered here is that due to interface states. It has been found[11] that such states lead to two terms, one due to interface-state capacitance modulation and the other due to the modulation of the dynamics of trapping and detrapping during transfer. For square-wave clocks and a large circulating charge or fat zero, it has been shown that the latter contribution will be small.[31] Thus we will consider here only the capacitance modulation term $\alpha_{C,SS}$. If Q_{SS} is the net charge trapped in interface states after transfer, then

$$\alpha_{C,SS} = Q_{SS}\left(\frac{1}{C_{SS}}\frac{dC_{SS}}{dQ_o}\right) \tag{27}$$

where C_{SS} is the interface-state capacitance. If we assume that this capacitance is also modulated by the channel-length modulation, then:

$$\alpha_{C,SS} = \frac{Q_{SS}}{C_D}\left(\frac{1}{L_e}\frac{dL_e}{dV_D}\right). \tag{28}$$

We have used this expression in a previous article.[11] On the other hand, Tompsett[29] has reported that variations in edge effects and in capture during transfer are important. These are included in (27); however, whereas the channel-width modulation leading to (28) can be greatly reduced by using two-step rather than single-step transfer processes (see below), edge effects, which depend on the *initial* amount of charge Q_o present, are nearly unaffected by merely increasing the number of transfer steps. Reduction of edge effects can come only by making the effective size of the well less dependent on Q_o, e.g., by ion-implanted barriers[7] or diffused regions, or by keeping the carriers away from the surface, e.g., by storing charge in diffused islands or buried

channels. Changes in capture during transfer can be greatly reduced by using zero-gap technology.[8,9]

It should be noted that apart from the intrinsic contribution α_i, the three contributions given above, α_D, α_C, and $\alpha_{C,SS}$, are all proportional to $(1/L_C)\cdot(dL_C/dV_D)$. Hence, even though our estimates of dL_C/dV_D tend to be crude (see Appendix C), the relative size of these contributions can be ascertained more precisely.

A.2 *Two-Step Process*

In a two-step transfer process as shown in Fig. 6b, the charge first transfers from C_S to an intermediate capacitor referred to as C_B, then to the drain capacitor C_D during a single transfer time τ. In this case transferable charge is left behind on both C_B and C_S, and the derivation of α becomes somewhat more complex. The main advantage of using a two-step process is that all of the contributions to α due to channel-length modulation can be reduced since modulation of C_S by the voltage V_D on C_D is a second-order effect (i.e., variations in V_D modulate slightly the value of V_B, which in turn modulates to a much lesser degree the value of V_S). For this reason, we will ignore here the channel-length modulation effects for the first step of the two-step process.

Referring to Fig. 6b for a definition of terms, the transferable charge on the first storage capacitor at time t is

$$Q_S = \int_{V_{S,0}}^{V_S} C_S dV + \int_{V_{SS1,0}}^{V_{SS1}} C_{SS1} dV. \tag{29}$$

In this expression we shall be able to ignore the effects of channel-length modulation, these being of second order in a two-step process. However, channel-length modulation effects are important for the charge Q_B on the intermediate capacitance C_B. We write

$$Q_B = \int_{V_{B0}}^{V_B} C_B dV + \int_{V_{SS2,0}}^{V_{SS2}} C_{SS2} dV \tag{30}$$

where C_{SS2} is only the interface-state term subject to first-order channel-length modulation. We can solve for the effective α for the first step of the process α_1 (see Appendix B)

$$\alpha_1 = \frac{dQ_S}{dQ_o} = \alpha_{1i} + \alpha_{1C,SS} \tag{31}$$

where

$$\alpha_{1i} = \exp\left[-\int_0^\tau \frac{g_{m1}}{C_S} dt'\right]$$

TABLE III—MAJOR CONTRIBUTIONS TO INCOMPLETE CHARGE TRANSFER IN TERMS OF SMALL-SIGNAL DEVICE PARAMETERS $\alpha = \alpha_i + \alpha_D + \alpha_C + \alpha_{C,SS}$

Type	Single-Step	Two-Step
Intrinsic, α_i	$\exp\left(-\int_0^\tau (g_m/C_S)dt\right)$	$\exp\left(-\int_0 (g_{m2}/C_B)dt\right) + \exp\left(-\int_0^\tau (g_{m1}/C_S)dt\right) \cdot (1 + g_{m1}C_B/g_{m2}C_S)$
Drain Conductance, α_D (Feedback)	g_rC_S/g_mC_D	$g_{r2}C_B/g_{m2}C_D$
Capacitance Modulation, α_C	$Q_S\left(\frac{1}{C_S}\frac{dC_S}{dQ_o}\right)$	$Q_B\left(\frac{1}{C_B}\frac{dC_B}{dQ_o}\right)$
Interface State Capacitance Modulation, $\alpha_{C,SS}$	$Q_{SS}\left(\frac{1}{C_{SS}}\frac{dC_{SS}}{dQ_o}\right)$	$Q_{SS1}\left(\frac{1}{C_{SS1}}\frac{dC_{SS1}}{dQ_o}\right) + Q_{SS2}\left(\frac{1}{C_{SS2}}\frac{dC_{SS2}}{dQ_o}\right)$

TABLE IV—MAJOR CONTRIBUTIONS TO INCOMPLETE CHARGE TRANSFER IN TERMS OF APPROXIMATE EVALUATION OF DEVICE PARAMETERS $\alpha = \alpha_i + \alpha_D + \alpha_C + \alpha_{C,SS}$

Type	Single-Step	Two-Step
Intrinsic, α_i	I/I_0	$\frac{I_1}{I_{10}}\left(1+\frac{g_{m1}C_B}{g_{m2}C_S}\right)+I_2/I_{20}$
Drain Conductance, α_D (Feedback)	$\frac{C_p\left(V_A+\frac{2kT}{q}\right)+C_GV_A\left[\frac{V_A+\frac{2kT}{q}}{V_A+\frac{kT}{q}}\right]}{2C_D}\frac{1}{L_C}\frac{dL_C}{dV_D}$	α_D for second transfer only
Capacitance Modulation, α_C	$\frac{C_GV_A}{C_D}\left(\frac{1}{L_C}\frac{dL_C}{dV_D}\right)$	$\frac{C_BV_A}{C_D}\left(\frac{1}{L_{C2}}\frac{dL_{C2}}{dV_D}\right)$
Interface State Capacitance Modulation, $\alpha_{C,SS}$	$\frac{Q_{SS}}{C_D}\left(\frac{1}{L_C}\frac{dL_C}{dV_D}\right)$	$\frac{Q_{SS2}}{C_D}\left(\frac{1}{L_{C2}}\frac{dL_{C2}}{dV_D}\right)+\alpha_{1C,SS}$

and $\alpha_{1C,SS}$ is given in (65). For the second step, however, the net current into C_B is the difference between I_1 and I_2 so that the equation to be solved is, using eq. (31),

$$\frac{d\alpha_2}{dt} = \frac{g_{m1}}{C_S} \exp\left[-\int_0^t \frac{g_{m1}}{C_S}\,dt\right] - g_{m2}\frac{dV_B}{dQ_o} + g_{r2}\frac{dV_D}{dQ_o} \tag{32}$$

where

$$\alpha_2 = \frac{dQ_B}{dQ_o}. \tag{33}$$

(Details for arriving at an expression similar to (32) are given in Appendix B.) From eq. (30),

$$\frac{dV_B}{dQ_o} = \frac{\alpha_2}{C_B} - \frac{1}{C_B}\int_{V_{B0}}^{V_B}\frac{dC_B}{dQ_o}\,dV - \frac{1}{C_B}\int_{V_{SS2,0}}^{V_{SS2}}\frac{dC_{SS2}}{dQ_o}\,dV \tag{34}$$

and

$$\frac{dV_D}{dQ_o} = \frac{1}{C_D}. \tag{35}$$

Solving for α_2, in a similar manner to that used in Ref. 10,

$$\alpha_2 = \alpha_{2i} + \alpha_{2D} + \alpha_{2C} + \alpha_{2C,SS} + \alpha'_{1i} \tag{36}$$

where

$$\alpha_{2i} = \exp\left[-\int_0^\tau \frac{g_{m2}}{C_B}\,dt\right] \approx \frac{I_2}{I_{20}} \tag{37}$$

is the intrinsic transfer rate term,

$$\alpha_{2D} \approx \frac{g_{r2}}{g_{m2}}\frac{C_B}{C_D} \tag{38}$$

is the drain conductance or feedback term, which can be evaluated using eq. (23),

$$\alpha_{2C} \approx Q_B\left[\frac{1}{C_B}\frac{dC_B}{dQ_o}\right] \approx \frac{Q_B}{C_D}\left(\frac{1}{L_{G2}}\frac{dL_{G2}}{dV_D}\right) \tag{39}$$

is the capacitance modulation term,

$$\alpha_{2C,SS} \approx Q_{SS2}\left[\frac{1}{C_{SS2}}\frac{dC_{SS2}}{dQ_o}\right] \approx \frac{Q_{SS2}}{C_D}\left(\frac{1}{L_{G2}}\frac{dL_{G2}}{dV_D}\right) \tag{40}$$

is the interface-state capacitance modulation term, and

$$\alpha'_{1i} \approx \frac{g_{m1}}{g_{m2}}\frac{C_B}{C_S}\alpha_{1i} \tag{41}$$

reflects the fact that charge transfers from C_S to C_B in addition to the transfer of charge from C_B to C_D. Realizing that the total incomplete transfer parameter is $\alpha_1 + \alpha_2$, the final result for a two-step transfer process can be written in terms of the parameters of the individual transfer steps as

$$\alpha = \alpha_{2i} + \alpha_{2D} + \alpha_{2C} + \alpha_{2C,SS} + \alpha_{1C,SS} + \alpha_{1i}\left(1 + \frac{g_{m1}}{g_{m2}}\frac{C_B}{C_S}\right). \quad (42)$$

Referring to eqs. (38), through (41), it is apparent that a significant improvement in α can be obtained in a two-step process by making C_B much smaller than C_D, provided the edge-effect contribution[29] to $\alpha_{1C,SS}$ can be reduced.

The results of this appendix are summarized in Tables III and IV.

APPENDIX B

General Derivation of the Incomplete Transfer Parameter α

In a previous paper[11] we outlined the details of the derivation of our general expression for α for the single-step process. In this appendix a similar derivation of α is given for the two-step process. The general derivation for an m-step process should then be straightforward to devise if needed.

Referring to Fig. 6b, as the size of the initial, transferable charge Q_o is varied, both $Q_S(t)$ and $Q_B(t)$ will also vary. If $Q_D(t) \equiv Q_o - Q_S(t) - Q_B(t)$ is the transferable charge on the drain, then α for transfer process may be defined as

$$1 - \alpha \equiv \frac{dQ_D}{dQ_o}. \quad (43)$$

It follows that

$$\alpha = \alpha_1 + \alpha_2 \quad (44)$$

where

$$\alpha_1 = \frac{dQ_S}{dQ_o} \quad (45)$$

referring to I_1, the current of the first transfer step, and where

$$\alpha_2 = \frac{dQ_B}{dQ_o} \quad (46)$$

which refers to both I_1 and I_2, I_2 being the current of the second transfer step. As in the case of single-step transfer, we shall derive a differential equation which can then be solved for α.

As before,[11] we first assume that we can write the currents governing the transfer of charge in the following form

$$I_1 = I_1(V_S, V_B, V_C, V_{SS1}) \tag{47}$$

and

$$I_2 = I_2(V_B, V_D, V_C, V_{SS2}) \tag{48}$$

where the additional voltages V_{SSi} $(i = 1,2)$ are just the voltages induced by the trapped charges Q_{SSi} on the effective capacitances C_{SSi} of the traps (V_C is the clock voltage). Q_S, Q_B, and Q_D are related to C_S, C_B, C_{SSi} $(i = 1,2)$, and C_D as follows

$$Q_S = \int_{V_{S,0}}^{V_S} C_S dV + \int_{V_{SS1,0}}^{V_{SS1}} C_{SS1} dV \tag{49}$$

$$Q_B = \int_{V_{B,0}}^{V_B} C_B dV + \int_{V_{SS2,0}}^{V_{SS2}} C_{SS2} dV \tag{50}$$

$$Q_D = \int_{V_{D,0}}^{V_D} C_D dV = Q_o - Q_S - Q_B . \tag{51}$$

From (49) to (51) and using (43) to (46) one can obtain the following relationships:

$$\frac{dV_S}{dQ_o} = \frac{\alpha_1}{C_S} - \frac{1}{C_S}\int_{V_{S,0}}^{V_S} \frac{dC_S}{dQ_o} dV - \frac{\alpha_{SS1}}{C_S} - \frac{1}{C_S}\int_{V_{SS1,0}}^{V_{SS1}} \frac{dC_{SS1}}{dQ_o} dV \tag{52}$$

$$\frac{dV_B}{dQ_o} = \frac{\alpha_2}{C_B} - \frac{1}{C_B}\int_{V_{B,0}}^{V_B} \frac{dC_B}{dQ_o} dV - \frac{\alpha_{SS2}}{C_B} - \frac{1}{C_B}\int_{V_{SS2,0}}^{V_{SS2}} \frac{dC_{SS2}}{dQ_o} dV \tag{53}$$

$$\frac{dV_D}{dQ_o} = \frac{1 - \alpha_1 - \alpha_2}{C_D} - \frac{1}{C_D}\int_{V_{D,0}}^{V_D} \frac{dC_D}{dQ_o} dV \approx \frac{1}{C_D} \tag{54}$$

where we have made use of the following definition:

$$\alpha_{SSi} \equiv C_{SSi} \frac{dV_{SSi}}{dQ_o}, \qquad (i = 1,2). \tag{55}$$

A differential equation for $\alpha = \alpha_1 + \alpha_2$ can now be derived at once. Since $dQ_S/dt = -I_1$ and $dQ_B/dt = I_1 - I_2$ (conservation of charge), it follows that

$$\frac{d\alpha}{dt} = -\frac{dI_2}{dQ_o} = -g_{m2}\frac{dV_B}{dQ_o} + g_{r2}\frac{dV_D}{dQ_o} - \frac{\partial I_2}{\partial V_{SS2}}\frac{dV_{SS2}}{dQ_o} \tag{56}$$

where as before $g_{m2} \equiv \partial I_2/\partial V_B$ and $g_{r2} \equiv -\partial I_2/\partial V_D$. Inserting (53)

to (55) into (56), replacing α_2 by $\alpha - \alpha_1$, and solving for α, one finds that

$$\alpha(t) = \int_0^t \alpha_1(t')E(t,t')dt' + \int_0^t \left(\int_{V_{B,0}}^{V_B} \frac{dC_B}{dQ_o} dV \right) E(t,t')dt' + \int_0^t (g_{r2}C_B/g_{m2}C_D)E(t,t')dt' + \int_0^t \left(\alpha_{SS2} \left(1 - \frac{\partial I_2}{\partial V_{SS2}} \frac{C_B}{C_{SS2}} \frac{1}{g_{m2}} \right) + \int_{V_{SS2,0}}^{V_{SS2}} \frac{dC_{SS2}}{dQ_o} dV \right) E(t,t')dt' \quad (57)$$

where $E(t,t')$, the suppression factor, is defined by

$$E(t,t') \equiv \exp\left(-\int_{t'}^t dt''/\tau_2(t'') \right) \Big/ \tau_2(t') \quad (58)$$

and

$$1/\tau_2(t') \equiv g_{m2}(t')/C_B(t'). \quad (59)$$

The second, third, and fourth integrals in (57) can be evaluated at once assuming the factor multiplying $E(t,t')$ varies more slowly than $E(t,t')$. This yields

$$\alpha(t) \equiv \int_0^t \alpha_1(t')E(t,t')dt' + \int_{V_{B,0}}^{V_B} dC_B/dQ_o dV + g_{r2}C_B/g_{m2}C_D + \alpha_{SS2} \left(1 - \frac{\partial I_2}{\partial V_{SS2}} \frac{C_B}{C_{SS2}} \frac{1}{g_{m2}} \right) + \int_{V_{SS2,0}}^{V_{SS2}} \frac{dC_{SS2}}{dQ_o} dV. \quad (60)$$

These terms are discussed in the text, in Appendix A, and in a previous work.[11]

To evaluate the first term in (57) we must calculate $\alpha_1(t)$. To do this we derive and then solve a differential equation for $\alpha_1(t)$. Since $dQ_S/dt = -I_1$, it follows that

$$\frac{d\alpha_1}{dt} = -\frac{dI_1}{dQ_o} = -g_{m1}\frac{dV_S}{dQ_o} + g_{r1}\frac{dV_B}{dQ_o} - \frac{\partial I_1}{\partial V_{SS1}} \frac{dV_{SS1}}{dQ_o}. \quad (61)$$

Before inserting (52) and (53) into (61), we should note the relative magnitudes of the contributions to α_1. dV_B/dQ_o is bounded by α/C_B

[see (60)]. Hence the contribution to α_1 of the term $g_{r1}dV_B/dQ_o$ is of the order of $\alpha \cdot \alpha_1$, which is quite negligible. As explained in Appendix A, variations in C_S are second order in ΔQ_o and hence can be ignored in (52). In Ref. 9, we also pointed out that dC_{SS}/dQ_o was the dominant interface-state contribution to α, the term in α_{SS} being much smaller. Here dC_{SS1}/dQ_0 and dC_{SS2}/dQ_o are the corresponding dominant trapping terms by the same reasoning. Hence, the third term in (52) as well as the fourth term in (60) can be dropped. This reduces (61) to

$$\frac{d\alpha_1}{dt} = -\frac{g_{m1}}{C_S}\alpha_1 + \frac{g_{m1}}{C_S}\int_{V_{SS1,0}}^{V_{SS1}} \frac{dC_{SS1}}{dQ_o}\,dV \tag{62}$$

the solution of which is

$$\alpha_1(t) = \alpha_{1i}(t) + \alpha_{1C,SS}(t) \tag{63}$$

where

$$\alpha_{1i}(t) = \exp\left(-\int_0^t (g_{m1}/C_S)_{t''}dt''\right) \tag{64}$$

and

$$\alpha_{1C,SS}(t) = \int_0^t dt' \exp\left(-\int_{t'}^t (g_{m1}/C_S)_{t''}dt''\right) \cdot \left(\frac{g_{m1}}{C_S}\int_{V_{SS1,0}}^{V_{SS1}} \frac{dC_{SS1}}{dQ_o}\,dV\right)_{t'} \tag{65}$$

$$\approx \int_{V_{SS1,0}}^{V_{SS1}} \frac{dC_{SS1}}{dQ_o}\,dV \tag{66}$$

$$\approx Q_{SS1}\frac{1}{C_{SS1}}\frac{dC_{SS1}}{dQ_o}. \tag{67}$$

Inserting (63) for $\alpha_1(t)$ into (60) we obtain an explicit expression for $\alpha(t)$ as desired.

Our expression for $\alpha(t)$ can be simplified somewhat. If $\alpha_{1C,SS}$ (66) can be assumed to be slowly varying near turnoff, then we can use the fact that $\int E\,dt = 1$ [see (58) and (59)] to write

$$\alpha(t) = \int_0^t \alpha_{1i}(t)E(t,t')dt' + \int_{V_{B,0}}^{V_B} dC_B/dQ_o dV + g_{r2}C_B/g_{m2}C_D + \int_{V_{SS1,0}}^{V_{SS1}} dC_{SS1}/dQ_o dV + \int_{V_{SS2,0}}^{V_{SS2}} dC_{SS2}/dQ_o dV. \tag{68}$$

In (68), we have dropped terms proportional to α_{SS1} and α_{SS2} as discussed above.

To simplify the first term of (68) we must proceed more carefully. Using (64), we may write this intrinsic term as

$$\alpha_{1i}(t)\int_0^t dt' \exp\left(-\int_{t'}^t dt''(g_{m2}/C_B - g_{m1}/C_S)\right)\cdot(g_{m2}(t')/C_B(t')).$$

This expression can be handled in various ways. In Appendix A we have assumed that $g_{m2}/C_B \gg g_{m1}/C_S$ in which case one can multipy and divide the integrand by $(g_{m2}/C_B - g_{m1}/C_S)$, assume $(g_{m2}/C_p)\cdot(g_{m2}/C_B - g_{m1}/C_S)^{-1}$ is slowly varying, and integrate as before to obtain the intrinsic term of α

$$\alpha_{1i}\cdot(1 - g_{m1}C_B/g_{m2}C_S)^{-1} \approx \alpha_1(1 + g_{m1}C_B/g_{m2}C_S).$$

Alternatively, if $g_{m2}/C_B = a_2 f(t)$ and $g_{m1}/C_S = a_1 f(t)$, then the integral may be performed without approximation, and one finds

$$\alpha_{1i}\frac{a_2}{a_2 - a_1}\left\{1 - \exp\left[-\int_0^t (a_2 - a_1)f(t')dt'\right]\right\}.$$

Finally, in the extreme case that $g_{m2}/C_B = g_{m1}/C_S$ one has for this term

$$\alpha_{1i}\log_e(1/\alpha_{1i})$$

which varies typically from $5\alpha_1$ to $9\alpha_1$ for α_1 from 0.007 to 0.0001. Being the intrinsic term, it dominates in α only for relatively high clock frequencies.[11]

APPENDIX C

In this appendix we consider several approximations which can be used to determine dL_C/dV_D. One approach is to simply define an appropriate one-dimensional depletion layer width L_D assumed to vary as the square root of voltage V_D, and assume that the effective channel length, L_c is $L_G - L_D$. This approximation, valid only when the oxide thickness (times the ratio of the dielectric constant of the oxide to that of the semiconductor) is much less than the space-charge width, we shall use when a channel in the substrate material empties into a heavily doped diffused region, as is the case for the simple, tetrode, and stepped-oxide bucket brigade. Under these conditions we find using eq. (4)

$$\frac{1}{L_c}\frac{dL_c}{dV_D} = \frac{L_D}{2(L_G - L_D)}\frac{1}{|V_D|}. \tag{69}$$

If, on the other hand, one has charge transport over a barrier into an inverted region at the surface of the substrate material, the length modu-

lation will be reduced approximately by a factor of $(1 + N_B/N_S)^{-1}$, where N_B is the doping in the barrier region and N_S is the doping in the substrate. This may be applied to the use of the C4D and the ion-implanted-barrier two-phase CCD. Thus one finds

$$\frac{1}{L_c}\frac{dL_c}{dV_D} = \frac{L_D}{2(L_G - L_D)}\frac{1}{|V_D|}\frac{1}{1 + N_B/N_S} \tag{70}$$

where L_D refers to the substrate material. Estimating dL_c/dV_D by equating it to the modulation in the size of the depletion region should represent an upper limiting case. That is, the actual dL_c/dV_D should be less than the value predicted by (69) or (70), making our resulting prediction for α conservatively larger than the actual result.

For CCD structures in which charge transfers are directly between two inversion regions (e.g., as in the simple polyphase CCD and the stepped-oxide, two-phase CCD), the depletion-width approximation discussed above is clearly very unsatisfactory. We attempted to find a better estimate for dL_c/dV_D in such cases but were unsuccessful.

We hope that better approximations will be motivated by extensions of existing calculations.[19,20]

Note: We point out that dL_c/dV_D might be interpreted as the reciprocal of an electric field. The first field that comes to mind is the average (or peak) field at the silicon-silica interface between inversion regions. For the device dimensions used in examples in the text $dL_c/dV_D \approx (10^6\ \text{V/cm}^2)^{-1}$, whereas computer calculations[21] suggest that the surface electric field is on the order of 10^4 to 10^5 V/cm. This disparity seems to rule out such a simple interpretation.

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