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A DC-to-2.3-GHz Amplifier Using an "Embedding" Scheme

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A novel circuit technique is described for embedding a high-frequency amplifier in a low-frequency circuit to achieve a defined, flat gain from dc to the cutoff frequency of the hf amplifier. The technique provides this low-frequency gain without compromising the hf design optimization. An embodiment of this technique is described which has provided, experimentally, amplifier gain from dc to a half-power point of 2.3 GHz.

I. INTRODUCTION

This paper describes a novel circuit technique for providing broadband amplifier gain response from dc to extremely high frequencies. The technique provides this wide spectrum response without compromising either the hf response or the dc stability. This performance is obtained by "embedding" a parameter-optimized hf amplifier within a dc gain-defining circuit, and providing means for ensuring a smooth transition between the low-frequency to high-frequency operating modes. This technique avoids the compromise of hf performance which is frequently present in direct coupled amplifiers.[1,2]

Amplifiers with response to dc are frequently required in communication systems employing a baseband Pulse Code Modulation (PCM) type encoding scheme where the entropy of the information signal is unknown. Because of the simplicity afforded by binary PCM, its use has been adopted in many optical systems.[3,4] In such cases, the channel information rate is restricted mainly by the bandwidth of the electronic driving circuits. The economics of noncoherent optical systems again dictate the use of extremely broadband amplifiers and, if the system simplicity is not to suffer,[5] a gain response to dc is required. Such systems should benefit from an hf optimized amplifier providing gain to dc. A particular realization of the embedding technique is described in this paper which may find use in such systems. This realization

provides essentially flat gain response up to approximately 0.5 of the constituent device common base cutoff frequencies. The technique results in an amplifier voltage gain of 8 dB over the range dc to 2.3 GHz with a step response rise time of 200 ps. At frequencies below the pre-cutoff resonance, inband ripple is typically less than 1.5 dB.

II. THE EMBEDDING TECHNIQUE

Amplifier embedding is applicable to a number of circuit realizations but is best described in terms of the simple common emitter stage shown in Fig. 1. At dc, this stage exhibits a gain of

$$G_{dc} \cong \frac{R_{C1} + R_{C2}}{R_{E1} + R_{E2}},$$

and at high frequencies the gain is simply $G_{hf} = R_{C1}/R_{E1}$, so that, by making the equality

$$\frac{R_{C1} + R_{C2}}{R_{E1} + R_{E2}} = R_{C1}/R_{E2},$$

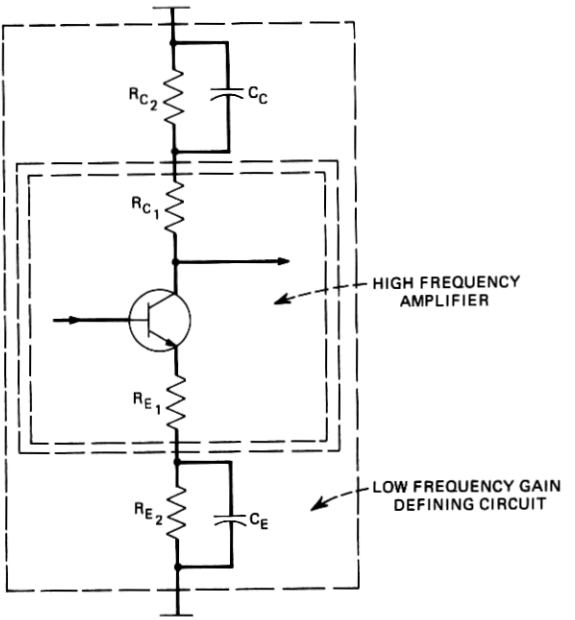

Fig. 1—Embedded common emitter stage.

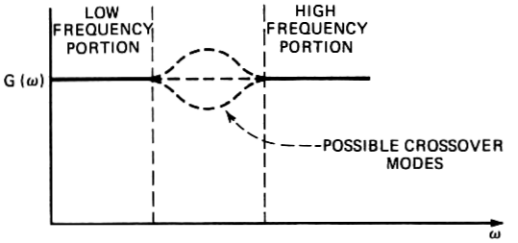

Fig. 2—Amplifier gain spectrum.

the two portions of the gain spectrum, shown in Fig. 2, will be equal. In addition to this requirement, a flat transitional crossover is required. This critical crossover point has always been the major difficulty in split-band additive amplifiers.[6] To analyze the requirements for a flat crossover, it is more meaningful to consider the practical circuit arrangement shown in Fig. 3. The circuit also incorporates emitter-follower buffering stages at the input and output. The additional

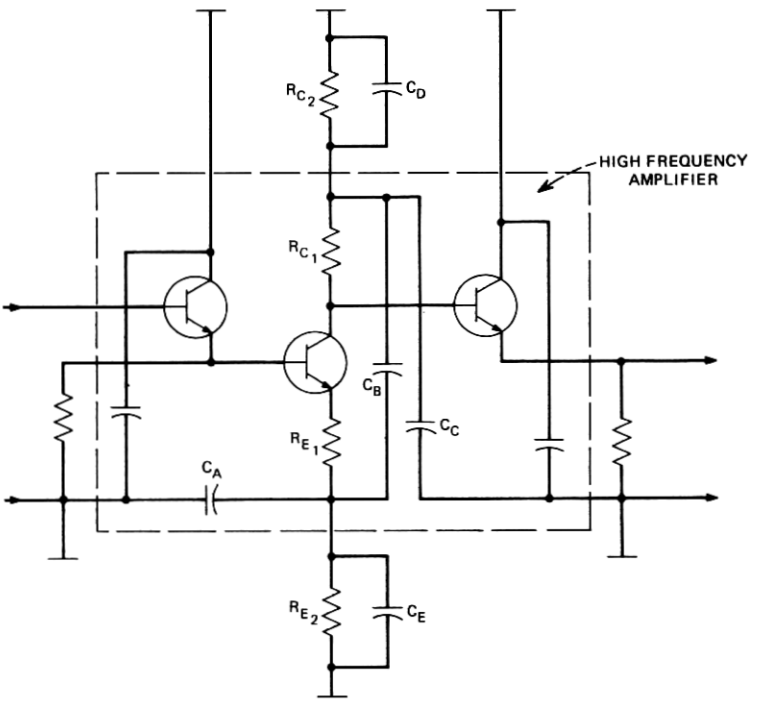

Fig. 3—Practical hf amplifier embedded in a low-frequency gain-defining circuit.

capacitances are for minimization of the lengths of the constituent current loops in the circuit for good high-frequency gain performance and the improvement of stability by effecting a reduction in the points of interaction of these loops. The condition for a flat gain spectrum can be analyzed using the simple equivalent circuit shown in Fig. 4. The simplicity of this circuit is afforded by the frequency of crossover (approximately 3kHz) being much less than the cutoff frequency of the transistor so that a low-frequency model is permissible.

The transfer function of this circuit is readily shown to be

$$\frac{V_0}{V_{in}} = \frac{R_{C1}}{R_{E1}}\left[\frac{1 + s\tau_C}{1 + s\tau_E}\right] \cdot \left[\frac{[R_{C1}/R_{E1}(1+s\tau_C)+1]D-[sC_BR_{C2}(1+s\tau_E)+sC_BR_{E2}(1+s\tau_C)]}{[R_{C1}/R_{E1}(1+s\tau_E)+1]D-[sC_BR_{C2}(1+s\tau_E)+sC_BR_{E2}(1+s\tau_C)]}\right]$$

where

$$D = (1 + s\tau_C)(1 + s\tau_E) + sR_{C2}C_B(1 + s\tau_E) + sR_{E2}C_B(1 + s\tau_C)$$

$$\tau_C = C_C'R_{C2}, \qquad C_C' = C_C + C_D$$

$$\tau_E = C_E'R_{E2}, \qquad C_E' = C_A + C_E$$

for

$$\frac{R_{E1}}{R_{C1}} = \frac{R_{E1} + R_{E2}}{R_{C1} + R_{C2}} \qquad \text{and} \qquad \alpha \cong 1.$$

It is clearly seen that by making $\tau_E = \tau_C$, the poles and zeros of the system cancel, thus producing a flat crossover. The value of C_B is seen to be unimportant. Large values of C_B will produce a dominant pole and zero which will tend to mask the required equality of τ_C and τ_E.

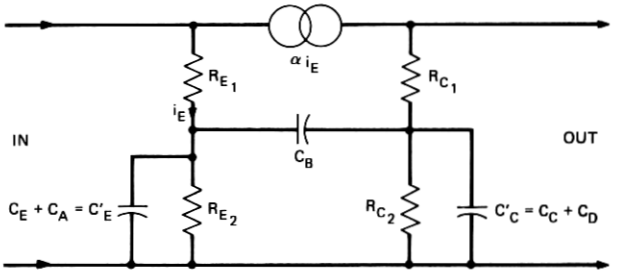

Fig. 4—Equivalent circuit of embedded gain cell.

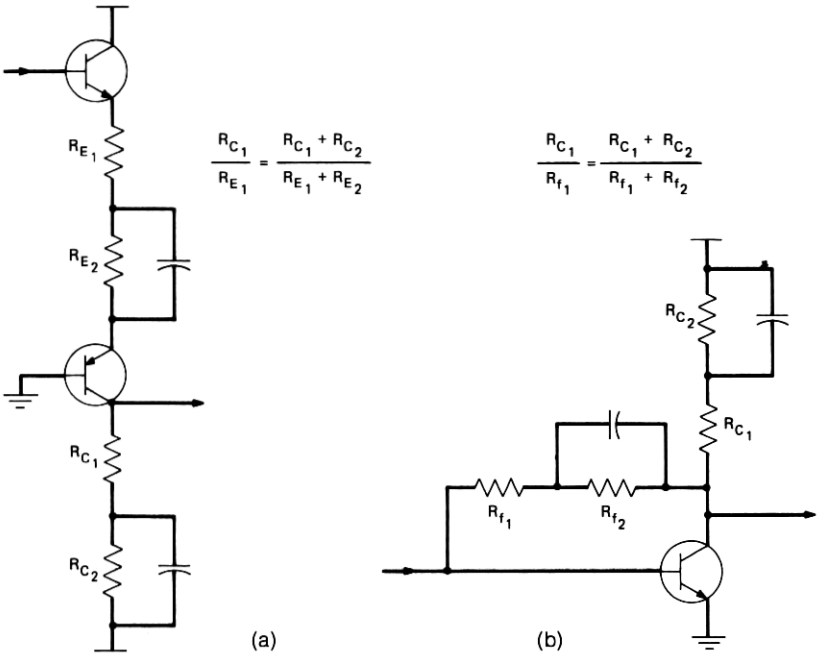

Fig. 5—Embedding technique applied to (a) modified cascode stage, (b) shunt feedback stage. (Gain equality requirement indicated for lf and hf cases.)

The consequence of separating the lf and hf gain-determining components is that the lf portion may be designed to ensure a high dc stability (e.g., R_{E_2} large) without impairment of the hf optimization.

The technique has more general applications to any gain stage where the stage gain is defined by the ratio of two real impedances; these further applications of embedding are shown for the modified cascode and shunt feedback stages of Figs. 5a and b. The realization of Fig. 5a is particularly important since the optimization of the high-frequency circuit parameters leads to frequencies of operation where the elimination of the Miller effect afforded by this circuit is important. Also, the low external emitter impedances presented provide an enhanced stability, important at these high frequencies.

These circuits constitute a class of split-band additive amplifiers. Split-band amplifiers were first described by Wheeler[7] many years ago, but their successful realization has been retarded by the difficulties of achieving a satisfactory crossover mode in extremely high-frequency amplifiers. The embedding scheme provides a crossover transition at

relatively low frequencies so that its physical synthesis is straightforward. Although the internal gain is provided in a product sense, the embedding technique is essentially additive, and thus related to the distributed amplifier of Percival[8] and the Gilbert[9] gain cell.

III. A DC-TO-2.3-GHZ EMBEDDED AMPLIFIER

The embedding principle has been embodied in a broadband amplifier of the type shown in Fig. 3. This amplifier has been designed for optimum hf performance. To demonstrate the way in which this optimization is achieved without compromising the low-frequency stability, it is pertinent to indicate briefly the hf design optimization. The design procedure is based on the simplifying assumptions that the major frequency-limiting mechanisms are the frequency fall-off of the transistor current gain α (modeled as a single pole fall-off), and the collector-base capacitance of the gain transistor (this being assumed to be the dominant parasitic reactance). For simplicity, both effects are evaluated separately. The consequence of the former effect is evaluated by substituting the single-pole approximation for α in the gain transfer function for the stage, assuming negligible loading at the output of the gain transistor (this latter approximation is justifiable since the practical realization employs double emitter follower buffering to the output). The gain transfer function is

$$\frac{V_0}{V_i} = \frac{\alpha R_{C_1}}{R_{E_1}}\left[\frac{R_{E_1}/(1-\alpha)^2}{R_{E_1}/(1-\alpha)^2 + R_s}\right],$$

R_s being the source resistance. Upon substitution of the single-pole approximation to α, and making the further simplification that α_0, the low-frequency, common-base, short-circuit gain, is equal to unity, the following equation results,

$$\frac{V_0}{V_i} = \frac{R_{C_1}}{R_{E_1}}\left[\frac{(1+s\tau_\alpha)}{1+2s\tau_\alpha + (1+R_s/R_{E_1})s^2\tau_\alpha}\right]$$

where τ_α is the time constant associated with the single-pole approximation to the frequency-dependent current gain ($\tau_\alpha \cong 1/\omega_T$). The dominant time constants here are a conjugate pair of poles at

$$p_1, p_2 = \frac{-1}{1+R_s/R_{E_1}} \pm j\frac{\sqrt{R_s/R_{E_1}}}{1+R_s/R_{E_1}}.$$

The position of these poles, normalized to τ_α, is shown in Fig. 6.

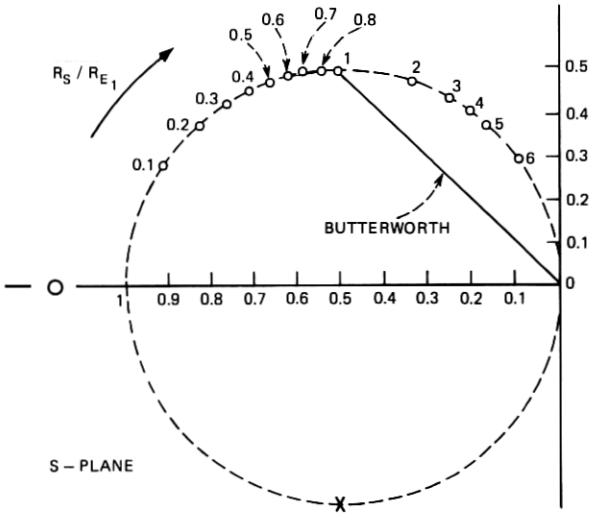

Fig. 6—Pole-zero loci for R_{E_1} variations (normalized to τ_a).

Selecting a normal Butterworth response ($Q = 0.7$) gives

$$\frac{1}{1 + R_s/R_{E_1}} = \frac{\sqrt{R_s/R_{E_1}}}{1 + R_s/R_{E_1}} \qquad \text{or} \qquad R_{E_1} = R_s.$$

This may be interpreted as an upper limit on R_{E_1} which, of course, prohibits the achievement of a high dc stability factor. Practically, the upper value of R_{E_1} is restricted by considerations of providing high-stage gain while maintaining a corner frequency, due to the collector base capacitance, of not less than the corner frequency due to high-frequency fall-off of the current gain. The devices used exhibited an f_T of 4 GHz and a C_{ob} of 0.25 pF. This output capacitance (plus other additive capacitance due to loading) restricts the value of R_{C_1} to 100 Ω for a stage gain of 8 dB, with the concomitant effect that R_{E_1} (including the dynamic internal emitter resistance) be approximately 30 ohms. For efficient quiescent point definition, and hence dc stability, the value of external emitter resistance should be of the order of 1000 ohms. These parameter values allow a complete description of all other parameter values used. The embedded amplifier was designed with a band transition frequency of approximately 3 kHz; this allows easily realizable synthesis. The actual circuit was fabricated using a hybrid technology consisting of tantalum nitride and gold thin films on alumina substrates with beam leaded

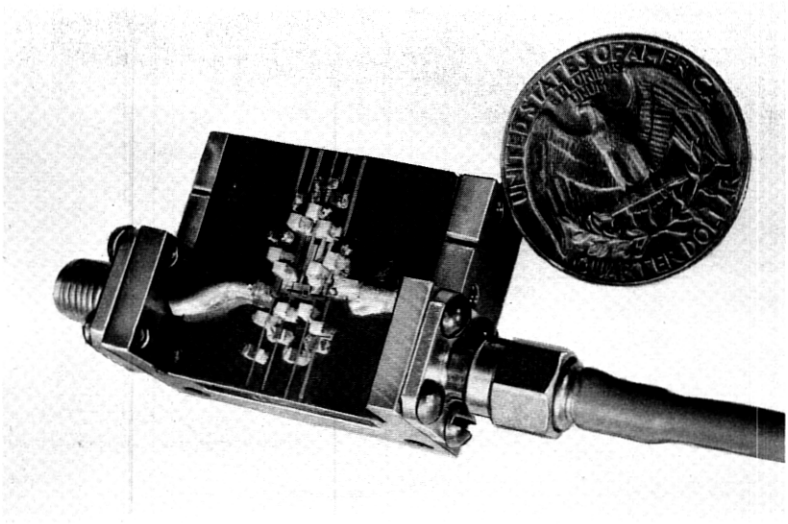

Fig. 7—Embedded amplifier in thin-film, beam lead technology.

device chips. A photograph of this realization is shown in Fig. 7. The pulse response (see Fig. 8) exhibits a 200-ps rise time with a gain of 8 to 10 dB; the frequency response (Fig. 9) shows a flat gain curve up to

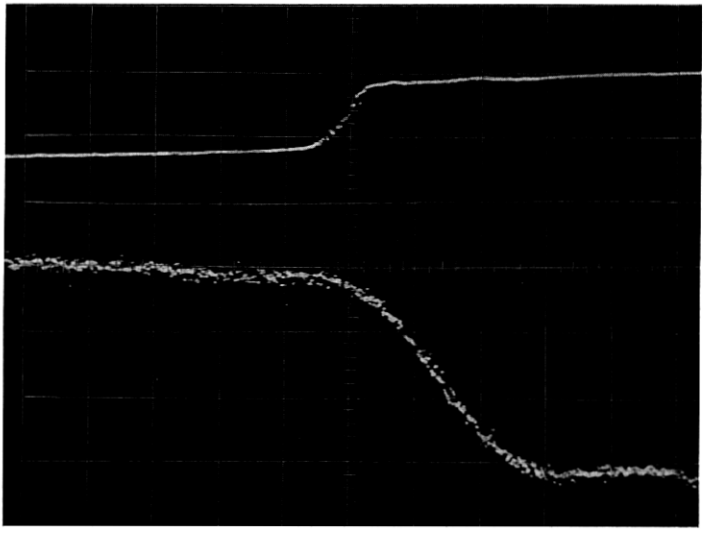

Fig. 8—Embedded amplifier pulse response. Upper trace, input. Lower trace, output. (200 mV/cm, 100 ps/cm.)

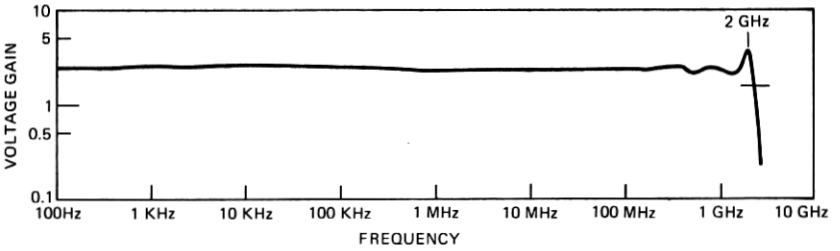

Fig. 9—Eight-decade gain response of broadband embedded amplifier.

2 GHz with the exception of some parasitic resonance-induced deviations just below 2 GHz. The conjugate pole resonance at 2 GHz is also apparent at the cutoff. This should easily be eliminated by choosing a suitable ratio of R_s/R_{E_1} to provide a subcritical Q factor.

The effect of mismatch of the emitter and collector circuit time constants, τ_C and τ_E, is shown in Fig. 10. These waveforms illustrate the effects of gross mismatches where the relaxation times observed are commensurate with a 3-KHz transition frequency.

IV. CONCLUSIONS

A technique has been described for providing gain to dc in hf amplifiers without compromising the hf circuit optimization. This

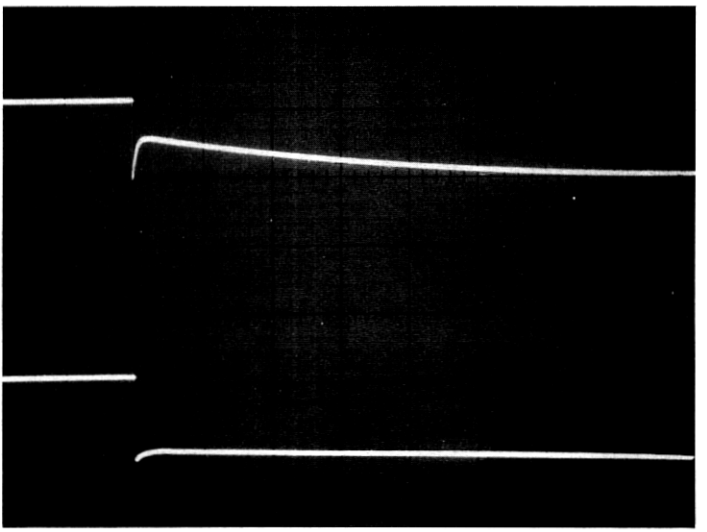

Fig. 10—Mismatch of emitter and collector time constants. Upper, $\tau_E \ll \tau_C$. Lower, $\tau_E \cong \tau_C$. (5 μs/cm.)

embedding technique can be applied to a number of types of gain stage. The common emitter stage, from which results have been obtained, exhibited a dc-to-2.3-GHz bandwidth with a voltage insertion gain of approximately 2.6. The gain was restricted to this value to minimize the effects of collector-to-base junction capacitance. With other stages, such as the modified cascode, this restriction is not as severe, and much higher gains are to be expected. The high-to-low-frequency transition is easily realized, in contrast to other split-level amplifier configurations.

The enhanced dc stability available from the embedding technique favors a cascading of individual gain cells to obtain larger amplifier gains. It is worth noting that the freedom of choice of device operating point inherent in the embedding technique allows an optimization of biasing conditions for low-noise operation, appropriate to post-detection amplification in optical PCM terminals.

V. ACKNOWLEDGMENTS

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