A Proper Model for Testing the Planarity of Electrical Circuits

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(Manuscript received August 25, 1972)

The question of whether an electrical circuit can be laid out on a plane, without resorting to crossovers or multilayer wiring, is usually answered by testing the planarity of a graph representing the circuit.

Two commonly used representations are shown to be inadequate. We present the following new representation, and show it to be complete and unrestrictive: The graph has one node for each circuit module, and one node for each net; for every net with k modules, there is a "star" of k edges connecting the net's node to each of the modules of the net.

I. INTRODUCTION

Electrical networks frequently consist of a set of modules (beam-leaded chips, DIPs, etc.), and a set of electrical interconnections or "nets" among two or more modules. Each net specifies a set of modules to be interconnected with a single conducting path. The planar design problem consists of placing the modules and the net wiring in the plane. The question of whether the interconnections can be accomplished in the plane without resorting to crossovers or multilayer wiring is usually answered by testing the planarity of a graph representing the circuit.

This graph is typically constructed by one of two mappings:

- (*i*) Module-to-Node Mapping. The modules are represented by the nodes (or points) of the graph; and the nets are represented by its edges (or lines); or
- (*ii*) Module-to-Edge Mapping. The modules are represented by the edges and the nets are represented by the nodes.

Since the edge of a graph connects exactly two nodes, these mappings are not uniquely defined and *a priori* design decisions must be made which may be either improper or restrictive, and may produce spurious crossovers (see Sections II and III).

We give a unique representation that maps both nets and modules into the nodes of a graph, G. In this representation, a k-module net will appear as a "star" with an edge from its node to each of the modules in the net. We show that this mapping is a complete and unrestrictive representation of an electrical circuit. The main result of this paper (Section IV) is that the network can be laid out in the plane without crossovers if and only if G is planar. Thus the practical problem of planarity of these networks is solved since there are good computer algorithms for testing planarity.[1-5] Such algorithms will do a good but not optimal job of minimizing crossovers in a nonplanar graph. As with other mappings, we are ignoring certain practical restrictions, such as a specified cyclic terminal order for a module. Usually, these restrictions can be forced on the graph by auxiliary strategies.

The representation presented here is similar to that given by Engl and Mylnski:[6] in order to properly represent a k-node net, the conventional definition of an undirected edge, i.e., a set of two nodes, was generalized to a set of k nodes. We demonstrate here that such generalized concepts are unnecessary. By mapping both nets and modules into nodes, we retain the conventional definition of an edge, which greatly simplifies the presentation and proof, and most importantly, permits the use of conventional planarity testing algorithms.

II. INADEQUACY OF THE MODULE-TO-NODE MAPPING

Since nets map into edges, and an edge connects exactly two nodes, there is an inherent restriction to two-module nets. A common embellishment of the module-to-node mapping, is to decompose a k-module
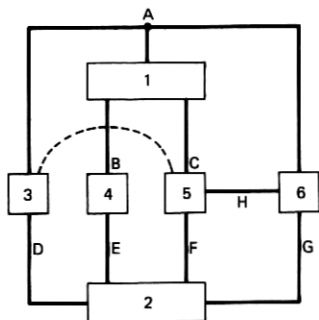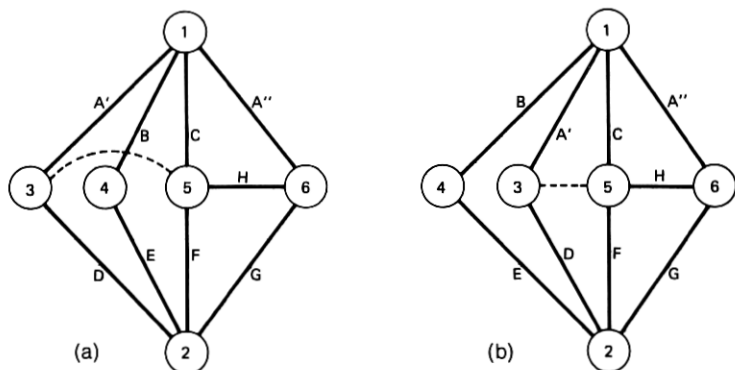

Fig. 1—Planar circuit (ignoring dashed net).

Fig. 2a.—Planar graph constructed using the module-to-node mapping on Fig. 1. Note A′ and A″ are adjacent on 1.

Fig. 2b—Alternative planar graph. Terminals for A′ and A″ are not adjacent on 1.

net $(k > 2)$ into a string of $k - 1$ two-module nets.* Thus $k - 2$ of the modules are formally permitted to have two terminals contacting the same net. Since the cyclic order of edges leaving a node is irrelevant in deciding whether a graph is planar, these two terminals may not be adjacent in a planar layout of the graph. If not adjacent, these two terminals may necessitate a crossover inside the module; we will term this a "module crossing."

For example, the electrical circuit in Fig. 1 has a three-module net A. If A is represented as two two-module nets A′ (3, 1) and A″ (1, 6) then the module-to-node mapping yields a graph having a planar layout shown in Fig. 2a. Since the A′ and A″ terminals on 1 are adjacent, they can be merged, and planarity is legitimately indicated.

However, this graph has a second, and equally acceptable, planar layout (see Fig. 2b) in which the A′ and A″ terminals on Module 1 are not adjacent, and a physical realization (see Fig. 3) of this second layout may require an unnecessary crossover inside Module 1, i.e., a module crossing.

If one adds the additional net (3, 5) (shown as a dashed line in Fig. 1) then the graph has only one planar layout (Fig. 2b), and that layout requires a module crossing for its physical realization (Fig. 3).

These two examples demonstrate that the module-to-node mapping, by arbitrarily inserting two terminals per module for certain nets, cannot distinguish layouts which are physically planar from those

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* The use of the complete graph for k nodes (all pair-wise connections), commonly but inaccurately used[7] in graphical representations for partitioning and placement algorithms, is clearly unacceptable here since the complete graph for five or more nodes is nonplanar.
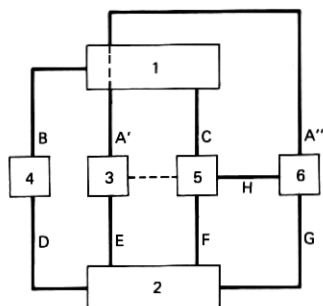
Fig. 3—Physical implementation of graph in Fig. 2b. Note "module crossing" at 1.

which use module crossings. Furthermore, if a planar layout of the graph requires the use of module crossings, there may or may not be an alternative planar layout of the graph which does *not* require the use of module crossings.

When a k-module net is decomposed into two-module connections, it is possible to choose a decomposition which will produce a nonplanar graph even though the circuit is planar. For example, the circuit in Fig. 4 is planar, and the module-to-node mapping will produce a planar graph if net A is decomposed into the string of three two-module nets: $(1, 2)$, $(2, 3)$, $(3, 4)$. However, one may have chosen the alternative decomposition $(1, 3)$, $(2, 4)$, $(3, 4)$ which yields the nonplanar graph shown in Fig. 5.

Certain technologies permit a limited amount of "under-module" wiring, which may permit the required module crossing in the above examples. However, even if this capability exists, there are two
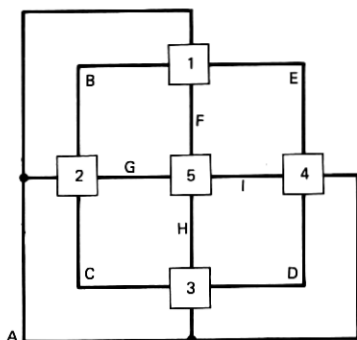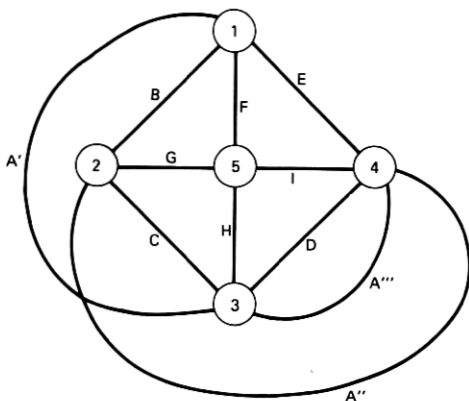

Fig. 4—Planar circuit.

Fig. 5—Nonplanar graph resulting from an inappropriate decomposition of Net A in Fig. 4.

objections to the use of this mapping: (*i*) the set of two-module nets which best represent the k-module net ($k > 2$) is difficult to determine *a priori*, and an arbitrary choice may result in unnecessary crossovers; and (*ii*) unnecessary module crossings may result.

III. INADEQUACY OF THE MODULE-TO-EDGE MAPPING

A module which connects to $k > 2$ nets cannot be simply represented as a single edge. A typical elaboration of this mapping[8] is to represent a k-net module as a ring of k two-net modules. For example, the four-net Module 2 in the circuit above (see Fig. 1–ignoring the dashed connection) could map into the four edges shown in Fig. 6a. With similar representations for Modules 1, 5, and 6, the module-to-edge mapping for this circuit has the planar layout shown in Fig. 7.

However, without the obviously planar schematic in Fig. 1 for guidance, one may have arbitrarily chosen the equally acceptable
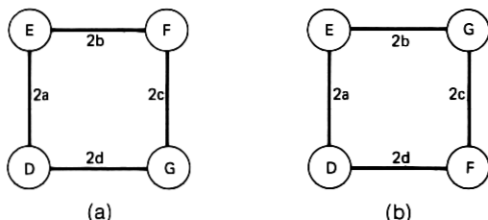

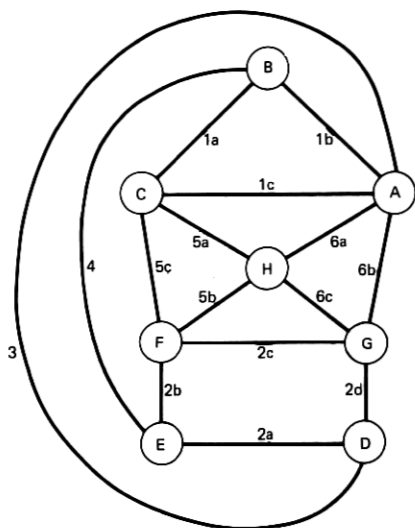Fig. 6—Alternative decompositions of Module 2 in Fig. 1.

Fig. 7—Planar graph constructed using the module-to-edge mapping on Fig. 1.

representation of Module 2 shown in Fig. 6b. In this case, the graph is not planar.

Basically, the representation of a k-net module $(k > 3)$ as a ring of edges, requires the specification of the sequence of terminals leaving a module—a specification which may not be required by the physical problem. As demonstrated in the above example, an arbitrary choice of terminal sequence may be restrictive and may yield a false indication of nonplanarity.

For certain designs, where the modules are predesigned and the terminal sequence *is* specified, the choice of ring sequence is obvious and not a restriction, but a practical requirement. Note, however, that the ring may appear as a mirror image in the planar layout of the graph; where the module cannot be physically mirrored, additional restrictions are necessary.

IV. MODULE-AND-NET-TO-NODE MAPPING

The previous two mappings fail to produce graphs which always reflect the planarity aspects of the circuit. In this section, we construct a graph, G, to represent the circuit and show that the circuit is planar if and only if G is planar. The graph G constructed from the net information has one node for each module plus a "net node" for every net. For every k-module net there is a "star" of k edges connecting the net
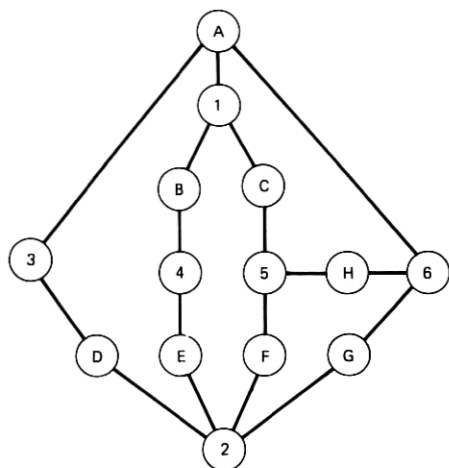
Fig. 8—Planar graph constructed using the new module-and-net-to-node mapping on Fig. 1.

node to each module in the net. Using this mapping, Fig. 8 shows the planar graph representing the circuit of Fig. 1.

The star-like subgraph is selected somewhat arbitrarily and can be replaced by any tree attached to the net's modules. Recall (Section I) that the cyclic order of edges at a module is unrestricted.

Theorem: The circuit is planar if and only if G is planar.

Proof: If G is planar, then clearly the circuit is planar. Conversely, suppose the circuit is planar. Consider the planar subgraph of any net. (Since they are electrically unnecessary, we may assume the subgraph has no loops.) We will modify it to form a star. First, create a node s at any point of the subgraph which is not a terminal. Continue to modify the subgraph by repeating the following process at s until a star subgraph results: (cf. Fig. 9).

Choose an edge (s, t) of the modified subgraph with t having at least two edges. Let (t, u) be the first edge at t in, say, clockwise order from (t, s). Create a new subgraph by replacing the edge (t, u) by an edge (dashed in Fig. 9) from s to u "running parallel" and on the left side of the path s, t, u. If t now has only two edges, then delete t and coalesce its two edges into one.

Since the subgraph of the net was planar, the resulting star subgraph is also planar and has a node s corresponding to the net. By replacing
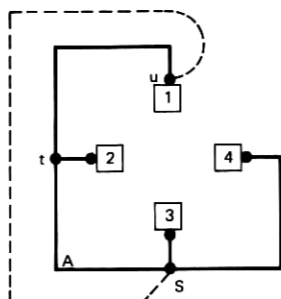
Fig. 9—Net A of planar circuit in Fig. 4.

every net subgraph by a star subgraph, we obtain a planar graph, G, of the desired type. Q. E. D.

Two observations may substantially reduce the size of the graph which is tested for planarity. Since a two-module net results in a star with only two edges, it is clear that planarity is unchanged if this net node is deleted and the two edges are coalesced into one. Similarly, a two-net module results in a node with only two edges connected to it; again, that module node can be deleted and the two edges coalesced into one.

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