Peripheral System

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The peripheral units of No. 2 ESS, described in this article, include the scanners, the network, the peripheral decoders and the trunks and service circuits. The scanners serve to collect information for the control complex. The network is a folded, space division network using ferreed switches. The peripheral decoder uses integrated circuits to control relays in user circuits as directed by the control complex. The program controlled trunks and service circuits provide an interface between the outside world and the remainder of the No. 2 ESS.

I. INTRODUCTION

Other articles in this issue describe the overall system organization and the processor complex with its busing and pulse distributing facilities.[1, 2] This article describes the major functional peripheral blocks of the system: the scanners, the network, the peripheral decoders and the trunks and service circuits.

II. SCANNERS

Electronic scanners may be broadly defined as circuits which sense or detect the absence or presence of voltage or current. In No. 2 ESS, scanners are used to detect the on-hook, off-hook status of a customer's line, to check the status of talking paths for flash and disconnect, to monitor certain test points in various frames and to scan other miscellaneous points about which information is desired. In a certain sense, the scanners may be thought of as the primary source of information to the control complex regarding the actual physical state of the customers and circuits associated with the outside world.

2.1 *Ferrods*

The ferrod is the sensing element used in No. 2 ESS.[3] A single ferrod consists of a ferrite rod or stick, approximately the size of a large paper match, around which is wound a pair of solenoidal control coils. Threaded through two holes in the center of the ferrite stick are hair-pin single-turn interrogate and single-turn readout windings. Figure 1 is a diagram of a ferrod.

To determine the state of the ferrod, a 0.5 amp bipolar pulse is applied to the interrogate winding. The positive half cycle, approximately 3 microseconds long, switches the ferrite around the holes, as

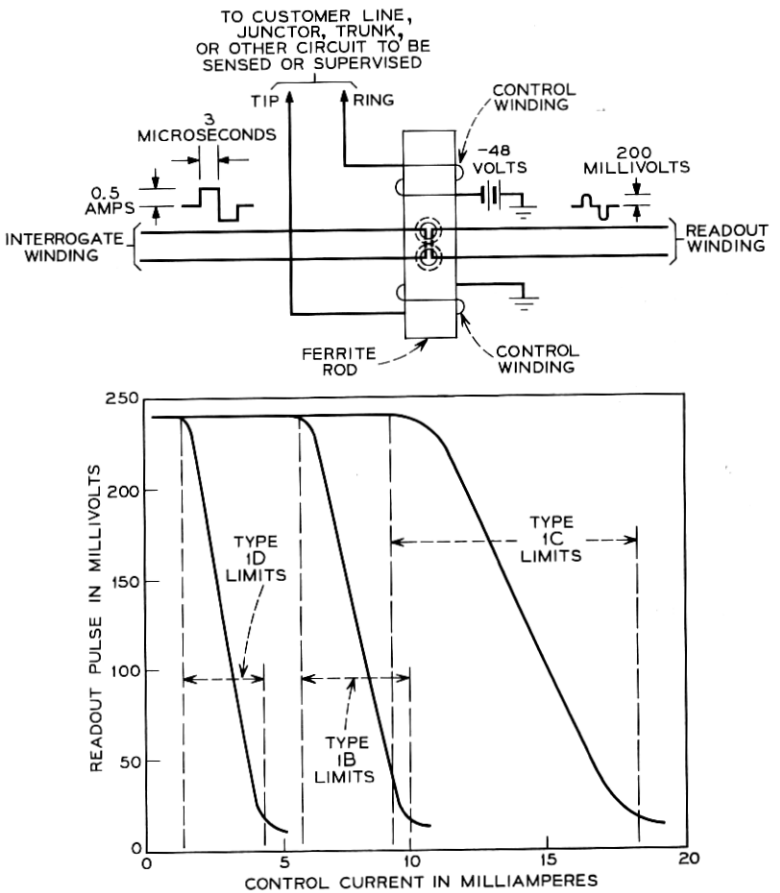


Fig. 1 — Ferrod schematic diagram and typical characteristics.

two small cores might be switched, and causes a voltage to be induced in the readout winding. This voltage is nominally 200 millivolts as read using an integrating circuit with a 1 microsecond time constant. The negative (second) half of the current pulse is used to reset the ferrite in the switched area. As current through the control windings is increased from zero, the ferrite stick becomes saturated, the switchable area of the "cores" decreases, and the output decreases. When the current level in the control windings completely saturates the ferrite stick, there is no ferrite switched and the output is less than 20 millivolts.

2.2 *Ferrod Types*

There are three types of ferrods used in No. 2 ESS. All operate as described above, and differ only in their sensitivity and winding resistance which are listed in Table I.

1B ferrods are used in the line scanner where they apply battery and ground to loop start lines. For ground start applications, such as coin or PBX lines, the two control coils are placed in series and supply battery voltage to the line. The 1B ferrod is wound with resistance wire which limits current flow in the presence of an accidental ground. The 1B ferrods are connected to the subscriber lines through contacts in the switching network so that they may be removed from the line during talking, because they would otherwise shunt the line and impair transmission.

The 1C and 1D ferrod assemblies, each consisting of two ferrods, are used for monitoring trunk and junctor circuits. The 1C ferrod is placed in series with the battery and ground leads to the junctor and to

TABLE I—ELECTRICAL SPECIFICATIONS OF FOUR FERROD SENSOR CODES

Ferrod Sensor	1B	1C	1D 1E*
Number of windings per ferrod	2	2	2
Resistance per winding (±10%)	660	19	35
Turns per winding	1600	930	1300
Approximate inductance (mH, both windings)	220	70	500
Maximum current (mA)	100	100	100
Maximum unbalance between windings (ohms)	—	1.0	1.0
Nonoperate current (mA)	5.5	9	1.8
Operate current (mA)	10	18	3.9

* The 1E ferrod is electrically identical to the 1D.

the customer side of trunk circuits. The 1D ferrod is used mainly on the distant office side of trunk circuits and in service circuits.

2.3 *Scanner Organization*

Groups of ferrods, controlled by a duplicated control circuit, make up a scanner. Each of the control circuits under the direction of the central processor can interrogate groups of 16 ferrods at a time, up to a maximum of 1,024 ferrods, at a rate of 16 ferrods every 12 microseconds.

The functional arrangement of a scanner is shown in Fig. 2. The 1,024 ferrods to be interrogated are arranged in a matrix consisting of 64 rows of 16 ferrods. To address a scanner, an enable pulse (0.5 microsecond) is sent to the desired controller from a central pulse distributor point. This pulse is stretched (2.5 microseconds) and causes the controller to read in parallel a 17-bit word (0.5 microsecond long) on the address bus from the active control unit into pulse-stretching address register circuits (3.8 microseconds). The 17-bit word contains two 1-out-of-8 selections that are used to pulse an 8×8 biased core matrix. The output from each core of the matrix is connected to interrogate one of the 64 rows of ferrods. The output of the ferrods are multipled along the columns and are connected to 16 duplicated readout amplifiers which in turn send back the status of the 16 ferrods to the central processor over the scanner answer bus (0.5 microsecond pulses). A 17th bus bit is used for maintenance purposes.

The leads going to the ferrod matrix from the core matrix of one controller are connected in series with the leads of the core matrix of the duplicate controller. In this manner, either controller may interrogate any of the 64 rows of ferrods. The 16 duplicated readout amplifiers return the ferrod status to the central processors over two identical buses. The duplication of the control and readout circuitry provides the two central processors with the means of scanning the ferrod matrix in the event that one of the processors or one of the scanner controllers is out of order.

2.4 *Types of Scanners*

Line scanners are used to detect customer line originations. In the network each control frame contains two complete 1,024 point scanners, except for the ferrods. The ferrods are provided as needed, in growth steps of 512, in the line-trunk switching frames.[4]

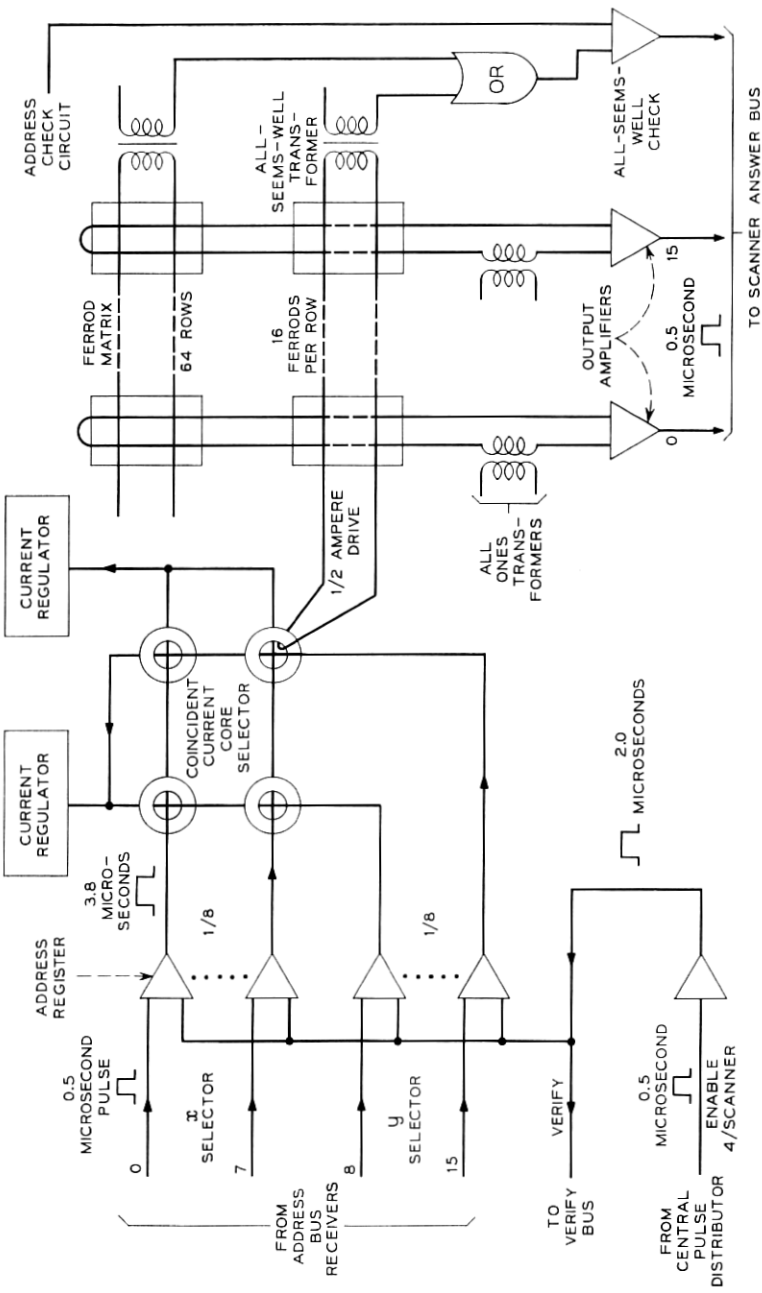


Fig. 2 — Functional diagram of a 1024-point scanner.

The master scanner is used for scanning miscellaneous trunks and service circuits and special scan points in various pieces of equipment around the office. The rate at which a row of ferrods is scanned in the master scanner is a function of the type of scan points contained in that row.

The universal trunk scanner is used for scanning trunk and junctor circuits mounted on the universal trunk and junctor frame. In most offices it also serves as a partial master scanner.

2.5 *Maintenance Features*

Each scanner controller contains several maintenance features designed to detect malfunctioning circuitry and inform the central processor when the information on the scanner answer bus is questionable. The enable pulse, which causes a controller to read the address information is also used to send an enable verify pulse back on the enable verify bus. Detectors are built into the core driver circuit in each controller to indicate that only one core drive horizontal, and one core drive vertical are pulsed. This will insure that only one row of ferrods is pulsed. In series with each ferrod row is a transformer, used to detect when that row of ferrods is pulsed. The outputs of all the transformers are ORed. A pulse on the output lead of the OR gate, along with the pulses indicating that only one horizontal and one vertical of the core matrix are being pulsed, will cause an ALL SEEMS WELL—SCANNER pulse to be transmitted on the seventeenth lead of the scanner answer bus. The absence of either of the three input signals will cause an ALL SEEMS WELL—SCANNER failure.

To determine that the output amplifiers are working correctly, provision is made to pulse all 16 outputs using a maintenance order. A seventeenth bit on the address bus is used, along with any address, to pulse 16 "all ones" transformers which are in series with each of the 16 ferrod readout loops. This simulates all ones to the readout amplifiers. The central processor expects to receive all ones and an ALL SEEMS WELL—SCANNER failure on this order.

III. SWITCHING NETWORK

The No. 2 ESS network is a space division, two-wire network in which metallic connections are established through ferreed switches.* The combined line-trunk switching network has lines and trunks assigned to terminals at one side of the four-stage array with junctors

* The operation of ferreed switches is described in Refs. 5 and 6.

interconnecting the switches on the opposite side to form the folded eight-stage network (Fig. 3). By not having a separate line network and trunk network, "getting started" costs have been minimized. Up to fifteen networks can be interconnected to provide an ultimate traffic capacity of over 100,000 hundred-call-seconds.

To establish connections, the processor selects the desired network paths and sends peripheral orders to the network control circuits. These circuits in turn execute these orders to establish the specified paths operating the four stages on a cycle of 20 milliseconds between the receipt of an order and the end of the operation for simple one-part orders. Two-part four-stage orders, such as checking for foreign potentials and then setting up a connection, can be executed at a maximum rate of one every 40 milliseconds.

3.1 *Network Topology*

A line-trunk switching network is composed of from one to four line-trunk switching frames and a network control junctor switching

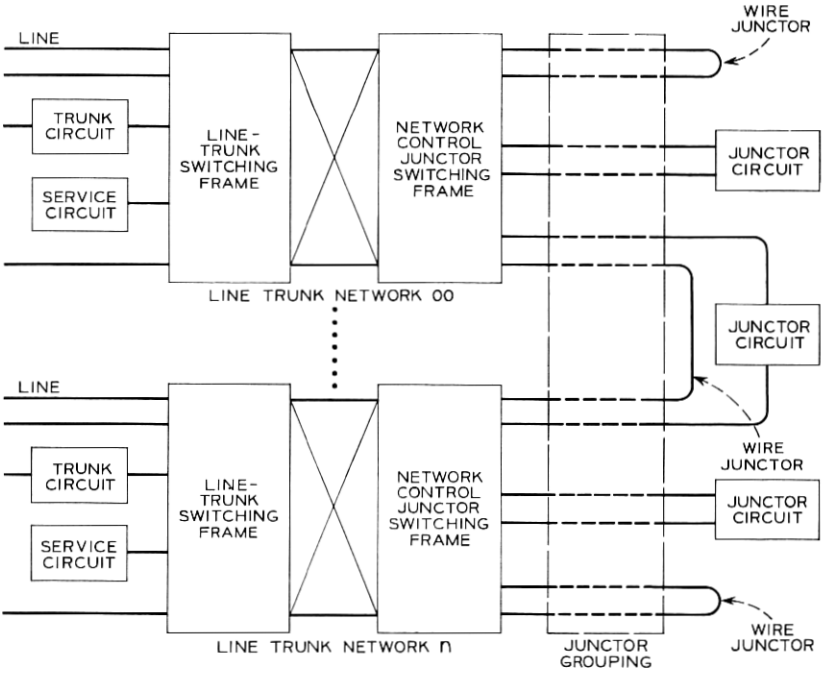


Fig. 3 — No. 2 ESS network diagram.

frame. The first two stages of the four stages of switching are located in the line-trunk switching frames. The third and fourth stages of switching are in the network control junctor switching frame. Concentration ratios of 2:1 and 4:1 are available. The concentration ratio is changed by the use of connectorized B-link multiples and equipping of line-trunk switching frames.[4]

Each line-trunk switching frame contains two concentrator groups, and each concentrator group contains eight line concentrators. A concentrator (Fig. 4) interconnects 32 lines and 16 B-links through its two stages. Thus, each concentrator group terminates 256 terminals on the input to the first stage switches and 128 B-links on the outputs

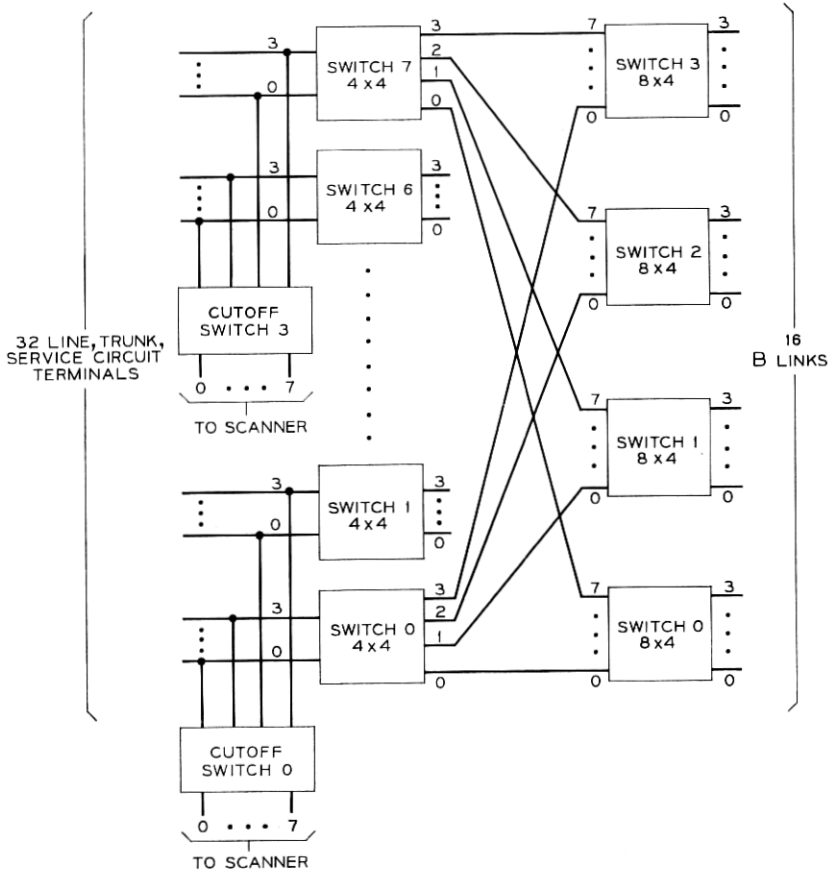


Fig. 4 — Tip-ring block diagram for 2:1 concentrator.

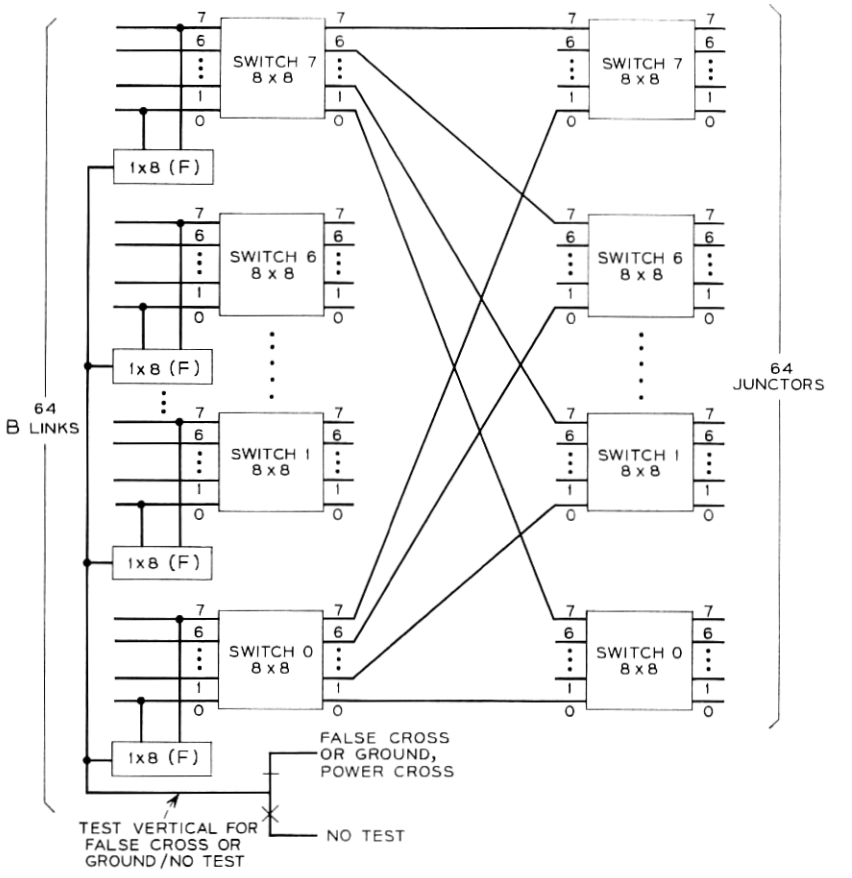


Fig. 5 — Tip-ring block diagram for junctor switches.

of the second stage switches. In addition to the crosspoint switches, each line-trunk switching frame contains one polar cutoff ferreed per input terminal to provide for scanner access.

The network control junctor switching frame contains eight grids, each of which is used to interconnect 64 B-links and 64 junctors through two switching stages (Fig. 5). The eight grids terminate 512 B-links on the input switches and 512 junctors on the output switches. There is also one polar ferreed per B-link, the F contact, for "test vertical" access.

The "test vertical" may be connected to either the no-test or to the

false cross or ground power cross circuits. The steering of the test vertical to either circuit is accomplished using two polar ferreeds connected in series with the coils in opposition. This permits opening the no-test contacts and closing the false cross or ground contacts with a pulse of one polarity, or the opposite with a pulse of reversed polarity. These two ferreeds are for each grid. The false cross or ground check is performed to check for internal network false crosses or grounds upon the establishing of new network paths. The power cross circuit is used to check for foreign potentials on customer lines. A bridged test connection may be made to any network path via the no-test contacts.

Eight grids are interconnected with four concentrator groups to form the fully equipped 2:1 network (Fig. 6). The addition of four more concentrator groups provides a 4:1 concentration ratio network (Fig. 7). The wiring pattern between concentrator groups and grids is such that two of the 16 outputs of a concentrator are wired to each of the eight grids. With this wiring pattern, each of the 1,024 terminals for the 2:1 concentration ratio (or each of the 2,048 terminals for the 4:1 concentration ratio) has access to each of the 512 junctors over either of two paths.

3.2 *Network Control Circuits*

The switching network is controlled by a pair of controllers, either of which can access the entire network (Fig. 8). Contacts on wire-spring relays are inserted in the control winding paths of every input, output, and intermediate link on both the concentrator groups and grids (Figs. 9 and 10). The interconnection of control windings between switches is parallel with the tip-ring interconnection pattern. The selection of a set of relays defines a unique control winding path.

A separate set of path selection relays is provided for each concentrator group and for each grid. The relays are double-wound so that they may be accessed by either controller. Under normal conditions, with both controllers in service, the controllers may operate simultaneously, provided that the two paths being connected are in different concentrator groups and in different grids.

3.2.1 *Network Input Information to Input Register*

The input information received by the network controller from the central processor consists of path data and order data sent in the form of a bipolar pulse stream from the central pulse distributor. Figure 11 depicts the information sent to the controllers. The path data is re-

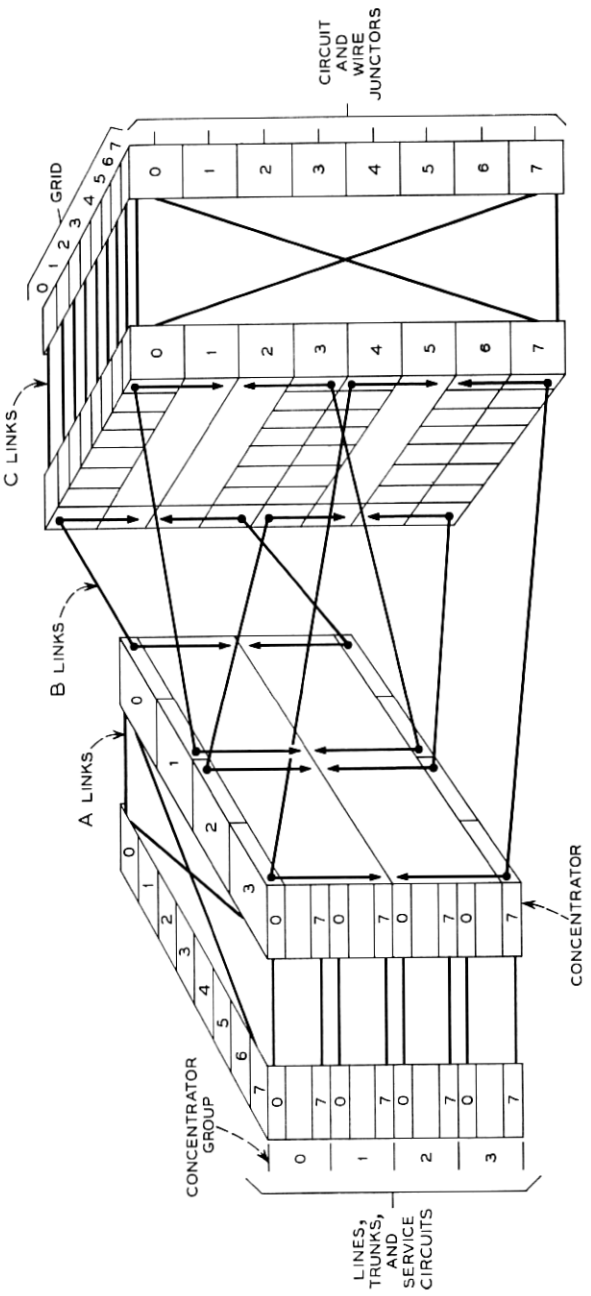


Fig. 6—2:1 concentration ratio line-trunk network fabric.

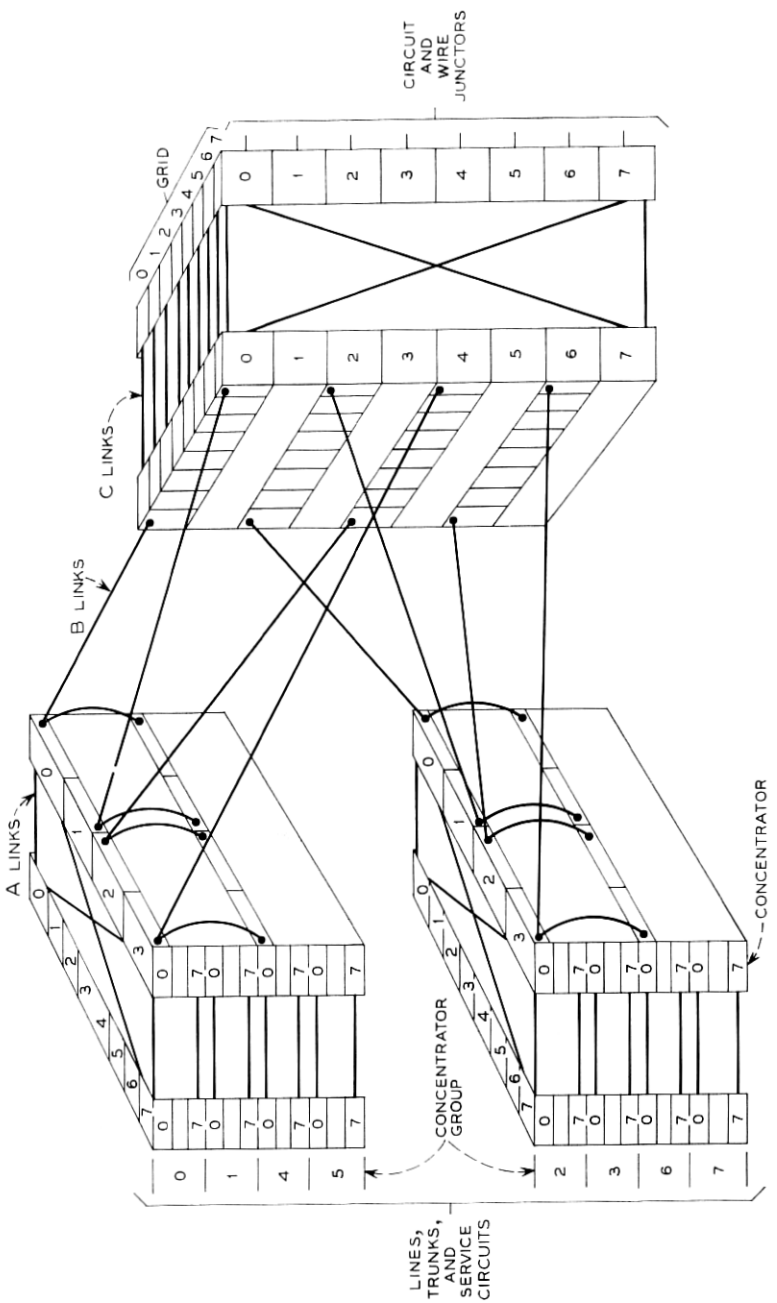


Fig. 7 — 4:1 concentration ratio line-trunk network fabric.

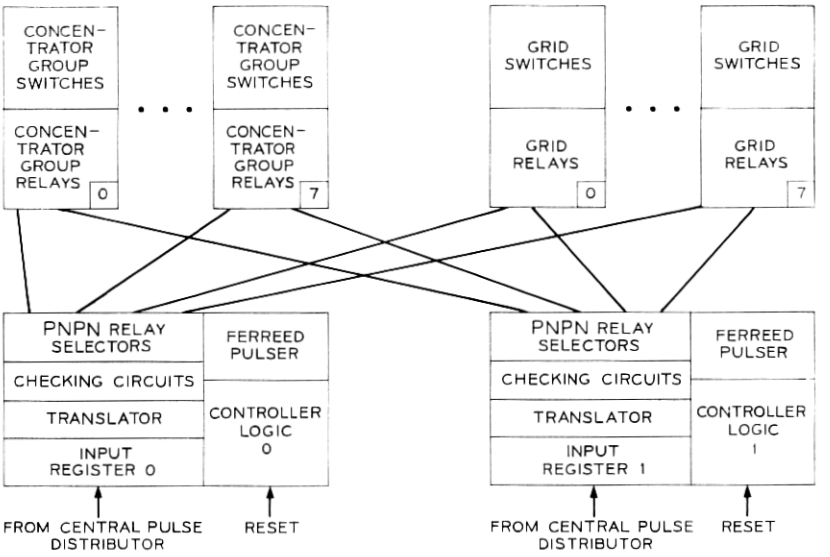


Fig. 8 — Network block diagram.

ceived in several subgroups. These groups contain information selecting the concentrator, the input switch and input level within the concentrator, the grid, and the output level and output switch within the grid. In addition, information is given as to which of the two B-links that interconnect these input and output points is the desired B-link. The information is provided in binary form and a parity check is made on the overall received information including the path, the order group data, and the start code. Parity will be odd, that is, an odd number of "1s" will be transmitted. By directly sending the input terminal identity and the junctor terminal identity in binary form, no translation of these quantities is required in the processor prior to sending a network order. Sixteen orders can be specified by the four order bits in the message. Thirteen are presently used. See Table II.

The bipolar pulses are received in a 28-bit integrated circuit shift register. The network responds with an "enable verify" pulse at the time that it receives the "first address bit" if that bit is a "one" and if no bits have been received since the controller finished its previous cycle or since the controller was reset using the external reset. The frame also responds with an "enable verify" to the central processor at the time that it has received all 28 bits and has checked that the parity and the start code of the information it has received is valid.

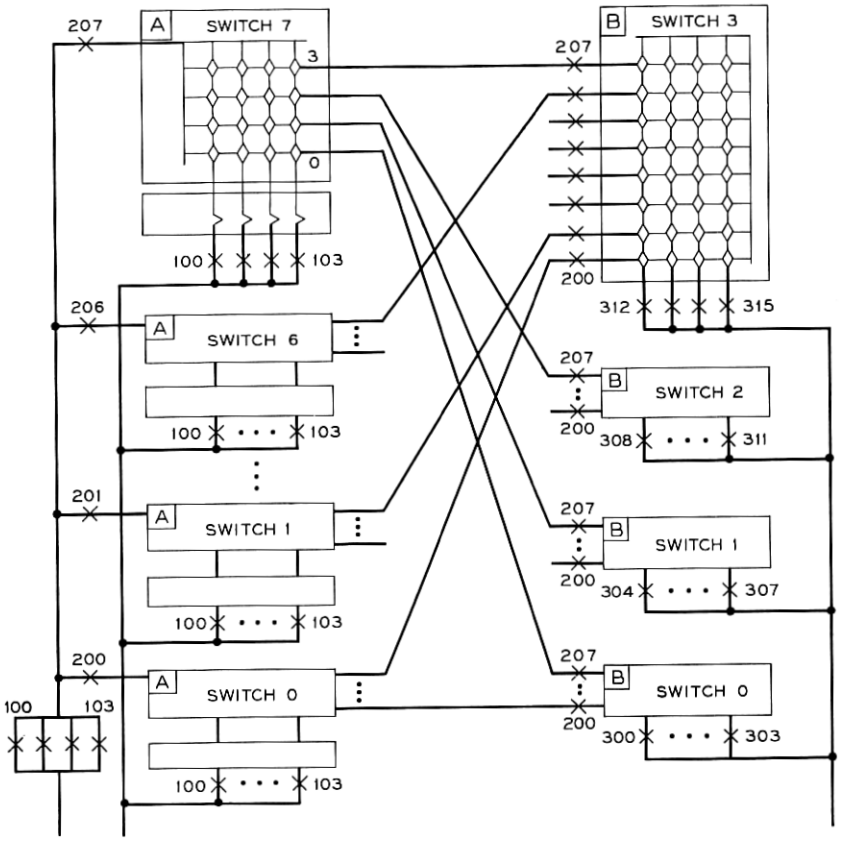


Fig. 9 — Ferreed control winding paths for concentrator 0. 100 series relays determine input level, 200 input switch, and 300 output level.

3.2.2 *Translators, Relays, and Control Logic*

The output of the 28-bit input register goes to two places in the network controller. The logical output that is used to generate the second "enable verify" is also used to send a start signal to the control logic portion of the network controller. The information concerning the input and the output points of the path goes to translators. The outputs of the translators are connected to PNPNS (silicon control rectifiers) which in turn operate wire-spring relays. The control logic portion of the controller is used to gate the output of the PNPNS to the wire-spring relays at the appropriate times and to cause the correct sequencing of the various internal circuits.

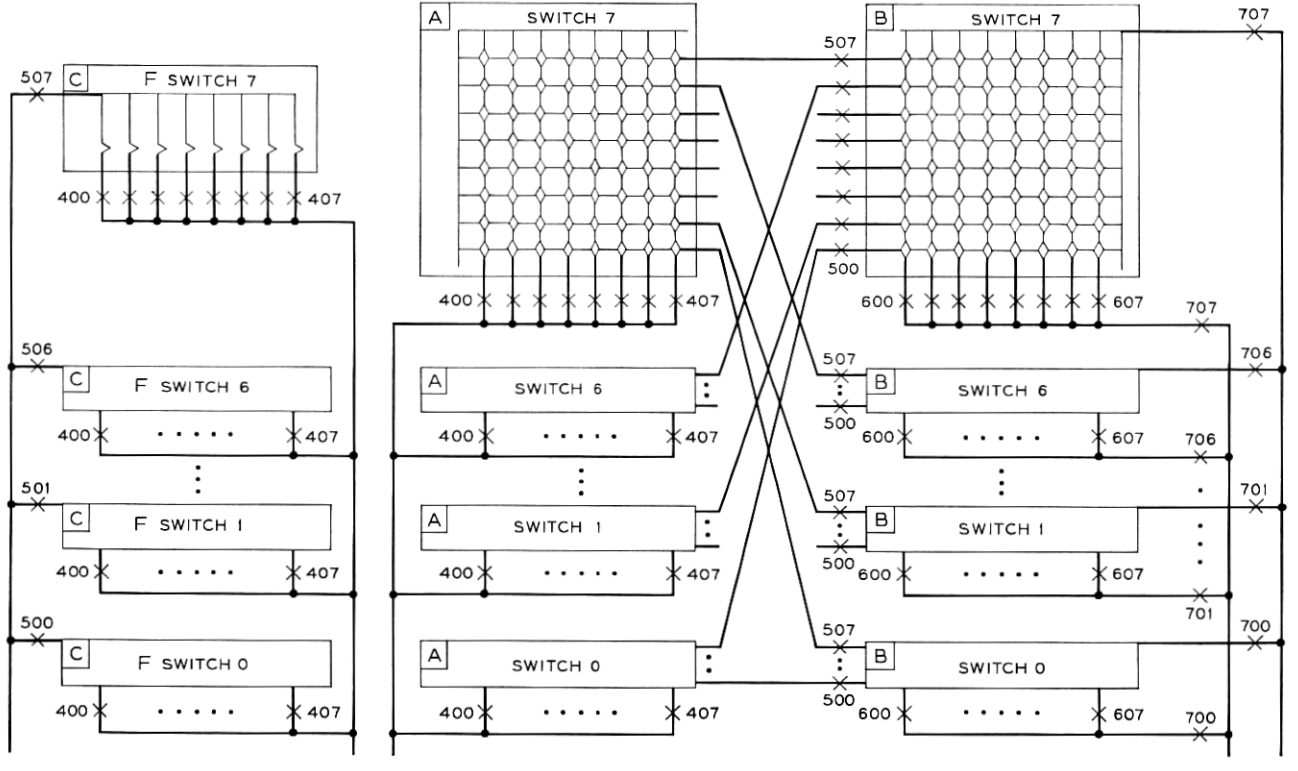


Fig. 10 — Ferreed control winding paths for grid 0. 400 series relays determine input level, 500 input switch, 600 output level, and 700 output switch.

3.2.3 *Ferreed Pulser*

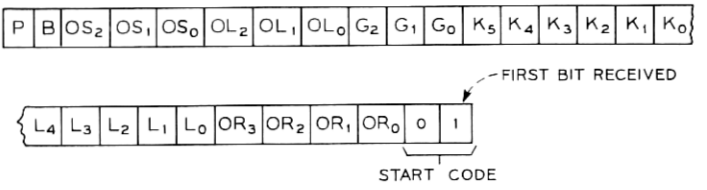
After the wire-spring relays have been operated and a pulsing path exists, the ferreed pulser fires. When the amplitude of the pulse flowing through the ferreed switches is above a certain minimum value, the ferreed pulser generates a pulser o.k. signal. If the order that is to be carried out requires only one pulsing of the ferreed network, the pulser o.k. signal causes the control logic circuit to reset itself. Certain orders to the network, however, require that the ferreed pulser fire into the network twice. For these orders, after the first ferreed pulser o.k. signal is received by the control circuit, a path is set up for the second half of the network operation. The ferreed pulser then fires a second time, and upon receipt of a second ferreed pulser o.k. signal, the control logic circuitry will be reset. Low and medium outputs are provided on the pulser and are used when fewer than the maximum number of ferreed coils are being pulsed.

3.3 *Maintenance and Check Features*

3.3.1 *General*

The internal checking circuits monitor the operation of the network controllers. These circuits will prevent the controller from processing an order if an invalid address or other malfunction is detected. The controller remains in the state that it was in when the malfunction was detected until an external reset signal is sent to that controller. The system can monitor the network operation via scan points. Three scan points, S, F, and T, are associated with each controller. These scan points are terminated at a master scanner indicating the state of the controller at any time. Table III shows the state information coded on these three ferrods. Prior to sending out network orders, the program checks the S, F, and T points to see if each controller has successfully cycled the previous order sent it and has returned to the "idle" state.

Should a controller have "locked up," diagnostic routines are run to localize the trouble. By sending special orders to the duplicate controller, the faulty controller can be switched into one of several diagnostic modes. Additional internal points are then connected to a common set of ferrods via a "diagnostic bus." After diagnosing the trouble, the faulty controller may be left in the quarantine mode. It is then prevented from operating any path select relays.



		NO. OF BITS
$OR_3\ OR_2\ OR_1\ OR_0$	---1/16 ORDER SELECTION	4
$L_4\ L_3\ L_2\ L_1\ L_0$	---1/32 INPUTS	5
$K_2\ K_1\ K_0$	---1/8 CONCENTRATORS	3
$K_5\ K_4\ K_3$	---1/8 CONCENTRATOR GROUPS	3
$G_2\ G_1\ G_0$	---1/8 GRIDS	3
$OL_2\ OL_1\ OL_0$	---1/8 OUTPUT LEVEL	3
$OS_2\ OS_1\ OS_0$	---1/8 OUTPUT SWITCH	3
B	---1/2 B LINK SELECTION	1
		25
	START CODE AND PARITY	3
	TOTAL BITS	28

OVERALL PARITY ON THE 28 BITS IS "ODD"

Fig. 11 — Network input message format.

3.3.2 *Group Check Circuit*

The group check circuit monitors to assure that one and only one relay is operated in each of the groups of wire-spring relays. The output of the group check circuit is fed to a separate flip-flop for each numbered group of relays. The output of each group check flip-flop can be connected to the diagnostic bus. This permits immediate identification of the numbered group that has caused a group check failure. In addition, to provide greater fault resolution, one contact on each wire-spring relay in each numbered group is connected to the diagnostic bus at the same point that the group check circuit for that numbered group is connected to the diagnostic bus. An additional flip-flop is connected to one bit of the diagnostic bus to indicate whether the information that is being presented on the diagnostic bus is the group check flip-flop failure indication or the wire-spring relay contact information. Multiplexing of the two functions, using one additional bus bit, saves seven diagnostic bus points.

TABLE II—NETWORK ORDERS

Network Order		Crosspoint Operation						
		CO	First	Second	FCG/NT	F	Third	Fourth
OR1	Connect with cutoff and F open	O	C	C	NC	O	C	C
OR2	Connect with FCG (two-part order)	NC O	O C	C C	FCG NC	C O	C C	O C
OR3	Open cutoff and first stage	O	O	NC	NC	NC	NC	NC
OR4	Close cutoff, open first stage	C	O	NC	NC	NC	NC	NC
OR5	Connect with cutoff closed and F open	C	C	C	NC	O	C	C
OR6	Connect no-test	NC	NC	NC	NT	C	NC	NC
OR7	Open F contact	NC	NC	NC	FCG	O	NC	NC
OR8	Power cross (two-part order)	O NC	C NC	C NC	FCG FCG	C O	C NC	C NC
OR9	FCG	NC	NC	NC	FCG	C	C	C
OR10	Test order	NC	NC	NC	NC	NC	NC	NC
OR11	FCG with first stage and cutoff closed	C	C	C	FCG	C	NC	NC
OR12	FCG with first stage closed, cutoff open	O	C	C	FCG	C	NC	NC
OR13	Special diagnostic order	NC	NC	NC	NC	NC	NC	NC

Orders 0, 14 and 15 are not assigned.
O = Open.
C = Closed.
NC = No change from previous state.
FCG = False cross or ground check.
F = Test vertical access fereed contact.

3.3.3 *Pulser Check Circuits*

The short-to-ground circuit in the ferreed pulser determines if there is a short to ground somewhere in the pulse path portion of the ferreed network. This circuit does not inhibit operation of the ferreed pulser but is available for connection to the diagnostic bus.

A check is made on the ferreed pulse path continuity before the ferreeds are pulsed. This check detects if a path exists.

A pulse verification check is the last check to be performed during a normal operating cycle. This circuit is operational every time the ferreed pulser is supposed to be firing. As described earlier the generation of pulser o.k. signals reset the controller to the idle state successfully completing the network cycles.

IV. PERIPHERAL DECODER

Every electronic switching system must give its control complex access to many points in the peripheral area that require action signals. Many such signals involve controlling relays in junctor, trunk, and service circuits. The No. 1 ESS uses a signal distributor containing a relay contact translation tree to drive magnetically latching relays in the user circuits.[3] It has been difficult in the past to compete economically with contacts on relays as decoding elements. The rapid progress of monolithic integrated circuits in recent years, however, has made them quite competitive as translators and memory elements. An all electronic action signal distribution scheme used in No. 2 ESS meets the system objectives of low cost, high reliability, and—especially important in a small size system—capability of graceful small modular growth.

4.1 *General Operation of Peripheral Decoder*

As described for the network controller in Section 3.2.1, signals are sent to the peripheral decoder in the form of a serial bipolar pulse stream; in this case, seven bits long. Figure 12 is a block diagram of a peripheral decoder. In its most numerous application the decoder will be connected to four trunk or junctor circuits, each having three relays. Each relay is connected to and operated by a flip-flop. Twelve flip-flops are grouped into four buffers each having three flip-flops. The first bit sent to a decoder from the central pulse distributor is a logical "1" start bit. Then come two bits (B0, B1) specifying which of the four buffers the message is destined for. Then the three information bits (I0, I1, I2) followed by a stop bit "1" are shifted in. Upon

TABLE III—CODING OF S, F, AND T FERROD STATES

Scan Points			State of Network Controllers
S	F	T	
0	0	0	Success state (idle)
0	1	0	Enabled state
1	0	0	Not assigned
1	1	0	FCG or power cross failure
1	1	1	Power removed mode
0	1	1	Diagnostic mode 1, 2, or 3
1	0	1	Not assigned
0	0	1	Quarantined mode

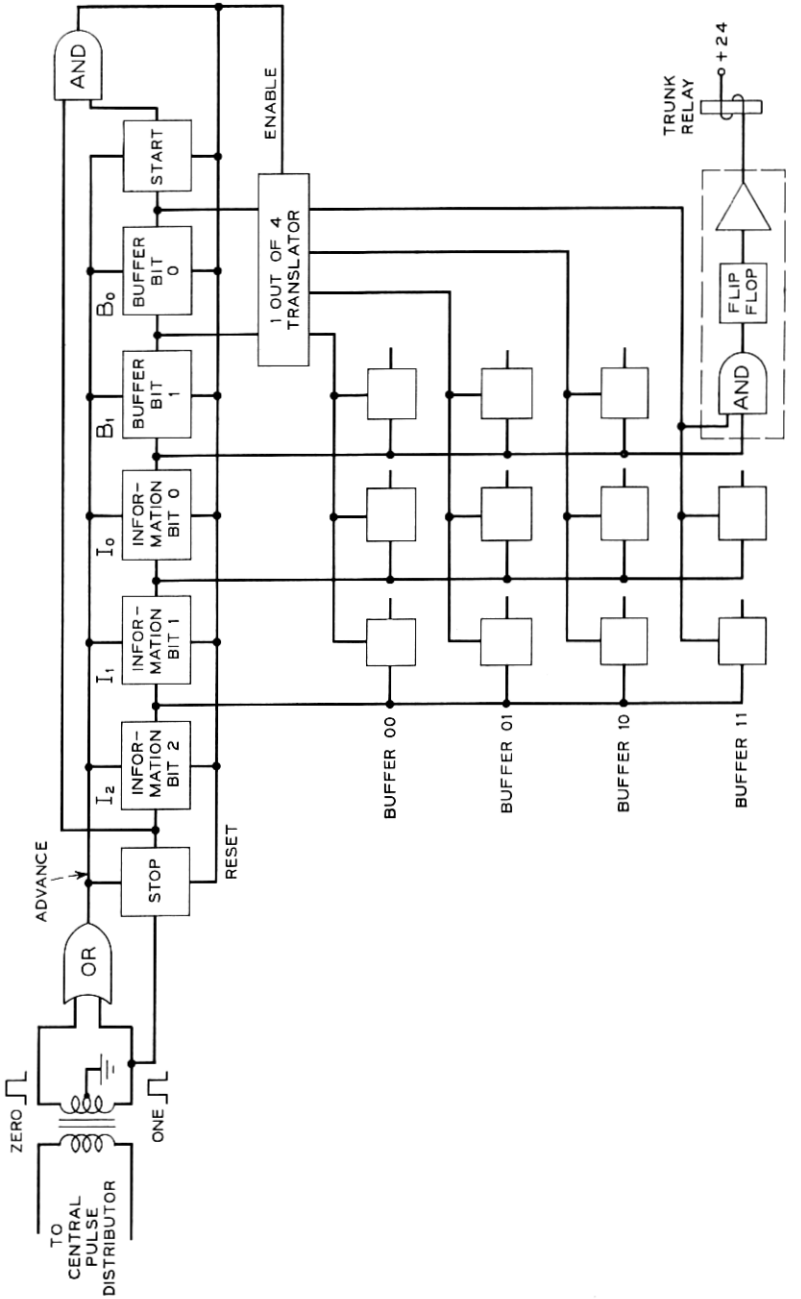


Fig. 12 — Peripheral decoder block diagram.

receipt of the stop bit, the three information bits are gated to the three flip-flops in the buffer specified by the two buffer bits. The shift register is then cleared. The three trunk circuit relays connected to the three flip-flops in the selected buffer will subsequently assume the same operated (released) states as the 1 (0) states of the buffer bits.

The signaling bits play an important role in indicating to the peripheral decoder that a message is complete and that it can now act upon the received information. If for some reason the processor cannot complete a message, the peripheral decoder can be cleared, without resulting in any relay action, by transmitting several logical zeros.

4.2 *Circuit Details of Peripheral Decoder*

4.2.1 *Nonracing, Static Shift Register*

A static shift register cell basically consists of a cross connected flip-flop to which nonracing features are added. The nonracing features permit orderly shifting of information without information loss or skipping one or several cells. Discrete component shift registers usually contain reactive components, such as capacitors. On monolithic integrated circuits, capacitors require unreasonably large silicon areas and for this reason other solutions have been developed. The peripheral decoder uses a D-type flip-flop as a shift register cell (Fig. 13). The feature that makes a D-type flip-flop nonracing is that the advance pulse, while sensing and forwarding the information on the input terminal at the same time locks up the input via the two feedback connections. The switching times of the gates that are used in the shift register can be assumed to be reasonably uniform.

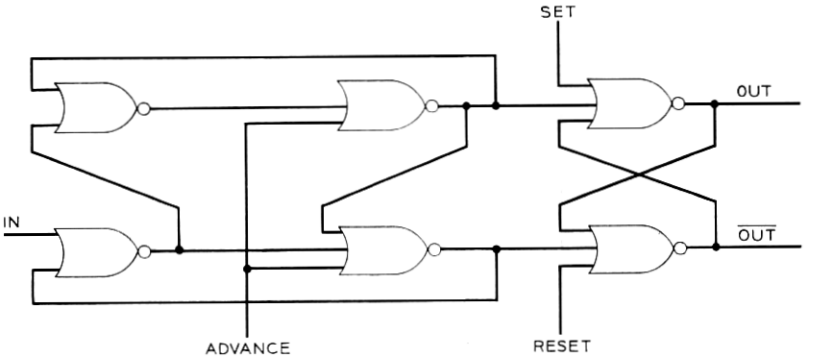


Fig. 13 — D-type flip-flop.

While the use of a D-type flip-flop eliminates races within the shift register itself, there still remain possible race conditions during the transfer and reset operations. Logically the transfer operation should be performed when seven serial bits that have arrived include the two signaling bits. If the shift register is so arranged that the arrival of the last bit, which is the second signaling bit, performs shifting of the bits already received, a race condition may result. The transfer may be attempted too soon and an ambiguous situation will result. This may be overcome by circuitry that behaves like a delay line. The signal generated by the presence of both signaling bits would be delayed long enough to assure that all the information bits have assumed their final position.

Delay circuits, however, usually involve external reactive elements. For this reason, a different approach is used in the peripheral decoder. The shift register is rearranged in such a way that after the sixth bit is received the shifting of the first six cells is inhibited (Fig. 14). The first signaling bit and all the information bits have assumed their final positions well before the expected arrival of the second signaling bit. When the last bit finally arrives it generates a pulse on the ONE side of the input circuit. This pulse is logically combined with the states of the sixth and seventh cells of the shift register. If both states are also ONE, a transfer signal is generated. The shifting between cells six and seven is never inhibited; therefore, a ONE is shifted from cell six into cell seven by the second signaling bit. This produces a properly delayed reset signal after the transfer is completed.

A reset signal for the first six cells should not be generated until the transfer signal disappears. This, again, could be accomplished by a delay circuit. Instead, certain properties of the basic shift register cell are utilized to perform a safe reset without using delay circuits. The advance or shift of information into a cell takes place when and only when the toggle input goes from a positive potential to ground. No shifting takes place on the opposite transition. The toggle input of the eighth cell is inverted so that information is shifted into it when the advance pulse disappears. Thus, the disappearance of the last signaling bit, which produced the transfer signal, shifts a ONE into the eighth cell. The cell in turn applies a reset signal on the first six cells and restores them to the ZERO state. The shift register is now ready to receive the next bit stream. The first bit in the next stream will restore cells seven and eight to ZERO and remove the reset signal.

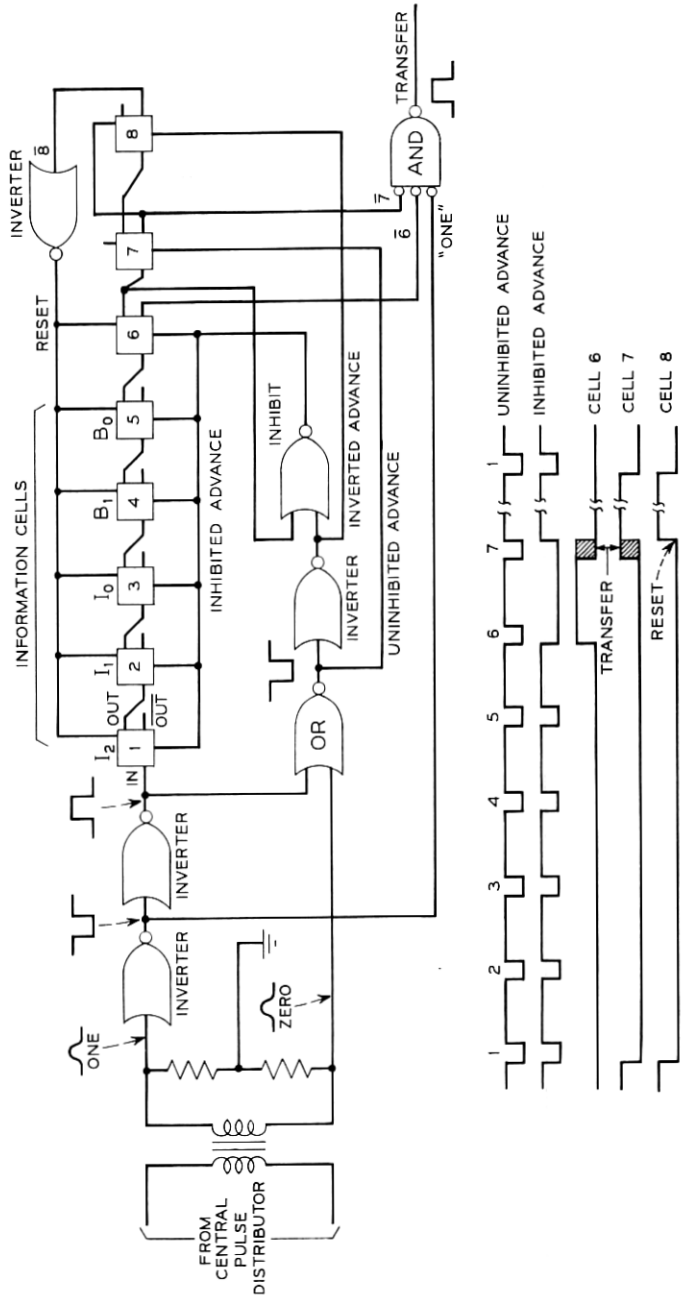


Fig. 14 — Peripheral decoder shift register showing generation of transfer and reset.

4.2.2 *Gated Flip-Flop*

Basically any type of gated flip-flop can be used in the memory matrix for the four three-bit buffers. The gating requirements are such that a flip-flop should be affected only when the proper binary combination exists in the B0 and B1 cells of the shift register and the transfer pulse is present. Whenever the above conditions are satisfied, the flip-flop must assume a state indicated by one of the three information cells.

A decoupling buffer is included to drive a relay driver transistor directly. The two stage buffering that results also helps to attenuate the electrical noise that is coupled into the peripheral decoder from the trunk and junctor circuits.

4.2.3 *Protection Against Noisy Environment*

Peripheral decoders operating relays in trunk and junctor circuits are exposed to severe electrical noise. The noise is generated whenever talking current that is fed to the subscriber through an inductor, is interrupted at or near the trunk or junctor circuit. This noise enters the peripheral decoder via the output leads which by necessity are near the tip and ring. If the noise is not blocked, it may change the state of either the buffer flip-flops or the shift register cells. This, of course, would result in erroneous operations. The problem is complicated by the fact that the noise levels generated on the tip and ring and the noise margins of the integrated circuits are several orders of magnitude apart.

The noise observable on the output leads may be several hundred volts in amplitude and of either polarity. Positive going noise is clamped by the relay coil protection diode, whereas negative going noise will tend to reverse the collector junctions of the buffers and enter the buffer flip-flop. A series diode in the output lead blocks negative going noise except for that part which, because of an extremely sharp wavefront, enters through the diode capacitance. A shunt capacitor of a value sufficiently higher than that of the diode provides the required attenuation.

4.2.4 *Low Voltage Supply*

Most integrated circuits today are designed for low voltage operation. Low supply voltage reduces power dissipation on the chip and permits faster switching times. In a telephone office the lowest voltage provided by the battery plant is +24 volts. The simplest way to ob-

tain low voltage from 24 volts is to use a dropping resistor and a regulating diode.

Unfortunately, the current required by the integrated circuits on a peripheral decoder is such that 9 watts may be dissipated on each circuit unit if a dropping resistor is used. The heat generated by this power far exceeds the allowable level. For this reason a dc to dc converter is provided on each peripheral decoder. The converter reduces the total power dissipated on the printed wiring board to less than 2 watts. It also keeps the integrated circuit supply voltage within the specified limits when the battery voltage drops because of commercial power failure. The integrated circuitry of the peripheral decoder together with the discrete component dc converter and noise filters, is mounted on a standard ESS printed wiring board.*

V. TRUNK AND SERVICE CIRCUITS

5.1 *Introduction*

The advent of stored program control in telephone switching systems has presented unique opportunities for simplifying and reducing size and cost of trunk and service circuits. Functions such as memory, timing, and logic previously performed by electromechanical relays have been taken over by software, with trunk circuits retaining only the most essential transmission related components. The concurrent development of fast switching networks has permitted the rapid connection of service circuits to customer lines and trunks for applying various tones and receiving or transmitting signals that were previously handled either autonomously by trunks or by common control circuits.

As a result of these developments, we have witnessed the fragmentation of large common control circuits of older switching systems into smaller, more specialized service circuits which are used more efficiently by the system. The trunk and service circuits of the No 2 ESS have, in general, followed this basic philosophy. In some cases, minimal hardware tradeoffs were made to avoid complex programs for time consuming system operations.

5.1.1 *General*

The relationship of junctors, junctor circuits, trunk circuits, and service circuits to the switching network and to the scanners and peripheral decoders is shown in Fig. 15.

* Additional equipment information on the peripheral decoder is contained in this issue in Ref. 4.

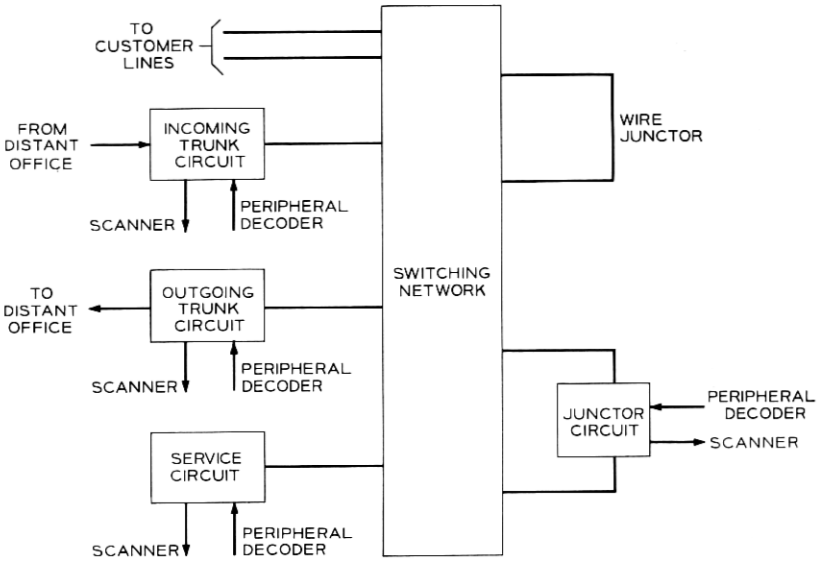


Fig. 15 -- Relationship of trunks, junctors and service circuits to switching network.

Customer lines, trunk circuits, and service circuits appear on one side of the network and wire and circuit junctors appear on the other. In general, circuit junctors are used in talking connections between customer lines of the same office, and in all other connections wire junctors are used. Trunk circuits terminate or originate transmission facilities from or to other offices. These circuits can be connected to each other or to customer lines through the network and wire junctors to establish telephone connections. Junctor and trunk circuits provide through transmission, talking battery voltage to customers, and means for receiving or transmitting call status signals (supervision).

To establish telephone connections a considerable amount of data is received from or transmitted to humans or machines. Service circuits are associated with customer lines and trunks for these functions.

Junctor, trunk, and service circuits receive control information from central pulse distributors via peripheral decoders and transmit call status information to the system processor via the various scanners. These circuits are switched in and out of a call under the control of the stored program as required by the progress of the particular type of call being handled. The points of supervision of a call reside in these circuits, passing from one to another as the call progresses. As examples, supervision is transferred from the calling line's line

ferrod to a ferrod in the customer dial pulse receiver when the dialing connection is established. In an intraoffice call supervision during talking is performed at the circuit junctor for both calling and called line.

5.1.2 *Basic Characteristics of Trunk and Service Circuits*

The basic switching design philosophy and transmission configuration of No. 2 ESS trunk and service circuits has followed the standards established by similar No. 1 ESS circuits.[7] The major circuit departure has been in the use of ordinary wire-spring relays rather than magnetic latching ones for trunk and service circuit control. These relays are controlled, as described in Section 4.1 directly by the central processor through peripheral decoders rather than signal distributors. In another departure, audible ringing tone is applied via junctor circuits and incoming trunk circuits. This eliminates a network connection to a tone circuit and the reservation of a network path. Significant processor real time is saved.

Regarding physical design, a new universal trunk and junctor frame has been designed that accepts junctor circuits, incoming and outgoing trunk circuits as well as operator trunk circuits. These circuits are permanently wired to 2-inch mounting plates. Each plate requires access to one peripheral decoder for relay control, and to eight ferrod sensors for scanner functions.

Tone circuits in No. 2 ESS are simplified and treated as lines. They respond to a connect signal from the circuit junctor or trunk circuit by connecting the assigned tone and restoring to normal when this connect signal is removed.

The power cross test made to customer lines prior to connecting sensitive service circuits to them is made a function of the network in No. 2 ESS. This permits not only savings from centralizing this function, but a substantial simplification of the service circuits that previously included such a test.

No. 2 ESS peripheral circuits have also been designed to permit operation with long customer loops using Uniguage design and to give coin lines dial tone before coin deposit for dialing the new universal emergency code (911), as well as emergency, ordinary assistance, information, and toll calls to operators.

5.2 *Trunk Circuits*

"Trunk circuits" are those control circuits that associate the switching network terminals with the transmission facility. In addi-

tion to voice frequency transmission elements, they contain means for transmitting and receiving call status signals (supervision) from or to other offices. "Trunks," on the other hand, are the entire channels from the switching network terminals of one office to the switching network terminals of another. They include trunk circuits, signaling equipment, transmission equipment as well as physical wires or carrier channels from one office to another.

Trunk circuits are classified in many ways. Considering methods of supervision, we have: loop (dc), reverse battery, high-low and E&M lead types. Considering signaling (address) language, we have: multifrequency and dial pulse types. And finally, considering direction of control, we have: one-way, which can be either incoming or outgoing; and two-way, which can be controlled from either connecting office.

The ESS trunk circuit philosophy of simplification and assignment of many of their functions to program control or service circuits has resulted in a significant reduction in the number of different types of trunk circuits needed in each office.

Trunk circuits can be divided into three categories; those to (*i*) central offices, (*ii*) switchboards, and (*iii*) test and repair desks.

A special case of the first category is a circuit connecting two customers of the same central office. This circuit is known as a junctor circuit because of its location in the center of the network fabric. It is to be distinguished from a junctor (wire junctor) which is similarly located but used in all other types of connections.

5.2.1 *Junctor Circuit*

Figure 16 illustrates the junctor circuit. The circuit is controlled by three relays making possible eight circuit states which are illustrated in Figure 17.

With all three relays released (BYPASS) the circuit reduces to two metallic paths connecting the two associated network terminals. Since this is exactly the form of the wire junctor, this circuit can be used as such at times when an idle wire junctor between two networks is not available.

With relays A and B operated (TALK) the circuit permits the two local customers connected via the network to its terminals to carry on a conversation. Talking battery voltage is fed to the customers' sets through ferrod sensors which are used to monitor their switchhook status. To prevent the shunting of the ac talking signal by the

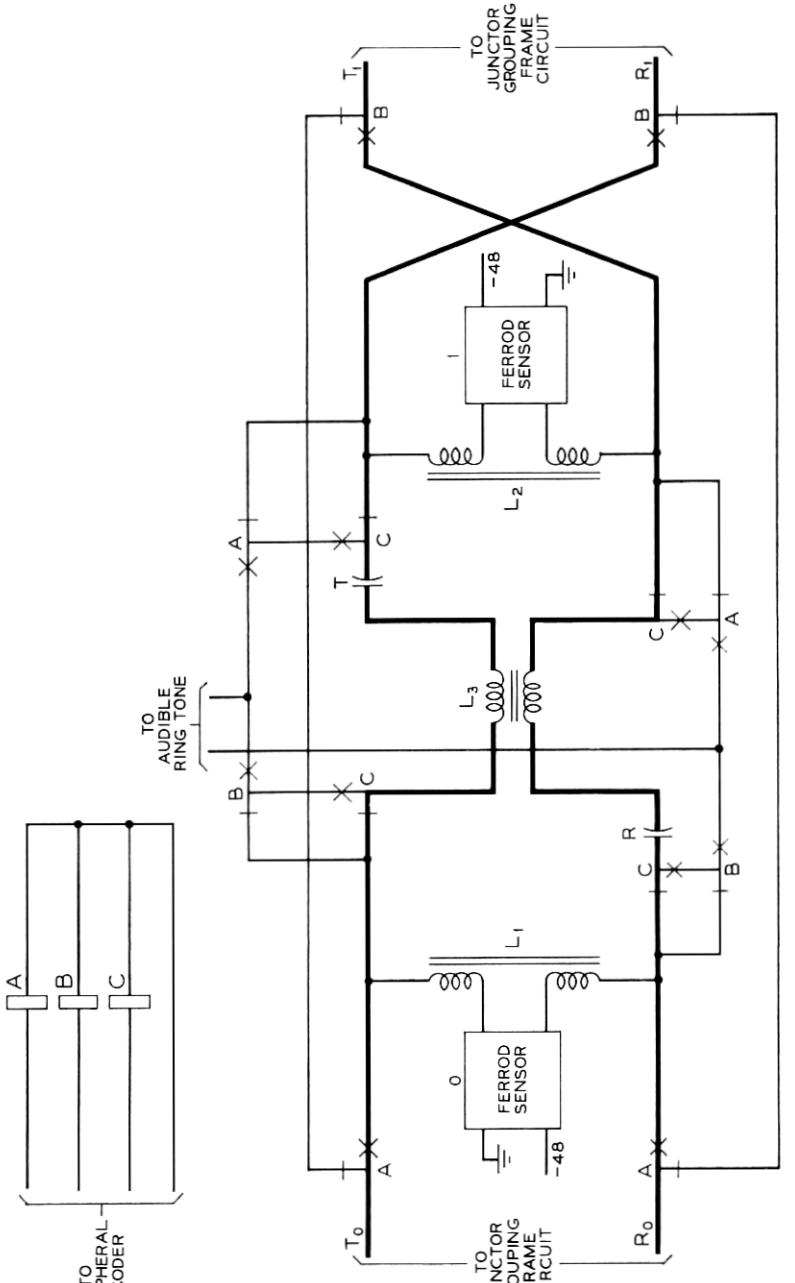


Fig. 16 — Junctor circuit.

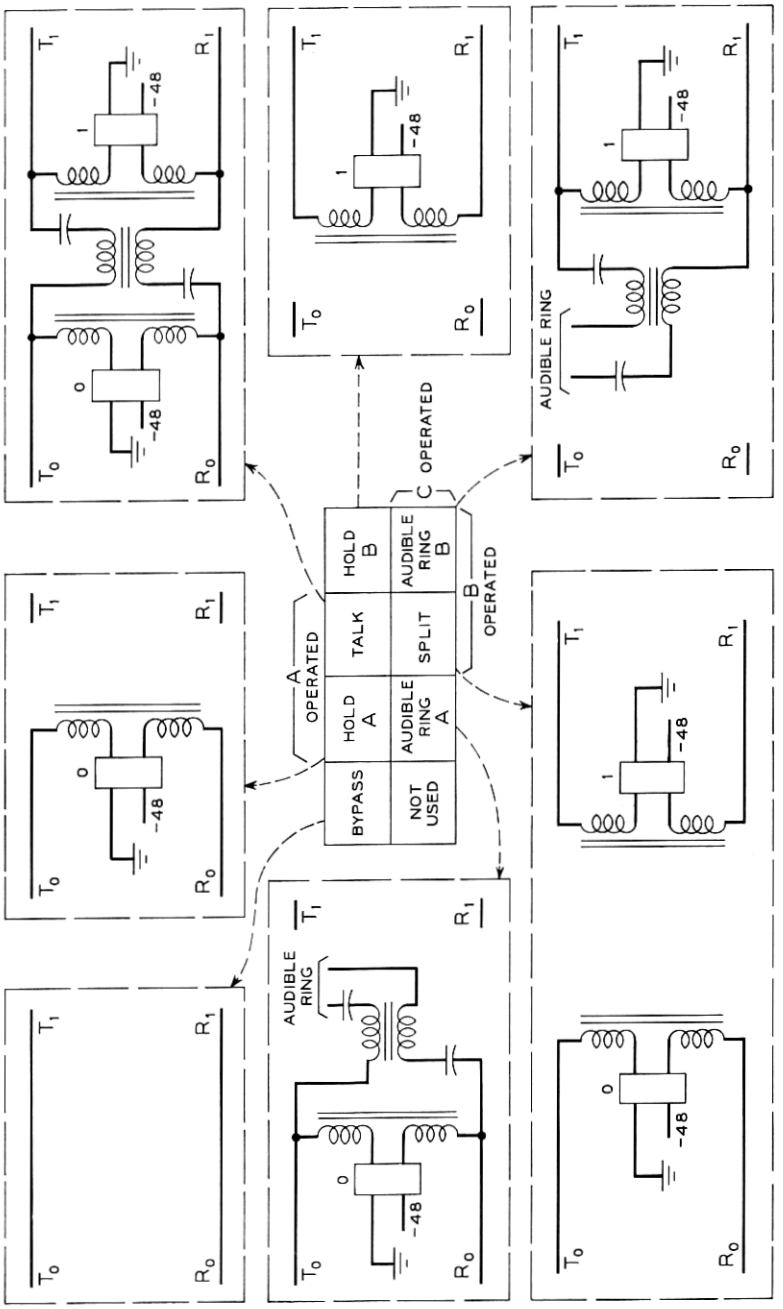


Fig. 17 — Possible junctor circuit states.

low impedance battery and ferrod sensors, series battery feed inductors are used.

With relay A or B operated (HOLD A or HOLD B) the circuit provides switchhook monitoring of either the customer connected to terminal A or the one connected to terminal B. This is an intermediate state in the processing of a call. The calling customer has finished his dialing and is waiting for the system to alert the called customer.

With relays A and C or B and C operated (AUDIBLE RING A or AUDIBLE RING B) the circuit provides switchhook supervision and audible ring tone to the calling customer. The junctor circuit is placed in this state when alerting of the called customer begins. Finally, with all three relays operated, the circuit provides for switchhook supervision of both customers connected to its terminals without permitting a talking path between them. This state is used, in some cases, when processing custom calling service calls.

5.2.2 *Outgoing Trunk Circuit*

Figure 18 illustrates the outgoing trunk circuit used with loop (dc) type supervision. This circuit together with the similar incoming trunk is the most commonly used circuit and great efforts were made to keep it simple. Connect and disconnect signals are transmitted to the distant office by closing or opening the dc "loop" toward it. This is accomplished by inserting in series with the outgoing terminals a low resistance ferrod sensor. This low resistance circuit causes current to flow, thus signaling the distant office. The distant office, in turn, responds by reversing the battery of the circuit. This is detected by the ferrod sensor since the associated diodes will permit current to flow through its windings. Three relays are used to control this circuit which assumes eight different states under program control. Figure 19 illustrates these states.

With no relay operated (IDLE) the circuit is open toward the network and offers an ac termination to the transmission facility (idle circuit termination). With C relay operated (BYPASS) the circuit is "bypassed"; that is, the transmission and supervisory elements are disconnected and the circuit reduces to two metallic paths. In this state, the circuit permits the direct association with the transmission facility, of an address transmitting circuit of a language (dial pulse or multifrequency) understandable by the distant office.

With B relay operated (HOLD) the circuit maintains a connect signal to the distant office while the address transmitter (which initiated this signal) is disconnected.

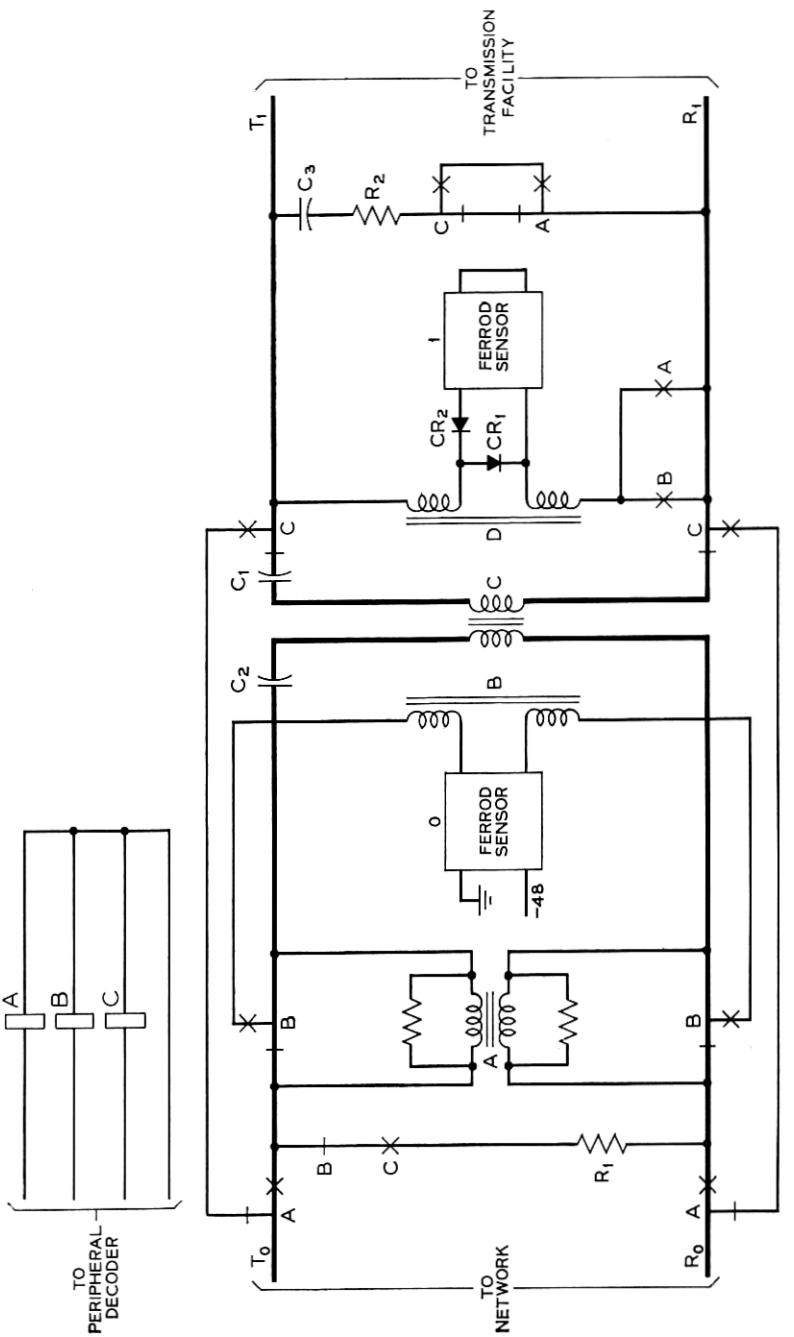


Fig. 18—Outgoing trunk circuit.

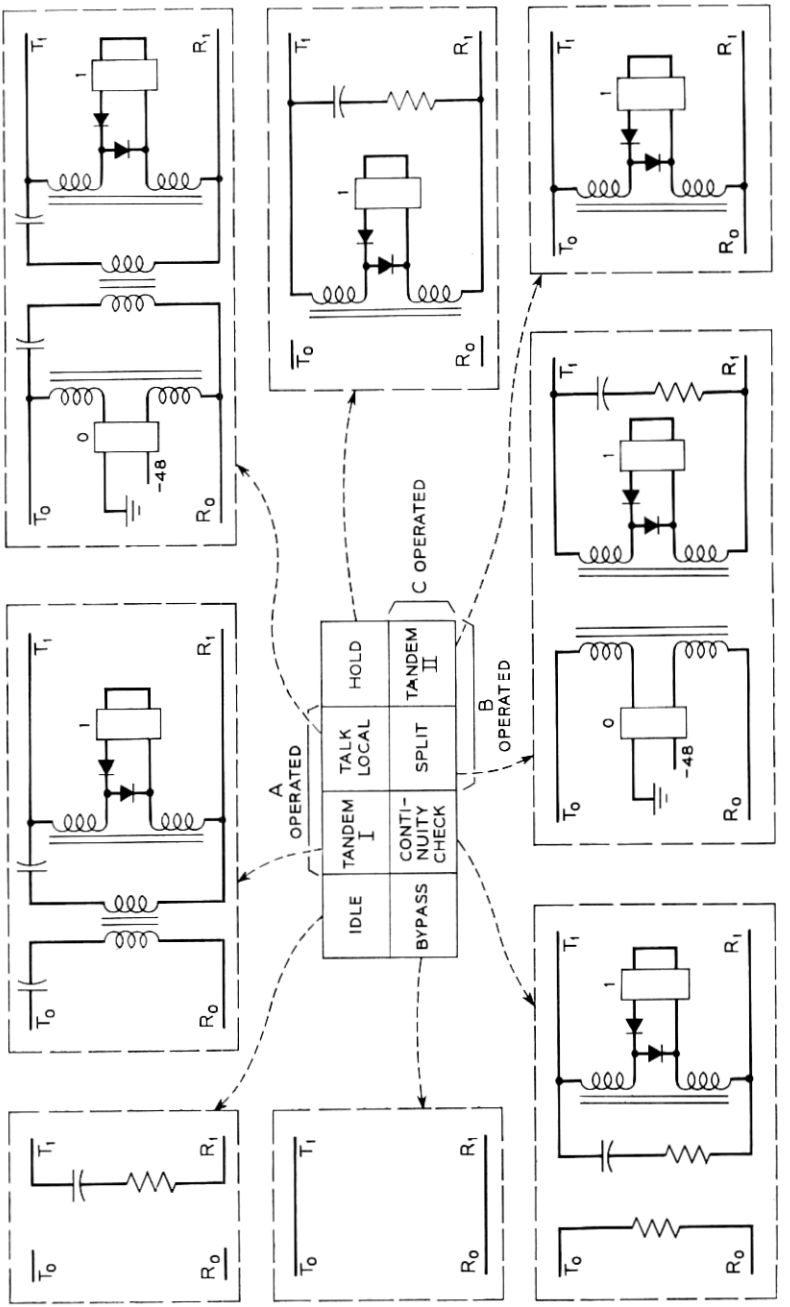


Fig. 19 — Possible outgoing trunk circuit states.

With relays A and B operated (TK LOC) the circuit provides for a local customer to talk to one in a distant office. Talking battery voltage is supplied to the local customer, and ferrod sensor scan points are connected to both parties for supervision.

When both the calling and called customers are in different distant offices and this third office is used as a tandem point, the respective offices are supervised by the ferrod sensors of the associated trunk circuits, the calling office at the incoming trunk circuit and the called office at the outgoing trunk circuit. Ferrod sensors used for local customers are not needed and are disconnected to improve transmission. Two talking states are provided for such calls, TDM I (A relay operated) and TDM II (B and C relays operated). The latter is used with operator incoming trunk circuits, which provide the transmission transformer and the former with incoming trunk circuits from other local offices.

Because in tandem states direct current does not flow through the network path, the integrity of the network path is checked by placing the incoming circuit in a local talking state and the outgoing in the CONT CHECK state. In this state a resistor is placed across the network terminals of the outgoing circuit causing current to flow through the ferrod sensor of the incoming circuit.

One final state, used in special applications, is the SPLIT state (all relays operated). In this state the circuit can supply talking battery voltage to a local customer and supervise both local and distant customers without permitting a conversation between them.

5.2.3 *Incoming Trunk Circuit*

Figure 20 illustrates an incoming trunk circuit of the loop (dc) type. This circuit can be thought of as the connecting circuit at the distant ESS office working with the outgoing trunk circuit just described. Again, three relays are used to control the circuit and two ferrod sensors are used to pass call status signals to the processor. Figure 21 illustrates the eight possible states of this circuit.

With no relays operated (IDLE) the circuit presents an idle circuit termination to the transmission facility while a low resistance ferrod sensor monitors for a connect signal from the distant office.

With the A relay operated (BYPASS) the transmission facility is bypassed to an appropriate digit receiver connected through the network.

With C relay operated (AUDIBLE RING) audible ring tone is returned to the distant office while the called local customer is alerted.

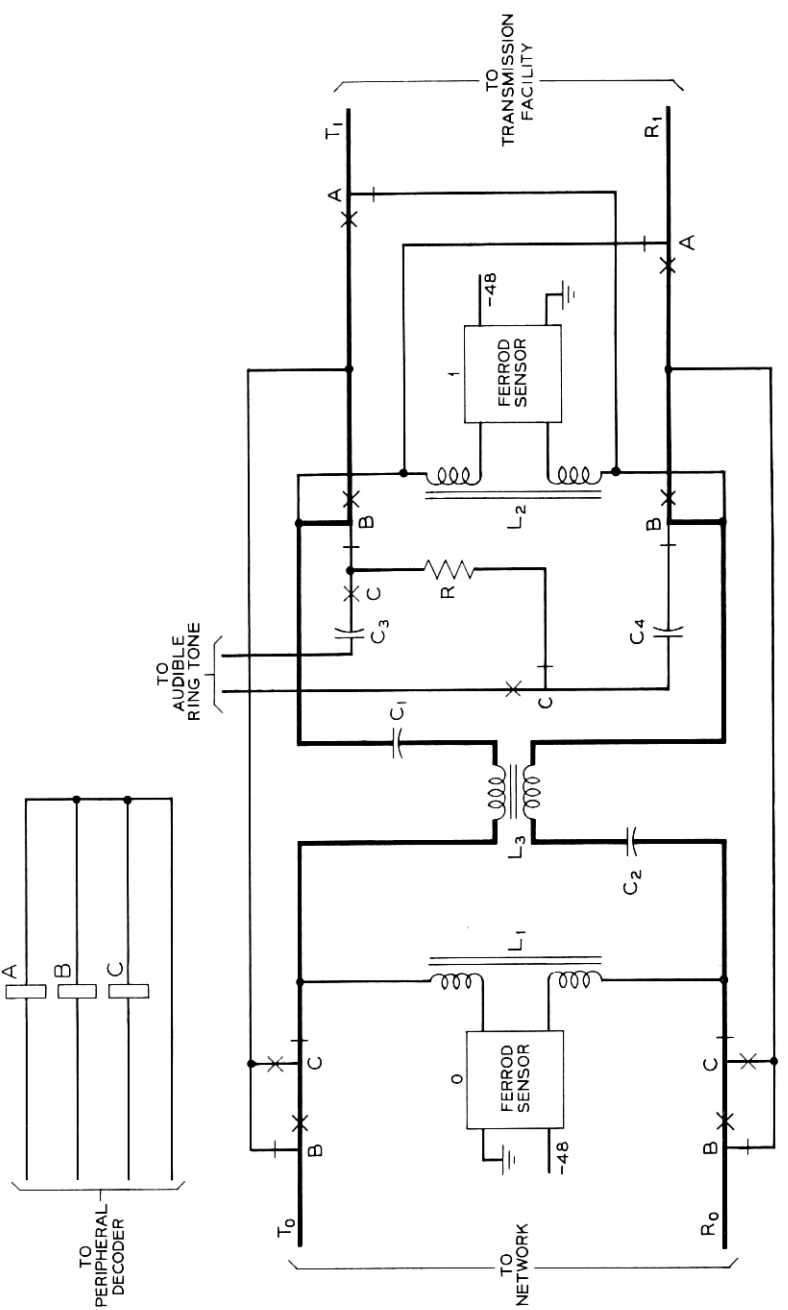


Fig. 20 — Incoming trunk circuit.

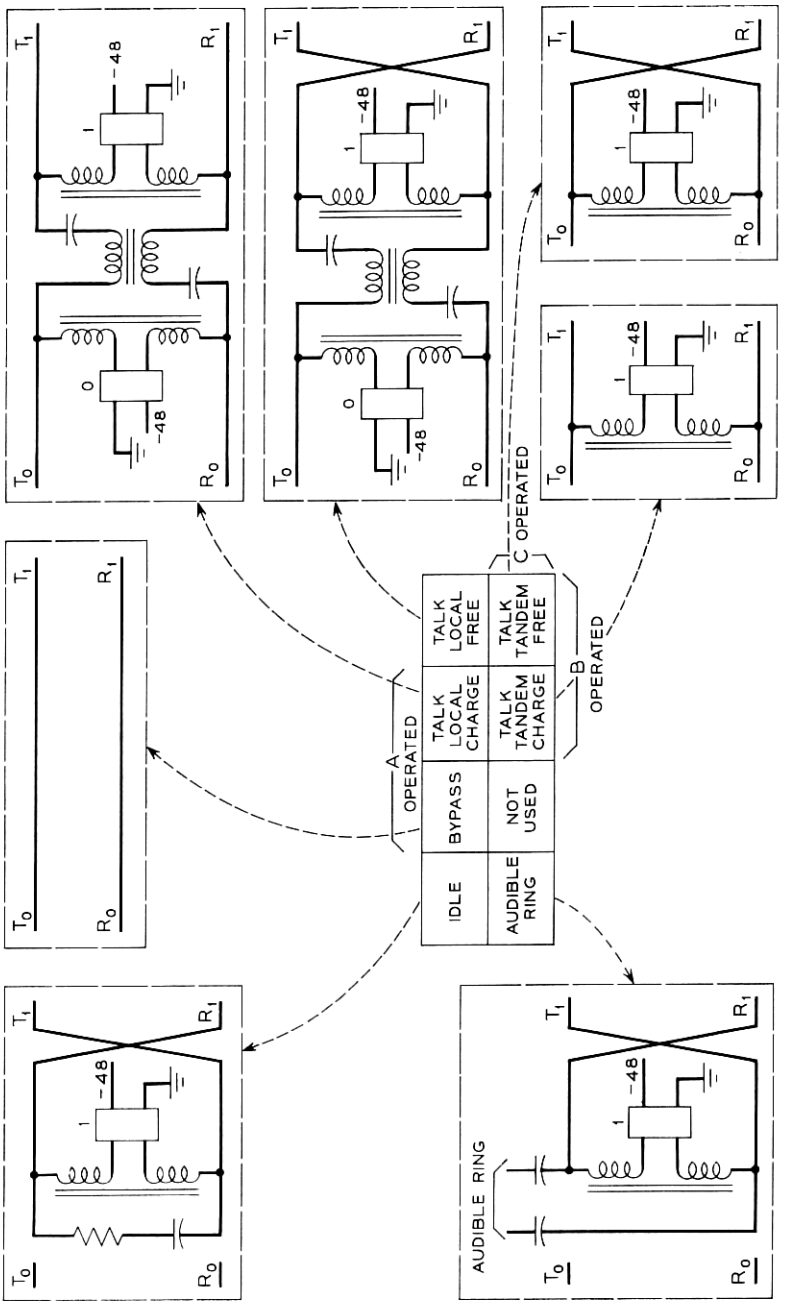


Fig. 21 — Possible incoming trunk circuit states.

When the called customer answers, the circuit is switched to the TALK LOCAL CHARGE state (A and B relays operated) if the call is to be charged or to the TALK LOCAL FREE if the call is free, such as a call to the telephone company business office.

The circuit provides two tandem states for calls to be routed to another office. TDM CHARGE (all relay operated) and TDM FREE (B and C relays operated) are used depending on charge information as just described.

5.2.4 *Other Trunk Circuits*

A number of small variations of the above circuits have been developed for use with offices of special character. Step-by-step offices, for instance, can transmit digit information immediately after sending the connect signal without waiting for a confirmation signal that a digit receiver is available. In such incoming trunk circuits a relay is provided in place of a ferrod sensor to receive and shape the dial pulses before passing them to the input-output logic.

Another variation is an outgoing trunk circuit to centralized automatic message accounting offices where monitoring of the transmission facility is required at all times regardless of whether a connect signal has been transmitted. Circuits have also been developed for transmission facilities using separate leads for supervisory signals (E&M leads). For connecting to switchboard operators both inband and dc signaling circuits have been developed.

5.3 *Service Circuits*

Service circuits are used to perform specialized functions such as digit reception and transmission, alerting, informing, coin control, and others. These circuits appear on terminals of the switching network, as shown on Fig. 15, which they use for access to lines and trunk circuits. Service circuits, like trunk circuits, communicate with the system control via scan points and peripheral decoders. Their holding time is generally less than that of trunk circuits and their use is primarily confined to the setup period of a call.

5.3.1 *Digit Receiving Circuits*

Address information, in the form of coded decimal digits can be received from either local customers or other central offices. Because of differences in codes and signaling methods, different digit receiving circuits are used in each case.

5.3.1.1 *Digit Receiving from Local Customers.* Local customers send address information either by means of dial pulses (generated by a rotary dial opening and closing a dc loop) or by *Touch-Tone*® telephone frequency tones. Because a local customer may have telephones of both types, the central office must be prepared to receive either type of pulsing. Two circuits, a customer dial pulse receiver circuit and a *Touch-Tone*® calling detector are associated with a customer line for this purpose. The former receives dial pulses and contains all the control features as well as facilities for dial tone and party testing. The latter is strictly an ac transistorized receiver with its input connected across the input of the customer dial pulse receiver.

5.3.1.2 *Digit Receiving from Other Offices.* Address information from other offices is received in the form of either a 2-out-of-6 multifrequency code or in dial pulses. It is not anticipated that the No. 2 ESS office will work with panel or other older design offices requiring facilities for reception of revertive or panel call indicator codes.

Multifrequency

The preferred method for sending digit information in modern telephone practice is by means of voice frequency tones coded to represent decimal digits on a 2-out-of-6 code (multifrequency pulsing). The distant office transmits a connect signal and the receiving office responds by connecting the incoming trunk circuit to a multifrequency receiver circuit which then signals the distant office that it is ready to receive the digit bearing MF pulses. The multifrequency receiver circuit is a transistor circuit with frequency discriminating ability which passes the digit information to ferrod sensor scan points. The central processor, by scanning these points, determines the digits sent which are then stored in the call store.

Dial Pulse

There are two types of dial pulsing that can be received by the No. 2 ESS office; pulsing from offices that use register type circuits which wait for a start signal before outpulsing and offices that are directly controlled by customer dials which do not wait for a start pulse but outpulse immediately following the transmission of a connect signal.

Pulsing from offices requiring a start pulsing signal is received in a simple relay service circuit called "trunk dial pulse receiver circuit." This is connected to the trunk circuit via the switching network in a manner similar to that used for multifrequency pulsing.

Dial pulsing, with no start pulsing signal, is received, primarily,

from nonregister type step-by-step offices. The office transmits a connect signal to the No. 2 ESS office and directs to it customer dialing. Part of the interdigital interval preceeding the first digit sent to the No. 2 ESS is used up at the step-by-step office in selecting a trunk to the No. 2 ESS office. Depending on traffic conditions, the balance of interdigital time left for the No. 2 ESS to select a receiver circuit is hardly sufficient. For this reason, pulsing of this type is received at the trunk circuit where pulses are collected by the system via scan points. A circuit similar to the loop incoming trunk circuit is used except that a special relay is used to receive the pulses. Because the input-output wired logic of the No. 2 ESS can scan for dial pulses at a nominal 10 millisecond rate, there is no need for special pulse stretching circuits.

5.3.2 *Digit Transmitting*

The problem of digit transmission is, of course, the inverse of the one just described. Address information is transmitted in coded decimal digits to other offices in the form of multifrequency pulses and dial pulses.

5.3.2.1 *Multifrequency Digit Transmission.* As described in Section 5.3.1.2, the most common method of digit transmission between central offices is by means of the 2-out-of-6 multifrequency code. Multifrequency pulsing is used with No. 5 crossbar, crossbar tandem, and No. 1 ESS offices. No. 2 ESS uses a service circuit that is connected to the transmission facility through the switching network and the trunk circuit. The trunk circuit is previously set at the "bypass" state which permits exchange of dc supervisory signals between the multifrequency transmitter circuit and the distant office. The absence of series and shunt circuit elements from the trunk circuit, when set at the bypass state, prevents any degradation or attenuation of multifrequency pulses.

The multifrequency transmitter circuit contains the necessary oscillators for generating the voice frequency signals which are keyed by relays under system control. This circuit also includes peripheral decoder controlled relays that transmit connect signals to distant offices as well as connections to the scanner circuit for receiving start pulsing signals.

5.3.2.2 *Dial Pulse Transmission.* Dial pulse digit transmission is used with step-by-step offices. Unlike the dial pulse sending circuits of crossbar systems which use self-contained pulse generating circuits, or

No. 1 ESS in which the central control signals the beginning and end of each dial pulse to each transmitter, No. 2 ESS dial pulse transmitters connect to a pair of duplicated common buses for dial pulse timing. Each pair of buses provides a source of two accurate timing signals. Signals on one bus indicate the beginning and signals on the other bus indicate the end of each dial pulse interval. These signals are gated into the transmitters by peripheral decoders for the time interval necessary to send each digit. This method minimizes pulse generating circuitry and program since only the beginning and end of each digit must be signaled to the transmitter.

5.3.3 *Alerting and Informing Circuits*

Alerting and informing circuits are used to permit communication between man and machine. In the first category we include ringing circuits which alert a customer to an incoming call; and in the second, various tone and announcement circuits which inform the customer about the progress of his call.

5.3.3.1 *Ringing Circuits.* Ringing circuits are used to apply a 20 Hz ac signal superimposed on −48 volt dc central office battery. The ac voltage is used to ring the bell in the customer's telephone which is bridged across the line with a series capacitor. The central office battery is used to energize a relay in the ringing circuit when the customer answers. This relay when operated disconnects (trips) ringing from the customer's line and causes the connection of a supervisory scan point to it. The connection of the ringing circuit is then removed and that between calling and called customers is established through the network.

Two ringing circuits have been developed for No. 2 ESS. One, used with most lines, alerts single and two party lines as well as PBXs while the other rings four and eight party lines. The former connects to lines interrupted (2 seconds ON, 4 seconds OFF) ringing obtained from the ringing and tone frame. The latter is connected to a continuous ringing source at the ringing and tone frame, which it interrupts under peripheral decoder control to suit the needs of the various four and eight party, and rural lines.

5.3.3.2 *Tone and Announcement Circuits.* Tone circuits in No. 2 ESS are treated like customer lines by the program. The circuit consists of a relay bridged across a pair of network terminals which operates when a junctor circuit or a trunk circuit connects to it. This relay connects to these terminals the tone assigned to it which is obtained from the ringing and tone plant. Tones such as 60 ipm (interruptions per minute)

busy, 120 ipm overflow, and the "no such number" tone are normally supplied by these circuits.

For verbal announcements, two circuits have been developed that connect to the recorded announcement frame. One connects to the announcement immediately when seized, the other waits until the beginning of the announcement before connecting it to the customer.

5.3.4 *Coin Control and Applique Circuits*

Coin station functions in No. 2 ESS are performed only by the coin control circuit which is associated with the coin line via a switching network connection for the duration of such functions. The centralization of these functions in the coin control circuit has permitted a considerable simplification of trunk circuits as well as the elimination of the distinction between coin and noncoin types.

Applique circuits are used whenever specialized information must be given to or obtained from the central processor.

5.3.4.1 *Coin Control Circuit.* The coin control circuit is connected to a coin line momentarily to verify the presence of a coin, and to collect or to return a coin. The circuit is controlled by relays operated by the peripheral decoder circuit to apply the appropriate dc potentials to the coin line. Ferrod sensor scan points are used to monitor supervision as well as to verify coin presence and the flow of coin collect or return current.

5.3.4.2 *Applique Circuits.* There are three types of applique circuits. The peripheral decoder applique, the master scanner applique, and the interrupter applique circuits. The peripheral decoder applique circuit consists of a single relay controlled by the system through the peripheral decoder. The contacts of this relay are used to light lamps or to control other functions not normally performed by a specific circuit. The master scanner applique circuit consists of a single resistor that converts relay operations to current suitable to ferrod sensor saturation at the master scanner circuit. These signals are from various types of monitoring devices at the central office such as alarming key operations. The interrupter applique circuit supplies 60 and 120 interruptions per minute contact closures to various circuits for busy or overflow indications.

5.4 *Test Circuits*

Line, trunk, and service circuits are tested by specific test circuits that use the switching network for access. There are three basic hard-

ware entities that perform tests on trunk and service circuits: the trunk test circuit, the group of service test circuits, and the automatic line insulation test circuit. Tests may be initiated by call processing programs when faults are detected, routinely by the trunk test circuit's test programs, or by teletypewriter requests. Automatic line insulation tests may also be requested by the local test desk.

5.4.1 *Trunk Test Circuit*

The trunk test circuit is mounted on its own frame in the maintenance area of the office. It is a manually operated circuit and maintenance craftsmen can obtain access to any of the trunks or service circuits through three access trunks to the switching network. The following test facilities are part of this frame:

(*i*) The Transmission Test Circuit permits testing lines and trunks by special terminations and tones.

(*ii*) The voltmeter circuit permits various leakage resistance measurements between trunk conductors or between one conductor and ground. It is also possible to test for the presence of foreign potentials and qualitative capacitance measurements.

(*iii*) The state change control permits placing any trunk or service circuit in any of its possible circuit states through peripheral decoder actions.

(*iv*) Test control permits taking circuits in and out of service and monitoring trunk circuit E&M leads.

(*v*) The impulse counter permits noise measurements.

5.4.2 *Service Test Circuits*

For every service circuit in the No. 2 ESS office there is a corresponding test circuit. This test circuit uses the switching network for access and proceeds, under program control, to introduce various extreme conditions under which the circuit being tested is expected to perform. Following is a brief description of the various test circuits and the tests they perform.

Customer signaling is received by the customer dial pulse receiver and the *Touch-Tone*® calling detector circuits. To test these circuits, the system can connect them to a customer dial pulse receiver test circuit and a *Touch-Tone*® calling detector test circuit. The customer dial pulse receiver test circuit then transmits a series of marginal dial pulses to the customer dial pulse receiver being tested while the associated program checks its response by observing the digit receiving

circuitry of the input-output control. In addition, specialized functions such as dial tone transmission, toll diversion, and party test features are tested. The *Touch-Tone®* calling detector test circuit is similarly a precise *Touch-Tone®* telephone frequency transmitter that transmits a series of test digits designed to test the circuit performance at the extreme ends of each channel. In addition, checks are made for the rejection of signals slightly out of channel, presence of third frequencies, and proper timing response.

Multifrequency transmitters and receivers are tested by using one to test the other. Rather than connecting a pair of these circuits together directly through the network for this purpose, the connection is made through a third circuit, the multifrequency test environment circuit. This circuit has two appearances on the switching network, one for the transmitter and one for a receiver. A number of tests are performed on the service circuits by altering this artificial environment. One such test is the flat loss test where the pair of transmitted frequencies is considerably attenuated and the receiver is checked for response. In another test, the twist test, one of the frequencies is attenuated relative to the other and the receiver is checked. Tests are also made for double keying, for response to modulation products, and for proper timing.

The tone presence detector is a circuit that can detect audio frequency tones. It is used to test the output of the various tone and recorded announcement circuits as well as the performance of the conference circuits.

A common circuit tests both the coin control and the ringing circuits. The ringing and coin control test circuit simulates a customer station set or a coin set and under extreme conditions tests for application of ringing potentials, operation of the ring trip relay, as well as the application of coin test, coin collect and coin return potentials.

The proper operation of the ringer at the customer's set is checked by the station ringer test circuit. This circuit is connected at the request of a craftsman by dialing a special code usually at the time of installation of a set. Associated with this circuit a *Touch-Tone®* telephone station test circuit may be used for testing the accuracy of the *Touch-Tone®* telephone oscillators. As expected, this is a precise receiver tuned to the *Touch-Tone®* calling frequencies.

5.4.3 *Automatic Line Insulation Test Circuit*

The automatic line insulation test circuit is used to test customer lines for insulation defects. It applies a small voltage to the customer

line and measures the resulting current. It reports this to the system control via ferrod sensor scan points. There are three test modes for this circuit.

(*i*) Testing for leaks between tip and ring leads and between ring and ground. The first test usually indicates trouble in drop wire at the customer premises; the second, in open wire conductors.

(*ii*) Testing for leaks between tip and ground and from ring to ground. This test detects troubles in cable terminals.

(*iii*) Testing for leaks to battery from tip or ring leads. This test is used to detect defects in cable sheaths. Such defects permit leaks to battery on ring leads of other lines of the same cable because moisture is present.

Line insulation tests may be started automatically by the system at a predetermined time or by a testman at a local test desk.

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