Design of Efficient Broadband Variolossers

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This paper describes new variolosser circuits which are suitable for use in high quality broadband IF amplifiers operating at several hundred MHz, and offering substantial improvements in power consumption, temperature stability, bandshape stability, minimum attenuation and attenuation range. Three variolossers of this type are used in the automatic gain control for the IF amplifier used in the short hop radio system experiment.

We present an analysis, a design procedure, and extensive measurements. As an example of the performance to be expected, one experimental vario-loser has a minimum attenuation of 1.35 dB, a maximum attenuation of 19.5 dB, and is flat to ±0.15 dB over a 40 percent band centered at 300 MHz.

I. INTRODUCTION

The gain control of broadband high quality transistor IF amplifiers has been a difficult problem for many years. Control of gain by variation of bias on the gain stages causes severe bandshape distortion, so it is customary to use one or more semiconductor diode variolossers for this purpose. The use of a variolosser, which introduces a large attenuation to the signal, can impair the noise figure of the amplifier; for this reason several variolossers of limited range are imbedded between suitable gain stages to minimize the effect on the noise figure. Several types of variolossers have been used but all of them have one or more of the following disadvantages.

(*i*) Complicated circuitry, making adjustment difficult and thermal stability hard to achieve.

(*ii*) Large minimum loss, which requires additional gain stages and adds to the noise figure problem.

(*iii*) Large bias power.

(*iv*) Parasitic reactances degrading the performance at high frequencies.

For some applications, power efficiency, thermal stability, and size are important parameters. This is true, for example, of the short hop radio system which has a pole-mounted repeater operating from a primary power source.[1] The circuits described in this paper were designed for such applications.

The basic variolosser circuit is a double-tuned IF stage in which a PIN diode is inserted to provide variable attenuation. At frequencies of several hundred MHz the parasitic reactances of the diode are important; it is a feature of the circuit that the parasitics can be absorbed in a simple way to improve the performance of the variolosser. For example, for a given bandwidth and flatness requirement, the attenuation range is doubled in dB, (see Fig. 4).

Bandwidths of 50 percent, flat to a few tenths of a dB over an attenuation range of 20 dB have been achieved with these circuits.

II. ANALYSIS OF BASIC CIRCUIT

The basic variolosser circuit is shown in Fig. 1 without bias circuits. The loss of the double-tuned interstage circuit is controlled by a PIN diode as indicated in Fig. 1a. An equivalent circuit including the output impedance of the transistor Q1 and the input impedance of Q2 is shown in Fig. 1b; L_2 is the sum of L_s and the input inductance of Q2, R_2 is the input resistance of Q2 plus the resistance R_s, and R_1 is the parallel resistance combination of the PIN diode and the output
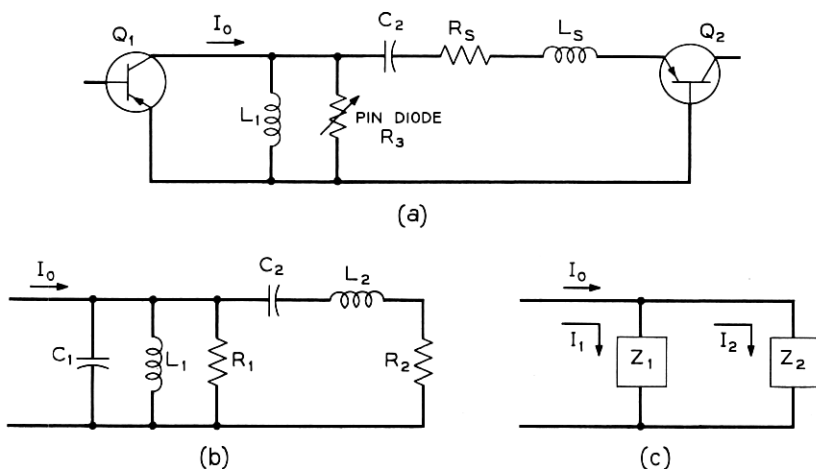

Fig. 1 — Basic interstage circuit.

resistance of Q1. The interstage has been further simplified in Fig. 1c where,

$$Z_2 = R_2 + j\left(\omega L_2 - \frac{1}{\omega C_2}\right), \tag{1}$$

$$Y_1 = G_1 + j\left(\omega C_1 - \frac{1}{\omega L_1}\right), \tag{2}$$

$$G_1 = \frac{1}{R_1}.$$

The design approach is to make the transfer function as flat as possible for a prescribed attenuation range and bandwidth. From Fig. 1c, the current transfer function is

$$\frac{I_2}{I_0} = \frac{1}{1 + Z_2 Y_1}. \tag{3}$$

After substituting (1) and (2) into (3), the transfer function can be written:

$$\left|\frac{I_2}{I_0}\right|^2 = \frac{1}{\left[A - B\gamma^2 - \dfrac{C}{\gamma^2}\right]^2 + \left[D\gamma - \dfrac{E}{\gamma}\right]^2} \tag{4}$$

where,

$$A = 1 + G_1 R_2 + \frac{L_2}{L_1} + \frac{C_1}{C_2},$$

$$B = \omega_0^2 C_1 L_2,$$

$$C = \frac{1}{\omega_0^2 L_1 C_2},$$

$$D = \omega_0 R_2 C_1 + \omega_0 G_1 L_2,$$

$$E = \frac{R_2}{\omega_0 L_1} + \frac{G_1}{\omega_0 C_2},$$

$$\gamma = \frac{\omega}{\omega_0}.$$

The transfer function is maximally flat when

$$B = C, \tag{5}$$

$$D = E, \tag{6}$$

and

$$D^2 = 2B(A - 2B). \tag{7}$$

From (5) and (6)

$$\omega_0^2 C_1 L_1 = \omega_0^2 C_2 L_2 = 1, \tag{8}$$

so the primary and secondary circuits both resonate at frequency $f_o = \omega_0/2\pi$.

Substituting (8) into (4), the transfer function is conveniently expressed as

$$\left| \frac{I_2}{I_0} \right|^2 = \frac{1}{(A - 2B - BF^2)^2 + (DF)^2}, \tag{9}$$

where $F = (\gamma - 1/\gamma) = (\omega/\omega_0 - \omega_0/\omega)$. Equation (9) can also be written in the form:

$$\left| \frac{I_2}{I_0} \right|^2 = \frac{1}{\left(1 + G_1 R_2 - \dfrac{C_1}{C_2} F^2\right)^2 + (\omega_0 R_2 C_1 + \omega_0 G_1 L_2)^2 F^2}. \tag{10}$$

The midband loss is given when $F = 0$

$$\left| \frac{I_2}{I_0} \right|^2_{F=0} = \frac{1}{(1 + G_1 R_2)^2}. \tag{11}$$

The attenuation of the circuit can be controlled by the choice of G_1 and R_2. As shown in Fig. 1, the PIN diode provides variation in G_1. Assuming that the parameters have been chosen for a maximally flat transmission for some particular G_1 and R_2, and that only G_1 or R_2 will be changed, then (10) gives the amplitude response as a function of G_1 and R_2.

If (7) is also satisfied, then the current transfer ratio will be maximally flat and (9) becomes

$$\left| \frac{I_2}{I_0} \right|^2 = \frac{1}{(A - 2B)^2 + B^2 F^4}. \tag{12}$$

Equation (12) also can be expressed in the form:

$$\left| \frac{I_2}{I_0} \right|^2 = \frac{1}{[1 + G_1 R_2]^2 + \left(\dfrac{C_1}{C_2}\right)^2 F^4}. \tag{13}$$

The midband loss of the interstage is determined when $F = 0$:

$$\left| \frac{I_2}{I_0} \right|^2_{F=0} = \frac{1}{[1 + G_1 R_2]^2}.$$ (14)

The midband loss expressed in dB is

$$L = 20 \log \left| \frac{I_2}{I_0} \right| = 20 \log \frac{1}{1 + G_1 R_2} \text{ in dB.}$$ (15)

2.1 Design Equations and Procedure

The value of $G_1 R_2$ can be determined by writing (15) in the following form and using the maximum value of attenuation, which the designer must choose.

$$R_2 G_{1_{max}} = \frac{1}{\log^{-1} \left(\dfrac{-L_{max}}{20} \right)} - 1.$$ (16)

The required value of R_2 can be determined by choosing a maximum value of G_1 from the PIN diode characteristic. Such a characteristic is shown in Fig. 2 for a Western Electric L-2480 PIN diode.

The minimum attenuation is determined by using R_2 and the minimum value of G_1. $G_{1_{min}}$ is the parallel combination of the PIN diode at zero bias, the output impedance of transistor $Q1$, and diode bias resistors. From (15) the minimum midband attenuation if given by

$$L = 20 \log \frac{1}{1 + G_{1_{min}} R_2}.$$ (17)

From (7), which must be satisfied to obtain a maximally flat transmission characteristic at the minimum loss point, we obtain

$$C_1 C_2 = \frac{1 \pm [1 - (R_2 G_{1_{min}})^2]^{\frac{1}{2}}}{\omega_0^2 R_2^2},$$ (18)

where $\omega_0 = (\omega_1 \omega_2)^{\frac{1}{2}}$, and ω_1 and ω_2 are the band edges. From (13) the response is down 3 dB when

$$F_{3\,dB} = \left[(1 + R_2 G_{1_{min}}) \frac{C_2}{C_1} \right]^{\frac{1}{2}}.$$ (19)

Letting this value of $F_{3dB} = \beta$ where

$$\beta = \frac{\omega_2 - \omega_1}{(\omega_2 \omega_1)^{\frac{1}{2}}} = \frac{\omega_2 - \omega_1}{\omega_0},$$
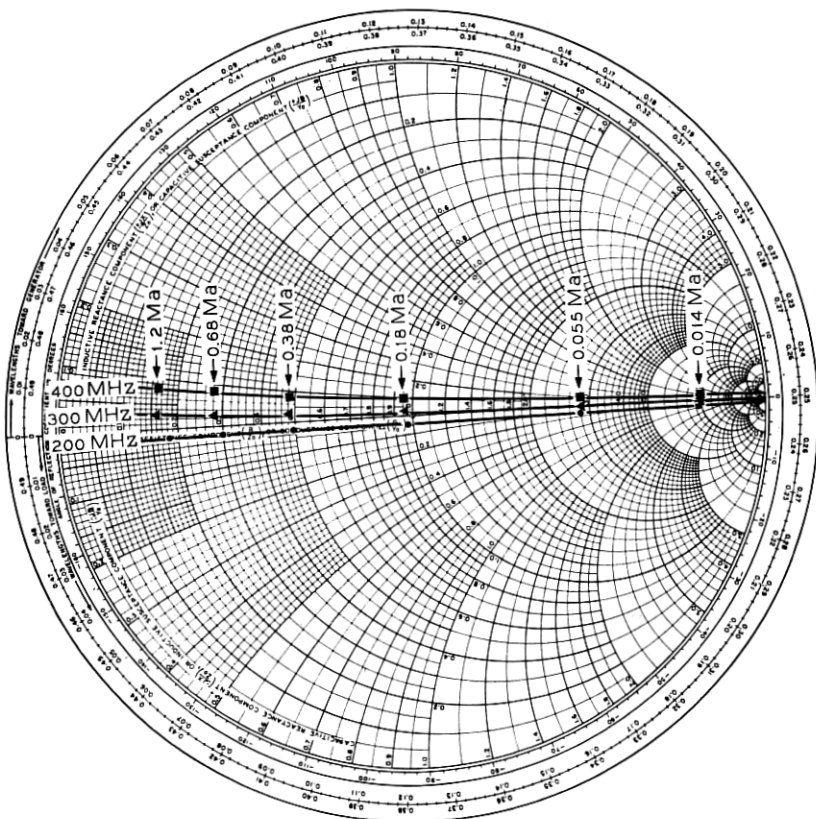
Fig. 2 — Impedance of W. E. 2480 PIN diode as a function of frequency and diode current.

yields

$$\beta = \left[(1 + R_2 G_{1\min}) \frac{C_2}{C_1} \right]^{\frac{1}{2}}. \tag{20}$$

From (8)

$$L_1 = \frac{1}{\omega_0^2 C_1} \tag{21}$$

and

$$L_2 = \frac{1}{\omega_0^2 C_2}. \tag{22}$$

2.2 PIN *Diode Characteristic*

The PIN diode used in this variolosser is a Western Electric L2480 diode.[2] The diode is essentially resistive over a wide frequency range and over a large range of diode currents as shown by the Smith chart plot of Fig. 2. This data shows the impedance of the diode at 200, 300, and 400 MHz as a function of the diode current. The data were obtained using the circuit shown schematically in Fig. 3a. The mechanical arrangement of the diode mounting with its bias circuit, as shown in Fig. 3b, consists of a cap, a clip, and a low inductance capacitor. This capacitor is chosen to resonate with the inductance of the diode and its mount at 300 MHz; the circuit has a Q of 0.3 when the diode has a resistance of 10 ohms.

2.3 *Design Example of a Common Base, Common Base Variolosser*

A variolosser operating in the 200 to 400 MHz band was designed as outlined in Section 2.1. The bandwidth was chosen narrow compared with the maximum bandwidth obtainable so that the variation in the band shape as a function of attenuation could be observed. The conditions were that:

(*i*) Attenuation of the interstage be 20 dB for a PIN diode current of 0.68 mA.

(*ii*) $\beta = 0.725$.

(*iii*) $f_o = 283$ MHz.

From the PIN diode characteristic of Fig. 2, the conductance at a diode current of 0.68 mA was found to be 0.0715 mhos. From (16), R_2 was computed to be 126 ohms. From the diode characteristic and interstage circuit, G_{min} was found to be 1.33 millimhos. Using (17), the minimum loss was computed to be 1.35 dB. From (18) and (20),
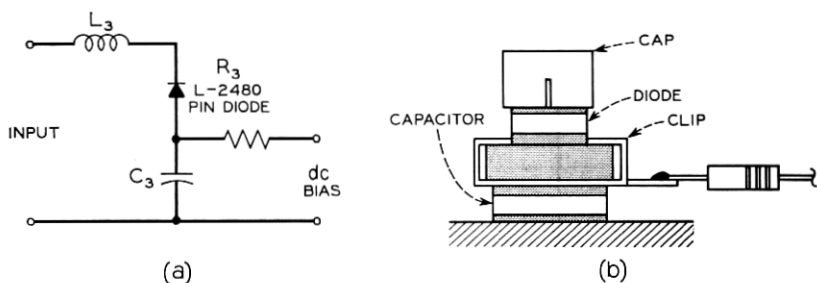

Fig. 3 — L-2480 PIN diode mounting.

the values of C_1 and C_2 required to satisfy the bandwidth and maximally flat transmission characteristic at the minimum loss point are

$$C_1 = 9.38 \text{ pF}, \qquad C_2 = 4.22 \text{ pF}.$$

From (21) and (22), $L_1 = 34$ nH, $L_2 = 75$ nH.

The computed frequency response of a variolosser using the above design values and equation (10) is shown by the dotted curves in Fig. 4. These data show the loss relative to the loss at ω_o for various interstage losses. Figure 4a shows the frequency response for an interstage loss of 1.35 dB which is the minimum loss. Figures 4b and 4c show the response for a loss of 9.5 and 19.5 dB, respectively. These figures show the undercoupled response that is obtained as G_1 is varied. It also shows that by designing for a 3 dB bandwidth large compared with the desired bandwidth, that the amplitude distortion over a given attenuation range can be small. This design provides 19.5
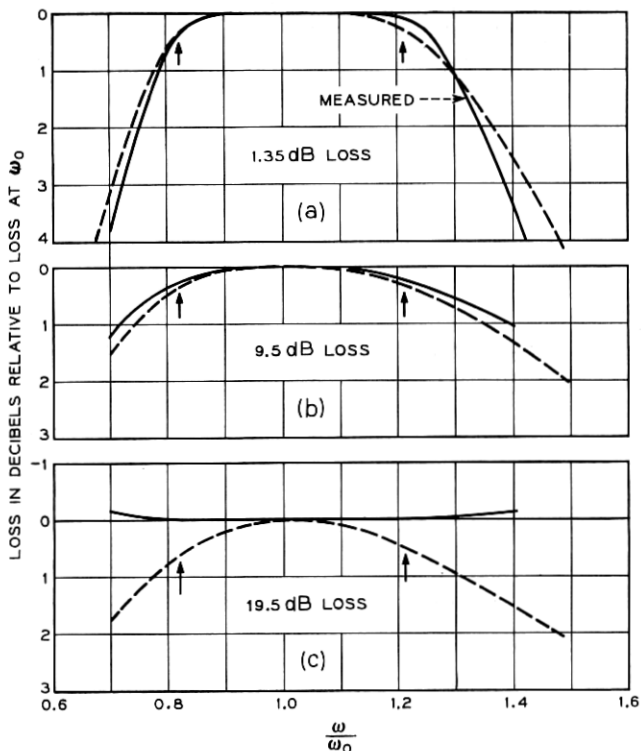

Fig. 4 — Common base, common base variolosser characteristics.

dB attenuation over a 30 percent band with a variation in amplitude of ±0.15 dB. This bandwidth can be increased by providing a compensating circuit as discussed in Section III.

III. ANALYSIS OF COMPENSATED CIRCUIT

Variolossers used to control the gain of an amplifier are usually operated near the maximum attenuation point and varied toward the minimum loss point. In this application it is desirable to have the frequency response flat near the maximum loss point. The addition of one inductor in series with the PIN diode allows the Q of this circuit to be chosen so that the impedance of this arm varies with frequency in the correct way to compensate the under-coupled characteristic of the double tuned circuit. As the interstage attenuation is decreased, the Q of the series resonant circuit is also decreased and thus the compensating circuit has little effect on the minimum loss point.

Figure 5a shows the interstage circuit with L_3 and C_3 in series with R_3 to form a series resonant circuit. This interstage has been simplified as shown in Fig. 5b. The current transfer function for the circuit in Fig. 5b is

$$\frac{I_2}{I_0} = \frac{Z_3}{(1 + y_1 Z_2)Z_3 + Z_2} \tag{23}$$

(a)

(b)

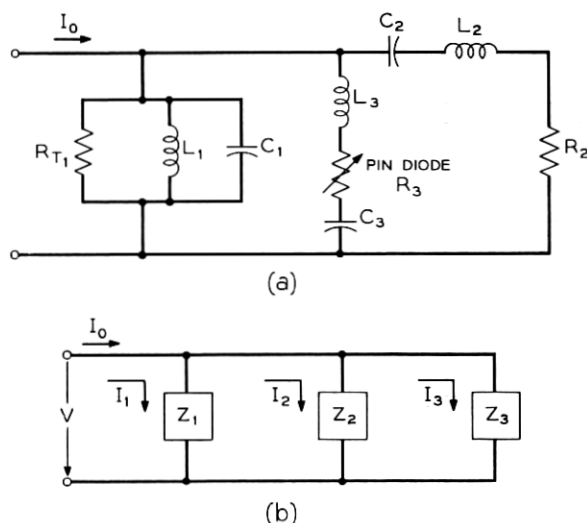Fig. 5 — Variolosser with compensating circuit Z_3.

where

$$y_1 = G_1 + j\left(\omega C_1 - \frac{1}{\omega L_1}\right), \qquad G_1 = \frac{1}{R_{T1}}, \tag{24}$$

$$Z_2 = R_2 + j\left(\omega L_2 - \frac{1}{\omega C_2}\right), \tag{25}$$

$$Z_3 = R_3 + j\left(\omega L_3 - \frac{1}{\omega C_3}\right). \tag{26}$$

The magnitude of the transfer function is

$$\left|\frac{I_2}{I_0}\right|^2 = \frac{1+(Q_3 F)^2}{\left[1+G_1 R_2 + \frac{R_2}{R_3} - \left(\frac{C_1}{C_2} + DQ_3\right)F^2\right]^2 + \left[\left(1+G_1 R_2 - \frac{C_1}{C_2}F^2\right)Q_3 + \frac{R_2}{R_3}Q_2 + D\right]^2 F^2} \tag{27}$$

where

$$G_1 = \frac{1}{R_{T1}}, \qquad Q_2 = \frac{1}{\omega_0 C_2 R_2}, \qquad Q_3 = \frac{1}{\omega_0 C_3 R_3},$$

$$D = \omega_0 G_1 L_2 + \omega_0 R_2 C_1.$$

The frequency characteristic of (27) will have a flat amplitude response over a wide band at the maximum loss point if Q_3 is properly chosen. As the loss is adjusted from maximum to minimum, the value of R_3 must increase and thus Q_3 decreases. At the minimum loss point Q_3 is very small and the amplitude response is the maximally flat interstage characteristic that was used as the design point.

The common base, common base variolosser described in Section 2.3, whose characteristic is shown by the dotted curves in Fig. 4, was compensated at the 19.5 dB loss point by setting Q_3 equal to 0.832. The results are shown by the solid curves in Figs. 4b and 4c, and the dotted curve in 4a which applies to both the compensated and uncompensated case. Over the 40 percent band indicated by the arrows, the compensated characteristic deviates ±0.15 dB from a flat transmission characteristic for a variolosser that has a minimum loss of 1.35 dB and a change in attenuation of 18 dB. The interstage characteristic is flat at the maximum loss point.

IV. COMPUTED AND EXPERIMENTAL RESULTS

4.1 *Measured Performance of a Common Base, Common Base Variolosser*

A common base, common base variolosser was constructed using the design values computed in Section 2.3. The measured characteristic, without compensation, is shown by the series of pictures, Figs. 6a, b,
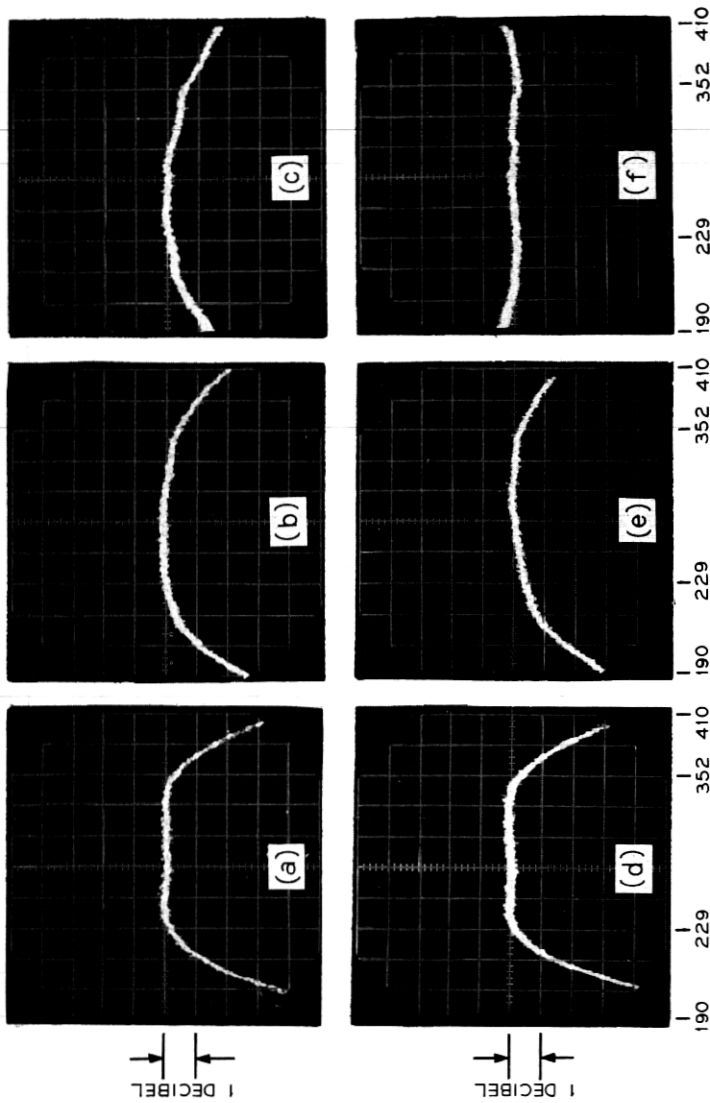
Fig. 6 — Frequency characteristic versus attenuation for 300 MHz common base-common base variolosser without compensation at attenuations of (a) 1.35 dB, (b) 9.5 dB, (c) 19.5, and with compensation at attenuations of (d) 1.35 dB, (e) 9.5 dB, and (f) 19.5 dB.

and c, for the minimum loss point, at an interstage loss of 9.5 dB, and at an interstage loss of 19.5 dB. The measured characteristic is also shown by the solid line in Fig. 4a at the minimum loss point. As described in Section III, the interstage was compensated to provide a flat transmission characteristic at the 19.5 dB loss point over the 229 to 352 MHz range. The effect of this compensation is shown by the series of pictures, Figs. 6d, e, and f. At 19.5 dB, the frequency characteristic is virtually flat over the 229 to 352 MHz range. At 9.5 and 1.35 dB, the compensating circuit has little effect on the frequency characteristic over the same frequency range. It was necessary to decrease the loss approximately 0.7 dB at 229 MHz to provide the desired frequency characteristics. The variolosser is shown schematically in Fig. 7.

4.2 *A Wideband Common Base, Common Base Variolosser*

A variolosser was designed for a large bandwidth and low amplitude distortion to demonstrate the wideband possibilities of the circuit. The essential difference between this design and the design presented in Section 2.3 is that the minimum loss is greater, the variation in attenuation is smaller, and the interstage has been designed to have
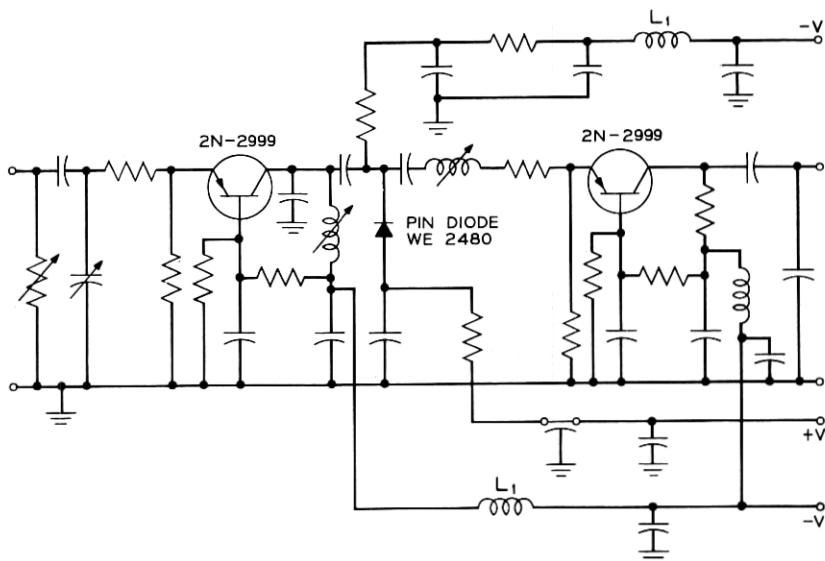

Fig. 7 — Common base, common base variolosser schematic.

a large 3 dB bandwidth. A compensating circuit with a Q equal to 0.458 was used to provide a flat amplitude characteristic over a 50 percent band at the 17 dB loss point. The amplitude versus frequency characteristic was computed using equation (27); the results are shown by the series of curves in Fig. 8. This figure shows the amplitude characteristic at the 17 dB attenuation point, where the interstage was compensated, and the characteristic at 5 dB intervals down to the minimum loss of 2 dB. The arrows indicate a bandwidth slightly greater than 50 percent. Over this band the amplitude distortion does not exceed 0.1 dB for any attenuation level.

4.3 Common Emitter, Common Base Variolosser

A transistor operating in the common emitter configuration has an output admittance which is capacitive and resistive. Thus, transistor Q1 of Fig. 1 could be operated in the common base configuration, or in the common emitter configuration, without requiring a change in the basic circuit. The value of C_1 and the maximum value of R_1 depends upon the configuration. The equations in Section 2.1 can be
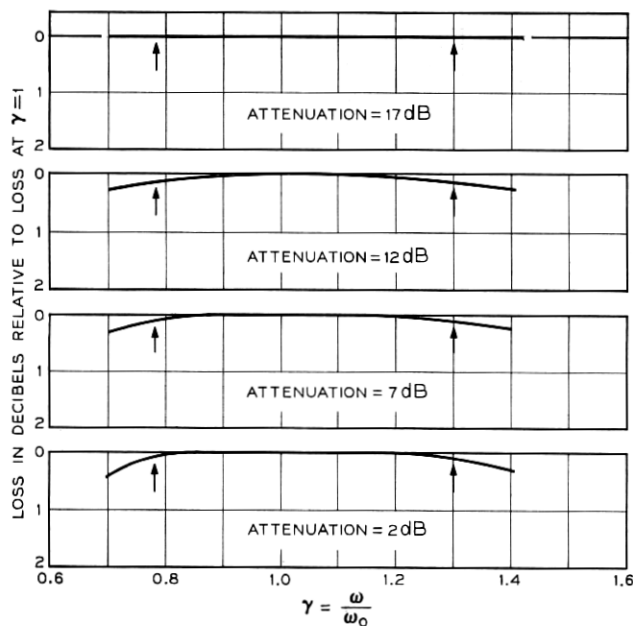

Fig. 8 — Wideband variolosser characteristics.

used equally well to design a common base, common base, or a common emitter, common base variolosser. The main difference between the two configurations is that the output conductance is considerably larger for common emitter operation, resulting in a higher minimum loss. Measurements at 300 MHz for the WE 2526 transistor show that the common emitter configuration has an output capacity of 1.7 pF shunted by 500 ohms. Using the combined shunt resistance for the PIN diode, a bias resistor of 1200 ohms, and equation (17), the minimum loss for a common emitter, common base variolosser is computed to be 2.7 dB. The maximum attenuation for $R_2 = 126$ ohms would remain at 20 dB.

4.4 Performance of Common Emitter, Common Base Variolosser

Figure 9 shows a variolosser operating between 240 and 360 MHz using the common emitter, common base configuration, designed to provide automatic gain control in a main IF amplifier.[3] This figure shows one section of the amplifier that contains the variolosser. By connecting point A of an identical section to point B of the one shown, gain-variolosser sections are cascaded.

The performance of three such sections cascaded to provide an attenuation range of 43 dB and operating from 240 to 360 MHz is shown in Fig. 10. The attenuation shown in the photos does not in-
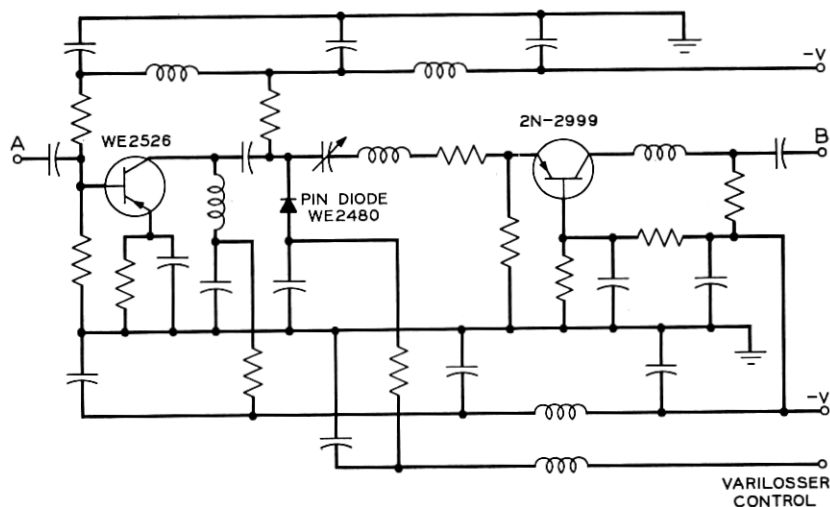

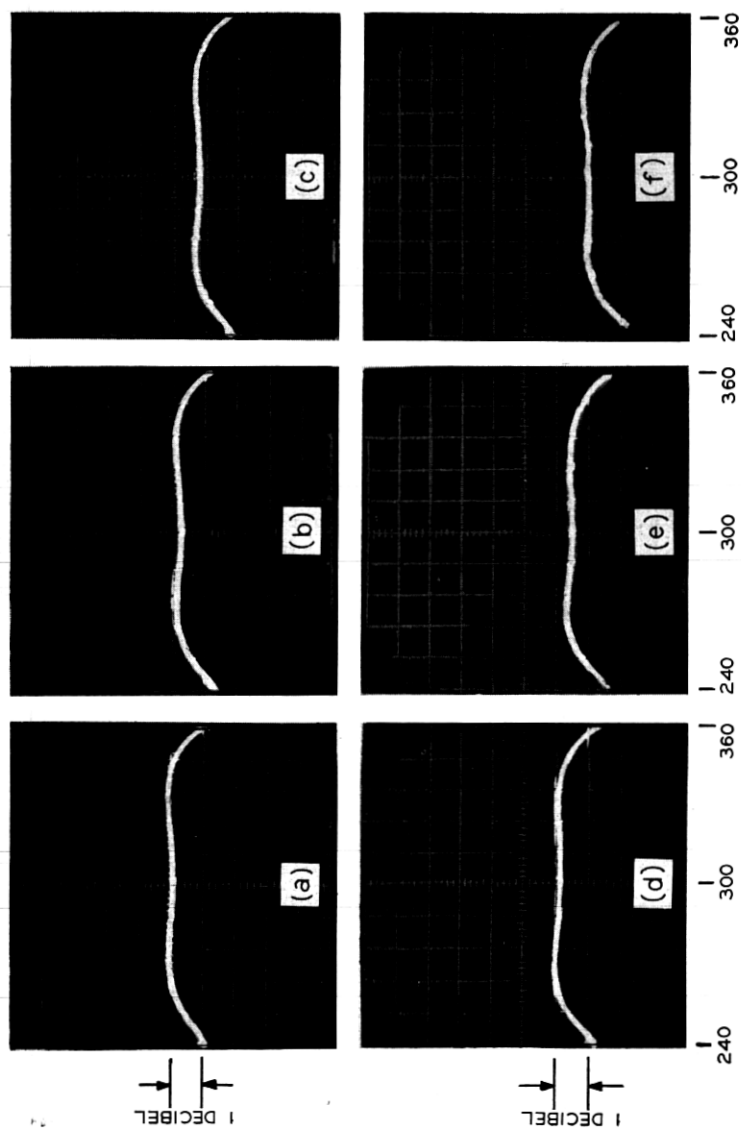Fig. 9 — Common emitter, common base variolosser schematic.

Fig. 10 — Frequency characteristic versus attenuation for three variolossers operating in 300 MHz IF amplifier at attenuations of (a) 39 dB, (b) 36 dB, (c) 26 dB, (d) 16 dB, (e) 6 dB, and (f) 0 dB.

clude the minimum loss of each section of approximately 2.7 dB. The falloff at the band edges is the result of several fixed gain stages following the variolossers. The frequency characteristic versus attenuation is shown when the three sections are providing attenuations of 39, 36, 26, 16, 6, and zero dB. There is an additional 4 dB range in attenuation which is used to correct for the variation in gain of the amplifier over the −40°F to +135°F temperature range. This series of photographs show the large range in attenuation and the small change in band shape that can be realized using the design method described in this paper.

V. CONCLUSIONS

A high quality, wideband variolosser can be made by coupling the common base, common base or the common emitter, common base configuration with a double tuned circuit, and varying the shunt impedance with a PIN diode. A minimum attenuation of 1.35 dB for the common base, common base configuration and 2.7 dB for the common emitter, common base configuration is realizable at 300 MHz. The minimum losses would be lower at lower frequencies. A maximum attenuation greater than 20 dB is possible for both configurations.

By designing the interstage circuit for a 3 dB bandwidth that is large compared with the desired bandwidth and compensating the circuit to provide a flat transmission characteristic at the maximum loss point, a variolosser with a loss variation of 15 dB can be made to operate over a 50 per cent bandwidth with little distortion in the frequency characteristic as a function of attenuation.

VI. ACKNOWLEDGMENTS

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