Broadband 300 MHz IF Amplifier Design

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Short hop radio systems of the type described in this issue require broadband intermediate frequency amplifiers in the range of a few hundred MHz which have a large gain control range and stable characteristics with respect to temperature; they must also make efficient use of bias power and have well behaved noise properties.

This paper describes the design of such amplifiers. We give extensive measurements for an amplifier with a 1 dB bandwidth of 120 MHz centered at 300 MHz and an automatic gain control range of 43 dB.

I. INTRODUCTION

The incentive for this work arises from the need for IF amplifiers in short hop radio systems. Such systems may be powered by thermoelectric generators driven by propane gas and have the electronic repeater mounted at the top of a pole. Amplifiers used for this application must:

(*i*) Be sufficiently broadband to amplify, with low distortion, large index analog FM or PSK-PCM signals.

(*ii*) Have good temperature stability since they operate at outdoor ambient temperatures.

(*iii*) Be small and lightweight to fit into the limited space of the pole mounted enclosure and to keep the weight loading at the top of the mounting to a minimum.

(*iv*) Have low power consumption to operate from a thermoelectric generator which is the primary power source.

(*v*) Be designed, if possible, with a thought toward the use of integrated circuitry for future amplifiers.

In the amplifier designed to satisfy these requirements, most of the gain is obtained in broadband common emitter stages. Transistors with a low current gain are used so that the interstage is simple,

stable, and has good power handling capabilities. Broadband variolossers, separating the early gain stages, provide the necessary automatic gain control range. Band shaping is obtained in the transformer coupled output stages.

II. LOW LEVEL STAGES

Most of the gain and all of the gain control range are accomplished in the low level section of the amplifier. It is important to do as much as possible at low signal levels so that the total power consumption—an important system consideration—is minimized. The low level section consists of eight transistors connected alternately in common base and common emitter configurations. The common emitter stage provides current gain, while the interstage network, coupling the common emitter common base stage, is part of a broadband variolosser used in the automatic gain control circuits. The common emitter common base gain-variolosser stages are coupled together by a simple peaking circuit to distribute both the gain and variable loss throughout the amplifier. This gain-variolosser-coupler arrangement illustrated schematically in Fig. 1 was chosen for the following reasons:

(*i*) Gain is achieved through the current gain of the common emitter transistor, obviating the need for transformers and lending the interstage to future circuit integration.

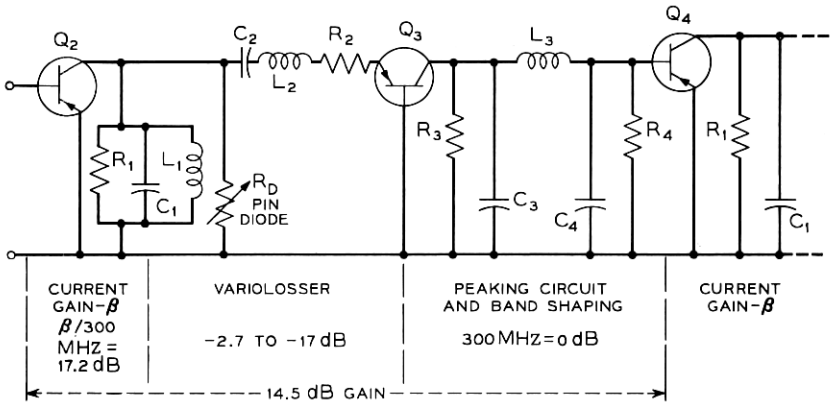

Fig. 1 — Common emitter-common base gain-variolosser stage and peaking circuit.

(*ii*) The output impedance of the common emitter stage is readily adapted to a simple broadband variolosser circuit.

(*iii*) The zero frequency current gain of the transistor β_o, can be tailored to the requirements on gain and bandwidth. For the low β_o used in this amplifier, the result is a stable gain-frequency characteristic achieved without the use of feedback circuits.

(*iv*) The common base stage provides isolation between the variolosser and the peaking circuit. This configuration is a satisfactory load for the broadband variolosser and provides a stable broadband high impedance generator for the common emitter stage.

(*v*) A low intermediate frequency favors low power consumption and increases the gain of the upper-sideband varactor amplifier which is driven by the IF amplifier.[1] The intermediate frequency of 300 MHz chosen for this application is sufficiently high to obtain a 120 MHz IF bandwidth.

2.1 *Common Emitter Gain Stage*

The common emitter transistor is a Bell Telephone Laboratories L-2526 microwave transistor chosen to have a low frequency current gain between 8 and 10 and a minimum gain bandwidth product $F_T = 2{,}500$ MHz. With this combination of high F_T and low β_o substantial current gain and a reasonable high frequency characteristic are obtained without using external feedback. In addition, the low β_o transistor has higher power capability than a high β_o transistor with external feedback unless the feedback can be maintained down to dc. The difference in power handling capability can be seen by referring to Fig. 2. This plot shows a transistor with a high β_o which has sufficient feedback to reduce the high frequency current gain to β_1. The feedback is not maintained down to dc. Curve 2 shows the frequency characteristics of a low β transistor with a low frequency current gain equal to β_1. Consider first the high β transistor. The ratio of collector current to base current at dc is given by

$$\frac{I_{cdc}}{I_{bdc}} = \beta_o \, . \tag{1}$$

At some high frequency f_1 the ratio of collector current to base current is

$$\frac{I_c}{I_b} \cong \beta_1 \, . \tag{2}$$

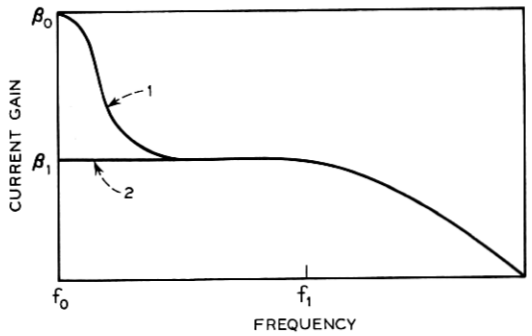

Fig. 2 — Common emitter transistor characteristics.

If the base is not driven beyond cutoff, then the peak current swing in the base at frequency f_1 is limited to

$$I_{b\text{peak}} = I_{bdc} = \frac{I_{cdc}}{\beta_o}. \tag{3}$$

Combining (2) and (3) yields the peak collector current swing at frequency f_1 for a high β transistor

$$I_{c\text{peak}} = I_{cdc} \left(\frac{\beta_1}{\beta_o}\right). \tag{4}$$

Thus, the peak collector current is reduced by the ratio of the high frequency to low frequency current gain. For the low β transistor, $\beta_1/\beta_o \cong 1$ and

$$I_{c\text{peak}} \cong I_{cdc}.$$

The peak collector current of a high β unit is (β_1/β_o) less than that obtainable from the low β unit, and the power output is reduced by the square of this ratio. This is important since the variolosser must be operated at a reasonably high power level to maintain a good amplifier noise figure. The power dissipation is minimized by the proper choice of β_o.

2.1.1 *Common Emitter Frequency Characteristic*

The frequency characteristic of the common emitter stage as a result of the variation of β is given by[2]

$$\beta = \frac{\beta_o}{1 + \dfrac{jf}{(1 - \alpha_o)f_{\alpha b}}} \tag{5}$$

where

α_o = low frequency grounded base current gain
β_o = low frequency grounded emitter current gain

and

$f_{\alpha b}$ = alpha cutoff frequency.

Assuming a β_o of 9 and an $f_{\alpha b}$ of 3.8 GHz for the 2526 transistor, the frequency characteristic given by equation (5) is shown in Fig. 3, curve 1. The 240 to 360 MHz band indicated by the arrows is the IF band of interest. There is a negative slope across the IF band of 1.3 dB. Because this slope is small, it can be readily compensated for by a peaking circuit, and the IF band will be flat and stable.

2.1.2 *Common Base Common Emitter Coupling and Peaking Circuit*

As shown in Fig. 1, the output of the common base stage Q3 is a capacitor shunted by a resistor of approximately 1K. The input impedance of the common emitter stage Q4 is also capacitive, and has approximately 35 ohms in shunt. The addition of one inductor L_3, forms a simple series peaking circuit which has been used extensively in tube amplifiers.[3] This interstage circuit can be adjusted to have a positive slope across the band which compensates for the negative

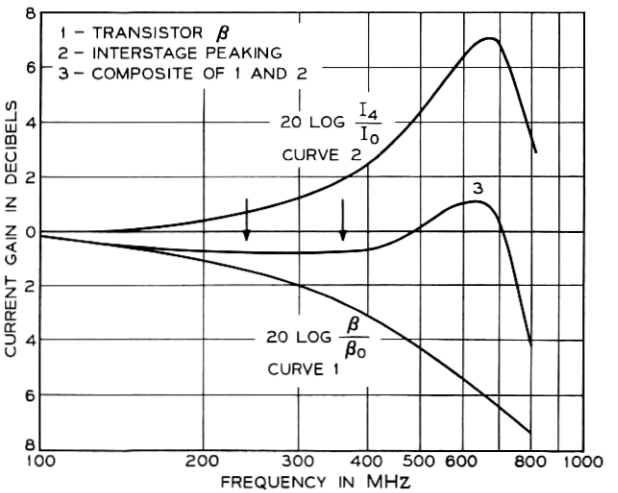

Fig. 3 — Low power gain stage characteristics.

slope of the β characteristic. The slope can be varied by changing R_4 or L_3. The peaking circuit shown in Fig. 1 has been redrawn in Fig. 4 where

$$Y_1 = \frac{1}{R_3} + j\omega C_3 , \tag{6}$$

$$Y_2 = \frac{1}{j\omega L_3} , \tag{7}$$

$$Y_3 = j\omega C_4 , \tag{8}$$

$$Y_4 = \frac{1}{R_4} . \tag{9}$$

The current transfer ratio for this network is

$$\frac{I_4}{I_o} = \frac{y_4}{\left[y_1 + y_3 + y_4 + \dfrac{y_1(y_3 + y_4)}{y_2}\right]} . \tag{10}$$

Substituting (6), (7), (8), and (9) into (10), the transfer function becomes

$$\left|\frac{I_4}{I_o}\right|^2 = \frac{1}{\left[1 + K - \left(\dfrac{C_3 + KC_4}{C}\right)\gamma^2\right]^2 + \left[\left(\dfrac{1 + Q_3Q_4}{Q_4}\right)\gamma - \dfrac{C_3C_4}{C^2Q_4}\gamma^3\right]^2} \tag{11}$$

where

$$\gamma = \frac{\omega}{\omega_o} , \qquad \omega_o = \frac{1}{(LC)^{\frac{1}{2}}} , \qquad C = C_3 + C_4 ,$$

$$K = \frac{R_4}{R_3} , \qquad Q_3 = \frac{1}{\omega_o C R_3} , \qquad Q_4 = \frac{1}{\omega_o C R_4} .$$

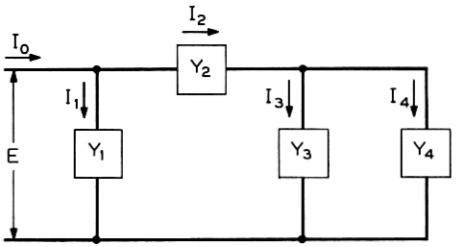

Fig. 4 — Common base-common emitter coupling and peaking circuit. $Y_1 = 1/R_3 + j\omega C_3$; $Y_2 = 1/j\omega L_3$; $Y_3 = j\omega C_4$; $Y_4 = 1/R_4$.

Equation (11) includes the loading from the common base as well as the common emitter stage and expresses the amplitude characteristic in terms of the currents which is a useful form for transistor circuits. Equation (11) has been plotted in Fig. 3, curve 2, for the case where $C_3 = C_4 = 2.5\rho$F, $L_3 = 25$ nH, $R_3 = 1$K, and $R_4 = 35\Omega$. This curve shows the positive slope needed to compensate for the fall off in the β characteristic. The peaking circuit is adjusted for a flat amplitude by adjusting L_3.

Curve 3 of Fig. 3 shows the complete transfer function of the gain stage; it is the product of the functions shown in curves 1 and 2. The amplitude characteristic is flat from 200 to 400 MHz which is considerably wider than the desired IF band, and it also shows that a peak will occur at approximately twice the center frequency of the IF band. Filtering proceeding the low level stages, and filtering resulting from the IF transformers following the low level stages, attenuate this peak so that it has a small effect on the overall amplifier characteristic.

2.2 *Variolosser*

The electronically variable attenuator used in this amplifier uses one Western Electric 2480 PIN diode to vary the loading on the primary of a double tuned circuit and in this manner changes the interstage loss. This attenuator is described in detail in Ref. 4 where it has been shown that at the midband, the interstage loss is given by

$$\text{loss in dB} = 20 \log \frac{1}{1 + G_1 R_2}. \tag{12}$$

R_2 is the total resistance in the emitter of transistor Q3 of Fig. 1 and G_1 is the parallel combination of the output resistance of Q2 and the PIN diode R_D. Thus, the interstage loss can be changed over a wide range by varying G_1 or R_2.

The parallel—series tuned circuit incorporates the output capacity of the common emitter stage and the input inductance of the common base stage as part of the interstage circuit. The interstage is designed to have a bandwidth considerably wider than the IF band and to have flat transmission characteristics at the minimum loss and at the nominal operating loss points. As the variolosser is varied from the maximum attenuation of 17 dB to the minimum attenuation of 2.7 dB there is little change in the band shape, that is, less than 0.1 dB across the band. Three variolossers, used as part of the low level stages, distrib-

ute the loss throughout the amplifier so that the attenuation can be varied over a 43 dB range and the main amplifier will still have a reasonable noise figure at the high attenuation point.

III. DRIVER AND OUTPUT STAGES

The driver and the output stages are common base transformer coupled stages as shown in Fig. 16. Two Western Electric 2254 transistors are used in parallel in the output stage to provide +7.5 dBm of power into a 50 ohm load. The transformers are parallel-series tuned transformers designed to have 0.25 dB loss at 240 and 360 MHz. They provide the primary band shaping for the amplifier and are also used to provide:

(*i*) 6 dB current gain in the interstage and to match the common emitter transistor Q8 and the common base transistor Q9;
(*ii*) 4.5 dB current gain between transistor Q9 and the output stage. This transformer is designed as a mismatched transformer with the loading on the secondary;
(*iii*) An impedance match between the output transistors and the 50 ohm load.

The output stage can supply +7.5 dBm of power into a 50 ohm load with 0.5 dB of compression as shown by Fig. 5. This curve is a plot of the ouput power into a 50 ohm load as a function of the input power to the amplifier.

IV. NOISE FIGURE

The noise figure of a main IF amplifier used in a radio system should not appreciably increase the overall noise figure of the system. Thus, a satisfactory noise figure for the main amplifier is affected by preamplifier gain and down converter preamplifier noise figure. The main amplifier spot noise figure (at 300 MHz) varies from 8.6 dB at maximum gain to 13.6 dB at the normal operating level, and has a value of 14.8 dB at minimum gain. At the normal operating level, the main amplifier will increase the receiver noise figure by 0.4 dB.

The noise figure of the amplifier as a function of frequency with gain as a parameter is shown in Fig. 6. This noise figure is measured in a 1 MHz band.

4.1 *Variolosser Placement*

The amplifier noise figure is affected by the number of variolossers and their distribution throughout the amplifier. Variolossers placed

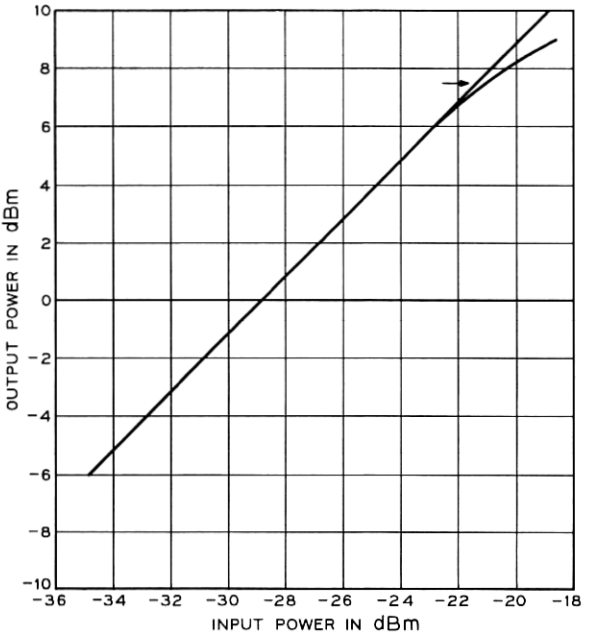

Fig. 5 — Compression characteristic of amplifier.

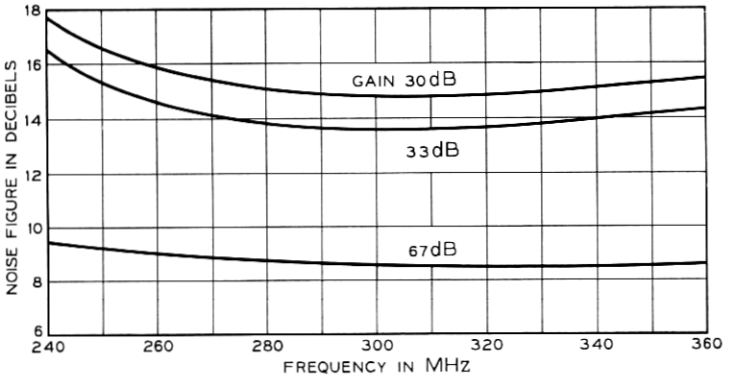

Fig. 6 — Noise figure verses frequency and amplifier gain.

in the early stages of the amplifier must have a limited range if a low noise figure is required. Variolossers placed near the output of the main amplifier can have a large attenuation range; however, the early stages of the amplifier and the variolosser will then operate at high power levels which results in greater dc power consumption.

The noise figure of several networks in cascade is given by the expression[5,6]

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \cdots , \tag{13}$$

where

F_T is the overall noise figure,

F_1, F_2, F_3 are the noise figures of each cascade section,

and

$G_1, G_2, \ldots$ are available gains of each cascade section.

If G_1 can be made large, then the noise figure is essentially F_1. If G_1 is small, F_2, F_3, and so on, contribute to the overall noise figure.

As used in the radio system, the main IF amplifier is preceded by a preamplifier with 24 dB gain. The available gain from this amplifier greatly reduces the noise contribution to the system noise figure from the main amplifier and places the first stages of the main amplifier at an intermediate power level.

Three variolossers are placed in the first three stages of the amplifier, and the attenuation range of each one is limited to 14 dB, primarily by noise figure considerations. Several variolossers, each with a moderate attenuation range, placed at an intermediate power level, provide a good compromise between radio system noise figure, the number of variolossers required, and the dc power consumption. The available gain of each amplifier-variolosser section varies with attenuation setting and approaches a value slightly greater than one at the nominal amplifier gain of 33 dB. Thus, from equation (13), the noise figure should vary with amplifier gain. The variation in noise figure as a function of amplifier gain and frequency is shown in Fig. 6.

4.2 *Distribution of Gain and Loss*

The distribution of the gain and loss throughout the amplifier is shown in Fig. 7. A gain stage is followed by a variable attenuator stage so that each low level section has a maximum gain of 14.5 dB. Three such sections with a maximum gain of 43.5 dB are followed by a common emitter transformer coupled stage which provides 22 dB

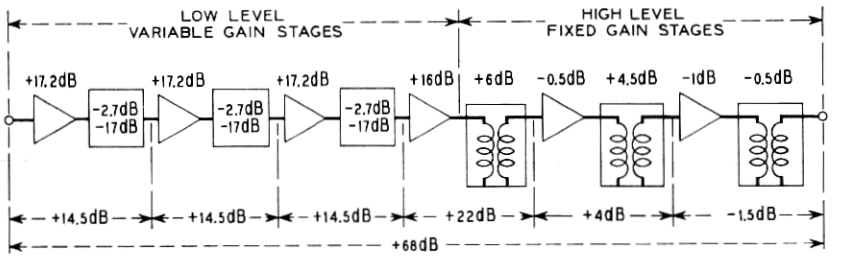

Fig. 7 — Gain-loss distribution of IF amplifier at maximum gain.

of fixed gain. The driver stage has a net gain of 4 dB while the output stage matches the amplifier to 50 ohms with 1.5 dB loss.

V. AUTOMATIC GAIN CONTROL

The automatic gain control samples the output power and provides an error signal to the variolossers to correct for changes in amplifier input power or for amplifier gain as a function of temperature. As shown by Figs. 8 and 16, the automatic gain control consists of a detector diode D4, two dc amplifiers Q12 and Q13, and variolosser diodes D1, D2, and D3. The amplifier output is sampled by diode D4 and any error signals are amplified by the dc amplifiers to change the

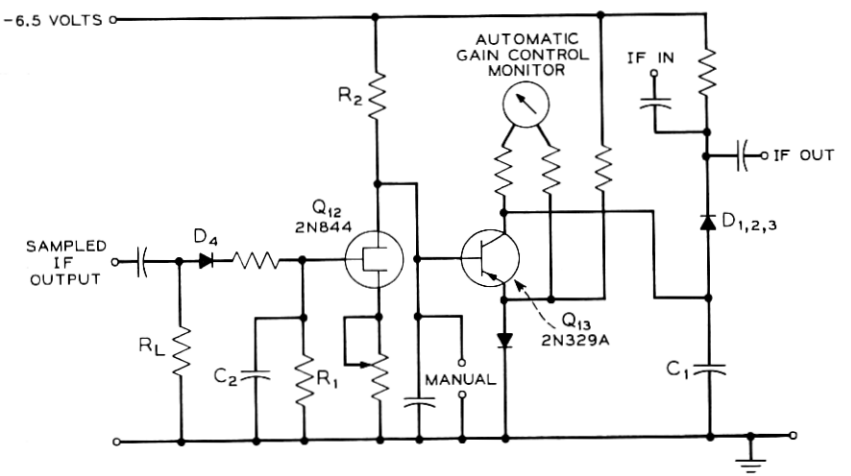

Fig. 8 — Automatic gain control schematic.

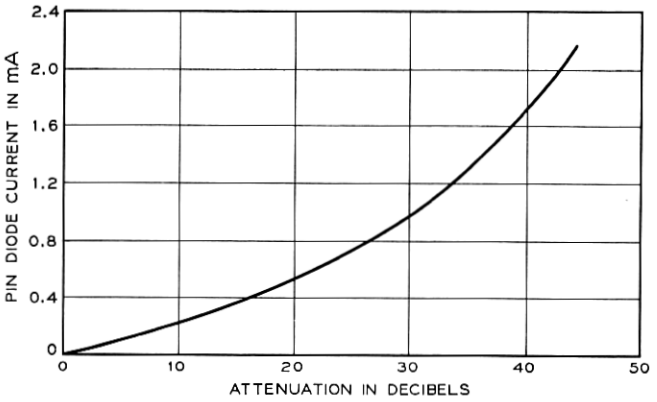

Fig. 9 — PIN diode current verses attenuation.

current through the three PIN diodes. The resistance of the PIN diodes varies with the diode current to form a variable current divider in the IF path. The use of a PIN diode to vary the interstage loss is discussed in Section 2.2 and in Ref. 4. As used in this amplifier, the PIN diode will provide a large change in attenuation for a small variation in diode current. This is shown in Fig. 9 which also shows the attenuation of three variolossers as a function of the total diode current. A 43 dB change requires slightly over 2 milliamperes. This small variation in current makes the power requirements of the amplifier virtually constant at all gain settings.

The loop gain of the AGC circuit varies with variolosser setting; however, it is greater than 25 dB over most of the attenuation range. The output power decreases 1.2 dB for a 30 dB decrease in signal level.

5.1 *Manual Gain Control*

A manual gain control is necessary to adjust the gain of the IF amplifier when some radio system measurements are made. In order for the amplifier to reproduce a swept input signal accurately, the response time of the AGC must be long compared with the sweep rate of the generator. For a generator using a 60 cycle sweep rate, the 0.4 second time constant of the AGC loop is satisfactory; however, in some system measurements, the sweep rate can be as low as one cycle per second. The manual gain control clamps the gain of the amplifier at a selected level; the IF amplifier characteristic can then be measured without being distorted by the AGC. This control is shown in

Fig. 10. The main requirement for this control is that it can supply a stable negative voltage that can be varied from −3.8 to −4.1 volts.

5.2 *AGC Monitor*

The AGC monitor is used to indicate the input power to the main IF amplifier. As shown in Fig. 8, this monitor measures the voltage across the collector-emitter junction of transistor Q13. The meter has been calibrated as shown in Fig. 11 to indicate the input power to the amplifier in dBm with temperature as a parameter. In the system experiment the AGC monitor is used as a remote indicator approximately 60 feet from the main IF amplifier.

VI. AMPLIFIER PERFORMANCE

The performance of the amplifier as a function of gain control setting, temperature, and power supply variations is shown by the series of pictures in Figs. 12, 13, and 14. The input and output impedance match is shown in Fig. 15.

6.1 *Amplifier Performance with Gain Changes*

The performance of the amplifier as a function of the gain control setting is shown in Fig. 12. This series of curves show three characteristics of the amplifier:

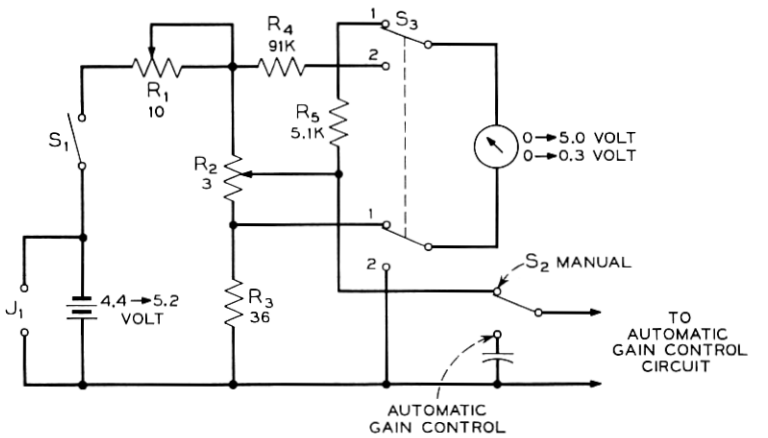

Fig. 10 — Manual gain control schematic (J1-battery charge jack; S1-battery switch; S2-manual or AGC selector; S3-battery test).

(*i*) The basic amplitude characteristic over the 240 to 360 MHz range (−26 dBm input signal level),

(*ii*) The distortion contributed to the amplitude characteristic by the three variolossers as the gain is varied from 26 dB (−18 dBm input) to the maximum gain of 67 dB (−62 dBm input),

(*iii*) The performance of the AGC loop by showing the output power changes as a function of the input power.

Each photograph shows the amplitude characteristic as a function of frequency with input power as a parameter. The vertical scale is 1 dB per division. The input power level is shown for each photo as well as an output power level of +7.5 dBm. Figure 12a shows the characteristic when the amplifier is driven with a −18 dBm signal level. This is 8 dB greater than the normal signal level. Figure 12b shows the characteristic for a normal input signal level of −26 dBm.

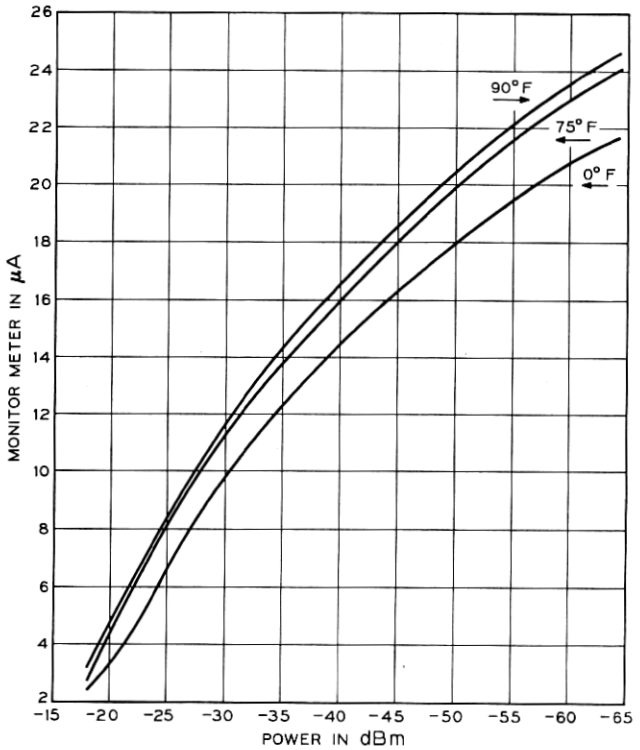

Fig. 11 — Automatic gain control moniter calibration.

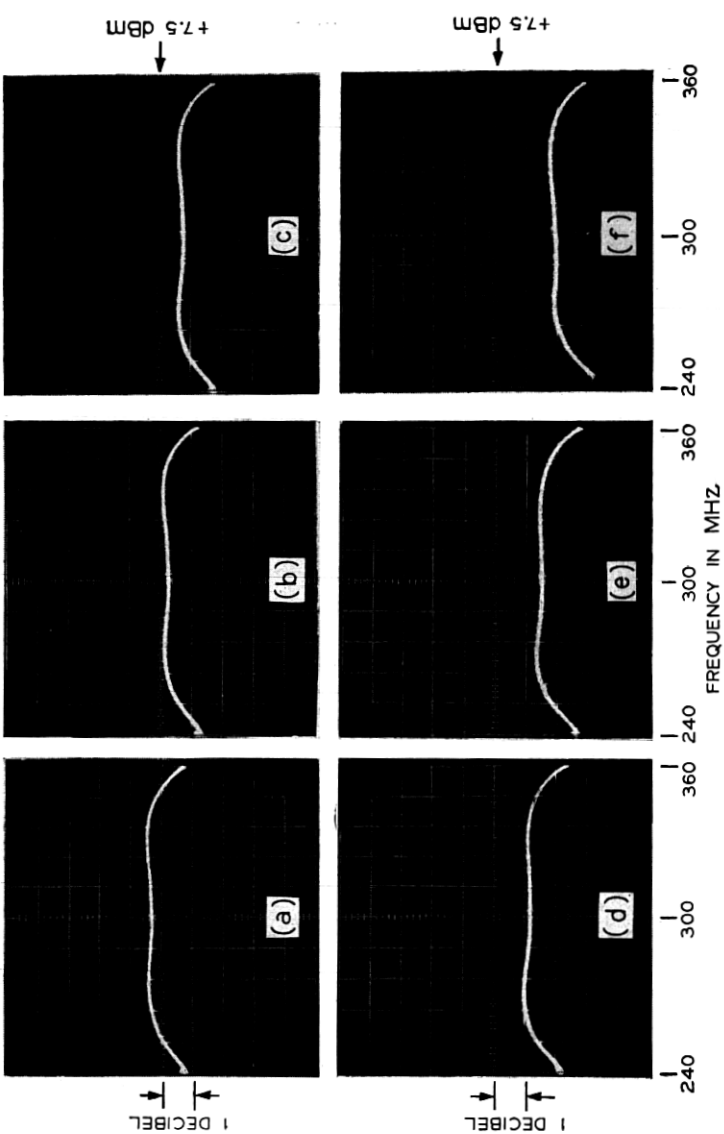

Fig. 12 — Amplitude characteristic and output power as a function of input power at (a) —18 dBm, (b) —26 dBm, (c) —36 dBm, (d) —46 dBm, (e) —56 dBm, and (f) —62 dBm.

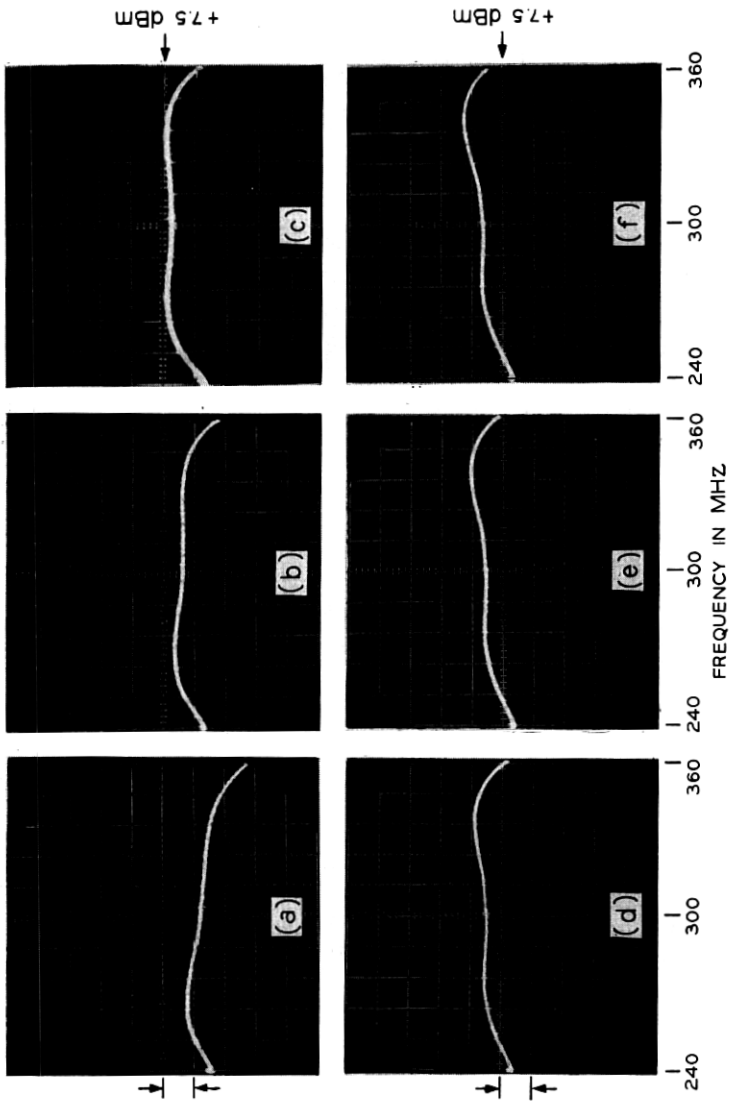

Fig. 13 — Amplitude characteristic verses temperature at (a) 140°F, (b) 100°F, (c) 75°F, (d) 0°F, (e) —25°F, and (f) —40°F.

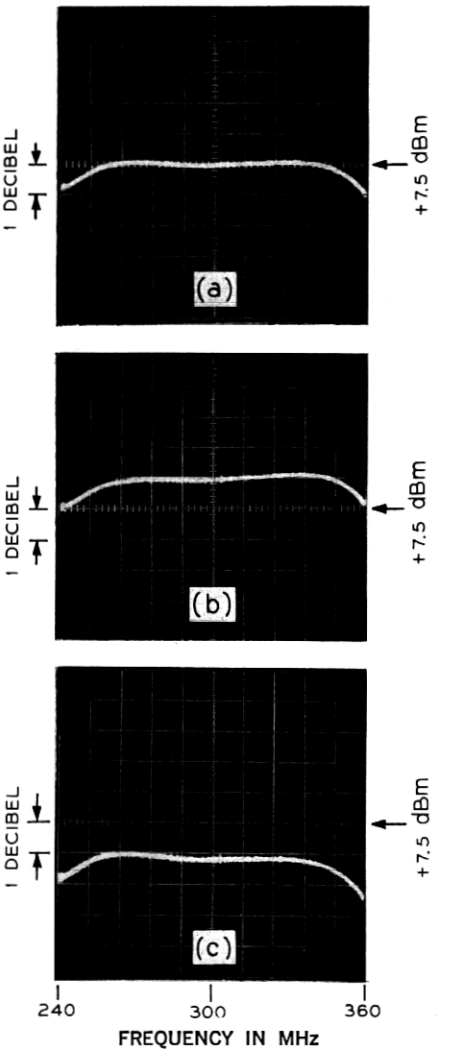

Fig. 14 — Amplitude characteristic and output power as a function of dc supply voltage at (a) 6.5 V, (b) 6.175 V, and (c) 6.825 V.

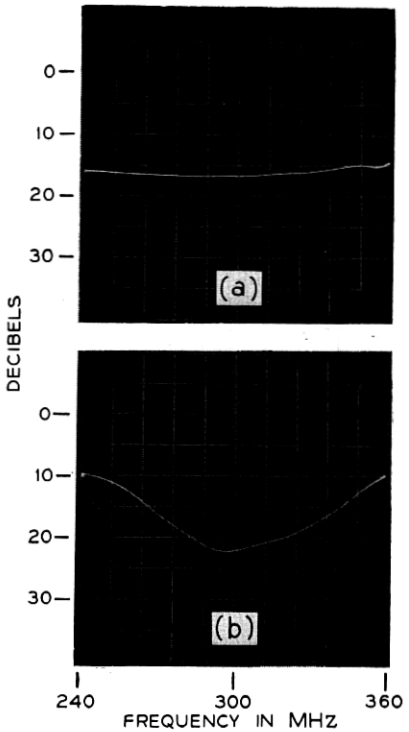

Fig. 15 — Return loss verses frequency for amplifier input and output circuits: (a) IF input, and (b) IF output.

This is the point where the amplifier was adjusted for a flat transmission characteristic with an output power of +7.5 dBm. Figures 12c through f show the frequency characteristic and the output power delivered by the amplifier for decreasing signal levels.

6.2 *Amplifier Performance with Temperature Changes*

The amplifier must operate in a temperature range from −40°F to +135°F. The variation in the amplitude characteristic as a function of temperature is shown by the series of curves in Fig. 13. The input signal level was held constant at −26 dBm and the output power was set at +7.5 dBm at 75°F. The vertical scale is 1 dB per division. In addition to the amplitude-frequency characteristic, the curves show how the output power changes with temperature from the value set at 75°F.

6.3 *Amplifier Performance with Power Supply Variations*

The −6.5 volts supplied by the radio system power supply will vary less than ±2 percent for expected input voltage variations, load variations, and temperature changes.[7] The three curves in Fig. 14 show the frequency characteristic and the change in output power for supply voltage that are normal, 5 percent high, and 5 percent low. The vertical scale is 1 dB per division. These curves show that for ± 2 percent change in power supply voltage, the output power will vary ±0.4 dB and the frequency amplitude characteristic will remain constant.

6.4 *Input Impedance*

The input transformer, used to match a 50 ohm source to the impedance of the common base stage, consists of a low pass circuit as shown in Fig. 16. The input impedance of transistor Q1 is inductive and resistive. A resistor in series with the input of transistor Q1 adjusts the Q of the network to provide a flat transmission characteristic over a wide frequency range.

The measured return loss of the input circuit from 240 to 360 MHz is shown in Fig. 15a. The return loss is 17 dB at the center of the band and approximately 15 dB at the band edges.

6.5 *Output Impedance*

The amplifier has an output impedance of 50 ohms, and it is matched by means of a double tuned transformer. This circuit is shown in the collector stage of Q10 and Q11 of Fig. 16. The load resistor for the parallel-tuned series-tuned transformer is also used as a dc return for the automatic gain control diode detector D4.

The measured return loss of the output circuit from 240 to 360 MHz is shown by the photo in Fig. 15b. The return loss in the center of the band is 22 dB; it decreases to 10 dB at the band edges.

VII. MECHANICAL DESIGN

The IF amplifier is constructed on a $\frac{1}{16}$ inch thick epoxy glass board, laminated on both sides with two ounce copper and enclosed in a brass box with removable top and bottom covers. The enclosure with covers in place measures $1\frac{3}{4}$ inches × $1\frac{3}{4}$ inches × $10\frac{1}{2}$ inches. The transistor bias and RF circuits are mounted on the top of the board and the AGC circuits on the bottom as shown in Figs. 17 and 18. This type of construction is used to keep lead lengths in the RF circuits to a minimum. To insure a common ground plane, the board is fastened

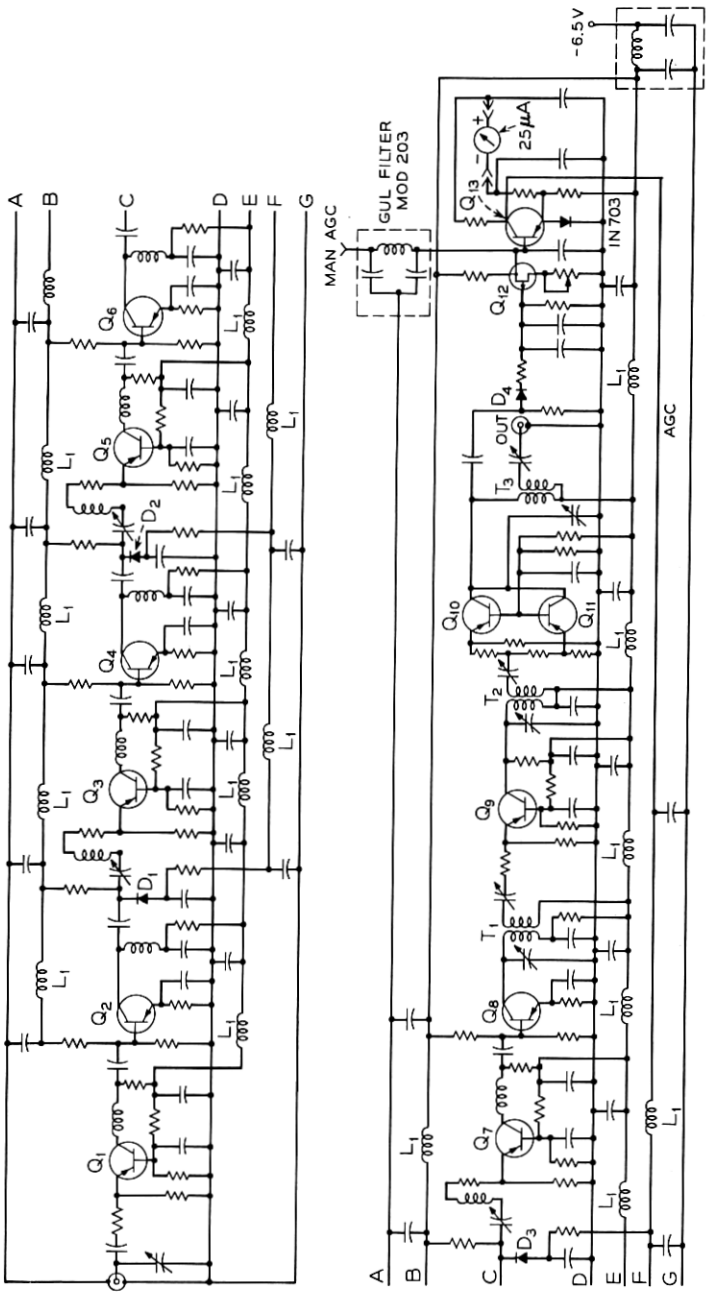

Fig. 16 — IF amplifier schematic.

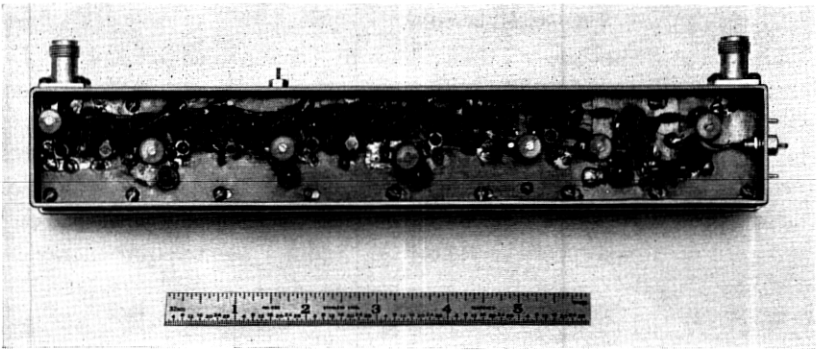

Fig. 17 — Top view of IF amplifier.

to a $\frac{3}{16}$ inch wide support on the inner walls of the box with screws spaced approximately $1\frac{1}{4}$ inches apart. The covers are constructed to overlap and to be screwed to the outside walls of the box. Silver-plated phosphor bronze fingers, attached to the inside of the covers, make contact with the inner walls of the box. This shielding is necessary because the amplifier is normally operated close to a 320 MHz source with an output power 76 dB greater than the minimum input power to the IF amplifier. With the covers in place, no interference from the power source was observed in the amplifier.

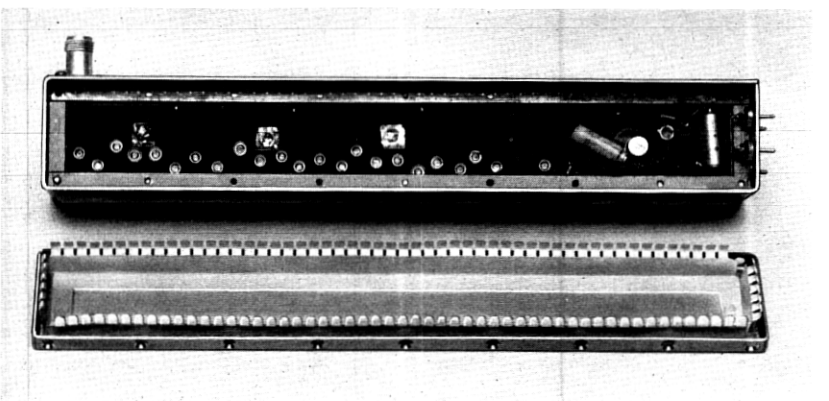

Fig. 18 — Bottom view and cover of IF amplifier.

VIII. DISCUSSION

It has been demonstrated that a high performance wide band amplifier can be made using a combination of common emitter-common base stages to obtain current gain and a stable wideband variolosser. The use of low β_o transistors leads to a simple interstage with good power handling capabilities and a stable temperature characteristic. The low power consumption of 0.65 watts for an amplifier with a maximum gain of 67 dB meets the short hop radio system requirements.

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