Computer-Aided Circuit Design by Singular Imbedding

By E. B. KOZEMCHAK and M. A. MURRAY-LASSO

(Manuscript received August 5, 1968)

We give a new and powerful method for the direct solution of circuit design problems. The method begins with a prespecified topology and some or all elements undetermined in value. The designer imposes on the circuit any desired set of node-pair voltages, branch currents, or driving point and transfer immittances. Values of circuit elements that satisfy the constraints are directly calculated. This direct method of solution avoids the usual iterative analysis-optimization schemes, reducing computer times by up to three orders of magnitude.

A linear set of design equations is formulated by choosing undetermined element currents and node voltages as the variables. Singular elements are introduced to impose the desired constraints. Inequality as well as equality constraints are permitted. Element values are determined from the solution of these equations. In this paper we emphasize our method of solution in relation to dc networks.

I. INTRODUCTION

The most significant advances made in computer-aided circuit design have been in analysis programs. The designer can now choose from among several general purpose programs that program which most nearly suits his particular needs. In designing a circuit to meet a given set of requirements, the usual approach has been to use analysis programs in some optimization scheme. Through an iterative process, carried out by the machine, the man, or a man-machine interaction, a final design is reached. The approach presented here provides a direct solution, and does not rely on such iterative schemes.

The method is most fertile in the area of active network design, where one often wishes to choose element values in a specified topology in order to meet some set of requirements. The method has been applied to a number of design problems of current interest including

biasing direct coupled transistor circuits; designing transistor amplifiers for specified midband gain, input, and output impedances; and simultaneously realizing several specified impedance or admittance parameters of a network.

In the design of electronic circuitry, one usually wishes to imbed passive elements into a network containing active devices, and to determine the required passive element values. Therefore, this paper deals with the determination of element values in a prespecified topology for which a given performance is required. Two new elements, a voltage forcing element (VFE) and current forcing element (CFE), are introduced in order to constrain network voltages and currents. These elements may be realized with independent voltage and current sources, and the nullator, a somewhat "pathological" element used in theoretical network studies.

The method of singular imbedding places the VFE's and CFE's in a network to constrain the desired variables. The terminal voltage-current behavior of the variable elements is not specified. Instead, the constraints imposed upon the network by the VFE's and CFE's are used to determine allowed voltage-current relations for the variable elements. The formulation remains linear in these variables. The last step involves determining the element values through Ohm's law once the allowed voltage-current relations are known.

By appending the original set of equations with a set of inequality constraints, it is possible to restrict the range of element values in the solution. For example, realizations employing only element values between specified lower and upper bounds are possible. For simplicity, only the case of linear dc networks are illustrated. Extensions of the method to ac and nonlinear design are considered elsewhere.

II. A NEW APPROACH

To understand the philosophy of this new approach to design, consider the train of events in realizing a set of requirements with electronic circuitry. Since the choice of topology is better handled by the man than the computer, we will assume some specified topology in which some or all of the element values are to be chosen to meet the given criteria. For example, in designing transistor circuitry it is necessary to choose some resistance values to properly bias the transistors. Similarly, one must often choose element values to give a desired voltage gain, driving point impedance, transfer impedance, or similar network function.

The invariant feature in all of these problems is that a set of network currents and voltages, or their ratios, has been constrained. The design problem is to find any set of element values consistent with these constraints. If the problem is posed with sufficient freedom, many sets of element values may exist consistent with the imposed constraints. Conversely, if the problem is posed with insufficient freedom, inconsistent equations arise and there is no solution.

If one can find a general method of imposing these network constraints, and can simultaneously monitor the voltage-current relations these constraints force at the terminals of the variable elements, then indeed a direct solution to many computer-aided design problems will have been found.

Before proceeding, however, consider a very simple example of how one might presently handle the design problem and the difficulties that would ensue. Suppose in the network of Fig. 1, one wishes to choose G_1 and G_2 such that V' is constrained to be 0.1 volt. A set of nodal equations may be written:

$$\begin{bmatrix} 1 + G_1 & -G_1 \\ -G_1 & G_1 + G_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}. \tag{1}$$

The first step involves a transformation of coordinates so that the desired quantities appear explicitly in the equations. In general, this will necessitate using hybrid parameters. For this case, the following transformation might be used:

$$\begin{bmatrix} V_1^\dagger \\ V_2^\dagger \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{2}$$

Inverting the relation, we have

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_1^\dagger \\ V_2^\dagger \end{bmatrix} \tag{3}$$

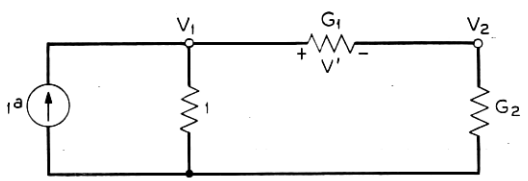

Fig. 1 — Simple design problem.

and the current-law equations become

$$\begin{bmatrix} 1 + G_1 & -G_1 \\ -G_1 & G_1 + G_2 \end{bmatrix} \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_1^\dagger \\ V_2^\dagger \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} 1 + G_1 & 1 \\ -G_1 & G_2 \end{bmatrix} \begin{bmatrix} V_1^\dagger \\ V_2^\dagger \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}. \tag{5}$$

Substituting the constant $V' = V^\dagger_1 = 0.1$, the set of equations becomes

$$\begin{aligned} 0.1(1 + G_1) + V_2^\dagger &= 1 \\ -0.1G_1 + G_2 V_2^\dagger &= 0. \end{aligned} \tag{6}$$

Thus, even if one is successful in finding a transformation to a basis that includes the variables that are constrained, the result is usually a set of nonlinear equations in the network elements and voltage variables. Solving this set of nonlinear equations for the unknown voltages and element values is extremely difficult. A method of handling this difficulty has been suggested, involving the use of optimizing techniques to vary element values until the network variables take on their desired values—in this case $V' = 0.1$ volt.[1] While this is a useful approach, it has several disadvantages. First, it is time consuming since many iterations are required for convergence. Second, local minima, or lack of sufficient numerical accuracy, may prevent convergence to a correct solution. Finally, although an infinity of sets (G_1, G_2) exist to satisfy the given constraints, the optimization yields only one of these sets.

With these difficulties in mind, let us repeat the philosophy of design presented here. We first determine how the requirements constrain network currents and voltages. We then force these currents and voltages to take on the desired values. Finally, we determine the effect of such constraints upon the voltage-current relations at the terminals of variable elements. These $v - i$ relations then determine the values of the variable elements.

III. NETWORK CONSTRAINTS

The common feature of all network synthesis problems is that they require some specified relation between some voltages and currents in the network. For example, synthesis of a given driving point impedance constrains the ratio of a port voltage to the current at that port. Synthesis of a transfer impedance constrains the ratio of a port

voltage to the current at a different port. A specified voltage or current gain constrains the ratio of two port voltages or port currents, respectively. Indeed the synthesis of entire network matrices is a combination of such constraints. Similarly, the static design problem in electronic circuits involves fixing certain branch currents and branch voltages. For example, one usually wishes to bias a transistor for a given collector current and collector-emitter voltage. Resistance values are chosen consistent with these constraints.

It is essential to demonstrate a method for constraining voltages and currents in a network. The required constraints are shown in Fig. 2. We introduce two new elements, a current forcing element, CFE(I_o), and a voltage forcing element, VFE(V_o), which will be realized with more conventional elements shortly. We want the CFE(I_o) to be such that it constrains the current through branch j to be I_o, without otherwise affecting the behavior of the network. We want the VFE(V_o) to be such that it constrains the voltage across branch j to be V_o without otherwise affecting the behavior of the network.

In discussing the properties of the CFE and VFE, we use the concept of admissible or allowed pairs of voltage and current variables (v, i).[2] The set of voltage-current pairs that a system N allows can be used to completely describe that system.[3] For example, let the system under consideration, N_R, consist of a single resistor of value R. Then the system is completely described by its allowed terminal voltage and current pairs; namely, $(Ri, i) \in N_R$. Similarly, a capacitance of value C, denoted N_C, is completely described by its allowed pairs $(v, d(Cv)/dt) \in N_C$.

We now define the CFE(I_o) and VFE(V_o) in terms of their allowed pairs.

Current forcing element (I_o):

$$(0, I_o) \in N_{\mathrm{CFE}(I_o)} . \tag{7}$$

Here we postulate an element which allows no voltage drop across its terminals, and passes only a specified current I_o.

Next, we postulate an element which allows only a fixed voltage V_o to exist at its terminals, and passes no current.

Voltage forcing element (V_o):

$$(V_o , 0) \in N_{\mathrm{VFE}(V_o)} . \tag{8}$$

Figure 2 makes clear the use of these elements in constraining network variables. In Fig. 2a, the current in branch j is forced to be

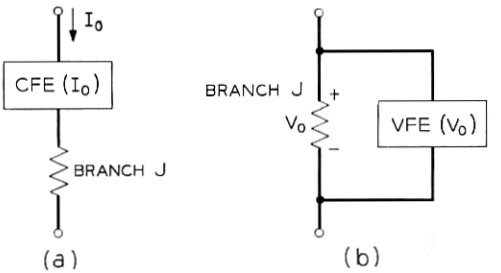

Fig. 2 — Network constraints. (a) Branch J current constrained by current forcing element (CFE); (b) Branch J voltage constrained by voltage forcing element (VFE).

I_o by inserting a CFE in series. Since the CFE(I_o) allows no voltage to exist across its terminals, its presence affects Kirchhoff's current and voltage laws only to the extent that branch j current is constrained to be I_o. Notice that this would not be the case had we inserted a current source in series with branch j. The current source would allow some voltage to exist between its terminals which would have been included in Kirchhoff's voltage law equations. Thus, a current source of value I_o would not only constrain branch j current to be I_o, but would also introduce a new degree of freedom, namely, the voltage across the current source.

Similar reasoning can be applied to Fig. 2b. Here a VFE(V_o) is applied across branch j to constrain that voltage to be V_o. Since the VFE(V_o) passes no current, Kirchhoff's laws are affected only to the extent that branch j voltage is now constrained to be V_o. The network cannot respond with a new degree of freedom, as it could if a voltage source were placed across branch j and thus allowed to introduce a new current variable in Kirchhoff's current law equations. It should be noted that the VFE(V_o), can be placed between any two nodes to constrain the voltage between those nodes; it need not be placed across a branch.

By using current sources and voltage sources in conjunction with VFE's and CFE's, current-voltage ratios may be constrained. For example, in Fig. 3a,

$$\frac{V_1}{I_1} = \frac{V_o}{I} = \frac{ZI}{I} = Z. \tag{9}$$

In Fig. 3b,

$$\frac{I_1}{V_1} = \frac{I_o}{V} = \frac{YV}{V} = Y. \tag{10}$$

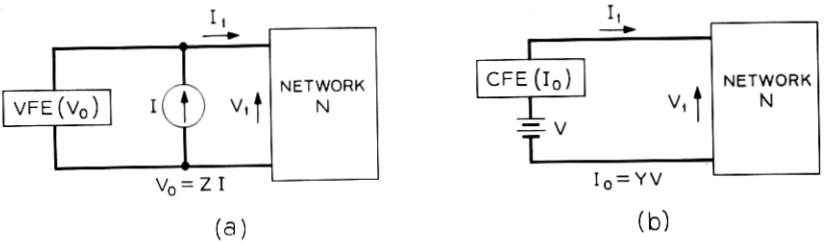

Fig. 3 — Methods of constraining current-voltage ratios. (a) Impedance forcing element [IFE(Z)]; (b) admittance forcing element [AFE(Y)].

Thus we are constraining the network N to have, in the first case, a driving point impedance Z, and in the second case, a driving point admittance Y. The configurations used to constrain impedances or admittances will be denoted impedance forcing elements, IFE(Z), and admittance forcing elements, AFE(Y). Notice that IFE's and AFE's are composed of CFE's, VFE's, and independent sources. They are useful in constraining a network to have a desired driving point impedance or admittance.

We already mentioned that VFE's and CFE's could be realized in terms of existing elements. The necessary elements are the ideal current source, the ideal voltage source, and the nullator, a somewhat "pathological" network element introduced by Tellegen.[4] Returning to the allowed pair concept, the nullator is defined to be a two-terminal element for which the only allowed voltage-current pair is (0, 0). It can be looked upon as a simultaneous open and short circuit, since it allows only zero voltage at its terminals and passes no current.

From its definition, one could not hope to physically realize and isolate such a device. However it's characteristics may be observed at the input to an operational amplifier imbedded in a feedback network, where the input is at a virtual ground (short circuit) and yet passes no current (open circuit). The nullator is represented schematically in Fig. 4.

By appropriate connections of voltage sources, current sources, and nullators, the VFE's and CFE's may be realized as in Fig. 5. Remembering that the nullator passes zero current and has zero voltage across its terminals, the equivalents of Fig. 5 becomes clear. In

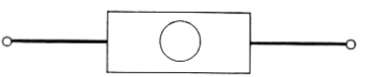

Fig. 4 — Schematic representation of nullator.

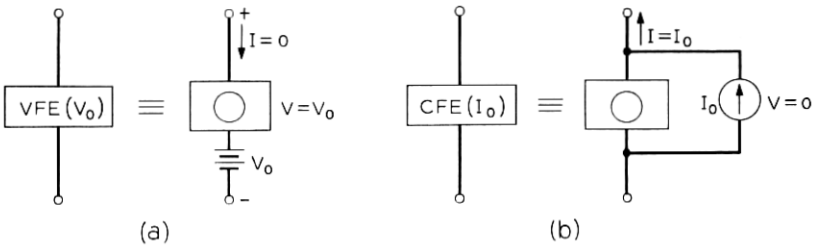

Fig. 5 — Equivalent circuits for VFE and CFE using nullators.

Fig. 5a, the terminal voltage must be V_o, and since no current exists in the element the combination voltage source and nullator is by definition a VFE(V_o). In Fig. 5b, a current I_o exists at the terminals but no voltage drop exists across the terminals. Thus by definition, the combination current source and nullator is a CFE(I_o).

IV. ADDING FREEDOM TO THE NETWORK

In the previous section, we placed constraints on the network that would generally lead to a set of inconsistent equations if all the elements were also specified. However, if some network elements are variable, we can determine how the constraints affect the voltage-current relations at the variable element terminals, and then choose variable elements in such a way as to be consistent with these $v - i$ relations.

We propose two methods of characterizing the variable elements. First, since the element is variable, we can ascribe no functional relation between the voltage and current of that branch. This is handled in writing the nodal equations for the network by explicitly adding the currents through variable elements into the equations, rather than first transforming them into voltage variables through a functional relation of the form

$$i_b = Y_b v_b \tag{11}$$

where the b implies the variable refers to some branch. The nodal equations are of the form

$$[\mathbf{Y}_f]\mathbf{V}] = \mathbf{I}_S] + [\mathbf{C}]\mathbf{I}], \tag{12}$$

where

$\mathbf{V}]$ is an n-vector of node voltages.

$\mathbf{I}_S]$ is an n-vector of forcing currents at each node.

$[\mathbf{Y}_f]$ is the $n \times n$ nodal admittance matrix of the fixed portion of the network.

$\mathbf{I}]$ is an r-vector of unknown currents through variable elements (r is the number of variable elements).

$[\mathbf{C}]$ is the $n \times r$ node cutset matrix for the graph of variable elements.

$\mathbf{I}]$ and $\mathbf{V}]$ are both vectors of network variables, and may be combined by matrix partitioning as

$$[-\mathbf{C} \mid \mathbf{Y}_f] \left[\frac{I}{V}\right] = I_s]. \tag{13}$$

Equation (13) describes a network in which some element values can be chosen to meet the given constraints. In the remainder of this paper, we combine the added degrees of freedom given by the variable elements in equation (13) with the constraints imposed by the CFE's and VFE's. All networks, satisfying the VFE and CFE constraints and the specified topology, with be generated.

A simple example will help clarify these concepts. Figure 6 is the network of Fig. 1, with the 1-ohm resistor replaced by a known resistance of R ohms. Currents I_1 and I_2 are those carried by the variable conductances G_1 and G_2, respectively. The set of nodal equations is

$$\begin{bmatrix} 1/R & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \begin{bmatrix} -1 & 0 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{14}$$

Rearranging into the form of equation (13),

$$\left[\begin{array}{cc:cc} 1 & 0 & 1 & 0 \\ -1 & 1 & 0 & 0 \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}. \tag{15}$$

From this example, the method of generating equation (13) should become clear.

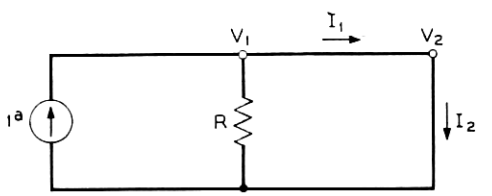

Fig. 6 — Simple design problem.

The second approach useful in dealing with variable elements in a network is the introduction of another pathological element, the norator, shown in Fig. 7, also introduced by Tellegen.[4] The norator is a two-terminal element with allowed pairs (v, i), with v and i independent and arbitrary. Thus, any voltage and current may appear across its terminals simultaneously, which is the property that we desire of variable elements. We do not wish to force any functional relation between the voltage across and the current through variable elements. We wish only to observe constraints that may be imposed on the $v - i$ relations by the VFE's and CFE's. The norator allows the network the extra degree of freedom taken away by the introduction of nullators.

V. FORMULATION OF NETWORK EQUATIONS

Since the introduction of nullators and norators into a network will generally introduce singularities into the corresponding equations, we call the approach we are considering the method of singular imbedding. It has been demonstrated that the design problem can be reduced to the appropriate imbedding of nullators, norators, and independent voltage and current sources. Let us now examine the effect of such imbedding on the network equilibrium equations. Since a nodal admittance formulation is used, it is important to determine the effect of nullators and norators on the admittance matrix.

Independent voltage sources may be conveniently incorporated into an admittance formulation. If a series impedance exists with the voltage source, application of Norton's Theorem is sufficient. If no series impedance exists, the introduction of positive and negative impedances is necessary in transforming the voltage source to an independent current source (see Fig. 8).

The effect of nullators and norators upon the admittance matrix of a network has been considered by A. C. Davies.[5] Let us write the nodal equations for the network with all nullators and norators removed. The equations are of the form

$$[\mathbf{Y}_o][\mathbf{V}] = \mathbf{I}_s] \tag{16}$$

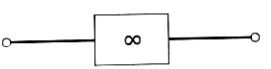

Fig. 7 — Schematic representation of norator.

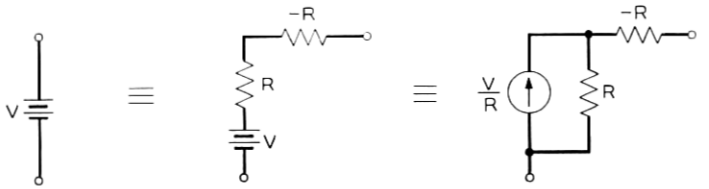

Fig. 8 — Equivalent circuit for ideal voltage source.

where

$[\mathbf{Y}_o]$ is the admittance matrix of the network with nullators and norators removed

$\mathbf{V}]$ is the vector of node voltages with respect to ground

$\mathbf{I}_S]$ is the vector of currents injected into each node.

Suppose now that a nullator is connected between nodes i and j. Since the nullator passes only zero current, the current law equations at those nodes are not affected. However, since there is zero voltage across the nullator, V_i and V_j are now constrained to be equal. Call this new value V_{ij}. Clearly, one degree of freedom has been removed from the network response. In addition to the matrix equation (16), one equation of the form

$$V_i = V_j \tag{17}$$

is added for each nullator imbedded in the network. Thus, if k nullators are imbedded, k additional constraint equations are added.

Two viewpoints can be taken here. First, the original set of equations, equation (16), has been appended by a set of the form

$$[\mathbf{B}]\mathbf{V}] = \mathbf{0}] \tag{18}$$

where

$\mathbf{V}]$ is the n-vector of node voltages.

$[\mathbf{B}]$ is a $k \times n$ matrix of -1, 0, 1 entries expressing the set of constraints of equation (17) for the k nullators.

The final set of equations becomes

$$\left[\begin{array}{c} \mathbf{Y}_o \\ \hline \mathbf{B} \end{array}\right] \mathbf{V}] = \left[\begin{array}{c} \mathbf{I}_S \\ \hline \mathbf{0} \end{array}\right]. \tag{19}$$

A second approach to the problem was suggested by Davies.[5] In

the nodal equations below

$$\begin{bmatrix} y_{11} & \cdots & y_{1i} & \cdots & y_{ij} & \cdots & y_{1n} \\ y_{21} & & y_{2i} & & y_{2j} & & \\ \vdots & & & & & & \\ y_{n1} & \cdots & y_{ni} & \cdots & y_{nj} & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_i \\ \vdots \\ V_j \\ \vdots \\ V_n \end{bmatrix} = I_S] \tag{20}$$

the addition of a nullator between nodes i and j makes $V_i = V_j = V_{ij}$. The ith and jth column of the Y matrix are both multiplied by V_{ij}, thus they may be added and the equations written as

$$\begin{bmatrix} y_{11} & \cdots & (y_{1i} + y_{1j}) & \cdots & y_{1n} \\ y_{21} & & (y_{2i} + y_{2j}) & & y_{2n} \\ \vdots & & & & \\ y_{n1} & & (y_{ni} + y_{nj}) & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_{ij} \\ \vdots \\ V_n \end{bmatrix} = I_S]. \tag{21}$$

The addition of k independent nullators (no nullator loops) causes k additions of columns of Y and reduces the dimension of $V]$ by k. We denote the reduced set of equations by

$$[\mathbf{Y}'_o]_{n\times(n-k)}\ V']_{(n-k)\times 1} = I'_S]_{n\times 1}. \tag{22}$$

In either interpretation, we observe that the resulting set of equations is no longer square. In the first interpretation, we are increasing the dimensionality of the vector space that the column vectors must span, without adding new basis vectors to span that space. In general, the equations will be inconsistent. In the second interpretation, we are keeping the dimension of the space fixed, but reducing the number of vectors available to form a basis and the space may no longer be spanned. Again inconsistencies will generally arise. In either interpretation, the inconsistencies are to be expected since nullators (VFE's or CFE's) have been introduced to constrain network variables.

Let us now examine the way in which variable elements (additional degrees of freedom) remove these inconsistencies. Again two points of view may be taken. One provides us with new basis vectors to span

the space of possible injected current vectors $\mathbf{I}_S]$, the second reduces the dimensionality of the space of $\mathbf{I}_S]$ in order that the existing number of basis vectors might again span the space.

Section III gives the essence of the first interpretation with the important result, equation (13). Observe that imbedding variable elements in a network provides an additional set of column vectors, namely, those of $[-\mathbf{C}]$, that may be used as basis vectors in spanning the space of possible $\mathbf{I}_S]$. Thus, if one has complete freedom in selecting variable elements, a set of column vectors, the columns of $[-\mathbf{C}]$ can always be found to assure that the space of all possible $\mathbf{I}_S]$ will be spanned, regardless of how the nullators reduce the space of the column vector of the $\mathbf{Y}$ matrix. This concept, which involves growing new elements to satisfy imposed constraints, will be the subject of future study.

A second approach in handling the freedom introduced by variable elements is to replace each variable element by a norator, as suggested in Section III. The method of Davies may then be employed to analyze the network containing norators.[5] Again assume that the admittance matrix $\mathbf{Y}_o$ of the network without nullators and norators is available. Thus,

$$[\mathbf{Y}_o]\mathbf{V}] = \mathbf{I}_S]. \tag{23}$$

Now suppose that a norator is connected between nodes h and k, and that the reference direction for the arbitrary norator current I_o is from h to k. The current-law equations for nodes h and k will be of the form

$$I_{Sh} - I_o = \sum_i Y_{hi}v_i \tag{24}$$

$$I_{Sk} + I_o = \sum_i Y_{ki}v_i. \tag{25}$$

Since I_o is arbitrary, and is not needed to solve for the node voltages, adding the two equations gives

$$I_{Sh} + I_{Sk} = \sum_i (Y_{hi} + Y_{ki})v_i. \tag{26}$$

This corresponds to the addition of rows h and k of the nodal equations of the network without norators. Thus for a network containing n nodes and r norators, only $n - 1 - r$ independent equations can be written.

Observe in Fig. 9 that the effect of connecting the norator between nodes h and k is to replace the nodal equations for nodes h and k

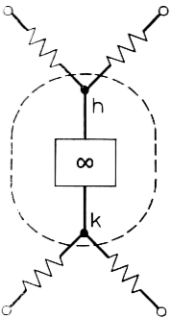

Fig. 9 — Effect of connecting norator between two nodes.

by a single current law equation for the ambit (broken line) surrounding both nodes h and k. Thus any functional relation between the current and voltage of branch j is removed, as is desired for a variable element.

To summarize thus far, the following manipulations may be performed on the network current law equations to deal with VFE's, CFE's and variable elements. To include network constraints, first imbed the CFE's and VFE's. Write the Y matrix with nullators removed. Then reduce the matrix by adding appropriate columns. This may be stated compactly by a matrix transformation as[5]

$$\mathbf{I}_S] = [\mathbf{Y}_0][\mathbf{U}_c]\mathbf{V}] \tag{27}$$

where $[\mathbf{U}_c]$ is a matrix obtained from the unit matrix by adding columns corresponding to nodes between which nullators are connected. Since the transformation $[\mathbf{U}_c]$ is singular, not all components of $\mathbf{V}]$ are determined. The undetermined ones are found from the relation

$$[\mathbf{B}]\mathbf{V}] = \mathbf{0}]. \tag{28}$$

To include variable elements, either

(*i*) Augment the $\mathbf{Y}$ matrix of the fixed portion of the network with the node cutset matrix of the graph of the variable elements to get

$$\left[-\mathbf{C} \,\vdots\, \mathbf{Y}_a\right] \left.\frac{\mathbf{I}}{\mathbf{V}}\right] = \mathbf{I}_S] \tag{29}$$

or

(*ii*) Add the current law equation corresponding to nodes to which a nullator is connected. This is compactly stated by a matrix transforma-

tion as[5]

$$[\mathbf{U}_r]\mathbf{I}_S] = [\mathbf{U}_r][\mathbf{Y}_o]\mathbf{V}] \tag{30}$$

where $[\mathbf{U}_r]$ is a matrix obtained from the unit matrix by adding rows corresponding to nodes between which norators are connected. The vector of currents through variable resistors is then formed by equation (29).

VI. SOLVING THE NETWORK EQUATIONS

We now wish to solve the set of equations after imbedding CFE's, VFE's, and variable elements. We assume equation (29) to be our starting point. A similar formulation may be made using equation (30) as the starting point. CFE's and VFE's are imbedded, variable elements are specified, and nullators are removed to generate the set of equations

$$\left[-\mathbf{C} \mid \mathbf{Y}_o\right] \left[\frac{\mathbf{I}}{\mathbf{V}}\right] = \mathbf{I}_S]. \tag{31}$$

Addition of nullators to the network adds the set of equations

$$\mathbf{B}\mathbf{V}] = \mathbf{0}] \tag{32}$$

and, from equation (27), the corresponding transformation $[\mathbf{U}_c]$ on the admittance matrix. Thus the final set of equations becomes

$$\left[\begin{array}{c|c} -\mathbf{C} & \mathbf{Y}_f\mathbf{U}_c \\ \hline \mathbf{0} & \mathbf{B} \end{array}\right] \left[\frac{\mathbf{I}}{\mathbf{V}}\right] = \left[\frac{\mathbf{I}_S}{\mathbf{0}}\right]. \tag{33}$$

As seen in the previous section, the transformation $[\mathbf{U}_c]$ (which adds columns of $\mathbf{Y}_f$) is consistent with the set of equations $[\mathbf{B}]\mathbf{V}] = 0$. Thus the second matrix equation in equation (33) will always have a solution, provided the first one does. It remains only to solve

$$\left[-\mathbf{C} \mid \mathbf{Y}_f\mathbf{U}_c\right] \left[\frac{\mathbf{I}}{\mathbf{V}}\right] = \mathbf{I}_S]. \tag{34}$$

in order to determine the proper element values. Let

$$\left[\frac{\mathbf{I}}{\mathbf{V}}\right]_{(r+n-k)\times 1} = \mathbf{x}].$$

By using the Gauss–Jordan method one can bring these equations into the form

$$\left[\begin{array}{c|c} \mathbf{U} & \mathbf{Q} \\ \hline \mathbf{0} & \mathbf{0} \end{array}\right] \left[\frac{\mathbf{X}_1}{\mathbf{X}_2}\right] = \left[\frac{\mathbf{I}_{S1}}{\mathbf{I}_{S2}}\right] \tag{35}$$

where

$\mathbf{X}_1|\mathbf{X}_2]$ is a vector of node voltages and currents through variable resistors,

$[\mathbf{U}]$ is the unit matrix,

$[\mathbf{Q}]$, $\mathbf{I}_{S1}]$, $\mathbf{I}_{S2}]$ are the resulting submatrices after transformation.

If $\mathbf{I}_{S2}] = 0$ (the equations are consistent), the first equation can be solved for $\mathbf{X}_1]$ in terms of $\mathbf{X}_2]$.

$$\mathbf{X}_1 = \mathbf{I}_{S1}] - [\mathbf{Q}]\mathbf{X}_2]. \tag{36}$$

The case $\mathbf{I}_{S2}] \neq 0$ implies that there are no values of variable elements consistent with the imposed constraints. For $\mathbf{I}_{S2}] = \mathbf{0}]$, equation (36) generates all solutions to the problem. Some network variables $\mathbf{X}_2]$ can be chosen arbitrarily and the remaining variables $\mathbf{X}_1]$ determined. At each setting of $\mathbf{X}_2]$ the variable elements can be determined since all node voltages and currents through variable elements are known.

Thus

$$Z_i = \frac{V_{i1} - V_{i2}}{I_i} \qquad \text{for} \qquad i = 1, r \tag{37}$$

where $i1$ and $i2$ are connection nodes of the ith variable element. By allowing the free variables $\mathbf{X}_2]$ to take on a continuum of values, all solutions to the problem are determined directly.

Returning to the example already discussed (Fig. b), let us apply the method of singular imbedding. The circuit is redrawn in Fig. 10 with the introduction of a VFE to constrain the voltage between nodes 1 and 2 to be 0.1* volt. With the nullator removed, a set of nodal equations is written in the form of equation (13)

$$\left[\begin{array}{cc:ccc} 1 & 0 & 1/R & 0 & 0 \\ -1 & 1 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 1 \end{array}\right] \left[\begin{array}{c} I_1 \\ I_2 \\ \hdashline V_1 \\ V_2 \\ V_3 \end{array}\right] = \left[\begin{array}{c} 1 \\ -0.1 \\ 0.1 \end{array}\right]. \tag{38a}$$

The introduction of a nullator between nodes 1 and 3 results in the addition of the corresponding columns and the equality $V_1 = V_3 =$

* Since the nullator passes zero current, the series battery in the VFE model may have a nonzero resistance and still maintain the proper terminal voltage. Thus the introduction of positive and negative resistances are unnecessary here.

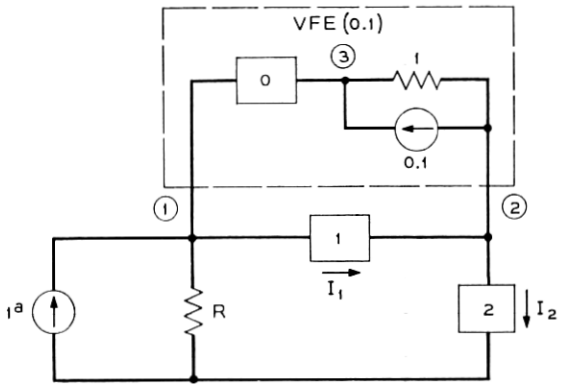

Fig. 10 — Network after singular imbedding.

V_{13}. Thus,

$$\begin{bmatrix} 1 & 0 & 1/R & 0 \\ -1 & 1 & -1 & 1 \\ 0 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_{13} \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ -0.1 \\ 0.1 \end{bmatrix}. \tag{38b}$$

With $R = 1$ ohm for ease of visualization, elementary row operations yield

$$\left[\begin{array}{ccc:c} 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & -1 \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ V_{13} \\ \hdashline V_2 \end{bmatrix} = \begin{bmatrix} 0.9 \\ 0.9 \\ 0.1 \end{bmatrix}. \tag{39}$$

Thus,

$$\begin{bmatrix} I_1 \\ I_2 \\ V_{13} \end{bmatrix} = \begin{bmatrix} 0.9 \\ 0.9 \\ 0.1 \end{bmatrix} - V_2 \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix}. \tag{40}$$

It is clear that V_2 can take on arbitrary values while maintaining the constraints. We will demonstrate this for two particular values of V_2. For $V_2 = 0$

$$\begin{bmatrix} I_1 \\ I_2 \\ V_{13} \\ V_2 \end{bmatrix} = \begin{bmatrix} 0.9 \\ 0.9 \\ 0.1 \\ 0 \end{bmatrix},$$

$$R_1 = \frac{V_1 - V_2}{I_1} = \frac{1}{9},$$

$$R_2 = \frac{V_2}{I_1} = 0.$$

It is easily verified that these values, when substituting into the circuit of Fig. 1, result in $V' = V_1 - V_2 = 0.1$ volt.

Similarly for $V_2 = 0.6$ volt

$$\begin{bmatrix} I_1 \\ I_2 \\ V_{13} \\ V_2 \end{bmatrix} = \begin{bmatrix} 0.3 \\ 0.3 \\ 0.7 \\ 0.6 \end{bmatrix}$$

and $R_1 = \frac{1}{3}$, $R_2 = 2$.

Again it is easily verified that $V' = V_1 - V_2 = 0.1$ volt. With this simple example in mind, let us consider the solution of more complicated networks by computer.

VII. COMPUTER SOLUTION

A program has been written to solve the design problem for resistive networks. The program performs the following operations

(*i*) Accepts input of circuit description in conversational mode. The circuit may contain resistors (both fixed and variable), VFE's CFE's batteries, independent current sources, and current controlled current sources.

(*ii*) Generates $\mathbf{C}$, $\mathbf{Y}_t$, and $\mathbf{I}_s$ matrices for the network.

(*iii*) Reduces equations to triangular form by a Gaussian reduction which pivots around largest elements in array.

(*iv*) Those variables not in the basis after gaussian elimination are passed to the right side and stepped through specified range. Resistance values are printed for each setting of the free variables. Each set of resistance values will satisfy the given constraints.

Four examples demonstrate the flexibility of the method. Suppose in the circuit of Fig. 11 one wishes to choose R_1 and R_2 to provide

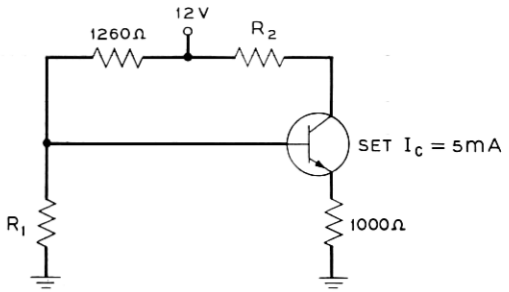

Fig. 11 — Transistor design problem.

a collector current of 5 mA. A CFE of value 0.005 is placed in series with the collector and the circuit of Fig. 12 is fed into the program as in Table I. After the program sets up the equations and performs the gaussian elimination, it prints, that the voltage at node 3 is free. It can be arbitrarily chosen to generate sets of solutions.

This free voltage is then, at the user's request, stepped from 7 volts to 10 volts in 1 volt increments. Combinations of R_1 and R_2 which provide a collector current of 5 mA are printed in Table I. To verify these results the program DCANAL[7] was used to determine the transistor collector current for the fifth set of resistor values. As the table shows, the collector current is 5 mA.

A second example involves simultaneously constraining $I_c = 5$ mA and VCE = 5 volts. As Fig. 13 shows, R_1, R_2, and R_3 are variable. The network with a VFE and CFE imbedded is shown in Fig. 14, and the results given in Table II. Verification of the first set of resistance values is given. Observe that $I_c = 5$ mA and VCE = 5 volts.

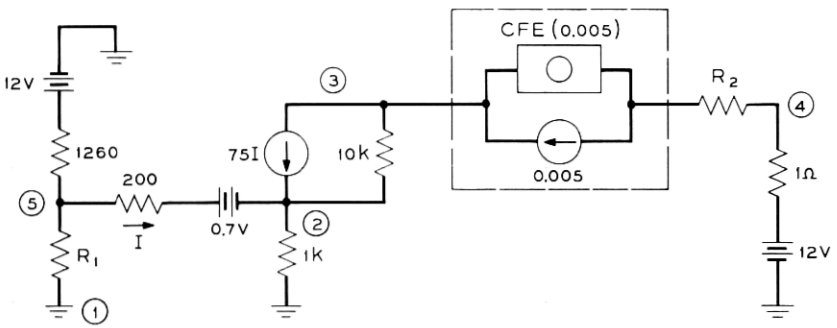

Fig. 12 — Network after transistor modelling and singular imbedding.

TABLE I—PRINTOUT OF THE SESSION TO SOLVE THE CIRCUIT OF FIGURE 11

```
 TYPE NO. OF BRANCHES,NODES,CONTROLLED SOURCES,BATTERIES,CURRENT SOURCES
A=7 5 1 3 0
TYPE BRANCH RESISTANCES
B=1. 1. 1260. 200. 1.E3 1.E4 1.
TYPE FOR EACH BRANCH: INITIAL NODE,FINAL NODE,BATTERY NO.
C=1 5 1   4 3 1   1 5 2   5 2 3   1 2 1   3 2 1   1 4 2
TYPE VALUES OF BATTERIES
D=0. 12. -.7
TYPE FOR EACH CONTROLLED SOURCE: BRANCH NO. AND CONTROLLING BRANCH NO.
E=6 4
TYPE VALUES OF BETAS
F=75.

OPTION COMMANDS=DESIGN R

TYPE NO. VAR. RESISTANCES,NO. VOLTAGE CONSTRAINTS, AND NO CURRENT CONSTRAINTS
I=2 0 1
TYPE BRANCH NO. OF VARIABLE RESISTANCES
J=1 2
TYPE BRANCH CURRENTS BEING CONSTRAINED
M=6
TYPE VALUE OF EACH CURRENT BEING CONSTRAINED
N=.005

THE FOLLOWING NODE VOLTAGES ARE FREE
      3

ENTER LOWER LIMIT AND INCREMENT FOR EACH FREE VARIABLE AND NO. OF SETTINGS
O=7. 1. 4

THE FREE VARIABLE= 7.
R( 1)=1.1850722E+03
R( 2)=9.9900005E+02

THE FREE VARIABLE= 8.
R( 1)=1.1841104E+03
R( 2)=7.9900003E+02

THE FREE VARIABLE= 9.
R( 1)=1.1831496E+03
R( 2)=5.99000000E+02

THE FREE VARIABLE= 10.
R( 1)=1.1821898E+03
R( 2)=3.9899998E+02

DESIGN COMMAND=KEEP
ENTER VALUES OF FREE VARIABLES FOR DESIRED SET
=10.

OPTION COMMAND=TRAN ALL

        VCE        IC
TRANS #
  1   4.9398502  4.9999999E-03
```

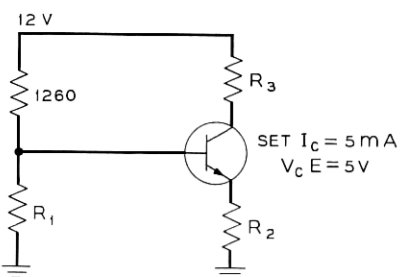

Fig. 13 — Transistor design problem.

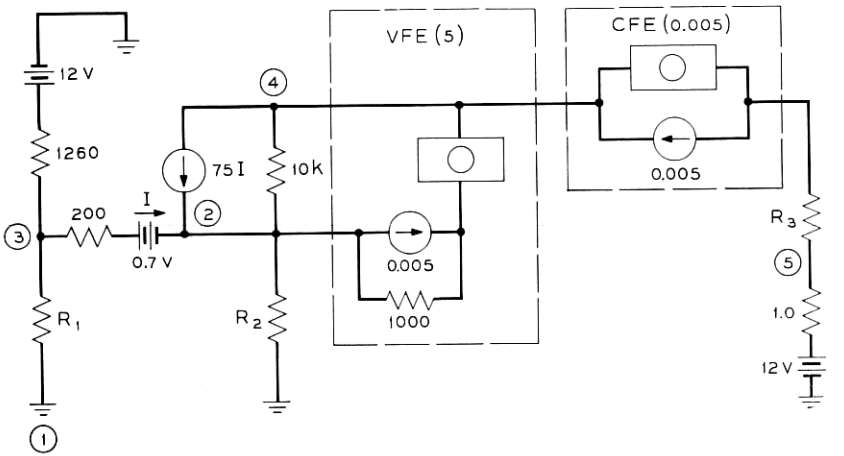

Fig. 14 — Network after transistor modelling and singular imbedding.

A third example involves the rather complex three transistor circuit illustrated in Fig. 15. The imbedding of VFE's and CFE's to constrain collector emitter voltages to 5 volts, and collector currents to 10 mA is shown.

Table III illustrates the results of a computer solution to the problem by the method of singular imbedding. Observe that currents through variable resistors 10 and 14 can be arbitrarily chosen and sets of resistors R_{10} through R_{18} generated. Four such sets are presented in Table III. Observe the results of an analysis indicating one such set properly biases the network. Table IV presents the results of an optimization program, based on pattern search,[1] to bias the network, for which forty-eight exploratory moves and 105 pattern moves were required. Each exploratory move involves between eight and 16 circuit analyses. Each pattern move involves an average of four analyses. Thus, approximately 1000 matrix inversions are required. Since each inversion involves $(n^3)/3$ operations, the number of operations to generate a single bias network $\approx$243,000.

Singular imbedding increases the number of nodes from 9 to 15. However, only one matrix inversion is required to generate a solution. Thus the number of operations $\cong n^3/3 \cong 1125$.

Singular imbedding increases the efficiency in finding a solution to this problem by a factor of approximately 200. What is even more important is the ease with which equivalent networks are generated. Each equivalent network is generated by a matrix multiplication of

TABLE II—PRINTOUT OF THE SESSION TO SOLVE THE CIRCUIT OF FIGURE 13

```
TYPE NO. OF BRANCHES,NODES,CONTROLLED SOURCES,BATTERIES,CURRENT SOURCES
A=7 5 1 3 0
TYPE BRANCH RESISTANCES
B=1. 1. 1. 1260. 200. 1.E4 1.
TYPE FOR EACH BRANCH: INITIAL NODE,FINAL NODE,BATTERY NO.
C=1 3 1   1 2 1   5 4 1   1 3 2   3 2 3   4 2 1   1 5 2
TYPE VALUES OF BATTERIES
D=0. 12. -.7
TYPE FOR EACH CONTROLLED SOURCE: BRANCH NO. AND CONTROLLING BRANCH NO.
E=6 5
TYPE VALUES OF BETAS
F=75.

OPTION COMMANDS=DESIGN R

TYPE NO. VAR. RESISTANCES,NO. VOLTAGE CONSTRAINTS, AND NO CURRENT CONSTRAINTS
I=3 1 1
TYPE BRANCH NO. OF VARIABLE RESISTANCES
J=1 2 3
FOR EACH VOLTAGE CONSTRAINT, TYPE PLUS AND MINUS NODES
K=4 2
TYPE VALUE OF EACH VOLTAGE CONSTRAINT
L=5.
TYPE BRANCH CURRENTS BEING CONSTRAINED
M=6
TYPE VALUE OF EACH CURRENT BEING CONSTRAINED
N=.005

THE FOLLOWING NODE VOLTAGES ARE FREE
      3

ENTER LOWER LIMIT AND INCREMENT FOR EACH FREE VARIABLE AND NO. OF SETTINGS
 0=4. 2. 2

THE FREE VARIABLE= 4.
R( 1)=6.3601035E+02
R( 2)=6.4979250E+02
R( 3)=7.4140005E+02

THE FREE VARIABLE=6.
R( 1)=1.2760788E+03
R( 2)=1.0450373E+03
R( 3)=3.4140001E+02

DESIGN COMMAND=KEEP
ENTER VALUES OF FREE VARIABLES FOR DESIRED SET
=4.

OPTION COMMANDS=TRAN ALL

        VCE              IC
TRANS #
   1   5.0000E+00    5.0001E-03
```

the vector of free variables, which is stepped through a specified range, and the matrix of vectors not taken into the basis after triangulation. In this case the matrix is 19×2 and the vector of free variables is 2×1. Each multiplication involves $2 \times 19 = 38$ operations. This means that up to 14,000 equivalent networks can be generated with the same number of operations needed to give one solution by optimization techniques.

The value of singular imbedding is apparent here. Only one equation need be solved, and from it, all solutions are generated.

As a fourth example, a network was designed for a specified z_{11}

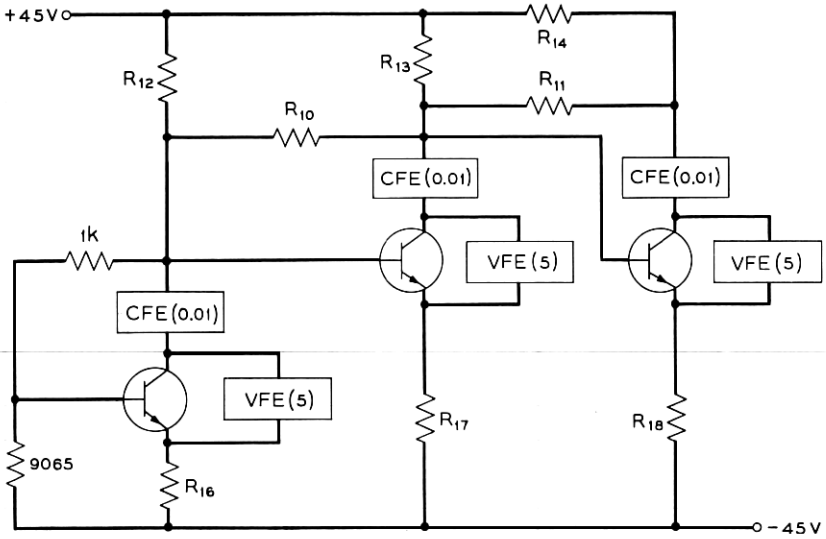

Fig. 15 — Three transistor network with VFE's and CFE's imbedded for desired biasing.

and z_{21} simultaneously. The circuit is given in Fig. 16. R_1, R_2, and R_3 are to be selected to give $z_{11} = \frac{2}{3}$ and $z_{21} = \frac{1}{3}$. After proper imbedding of VFE's and CFE's the network of Fig. 17 results. Table V gives the results of a computer run to design the circuit. The third set, $R_1 = R_2 = R_3 = 2$ is shown to give the desired z-parameters through the $Y - \Delta$ transformation of Fig. 18.

VIII. RESISTOR CONSTRAINTS

In many design problems it is desirable to constrain the values that the parameters take to lie within certain limits. For example, in biasing a transistor network, although solutions in which some resistors are negative are mathematically correct, in practice such networks are unacceptable.

If the designer has a good feeling for the circuit he is working with, his choice of the free variables resulting from gaussian elimination with maximum pivoting will usually yield resistors with positive values. There are, however, instances involving multiple feedback paths where intuition cannot always be relied upon. In these instances it is possible that the values given by the designer to the free variables yield negative resistances. Furthermore, it may be

TABLE III—PRINTOUT OF THE SESSION TO SOLVE THE CIRCUIT OF FIGURE 15

```
THE FOLLOWING BRANCH CURRENTS ARE FREE
          10
          14

ENTER LOWER LIMIT AND INCREMENT FOR EACH FREE VARIABLE AND NO. OF SETTINGS
 0=1.E-3  1.E-3  1.E-2 .2E-2  2

THE FREE VARIABLES ARE
     1.000E-03      1.000E-02
R(10)=4.2366667E+03
R(11)=1.1028088E+09
R(12)=3.7008484E+03
R(13)=4.0579244E+03
R(14)=4.1685477E+03
R(16)=3.3704454E+03
R(17)=3.7811070E+03
R(18)=4.1917495E+03

THE FREE VARIABLES ARE
     2.000E-03      1.000E-02
R(10)=2.1183333E+03
R(11)=1.1372716E+09
R(12)=3.9956586E+03
R(13)=3.7284580E+03
R(14)=4.1685477E+03
R(16)=3.3704454E+03
R(17)=3.7811070E+03
R(18)=4.1917495E+03

THE FREE VARIABLES ARE
     1.000E-03      1.200E-02
R(10)=4.2366667E+03
R(11)=2.1183293E+03
R(12)=3.7008484E+03
R(13)=4.9290360E+03
R(14)=3.4737897E+03
R(16)=3.3704454E+03
R(17)=3.7811070E+03
R(18)=4.1917495E+03

THE FREE VARIABLES ARE
     2.000E-03      1.200E-02
R(10)=2.1183333E+03
R(11)=2.1183293E+03
R(12)=3.9956586E+03
R(13)=4.4512615E+03
R(14)=3.4737897E+03
R(16)=3.3704454E+03
R(17)=3.7811070E+03
R(18)=4.1917495E+03

DESIGN COMMAND=KEEP
ENTER VALUES OF FREE VARIABLES FOR DESIRED SET
=2.E-3  1.E-2

OPTION COMMANDS=TRAN ALL
                VCE             IC
TRANS #
   1        5.0000E+00      1.0000E-02
   2        5.0000E+00      1.0000E-02
   3        5.0000E+00      9.9999E-03
```

difficult to explore the space of the free variables looking for regions where all the resistors are positive.

One possibility for finding positive resistor regions is to use an optimization technique in which, considering the free variables as adjustable parameters, the sum of the absolute magnitudes of the

negative resistors is reduced to a minimum. If there exist solutions with all resistors positive, the minimum (zero) hopefully would be found automatically by the optimization routine.

This optimization is more efficient than solving the problem by exploring a space in which all the variable resistors are parameters to be adjusted.[1]

Although the method given has been tried with success, a superior method having several advantages over the one proposed is explained in Section IX. The method avoids some of the most important problems associated with nonlinear programming.

Some of these problems are:

(*i*) The routine may get trapped in local minima.

(*ii*) Depending on the shapes of the surfaces involved and on the methods used the convergence towards the minimum may be very slow.

(*iii*) If the optimization is with constraints the nonlinear constraints are usually difficult to handle.

If it were possible to reduce the problem to a linear programming problem, the following would have been gained:

(*i*) If the problem has a finite minimum it will be achieved in a

TABLE IV—PRINTOUT OF OPTIMIZATION PROGRAM

```
INITIAL BRANCH RESISTANCES

R(10)=0.5000E+04
R(11)=0.5000E+04
R(12)=0.3000E+04
R(13)=0.3000E+04
R(14)=0.3000E+04
R(16)=0.3000E+04
R(17)=0.3000E+04
R(18)=0.3000E+04

EXPLORATORY MOVES      48

PATTERN MOVES          105

FINAL BRANCH RESISTANCES

R(10)=0.3730E+04
R(11)=0.4340E+04
R(12)=0.3732E+04
R(13)=0.4377E+04
R(14)=0.3795E+04
R(16)=0.3372E+04
R(17)=0.3783E+04
R(18)=0.4197E+04

TRANSISTOR OPERATING POINTS

TRANS #          VCE          IC
  1         5.000E+00     1.000E-02
  2         5.000E+00     1.000E-02
  3         5.000E+00     1.000E-02
```

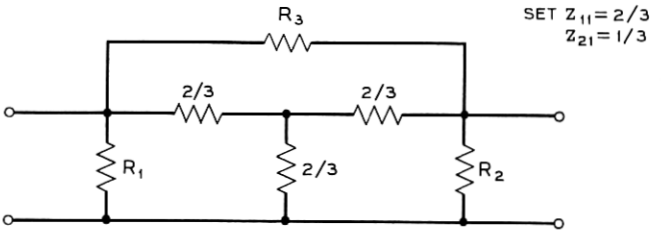

Fig. 16 — Z-parameter design problem.

finite number of steps. No local minima which are not also global minima exist.

(*ii*) Algorithms exist which converge to the minimum efficiently.

(*iii*) The linear constraints generally complicate the problem only moderately.

In Section IX the problem of biasing transistor networks is reduced to a linear programming problem.

IX. APPLIED LINEAR PROGRAMMING

Let us start by assuming a network in which the designer knows the correct signs of the node voltages with respect to the datum and the direction of the currents in the variable resistors. Generally the former is an easy task since it only involves knowing the nodes with the lowest potential. If this node is chosen as the datum, all the node voltages will be positive. Knowing the correct direction of the current through the variable resistors requires a better understanding of the circuit operation. Furthermore, there may be solutions in which the current through some resistors may flow in either direction. For this reason this requirement will eventually be relaxed.

Linear programming requires the right side vector of equation (33)

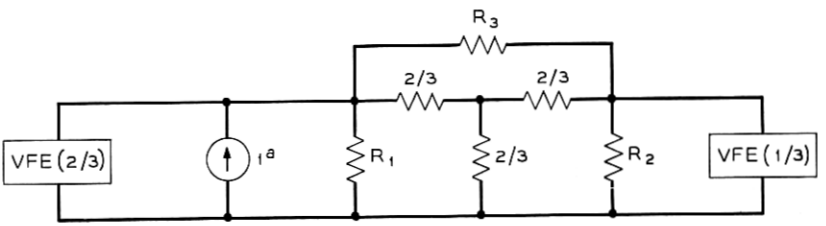

Fig. 17 — Network after singular imbedding

TABLE V—PRINTOUT OF THE SESSION TO SOLVE THE CIRCUIT OF FIGURE 16

```
TYPE NO. OF BRANCHES,NODES,CONTROLLED SOURCES,BATTERIES,CURRENT SOURCES
A=6 4 0 1 1
TYPE BRANCH RESISTANCES
B=1. 1. 1. .66666667 .66666667 .66666667
TYPE FOR EACH BRANCH: INITIAL NODE,FINAL NODE,BATTERY NO.
C=1 2 1   1 4 1   2 4 1   2 3 1   3 4 1   3 1 1
TYPE VALUES OF BATTERIES
D=0. 12. -.7
TYPE FOR EACH CONTROLLED SOURCE:BRANCH NO. AND CONTROLLING BRANCH NO.
E=6 5
TYPE VALUES OF BETAS
F=75.
TYPE FOR EACH INDEPENDENT SOURCE: INITIAL NODE AND FINAL NODE
G=1 2
TYPE VALUE OF EACH INDEPENDENT CURRENT SOURCE
H=1.

OPTION COMMANDS=DESIGN R
TYPE NO. VAR. RESISTANCES,NO. VOLTAGE CONSTRAINTS, AND NO CURRENT CONSTRAINTS
 I=3 2 0
TYPE BRANCH NO. OF VARIABLE RESISTANCES
J=1 2 3
FOR EACH VOLTAGE CONSTRAINT TYPE PLUS AND MINUS NODES
K=2 1  4 1
TYPE VALUE OF EACH VOLTAGE CONSTRAINT
L=.66666667  .33333333

THE FOLLOWING BRANCH CURRENTS ARE FREE
      1
ENTER LOWER LIMIT AND INCREMENT FOR EACH FREE VARIABLE AND NO. OF SETTINGS
0=-1.  .33333333 3

THE FREE VARIABLE = -1.0000
R( 1)= 0.66666670E+00
R( 2)=-0.66666667E+00
R( 3)=-0.66666680E+00

THE FREE VARIABLE = -0.6667E+00
R( 1)= 0.10000000E+01
R( 2)=-0.20000000E+01
R( 3)=-0.19999999E+01

THE FRE VARIABLE = -0.3333E+00
R( 1)= 0.19999997E+01
R( 2)= 0.20000000E+01
R( 3)= 0.20000013E+01
```

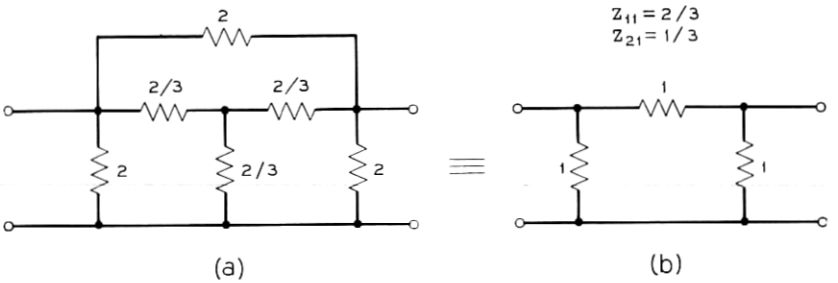

Fig. 18 — Verification of computer solution.

to have positive entries. This may be achieved by multiplying by -1 all those rows in equation (33) which have a negative entry in the right side vector and thus obtain the set of equations

$$\left[\begin{array}{c|c} \mathbf{H}_1 & \mathbf{H}_2 \\ \hline \mathbf{0} & \mathbf{H}_3 \end{array}\right] \left[\begin{array}{c} \mathbf{I} \\ - \\ \mathbf{V} \end{array}\right] = \left[\begin{array}{c} \mathbf{f} \\ - \\ \mathbf{0} \end{array}\right] \tag{41}$$

where

$$\mathbf{H} = \left[\begin{array}{c|c} \mathbf{H}_1 & \mathbf{H}_2 \\ \hline \mathbf{0} & \mathbf{H}_3 \end{array}\right]$$

is obtained from

$$\left[\begin{array}{c|c} -\mathbf{C} & \mathbf{Y}_f \mathbf{U}_c \\ \hline \mathbf{0} & \mathbf{B} \end{array}\right] \quad \text{and} \quad \left[\begin{array}{c} \mathbf{f} \\ - \\ \mathbf{0} \end{array}\right] \quad \text{from} \quad \left[\begin{array}{c} \mathbf{I}_S \\ \hline \mathbf{0} \end{array}\right]$$

by possibly multiplying some rows by -1.

To force all the branch voltages to be positive let us add the constraint

$$-[\mathbf{C}]\mathbf{V}] \geqq \mathbf{0}] \tag{42}$$

where $[\mathbf{C}]$ is the matrix appearing in equation (12).

Equation (41) and inequality (42) together with the condition

$$\left[\begin{array}{c} \mathbf{I} \\ \hline \mathbf{V} \end{array}\right] \geqq \mathbf{0}] \tag{43}$$

can be looked upon as a linear programming problem in which it is desired to find the value of a positive vector satisfying a set of linear equalities and inequalities and which minimizes the linear function where

$$z = \underline{\mathbf{D}} \left[\begin{array}{c} \mathbf{I} \\ \hline \mathbf{V} \end{array}\right] \tag{44}$$

$$\underline{\mathbf{D}} = [0, 0, \cdots, 0].$$

Since the minimization of the constant zero is of no interest, all that is required is to obtain the feasible solutions of the linear programming problem.[6]

Once the feasible solutions are obtained, the fact that the solution satisfies equation (41) guarantees that the circuit is properly biased while the positivity condition on the vectors $\underline{\mathbf{I}|\mathbf{V}}$ and $-[\mathbf{C}]\mathbf{V}]$ guarantee

that all the variable resistors are positive, since both the currents and voltages across them are positive.

To obtain the feasible solutions phase I of the two phase simplex method may be used.[6]

Phase I of the simplex method finds the basic positive solutions of the system of equations

$$\left[\begin{array}{c|c|c|c} \mathbf{H}_1 & \mathbf{H}_2 & \mathbf{0} & \mathbf{I} \\ \hline \mathbf{0} & \mathbf{H}_3 & \mathbf{0} & \mathbf{V} \\ \hline \mathbf{0} & -\mathbf{C} & -\mathbf{U} & \mathbf{w} \end{array}\right] = \left[\begin{array}{c} \mathbf{f} \\ \hline \mathbf{0} \\ \hline \mathbf{0} \end{array}\right] \tag{45}$$

where the vector $\mathbf{w}]$ (which is constrained to be positive) is a slack vector and $\mathbf{U}$ is a unit matrix.

By denoting with $\mathbf{A}$ the matrix on the left of equation (45), with $\mathbf{x}$ the column on the left, and with $\mathbf{b}$ the column on the right side, equation (45) may be written

$$\mathbf{Ax} = \mathbf{b}. \tag{46}$$

Let the dimensions be: $\mathbf{A}$, $m \times n$; $\mathbf{x}$, $n \times 1$; $\mathbf{b}$, $m \times 1$. Let $\mathbf{A}$ and $[\mathbf{A} \mid \mathbf{b}]$ have rank r. This implies equation (46) is compatible. (The case in which this is not true is of no interest since in such case no solution—whether positive or not—exists.)

Phase I of the simplex method finds positive solutions of equation (46) for r of the variables x_i, $i = 1, 2, \cdots, r$ setting the rest of the x_j, $j = r + 1, \cdots, n$ to zero.* Each one of this set is a basic feasible solution. There may be several such sets for a given problem. The totality of nonnegative solutions of equation (46) is the convex hull of the basic solutions. By extending the simplex algorithm so that once a basic feasible solution is found the other basic feasible solutions are also searched for, it is possible to obtain all basic feasible solutions.

Suppose $x^1, x^2, \cdots, x^P$ are basic feasible solutions. Then any vector x satisfying

$$\left.\begin{array}{rl} & x = \lambda_1 x^1 + \lambda_2 x^2 + \cdots + \lambda_P x^P \\ \text{with} & \\ \text{and} & \lambda_1, \lambda_2, \cdots, \lambda_P \geqq 0 \\ & \lambda_1 + \lambda_2 + \cdots + \lambda_P = 1 \end{array}\right\} \tag{47}$$

is also a feasible solution.

* In case no nonnegative solutions to equation (46) exist, the simplex algorithm is able to detect it.

If $x^1, x^2, \cdots, x^P$ is the set of all basic feasible solutions, then all the solutions of equation (47) constitute the complete set of feasible solutions.

X. RESISTORS WITH UPPER AND LOWER BOUNDS

In the previous discussion the appearance of nonnegative resistors was precluded by adding inequality (42). Often it is desirable to impose lower and upper bounds for the resistors because the technology used to realize them requires it. For example, if tantalum thin film resistors are used it is desirable to restrict them to lie between 10 and 10^5 ohms.

Let the kth variable resistor be connected from node i to node j. The value of R_k is given by

$$R_k = \frac{V_i - V_j}{I_k}.$$

If it is desired to have this resistor lie within 10 and 10^5 ohms the following conditions are imposed

$$\frac{V_i - V_j}{I_k} \geqq 10, \qquad I_k \neq 0$$

$$\frac{V_i - V_j}{I_k} \leqq 10^5, \qquad I_k \neq 0$$

which may be rewritten (recall I_k is nonnegative)

$$\left.\begin{aligned} V_i - V_j - 10I_k &\geqq 0 \\ V_i - V_j - 10^5 I_k &\leqq 0 \end{aligned}\right\}. \tag{48}$$

If instead of equation (42) inequalities similar to equation (48) are written for all variable resistors, the resulting circuits will have all variable resistors within specified upper and lower bounds (except for the possibility $I_k = 0$, which implies an open circuit, in which case the resistor disappears altogether).

The problem of biasing of transistor networks with positive resistors is equivalent to solving

$$\left[\begin{array}{c|c} \mathbf{H}_1 & \mathbf{H}_2 \\ \hline \mathbf{0} & \mathbf{H}_3 \end{array}\right] \left[\begin{array}{c} \mathbf{I} \\ \hline \mathbf{V} \end{array}\right] = \left[\begin{array}{c} \mathbf{f} \\ \hline \mathbf{0} \end{array}\right]$$

$$[\mathbf{D}_1 \mid -\mathbf{C}] \left[\begin{array}{c} \mathbf{I} \\ \mathbf{V} \end{array}\right] \geqq \left[\begin{array}{c} \mathbf{0} \\ \mathbf{0} \end{array}\right] \tag{49}$$

$$[\mathbf{D}_2 \mid -\mathbf{C}] \begin{bmatrix} \mathbf{I} \\ \mathbf{V} \end{bmatrix} \leqq \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$

$$\begin{bmatrix} \mathbf{I} \\ \mathbf{V} \end{bmatrix} \geqq \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$

where $\mathbf{D}_1$ and $\mathbf{D}_2$ are diagonal matrices whose diagonal elements contain the minima and maxima for the variable resistors. By adding positive slack vectors $\mathbf{w}_1$ and $\mathbf{w}_2$, equation (49) is equivalent to

$$\left[\begin{array}{c|c|c|c|c} \mathbf{H}_1 & \mathbf{H}_2 & \mathbf{0} & \mathbf{0} & \mathbf{I} \\ \hline \mathbf{0} & \mathbf{H}_3 & \mathbf{0} & \mathbf{0} & \mathbf{V} \\ \hline \mathbf{D}_1 & -\mathbf{C} & -\mathbf{U} & \mathbf{0} & \mathbf{w}_1 \\ \hline \mathbf{D}_2 & -\mathbf{C} & \mathbf{0} & \mathbf{U} & \mathbf{w}_2 \end{array}\right] = \begin{bmatrix} \mathbf{f} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{50}$$

where $\mathbf{U}$ is a unit matrix and the vector on the left is restricted to be nonnegative.

XI. RELAXING SIGN CONDITIONS

So far it has been assumed that the direction of the current flow in variable resistors is known beforehand. This condition may not hold for some cases and hence it is desirable to relax it.

When a variable in a linear programming problem is not required to be positive it is customary to write it as the difference of two positive quantities. Thus if I_k and $V_j - V_k = V$ are not required to be positive one may write

$$I_k = I_{k'} - I_{k''}$$

$$V_l = V_{l'} - V_{l''}$$

where $I_{k'}$, $I_{k''}$, $V_{l'}$, $V_{l''} \geqq 0$.

A current I_k of variable sign may be restricted to have a magnitude no less than $I_{ok} \geqq 0$ by imposing the pair of conditions*

$$I_k \geqq I_{ok} \quad \text{or} \quad -I_k \geqq I_{ok}\,. \tag{51}$$

Likewise a branch voltage V_l of variable sign across a resistor may be

* The constraint set on the currents is not convex, therefore it is necessary to solve the problem twice, once with each inequality, and take the union of the two solutions. If n variable resistors may have currents flowing in either direction, the solution will be the union of the solutions of 2^n problems in which all the combinations of the inequalities are used.

restricted to have a magnitude no greater than $V_{ok} \geqq 0$ by imposing the pair of conditions

$$V_l \leqq V_{ok} \quad \text{and} \quad -V_l \leqq V_{ok} . \tag{52}$$

If V_l is the voltage across the kth resistor and I_k its current, then inequalities (51) and (52) insure that the magnitude of the kth resistor satisfies

$$|R_k| \leqq \frac{V_{ok}}{I_{ok}} .^{*} \tag{53}$$

The resistor R_k may be negative or positive. However, if each variable resistor is made of two resistors in series one of value V_{ok}/I_{ok} and the second to be determined by the computer subject to equation (53), the series combination of the two resistors will never be negative. This constitutes a technique for guaranteeing positive variable resistors without previous knowledge of the directions of current flows.**

The method described can also handle circuits with variable resistors whose values lie within upper and lower limits. If $R_{k_{\min}}$ and $R_{k_{\max}}$ are the minimum and maximum values allowed for the kth variable resistor, the fixed series resistor should be

$$R_{kf} = R_{k_{\min}} + V_{ok}/I_{ok} \tag{54}$$

with V_{ok}/I_{ok} chosen such that

$$V_{ok}/I_{ok} = R_{k_{\max}} - R_{k_{\min}} . \tag{55}$$

The value of $R_{k_{\min}}$ may be zero. Thus, a resistor may disappear as a short circuit. If instead of bounding the value of a resistance from above, the value of an admittance is bounded, a dual method may be used to guarantee positive resistors.

Instead of equations (51) and (52) the following restrictions are imposed

$$I_k \leqq I_{ok} \quad \text{and} \quad -I_k \leqq I_{ok} , \tag{56}$$

$$V_l \geqq V_{ok} \quad \text{or} \quad -V_l \geqq V_{ok} .^{\dagger} \tag{57}$$

---

* Both V_{ok} and I_{ok} are variables in the linear program which will be determined by the simplex algorithm. The ratio is constrained by a linear inequality $I_{ok} \mid R_k \mid - V_{ok} \leq 0$, where $\mid R_k \mid$ is given.

** Another approach is to reverse the reference direction of the current and voltage drop across each variable resistor and apply the methods of the previous section. If n variable resistors may have currents flowing in either direction it is necessary to consider 2^n possibilities.

† See footnote to equation 51.

These guarantee that

$$|G_k| \leqq \frac{I_{ok}}{V_{ok}} \tag{58}$$

where $G_k = 1/R_k$. G_k may be positive or negative if each variable resistor is made of two resistors in parallel, one of admittance I_{ok}/V_{ok} and the second to be determined by the computer subject to equation (58). However, the parallel combination of the resistors will never be negative.

The dual method can also handle circuits with variable resistors whose admittance lies within upper and lower limits $G_{k_{max}}$ and $G_{k_{min}}$. The value of $G_{k_{min}}$ may be zero. Thus a resistor may disappear as an open circuit.

XII. CHOOSING TOPOLOGY BY COMPUTER

As already pointed out, Phase I of the simplex method obtains the basic feasible solutions of a set of linear equations. The set of equations may come from a set of equalities and inequalities to which slack variables have been added. Usually the number of variables (including slack variables) is greater than the number of equations and the system is redundant. If r is the rank of the system and n is the number of variables (including slack variables), at least n-r variables are set to zero in obtaining a basic feasible solution. Some of the variables set to zero may be node voltages or variable resistor currents. If a node voltage is set to zero, the corresponding node is grounded. If a variable resistor current is set to zero, the corresponding resistor disappears as an open circuit. If a slack variable is set to zero, the inequality constraints are met with equalities.

For example, for equation (50) if the kth entry of w, is zero, the kth resistor acquires its minimum allowed value.

One way of viewing equation (50) is to consider the columns of the matrix on the left as elements of a vector space and the entries of the column multiplying the matrix as those positive coefficients which synthesize the column on the right in the form of a linear combination of the columns of the matrix. A final tableau of Phase I of the simplex method will contain a number of independent unit columns (with all entries zero except one) equal to the rank of the matrix on the left side of equation (50). The unit columns are obtained by the special gaussian reduction provided by the simplex algorithm. Each column corresponds to a variable in the column multiplying the

matrix of equation (50). Those variables whose corresponding columns are not unit columns are set to zero.

If a set of columns corresponding to the currents through a set of variable resistors are linearly dependent, one or more of the currents will be set to zero. This implies the disappearance of a resistor as an open circuit. The choice of which resistors disappear is automatically determined with the aid of the simplex algorithm, so that the nonzero currents acquire positive values (if such a choice exists). If two columns of the matrix of equation (50), corresponding to currents through variable resistors, are linearly dependent it means that Kirchhoff's voltage and current law may be satisfied with one of the currents zero, making one of the resistors unnecessary.

The above argument provides a method for letting a computer program choose the topology and resistor values of a dc network in which certain voltages and currents are imposed by CFE's and VFE's. One connects an excess of resistors between different nodes (including additional internal nodes if desired). By using a linear programming formulation some node voltages and variable resistor currents are set to zero by the computer program, thus determining a set of "linearly independent positive resistors" that satisfy all the circuit equations.

XIII. EXAMPLES

Consider the circuit of Fig. 19(a). The equivalent circuit is shown in Fig. 19(b) with a VFE and CFE in place. As indicated on Fig. 19(b) it is desired to impose on the transistor a collector current of 5 mA and a collector-emitter voltage of 5 volts. The resistors marked R_1, R_2 and R_3 are variable.

The nodal equations for the circuit after the effect of the nullators introduced by the VFE's and CFE's are taken into consideration are, in matrix form

$$\begin{bmatrix} -1. & 1. & 0. & 0.005 & -0.005 & 0. & -1 \times 10^{-10} \\ 0. & 0. & 1. & -0.38 & 0.3811 & -0.0011 & 0. \\ 0. & 0. & 0. & 0. & 0. & 0.00333 & 0. \\ 1. & 0. & 0. & -1. \times 10^{-10} & 0. & 0. & 1. \\ 0. & 0. & 0. & 0. & -0.001 & 0.001 & 0. \\ 0. & 0. & 0. & 0.375 & -0.3751 & 0.0001 & 0. \end{bmatrix}$$

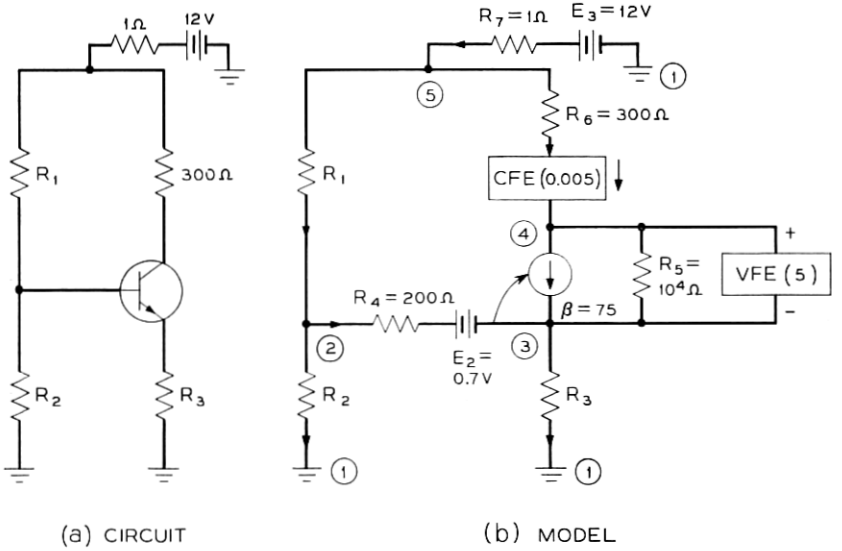

Fig. 19 — Circuit biased with constrained singular imbedding; (a) circuit, (b) model.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = \begin{bmatrix} 0.0035 \\ -0.27 \\ 0.035 \\ 12. \\ 0.005 \\ 0.2675 \end{bmatrix} \cdot \qquad (59a)$$

By multiplying the second row by -1, the entry -0.27 in the right side vector is made positive. (As indicated above, linear programming assumes the right side vector is nonnegative). Notice that since the matrix in equation (59a) is 6×7, we therefore generally expect a one parameter infinity of solutions. If the system of equations were solved using the simplex method (with arbitrary cost coefficients), solutions in which all the variables acquire non-negative values may be obtained. Resistors R_2 and R_3, which are grounded, will automatically be positive. However the voltage differences across ungrounded resistors may turn out to be negative, yielding negative re-

sistances. To assure a non-negative voltage difference across R, the following additional constraint will be imposed

$$V_5 - V_2 \geqq 0$$

which may also be written*

$$V_2 - V_5 \leqq 0. \tag{59b}$$

There are two basic feasible solutions to this problem:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = \begin{bmatrix} 5.788 \\ 5.78794 \\ 5.060073 \times 10^{-3} \\ 6.212 \\ 5.5 \\ 10.5 \\ 6.212 \end{bmatrix}, \quad \begin{bmatrix} 5.9966425 \times 10^{-5} \\ 0. \\ 5.060073 \times 10^{-3} \\ 6.212 \\ 5.5 \\ 10.5 \\ 11.99994 \end{bmatrix}. \tag{60}$$

The first basic solution yields the following set of resistors

$$\begin{aligned} R_1 &= \frac{V_5 - V_2}{I_1} = \frac{6.212 - 6.212}{5.788} = 0 \text{ ohms} \\ R_2 &= \frac{V_2}{I_2} = \frac{6.212}{5.78794} = 1.073266 \text{ ohms} \\ R_3 &= \frac{V_3}{I_3} = \frac{5.5}{5.060054 \times 10^{-3}} = 1086.941 \text{ ohms}. \end{aligned} \tag{61}$$

R_1 is a short circuit.

The second basic solution yields the set

$$R_1 = 97008.514, \qquad R_2 = \infty, \qquad R_3 = 1086.941.$$

R_2 is an open circuit. Notice also that R_3 is the same for both solutions. This is expected since the voltage of node 3 is virtually fixed by the requirements.

The totality of the solutions with non-negative voltage differences across the variable resistors may be written, according to equation (47)

$$x = \lambda x^1 + (1 - \lambda)x^2$$

where x^1 and x^2 are the basic feasible solutions of equation (60), and $0 \leqq \lambda \leqq 1$.

* When the right side of an inequality is zero, it is preferable to write it as a $\leqq$ inequality because the corresponding slack variable may be used as an artificial variable with savings on the size of the matrix to be manipulated.

Choosing $\lambda = \frac{1}{2}$ yields

$$x = \begin{bmatrix} 2.89402 \\ 2.89397 \\ 5.060073 \times 10^{-3} \\ 6.212 \\ 5.5 \\ 10.5 \\ 9.10597 \end{bmatrix}$$

which yields the set of resistors

$$R_1 = 0.997906, \qquad R_2 = 2.146532, \qquad R_3 = 1086941.$$

A continuous set of equivalent circuits, which achieve the requirements exactly and which have positive resistances, is obtained by varying λ between 0 to 1.

Suppose now that further considerations require that R_1 lie between 1000 and 2000 ohms. By replacing (59b) by

$$\frac{V_5 - V_2}{I_1} \geqq 1000 \qquad \text{and} \qquad \frac{V_5 - V_2}{I_1} \leqq 2000$$

which may be written

$$\begin{aligned} 1000\, I_1 - V_5 + V_2 &\leqq 0 \\ -2000\, I_1 + V_5 - V_2 &\leqq 0 \end{aligned} \tag{62}$$

the resistor R_1 is forced to remain between 1000 and 2000 ohms.

When the new problem is solved the basic feasible solutions are

$$x^1 = \begin{bmatrix} 5.782218 \times 10^{-3} \\ 5.722218 \times 10^{-3} \\ 5.060073 \times 10^{-3} \\ 6.212 \\ 5.5 \\ 10.5 \\ 11.99422 \end{bmatrix}, \qquad x^2 = \begin{bmatrix} 2.892554 \times 10^{-3} \\ 2.832554 \times 10^{-3} \\ 5.060073 \times 10^{-3} \\ 6.212 \\ 5.5 \\ 10.5 \\ 11.99711 \end{bmatrix}.$$

The basic feasible solutions yield the following sets of resistors

$$x^1 : R_1 = 1000., \quad R_2 = 1085.593, \quad R_3 = 1086.941$$

$$x^2 : R_1 = 2000., \quad R_2 = 2193.074, \quad R_3 = 1086.941.$$

Notice that R_1 acquired its allowable extreme values in each basic feasible solution.

Other sets of resistances may be obtained by convex combinations of the two basic feasible solutions.

As an example in which the topology of a circuit is determined by the computer, consider the circuit of Fig. 16 in which R_1, R_2, and R_3 are to be selected to give $z_{11} = \frac{2}{3}$ and $z_{21} = \frac{1}{3}$. The example was previously solved without linear programming techniques. Several solutions appear in Table V. By maximizing the negatives of the currents in the resistors, those currents which may be set to zero by taking them out of the basis for a basic feasible solution will be converted into open circuits. After the effect of the nullators introduced by the VFE's is accounted for, the matrix corresponding to the circuit of Fig. 16 is 5×6. We therefore expect a one parameter infinity of solutions and two basic feasible solutions which are

$$x^1 = \begin{matrix} I_1 \\ I_2 \\ I_3 \\ V_2 \\ V_3 \\ V_4 \end{matrix} \begin{bmatrix} 0.0 \\ 5.9652404 \times 10^{-3} \\ 5.965238 \times 10^{-3} \\ 44.096881 \\ 0.3333333 \\ 0.3333333 \end{bmatrix}, \quad x^2 = \begin{bmatrix} 0.28174743 \\ 4.5937138 \times 10^{-3} \\ 0.0 \\ 43.602828 \\ 0.33639577 \\ 0.3333333 \end{bmatrix}.$$

Notice that V_4 remains constant for both basic feasible solutions. This is expected since a VFE is connected from node 4 to node 1 (datum). The resistances corresponding to the basic feasible solutions are

$$x^1 : R_1 = \infty \quad R_2 = 55.879273, \quad R_3 = 7336.429$$

$$x^2 : R_1 = 154.4759, \quad R_2 = 72.5629, \quad R_3 = \infty.$$

In both basic feasible solutions one of the resistances disappeared as an open circuit. This indicates that given R_4, R_5 and R_6 with the values indicated in Fig. 16 the circuit is achievable with two topologies, each containing 5 resistors.

Let us now make R_6 a variable resistor. The nodal matrix after the elimination of the nullators is now 5×7. Thus we expect a two

parameter infinity of solutions and at least 3 basic feasible solutions. The following sets of resistors correspond to basic feasible solutions

(i) $R_1 = \infty$, $R_2 = \infty$, $R_3 = 1.33333$, $R_6 = 0.16666667$

(ii) $R_1 = \infty$, $R_2 = 0.333333$, $R_3 = 0.4444456$, $R_6 = \infty$

(iii) $R_1 = 0.88888898$, $R_2 = 1.333333$, $R_3 = \infty$, $R_6 = \infty$

(iv) $R_1 = 1.3333336$, $R_2 = \infty$, $R_3 = \infty$, $R_6 = 0.66666651$.

These sets provide four different topologies with which given two of the resistors (R_4 and R_5) a resistive network having $z_{11} = \frac{2}{3}$, $z_{21} = \frac{1}{3}$ may be realized.

The example illustrates how using the methods of this paper can solve the problem of realizing portions of a resistive matrix with certain elements prespecified. The prespecified elements need not be resistors but may also include controlled sources, gyrators, ideal transformers, and so on.

The methods discussed have been implemented on a time-shared

TABLE VI—PRINTOUT OF THE SESSION TO SOLVE THE CIRCUIT OF FIGURE 19

```
TYPE NO. OF BRANCHES,NODES,CONTROLLED SOURCES,BATTERIES,CURRENT SOURCES
A=7 5 1 3 0
TYPE BRANCH RESISTANCES
B=1. 1. 1. 200. 1.E4 300. 1.
TYPE FOR EACH BRANCH: INITIAL NODE,FINAL NODE,BATTERY NO.
C=5 2 1   2 1 1   3 1 1   2 3 2   4 3 1   1 4 3   1 5 3
TYPE VALUES OF BATTERIES
D=0. -.7 12.
TYPE FOR EACH CONTROLLED SOURCE: BRANCH NO. AND CONTROLLING BRANCH NO.
E=6 5
TYPE VALUES OF BETAS
F=75.

OPTION COMMANDS=DESIGN CKT
TYPE NO VARIABLE RESISTANCES,NO. VOLTAGE CONSTRAINTS, AND NO CURRENT CONSTRAINTS
 I=3 1 1
TYPE BRANCH NO. OF VARIABLE RESISTANCES
J=1 2 3
TYPE PLUS AND MINUS NODES FOR EACH VFE
K=4 3
TYPE VALUE OF EACH VFE
L=5.
TYPE BRANCH CURRENT FOR EACH CFE
M=5
TYPE VALUE OF EACH CFE
N=.005
TYPE COST COEFFICIENTS
O=1. 1. 1. 1. 1. 1. 1.
TYPE MINIMA OF VARIABLE RESISTANCES
P=1000. 0. 0.
TYPE MAXIMA FOR EACH VARIABLE RESISTANCE
Q=2000. 1.E8 1.E8

R( 1)= 9.9999995E+02
R( 2)= 1.0855930E+03
R( 3)= 1.0869498E+03
```

computer system. The program is conversational. A portion of a session in which a basic solution corresponding to the circuit of Fig. 19 with R_1 constrained betwen 1000 and 2000 ohms appears in Table VI.

XIV. CONCLUSIONS

The method of singular imbedding has been shown to be efficient for solving the following problem: Given a circuit with a prespecified topology, some of whose elements are prespecified, find the values of the unspecified elements which will yield desired node-pair voltages or branch currents. The unspecified element values may be restricted to lie within given upper and lower bounds.

By letting the upper and lower bounds become infinite and zero, the problem of finding the topology for the circuit may be also solved.

The method has been implemented on a time-shared computer, and several examples, including some practical transistor circuits, are given.

The usual approaches to the problems of this paper have been iterative analysis-optimization schemes. Singular imbedding requires, for a three transistor amplifier, three orders of magnitude less computation time. This makes the method appealing for time-shared applications.

Two new singular network elements, the voltage forcing element and the current forcing element, constrain node-pair voltages and branch currents without otherwise affecting the circuit. Elements of unspecified value are modeled by branches carrying unknown currents.

With the aid of these elements, the problem of design is reduced to one of analyzing a circuit containing unknown current sources and nullators. If there are more free elements than requirements, the solution space may be a linear manifold. By allowing the free circuit variables to take on a set of discrete values, sets of exact solutions to the design problem may be generated economically.

When the unspecified elements are required to lie within upper and lower bounds, the problem is one of analysis with linear inequality constraints. This may be solved efficiently using linear programming techniques.

Among the practical problems solved by singular imbedding are biasing a direct coupled transistor amplifier, designing midband gain and driving point impedance, synthesizing networks for several given admittance parameters, and determining circuit topology.

Areas being investigated include using singular imbedding in the

synthesis of resistance networks (the synthesis of a single column of a specified resistance matrix has been illustrated). Synthesis of an entire resistance matrix results from the intersection in resistance space of the solution spaces for each column of the matrix. Similarly, by considering the intersection of solutions spaces for both a small signal design and a biasing design, the method may be extended to designing transistor circuits for desired small signal design and bias points simultaneously.

Although only fixed value CFE's and VFE's were used in this paper, CFE's and VFE's which may take any value within a given range may also be used. For example, a branch current may be forced to be greater than 1 mA and less than 10 mA. These elements are also useful in insuring that models for devices stay within their valid limits. For example, a transistor can be constrained to remain in the active region, for which the linear model used is valid.

For simplicity, only the case of linear dc networks has been illustrated in this paper. However, the method has usefulness in ac design, combined ac and dc design, and non-linear design. These topics will be covered elsewhere.

REFERENCES

1. Murray-Lasso, M. A. and Baker, W. D., "Computer Design of Multistage Transistor Bias Circuits," *Proc. Fifth Annual Allerton Conf.*, Monticello, Illinois, October 1967.
2. McMillan, B., "Introduction to Formal Realizability Theory," B.S.T.J., *31*, No. 2 (March 1952), pp. 217–279.
3. Newcomb, R. W., *Linear Multiport Synthesis*, New York: McGraw-Hill, 1966.
4. Tellegen, B. D. H., "La Recherche pour une Serie Complète d'éléments de Circuits Ideaux Non Linéaires," Rendiconti Seminario Mathematico e Fisico, Milano, *25* (1953–54), pp. 134–144.
5. Davies, A. C., "Matrix Analysis of Networks Containing Nullators and Norators." *Electronics Letters*, *2*, No. 2 (February 1966), pp. 48–49.
6. Dantzig, B. B., *Linear Programming and Extensions*, Princeton, N. J., Princeton University Press, 1963.
7. Murray-Lasso, M. A. and Kasper, F. J., "On-Line Circuit Analysis and Optimization with Commercially Available Time-Shared Computer Systems," Proceedings of the Design Automation Workshop, Washington, D. C., July 1968.