Low-Resolution TV: An Experimental Digital System for Evaluating Bandwidth-Reduction Techniques

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An experimental digital television system has been constructed for evaluating digital techniques which involve storage and which may be used to reduce the bandwidth required for the transmission of television signals. The basic configuration of this system is presented.

The system is composed of a television camera chain, synchronizing generator, 8-digit analog-to-digital Gray code converter, Gray to natural-binary code translator, high-speed large capacity ultrasonic delay-line memory, digital control logic, 8-digit digital-to-analog converter, television display monitors, and video-tape recording equipment.

The picture format consists of 160 lines per frame sequentially scanned at 60 frames per second. The video signal is band-limited to less than 768 kHz, corresponding to a horizontal resolution of 160 samples per line. The required timing and synchronization signals for all equipment are derived from a common clock source.

I. INTRODUCTION

It is well known that redundancy is inherent in television signals. This fact invites the use of many coding techniques for the removal of redundancy in order to achieve bandwidth compression for increased efficiency of transmission. In the search for these techniques the human receiver must not be ignored since man is a constituent part of visual communication systems. For this reason, it is imperative that promising methods of coding be demonstrated in real time before final conclusions are drawn. This permits careful judgment to be made of picture impairment introduced by the coding scheme or transmission errors.

Subjective testing may also be performed to determine and evaluate

the factors affecting the acceptability of various bandwidth compression techniques. In the process of subjective testing, new knowledge of the perceptual properties of the human receiver may be gained which will be of value in the design of a communication system matched to the human channel.

Many effective techniques of removing the redundancy inherent in television signals require digitalization and storage of the picture signal. To explore this approach, an experimental low-resolution television system, which employs both digital and storage techniques, has been constructed to demonstrate various bandwidth compression techniques in real time.

The description of this facility is presented in its use to show frame repetition and uniform density picture replenishment systems. Experiments using this equipment have been described in a separate paper.[1]

II. GENERAL SYSTEM DESCRIPTION

The basic configuration of the system is shown in Fig. 1. A standard television camera chain, modified to produce a picture format consisting of 160 lines per frame sequentially scanned at a rate of 60 frames per second, is used to generate a video signal. The required synchronization pulses for the camera are derived from the synchronizing generator. All timing pulses required throughout the system are likewise derived from the synchronizing generator—all signals being derived from a common clock source.

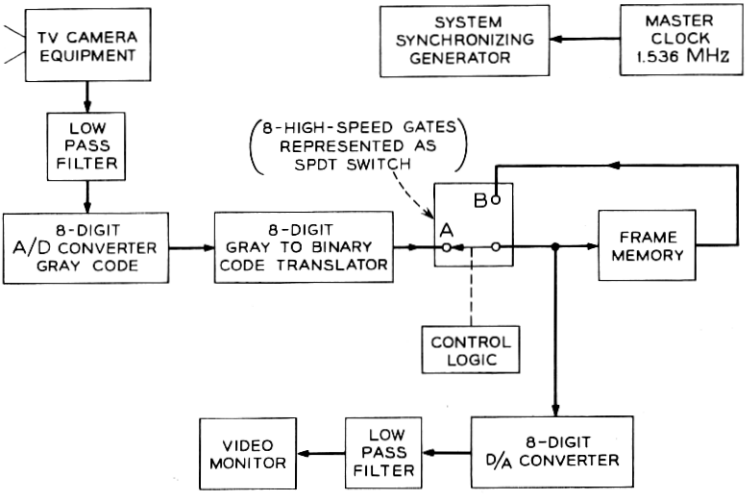


Fig. 1 — Basic configuration of experimental system.

The video signal from the camera is bandlimited to less than 768 kHz, corresponding to a horizontal resolution of 160 picture elements per line. This signal is presented to an 8-digit analog-to-digital (A/D) converter for conversion to the digital format.

Some bandwidth compression schemes to be investigated require logical operations to be performed on the digital encoded signal. Sufficiently small quantum steps are therefore required to allow flexibility of operation with a signal-to-noise ratio such that the PCM quantization noise is not visible. Results from such a system are then applicable to an equivalent system realized as a completely analog system.

The A/D converter converts the video signal to eight parallel digits of Gray code at a 1.536-MHz sampling rate. Since it is significantly easier to decode a natural binary encoded signal, translation from Gray code to natural binary code in parallel form is performed by a code translator. The output of the code translator is conveyed to high-speed gates controlled by digital logic which can be programmed for various system functions. These gates are represented as a single SPDT switch "S" in Fig. 1. With the switch S closed for transmission through path A, the output signal of the translator is coupled to the input of a delay line memory. With the switch S closed for transmission through path B, the digital output signal of the memory is coupled back to the input of the memory. Thus, by controlling the transmission path through the switch, either new information via path A is inserted into the memory or information previously stored in the memory is recirculated via path B. The digital storage media has sufficient capacity to store one complete frame of pictorial information in an 8-digit binary pulse code at the 1.536-MHz sampling rate.

The information coupled to the input of the memory is also conveyed to the 8-digit digital-to-analog (D/A) decoder in parallel form. The analog output signal from the decoder is filtered and displayed on a monitor.

All circuits are transistorized except the camera chain and monitors. A plug-in logic block approach has been used in the digital processing equipment to provide flexibility for system experimentation. Different encoding schemes may be readily tried and quickly modified.

III. CAMERA CHAIN

The composite video signal used for these experiments departs from television standards by operating at 60 frames per second with non-interlaced scanning, 160 lines per frame at a 9600-Hz line rate. A modified synchronizing and blanking pulse structure is employed which

eliminates equalizing pulses and serrated vertical synchronizing pulses. A 1:1 aspect ratio scanning format is used for the camera.

Major modifications of an RCA TK-21B vidicon camera chain were made to allow this operation, give stabilized pedestal and video levels, improve low frequency response, and to provide optional AGC of the output video signal. Further modifications of the camera include a transistorized gating circuit directly coupled to the vidicon cathode to provide beam current cutoff during the storage periods of an integrate mode of operation. This mode of operation will be discussed later.

IV. INPUT FILTER

The video signal from the camera is bandlimited by the input filter prior to sampling and encoding. The requirements imposed on this filter are discussed later with those of the output filter.

V. ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D converter used in the system converts the video information into an 8-digit Gray code (256 levels) at a 1.536-MHz sampling rate. The A/D converter is an all solid-state encoder of the "folding" type similar to an exploratory model[2] developed by the Digital Transmission Laboratory at Bell Telephone Laboratories.

The A/D converter, shown in Fig. 2, consists of four basic types of functional modules:

(*i*) Synchronized clamping circuit module.
(*ii*) Sample-and-hold circuit module.
(*iii*) Coder modules.
(*iv*) Digit amplifier modules.

The coder modules are essentially the same as the original design described by F. D. Waldhauer[3] while all the remaining modules were designed by E. M. Cherry.

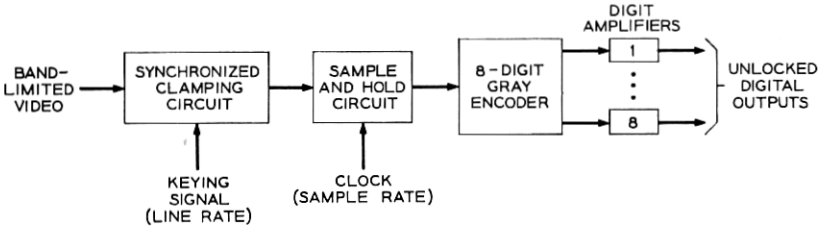


Fig. 2 — A/D converter.

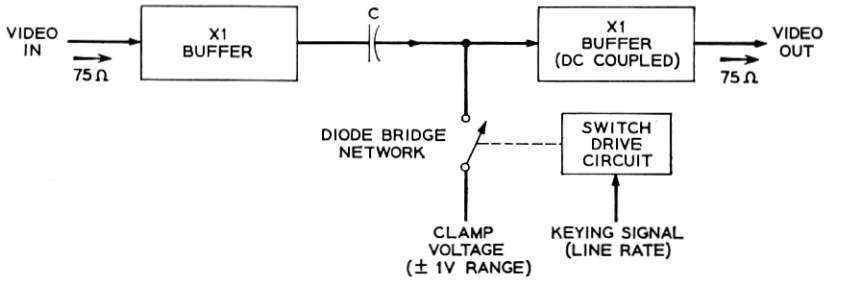


Fig. 3 — Synchronized clamping circuit block diagram.

5.1 *Synchronized Clamping Circuit*

To prevent dc wander, the dc component of the video signal is restored by the synchronized clamping circuit prior to sampling. A block diagram of this circuit is shown in Fig. 3. A 6-microsecond keying signal is applied to the clamp circuit. The keying signal is synchronous with the line rate and is timed to occur after the leading edge of the horizontal sync signal. The clamp level to which the sync tips are held when keyed is adjustable over a ±1 volt range. The synchronized clamping circuit was designed with unity gain and is capable of driving a 1-volt peak-to-peak signal within a ±1 volt range into a 75-ohm load. The overall bandwidth of this circuit is approximately 30 MHz.

5.2 *Sample-and-Hold*

In order to allow the coder modules to settle to a unique code, the input signal must be held constant during the sample interval. This function is performed by the sample-and-hold circuit. The sampling error of this circuit is less than 1 percent of the peak-to-peak signal amplitude for a 20-nanosecond sampling time, taken at a 1.536-MHz rate, and the variation of the held signal is less than 1 percent in 30 microseconds. The circuit was designed for a signal input of 1 volt peak-to-peak, symmetrical about zero, and is capable of driving 1 volt peak-to-peak into a 75-ohm load.

Three adjustments are provided for in the sample-and-hold circuit.

(*i*) A dc balance control is used to set the dc shift between the input and output terminals to zero.

(*ii*) A switching balance control is adjusted with no input signal to give the same output potential with the gate open or closed.

(*iii*) A drift control is adjusted so that the integrator drifts toward zero output. This gives the "flattest" held output waveform.

The sample-and-hold circuit is clocked at the master clock rate of 1.536 MHz. The camera sweeps are synchronized to the same clock so that the noise defects associated with sampling and encoding will not drift through the reconstructed picture.

5.3 *Coder Modules*

Eight coder modules, one for each digit, are used as shown in Fig. 4. Each coder stage is composed of two precision wideband operational amplifiers using nonlinear feedback. High-speed diodes are placed in the feedback network of each operational amplifier in such a way as to direct positive input signals to one output terminal and negative input signals to a second output terminal. The corresponding output terminals of each operational amplifier are coupled to separate summing nodes together with appropriate reference voltages which shift the residue signals, thus providing the "folding" action. Cascading each stage in a "balanced rail" arrangement, as shown in Fig. 4, allows coding into the Gray code. Balanced signals are provided to the input of the first coder stage by use of an inverter stage in one rail of the "balanced rail" arrangement.

An unclocked digit output signal and its inverse are generated by each stage of the coder. Although two outputs are available from each stage, only one output signal is used. The output amplitude characteristic for this signal is linear over a voltage range of ± 1.75 volts except for a small discontinuity near zero. This discontinuity in the output signal occurs where the digital information changes in value.

5.4 *Digit Amplifier*

A logical decision must be made on the digital output signal of the coder to provide a signal which has one of two possible voltage levels. This function is performed by the digit amplifier circuit. A block diagram of this circuit is shown in Fig. 5. This circuit clips the signal from the coder stage to effectively flatten the output voltage characteristics of the coder and is designed to have a ± 10 mV hysteresis in the threshold switching level of the tunnel diode regenerator which drives the output stage. The threshold setting of the digit amplifier is adjustable and is set to trigger about zero volts. The signal output of the digit amplifier, working into a 75-ohm load, is an unclocked voltage of 0 volts whenever the digit output signal of the coder is 0 + or

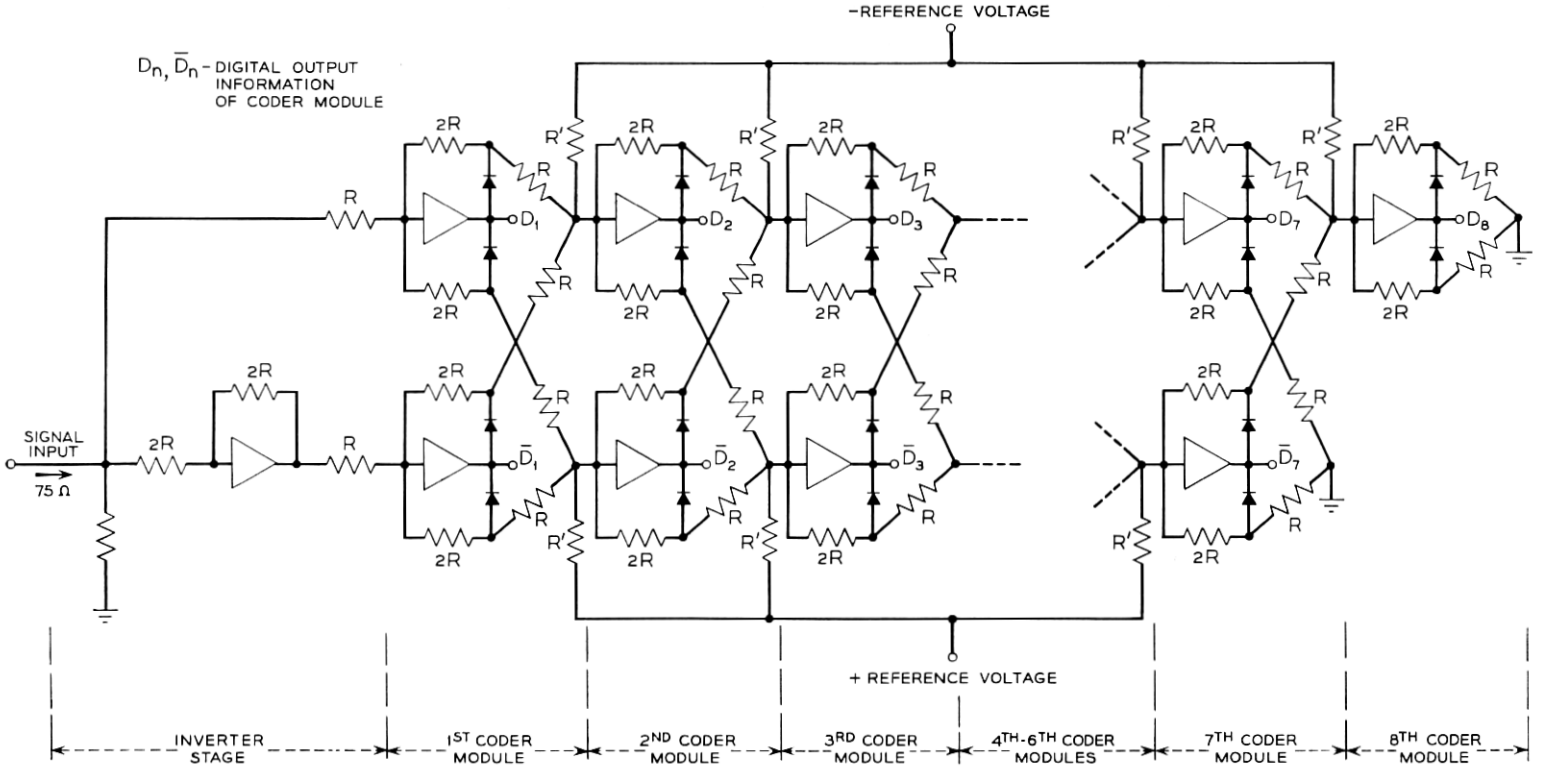


Fig. 4 — Balanced coder system.

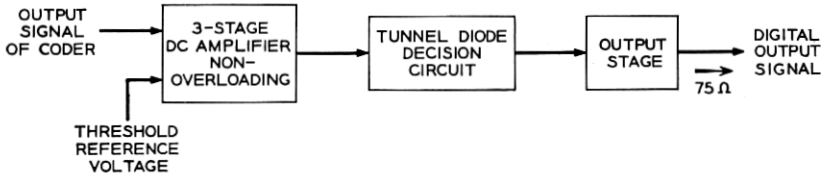


Fig. 5 — Digit amplifier block diagram.

greater and +2 volts whenever the coder digit output signal is 0 − or less.

A voltage standard method was used to perform the static alignment of the coder and to adjust the threshold setting of the digit amplifiers.

VI. CODE TRANSLATOR

The logical functions performed by the code translator are shown in Fig. 6. These functions are performed using high-speed (5 MHz) commercially available logic circuits.

The 8-digit Gray code output of the A/D converter is coupled in parallel form to the translator. All digits are clocked in parallel into an 8-bit flip-flop store at a 1.536-MHz rate. This allows the maximum time of one sample period to perform the Gray to binary code translation.

The exclusive OR logic function is used to perform the parallel translation as shown in Fig. 7. Although the translation is performed in parallel, the operation is inherently serial since the decisions made in the exclusive OR circuits are dependent upon the decisions made in the circuits of previous digits. By providing a clocked digit store of one sample interval preceding the translation, timing problems and translation errors are not encountered. The output digits of the actual translation are clocked at the 1.536-MHz rate and stored in parallel for one sample interval in a second 8-digit flip-flop store. The digital output of the translator in parallel form represents the video information encoded as 8-digit PCM in the conventional binary code pattern at 1.536-MHz rate.

VII. DIGITAL STORAGE MEDIA

The digital frame memory assembled for the system has sufficient capacity to store one complete frame of video information encoded as 8-digit PCM—a total of 204.8 kilobits at a rate of 1.536 MHz per

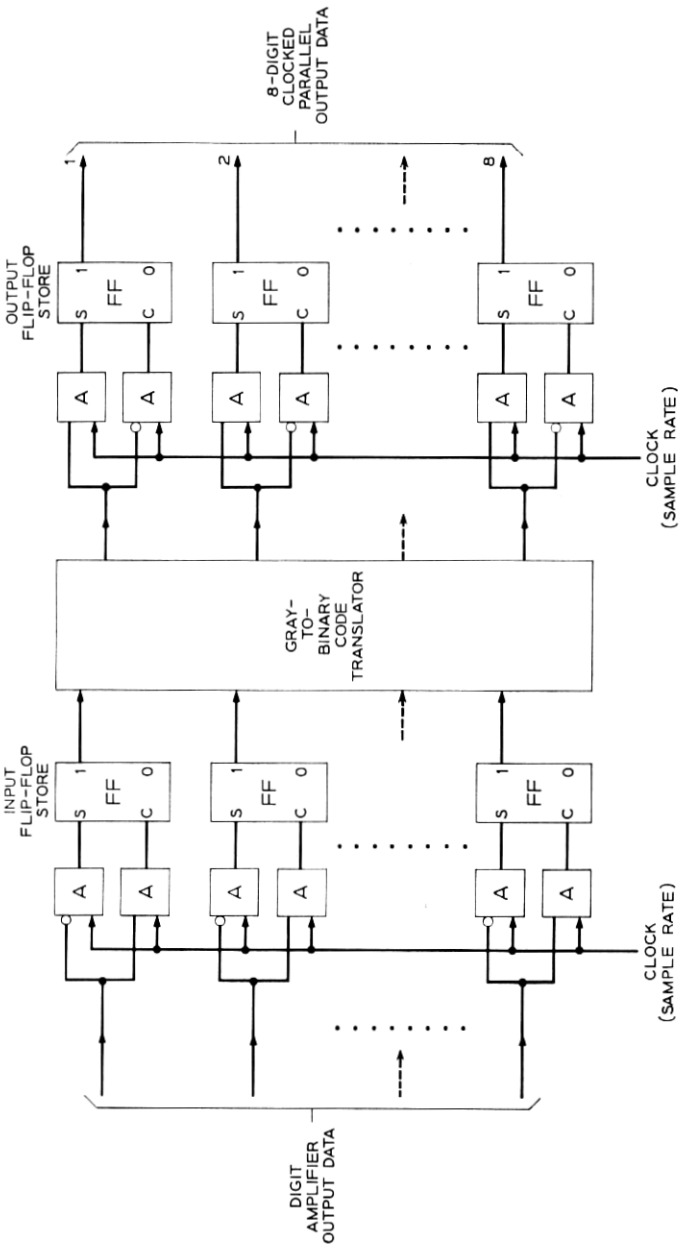


Fig. 6 — Code translator system.

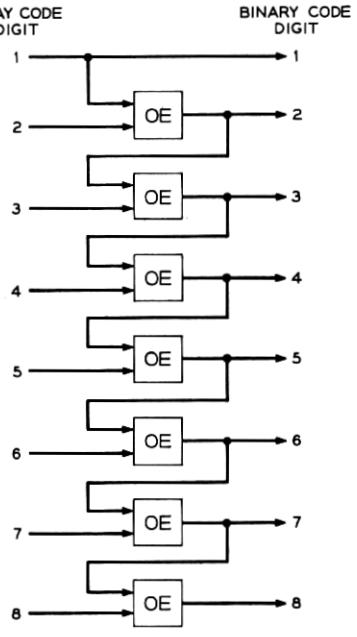


Fig. 7 — Parallel Gray-to-binary translation.

second. The frame storage period is 1/60 of a second. The basic configuration of the frame memory is shown in Fig. 8.

High-speed ultrasonic delay lines[4] are used as the storage media, each line having a delay of 4.2 milliseconds with an insertion loss of 34 dB and a bandwidth of 3 MHz at a mid-band frequency of 5 MHz. To give a total delay of one frame period for each digit, four such lines with associated clocked regenerators are connected in tandem, the output of which is directed into the first stage of a four-stage register. The shift register is considered a constituent part of the frame delay period. The data stored in the shift register is stepped along at the sample rate of 1.536 MHz, to the final stage of the shift register which is considered the output stage of the delay lines.

A total of 32 ultrasonic delay lines with associated clocked regenerators are required as part of the frame memory since the data is stored in parallel form. These lines are assembled in four temperature-regulated ovens, in groups of eight lines per oven, for accurate control of the temperature and hence the delay interval.

Additional logic is associated with the frame memory in the form

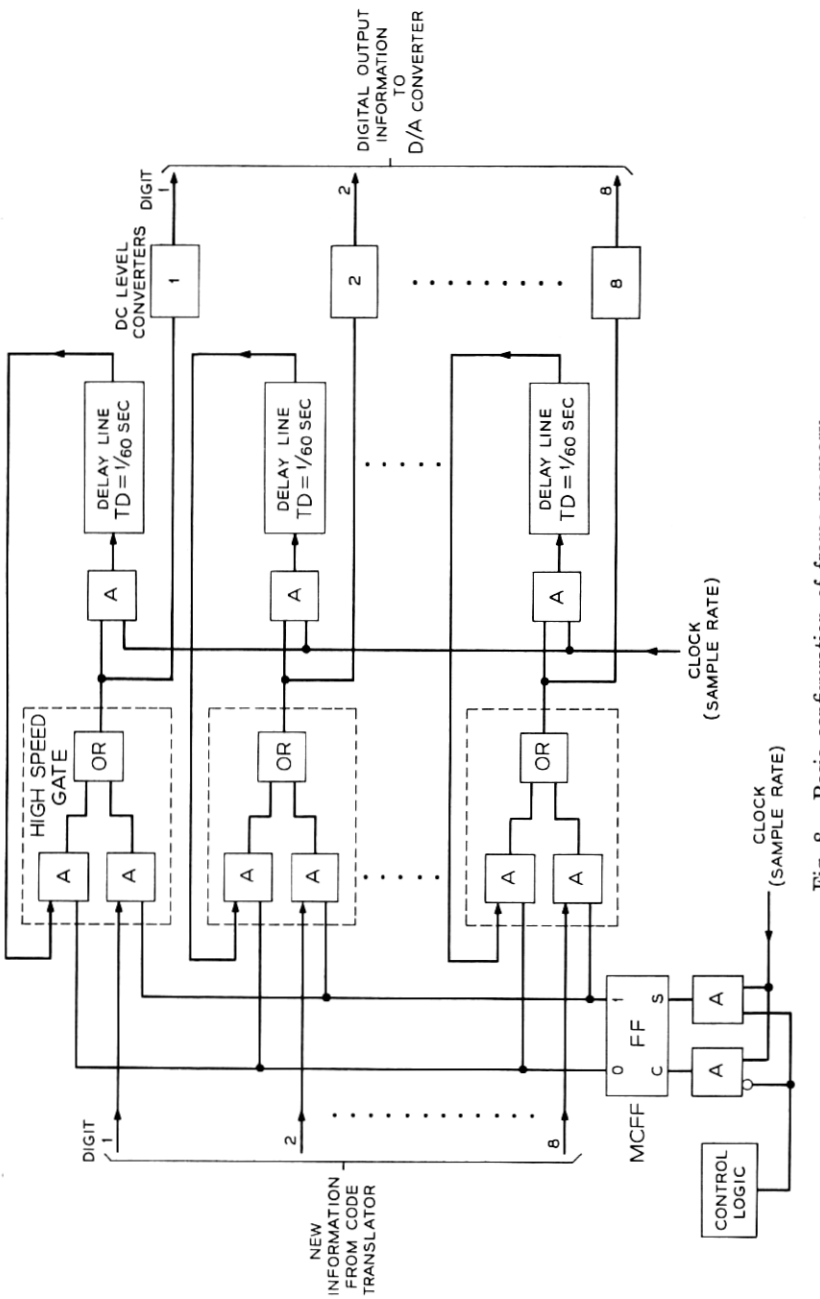


Fig. 8 — Basic configuration of frame memory.

of high-speed gates. The function of the high-speed gates is to convey to the input of the delay lines, in parallel form, either new information scanned from the vidicon camera which has been encoded, or previously stored data read from the output of the frame-memory shift registers.

Logically, a high-speed gate is comprised of two, two-input AND circuits feeding a two-input OR circuit. A separate high-speed gate is used to convey each digit to the frame memory with all AND circuits being controlled by a single flip-flop as shown in Fig. 8. Only one AND circuit per gate is enabled at any given time. The controlling flip-flop will hereafter be referred to as the memory control flip-flop (MCFF). Thus, by controlling the output state of the MCFF, either new information or data previously stored in the memory is coupled to the input of the delay lines. The information coupled to the input of the delay lines is also simultaneously decoded, filtered, and displayed on a television monitor for subjective evaluation. The information to be displayed on the monitor is taken from the input terminal of the frame memory rather than the output terminal to avoid the non-simultaneous presentation of the visual signal and the corresponding speech signal to the observer.

Once data is inserted into the delay lines, it can be stored for any desired number of integral frame periods or replaced with new information. Thus, two modes of operation are considered to exist for the frame memory—a write mode of operation and a repeat mode of operation. In the write mode, new information, read from the vidicon camera and encoded, is inserted into delay lines via the high-speed gates. The output of the MCFF assumes the 1-state for this mode of operation. In the repeat mode of operation, the digital output of the frame memory is directed to the input of the delay lines via the high-speed gates to recirculate the data previously stored in the memory. For this mode of operation, the 1 output of the MCFF assumes the 0-state.

Control logic is programmed to regulate the output state of the MCFF to realize frame-repeating and replenishment systems and will be discussed later.

VIII. DC LEVEL CONVERTERS

To provide the proper coupling between the output of the high-speed gates and the digit inputs to the decoder, output dc-level-converters are utilized. The function of this stage is to convert the digital processing logic voltage levels of 0 and -4 volts to $+2$ and 0 volts when working into the 75-ohm load presented by the decoder.

IX. DIGITAL-TO-ANALOG CONVERTER

The D/A converter used to convert the 8-digit binary code into its analog equivalent is similar to an exploratory model[5] designed for the high-speed PCM coaxial transmission system and is shown in Fig. 9. Some modifications were made with respect to the method of clocking the control circuitry, the choice of the network switching diodes, and the resampler circuit used.

The decoder is composed of an eight section 75-ohm balanced resistive ladder network controlled by appropriate digital logic. Since the decoder is operated at a lower sampling rate than required in the design of the original model by Kovanic, matched pairs of Fairchild type FD100 diodes proved adequate for the network switching diodes.

The control of the resistive ladder network is performed by clocked flip-flops, one flip-flop per digit. By using diode steering logic associated with each flip-flop, on command of a clock pulse a 1 is stored in the flip-flop whenever a 1-state signal is applied to the digit input of the flip-flop and a 0 is stored whenever a 0-state signal is present.

The input impedance for the clock input of each flip-flop was modified to give 75 ohms when all inputs were paralleled to permit use of a common pulse driver for the clock signal.

Since the output of the decoder exhibits transient effects as a function of level transitions, these transient disturbances would contribute to in-band noise. By resampling at a 1.536-MHz rate prior to low-pass filtering (the samples being taken at that portion of the output waveform which is free of transient disturbances), new transient disturbances will be generated which are not a function of level transitions and hence will contribute only out-of-band noise. The noise introduced by the resampling process will be removed by the system's low-pass output filter.

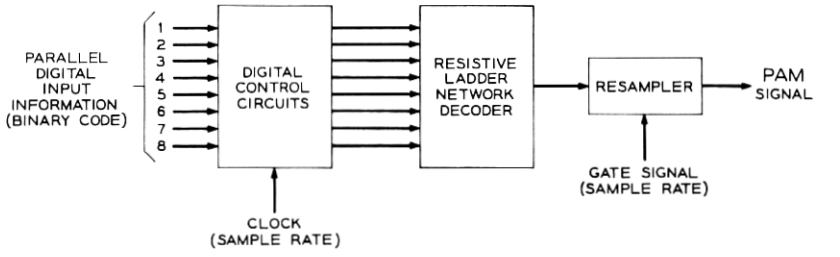


Fig. 9 — D/A converter.

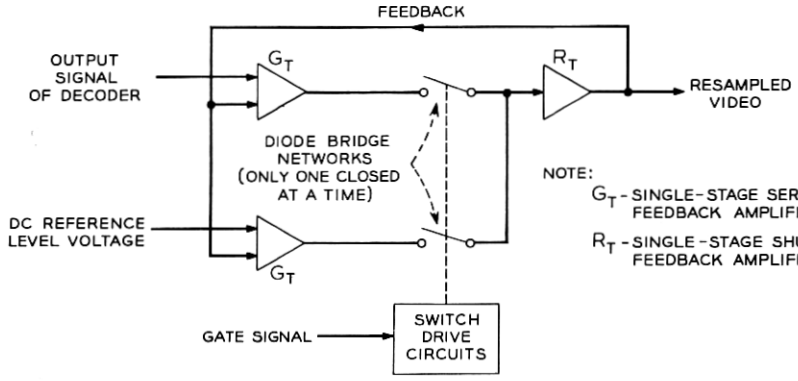


Fig. 10 — Resampler block diagram.

A block diagram of the resampler circuit is shown in Fig. 10 and is a two-input switch. Means are provided for switching one of the two-input signals to the output terminal by using diode bridge networks. The transmission path for each input signal is comprised of a series feedback amplifier, diode bridge network, and shunt feedback amplifier. The shunt feedback amplifier is common to both signal paths. Only one diode bridge network is closed at a time. Overall negative feedback is used to improve the transmission linearity. Switching rates of up to 5 MHz can be achieved with a 20-nanosecond change-over time. The transmission passband for each path is dc to 60 MHz. The circuit presents a 75-ohm input impedance and is capable of driving a 1 volt peak-to-peak signal within a ± 1 volt range into a 75-ohm load.

Using the two-input switch as a resampler circuit, the video output signal of the decoder is applied to one input terminal and a dc reference level voltage is applied to the other input terminal. A 1.536-MHz switching rate is used to alternately switch the input signals to the output terminal, thus resampling the video signal.

X. VIDEO FILTERS

In the encoding process the video signal is sampled at a 1.536-MHz rate. Foldover distortion can result, causing spurious patterns in the recovered television pictures, unless the high-frequency end of the camera signal spectrum is sufficiently suppressed. Subjective tests have been conducted to determine the loss required by the filters, at half

the sampling frequency, for the effects of the spurious patterns on a sampled television picture to be subjectively negligible. It was found that the combined loss of the input and output filters should be at least 16 to 19 dB at a frequency equal to one-half the sampling rate to insure negligible picture impairment. The resampling frequency component of 1.536 MHz must also be sufficiently attenuated by the output filter so that the resampling pattern cannot be resolved in the displayed picture.

In general, television pictures restricted by linear phase-shift filters exhibit greater apparent resolution and apparent freedom from ringing than is possible with ordinary minimum phase-shift filters.[6] It has also been shown by E. F. Brown of the Bell Telephone Laboratories that the apparent sharpness of a low-resolution TV picture can be significantly improved by introducing a controlled amount of overshoot in the transient response of the filters used in the video signal path. The optimum amount of overshoot is approximately 12 percent.

A linear-phase maximally-flat low-pass filter is used for the input filter. At half the sampling frequency the response of this filter is down 9.1 dB and down 38.8 dB at the sampling frequency. At a frequency of 1.39 MHz the response of the filter is down 59 dB and down 37 dB or more for all frequencies beyond 1.39 MHz.

A linear-phase low-pass filter with controlled overshoot is used for the output filter. At half the sampling frequency the response is down 10.5 dB and is down more than 60 dB at the sampling frequency. The step response of the filter was measured and found to have an 8 percent preshoot and 10 percent overshoot with respect to the step transition.

The composite loss of the pair of filters measured 19.6 dB at half the sampling rate (768 kHz) which meets the original 16 to 19-dB requirement.

Each filter is isolated by a pair of video amplifiers in order to provide resistive input and output impedances of 75 ohms. The amplifier gain of the input filter unit is adjusted to provide 0-dB transmission for a reference frequency at 100 kHz to compensate for the insertion loss of the input filter. The amplifier gain of the output filter unit is adjusted to provide 0-dB transmission at 100 kHz for the over-all system. This compensates for the insertion loss of the output filter as well as the signal loss encountered in the decoding operation.

XI. MONITORS

Two types of picture displays are used.

11.1 *Type I*

A Conrac CNA8 television monitor, modified to operate at the line rate of 9.6 kHz, is used as a general purpose monitor. This unit is completely self-contained and may be operated with a composite video signal with means provided for internal sync or separate horizontal and vertical external sync. The picture information is displayed on a five-inch square raster. The amplitude-frequency response of the video amplifier is flat to within ± 2 dB to 8 MHz. Provision for switching dc restoration in or out is also provided.

11.2 *Type II*

To facilitate the subjective testing of various television bandwidth reduction techniques, a variable parameter display system has been constructed which consists of two television monitors designed so that one functions as a master control unit and the other as a slave unit.

Test conditions are initially preset and viewed by the operator at the master monitor. The subject being tested views the pictorial information presented on the slave monitor. A-B control is permitted by the subject for viewing alternately any two given test conditions.

The two displays are capable of operating over a wide range of sweep rates, 3 kHz to 16 kHz for the horizontal rate and 30 Hz to 120 Hz for the vertical rate. Driven sweeps are employed, separate horizontal and vertical drive pulses being required.

The amplitude-frequency response of the video amplifiers is down 3 dB at 13.5 MHz. Using a sine wave response measuring technique, it has been determined that the frequency response of the kinescope is down 6 dB at 5 MHz at a highlight luminance of 10 footlamberts.

Whenever this display system is used in conjunction with the experimental television facility described herein, the horizontal line rate is restricted to 9.6 kHz and the vertical rate to 60 Hz. The video signal displayed on the monitors is band-limited to less than 768 kHz by the video filters.

XII. SYNCHRONIZING GENERATOR

All timing, gating, and blanking signals required are generated by the synchronizing generator as shown in Fig. 11. The required signal characteristics and timing sequences are described.

The precise sampling rate is determined by the storage capacity and delay period required for the frame memory, and is equal to the storage capacity divided by the delay period. The delay period is con-

stant and is equivalent to one TV frame period (1/60 second). The required storage capacity is determined by the picture format and at the present time is 25,600 samples. This results in a 1.536-MHz sampling rate. A temperature-controlled crystal oscillator is used to establish the sampling rate.

Digital count-down circuits are used to generate the synchronizing and blanking signals required for the operation of the camera chain and monitors. Separate horizontal sync and vertical sync signals are derived and are combined to generate a composite sync signal. A separate composite blanking signal is also established for system blanking while the composite sync signal serves to blank the camera.

The horizontal line rate of 9.6 kHz is derived by counting down from the sampling rate by a factor of 160. Since this factor is not an integer power of two, pulse steering techniques are used to alter the counting sequence of the counter to give the desired factor. The operations thus performed result in 160 samples per line, of which 20 samples are used to define the horizontal blanking interval, with 16 of the 20 samples being used to specify the horizontal sync period. The leading edge of the horizontal blanking interval precedes the horizontal sync period by one sample interval.

An additional count-down by a factor of 160 from the 9.6-kHz line rate is performed to generate the frame rate of 60 frames per second. Out of the total of 160 lines per frame thus established, 12 lines are used to define the vertical blanking interval with 6 of the 12 lines being used to specify the vertical sync period. The leading edge of the vertical blanking interval precedes the vertical sync period by one line interval. The composite blanking and composite sync signals are derived by using the AND operation to combine the horizontal and vertical blanking signals and the horizontal and vertical sync signals as shown in Fig. 11.

The results of the above operations limit the active region of the picture format to 140 samples per line and 148 lines per frame, all lines being scanned in sequential order each frame period.

Timing of the A/D converter, code translator, frame memory, and D/A converter is adjusted with respect to the 20-nanosecond sampling time of the A/D converter's sample-and-hold circuit which is used as reference. Each time that the sample-and-hold circuit is clocked at the sampling rate, sufficient time must be alloted for the A/D converter's coder modules to settle to a unique code before digital output information of the coder is clocked, in parallel, into the input flip-flop store of the code translator. Maximum time is allowed by storing in-

formation in the code translator just prior to clocking the following sample-and-hold operation.

The Gray-to-natural binary code conversion operation by the code translator is also allotted maximum time to settle to the binary code value by clocking results of the code conversion, in parallel form, into the output flip-flop store of the code translator just prior to inserting new information into the input flip-flop store. The digital output information of the code translator expresses encoded video information in the conventional binary code in parallel form.

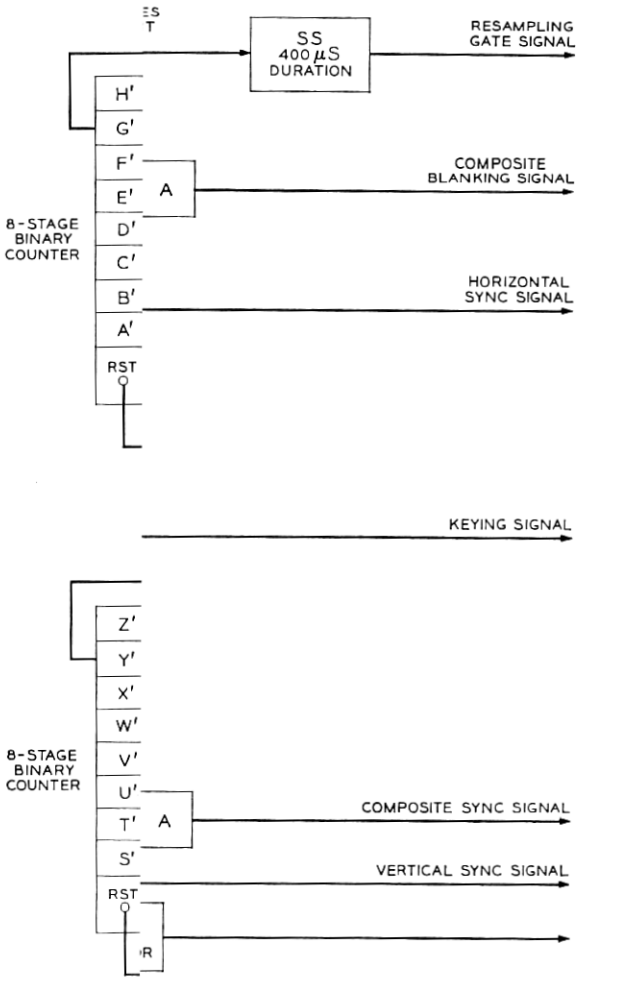
Output information of the code translator is conveyed to both the input of the frame memory and the D/A converter by high-speed gates which are controlled by the MCFF. Change of state of the MCFF is timed to occur during the transition time of the output flip-flop store of the code translator so as to maximize the interval of time in which each code word is presented to the frame memory.

In order to allow for any limited drift in frequency of the master oscillator and for slight changes in the delay period of the frame memory's delay lines, due to temperature effects, clocking of information into delay lines of the frame memory is adjusted under stable operating conditions to occur midway between transition periods of digital information which is presented to it.

Pulse output information of the delay lines which occurs in phase with clocking of the input information is inserted into the first stage of a four-stage shift register which is considered a constituent part of the frame delay period. The clock signal applied to the shift terminal of the shift register is timed to perform the shift operation one-half of a sample period later; therefore, timing of the frame memory's digital output information, taken from the last stage of the shift register, corresponds to the timing of the digital output of the code translator. Thus, the phase relationship of information conveyed to the input of the delay lines by high-speed gates is independent of the mode of operation of the frame memory.

The same relationship of clocking information into the flip-flop store of the D/A converter with respect to timing of the digital data applied, is the same as that maintained for the input of the delay lines.

Two additional gating signals, shown in Fig. 11, are generated by the sync generator. A 6-microsecond keying signal is required for operation of the synchronized clamping circuit. The keying signal is synchronous with the line rate and is timed to occur after the leading edge of the horizontal sync signal. The signal delay caused by the



OTE: τ_S - SAMPLE PERIOD
τ_L - LINE PERIOD

system's input filter must be compensated for. The remaining gating signal required for the system's operation is used by the resampler circuit employed in the D/A converter. A 400-nanosecond gating signal is applied to the resampler and timed to occur during that portion of the decoder output waveform which is free of transient disturbances.

A grating pattern for use in determining geometric linearity of both camera and monitor sweeps is also provided by the synchronizing generator.

XIII. SYSTEM APPLICATIONS

The application of this equipment to perform various system functions will be discussed in terms of the logic used to control the flow of information conveyed to the frame memory since this information is also simultaneously decoded and displayed on the system's TV monitor.

The information corresponding to a given picture point is available for processing only once each frame period, since the information is stored in delay lines. The information pertaining to all picture points which comprise any given frame of video information stored in the delay lines or any subset of picture points, thereof, can thus be updated with new information at a rate corresponding to the frame rate or a submultiple of the frame rate. The display rate of information conveyed to the monitor is kept constant at 60 frames per second to avoid the flicker problem, but the pattern and rate of displaying *new* information can be governed by direct control of the MCFF.

Frame repeating and selective replenishment systems have been demonstrated using this equipment. Their evaluation has been discussed in a separate paper.[1] The basic principles employed to implement these systems will now be discussed.

XIV. FRAME REPEATING SYSTEM

The basic frame repeating principle is illustrated by Fig. 12. The vidicon camera is sequentially scanned each frame period, resulting in an integration time of 1/60 second, but only every nth frame is simultaneously stored in the frame memory and displayed on the monitor. Every new frame of encoded information stored in the frame memory is repeated $(n - 1)$ times and is displayed on the monitor each time. Thus, every nth frame of video information scanned from the camera is displayed n times on the monitor. The display rate is

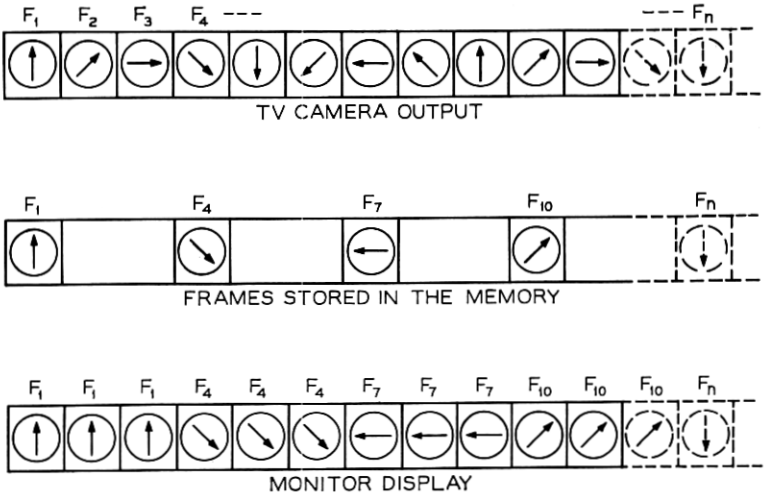


Fig. 12 — Basic frame repeating principle.

kept constant but the new picture rate can be varied by the choice of n. Straightforward logic techniques are employed for this case as shown in Fig. 13.

The state of the MCFF is controlled as follows: The frame rate is counted down by a factor n where n is an integral number and represents the number of times a given frame of video information is frame repeated. The output of the counter is coupled to the set input of the MCFF. The frame pulse applied to the input of the counter is also coupled to the clear (reset) input of the MCFF. A complementary flip-flop is used for the MCFF, and whenever a 1-state signal is applied to both the set and clear inputs simultaneously, the state of the flip-flop is reversed. Therefore, as it is used here, the 1 output of the MCFF assumes the 1-state whenever a 1-state signal is applied to the set input. Once the MCFF is set the following frame pulse will reset the stage and it will remain in this state until the next set pulse occurs. Thus, every nth frame period the MCFF will be set for one frame period in duration, conveying new information into the frame memory and reset for $(n - 1)$ frame periods, thereby circulating the data stored in the frame memory. Thus, each new frame of video information stored in the memory will be presented a total of n times to the monitor.

The change of state of the MCFF is directed to occur during the

vertical retrace period so that an integral frame of video information is stored in the frame memory. In this manner, a break in continuity of the video information will not occur in the active region of the picture.

With a vidicon integration time of 1/60 second, frame repeating was observed using rates of 30, 20, 15, 12, 10, 8.6, 7.5, 6.7, and 6 new pictures/second. A single frame of processed video information can be stored indefinitely in the frame memory by removing the set pulse applied to the MCFF after the information has been stored in the memory. This feature allows a photograph to be taken of a single frame of video information displayed on the monitor each frame period. Because the stored picture is available for long periods of time, any particular area of interest in the picture may be examined on the monitor under different contrast and brightness conditions. An oscilloscope may be used for observing any particular waveform characteristic in detail.

In the frame repeating experiment the vidicon camera is sequentially scanned every frame period with every nth frame being stored in the frame memory in digital form. By scanning the vidicon every frame period, each picture read out has been integrated on the vidicon photocathode for 1/60 of a second. The integration time of the vidicon may be varied by scanning the vidicon every nth frame period instead of every frame period. Each picture read from the camera is stored in the memory and repeated n times on the monitor. In this manner, the visual signal is integrated on the vidicon photocathode for $n/60$ of a second for each picture read out. This type of camera operation is defined as the integrate mode of operation.

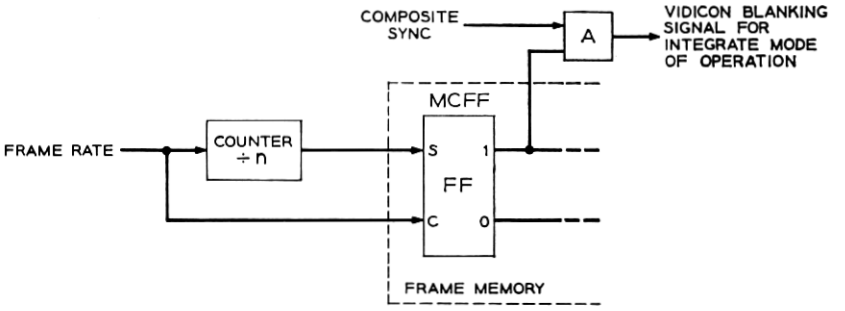


Fig. 13 — Control logic for frame repeating system.

An effort has been made to control the integration time of the vidicon for a frame repeat system where each frame is repeated four times. A special gating signal is provided for the vidicon in the integrate mode of operation. For this mode of operation, the vidicon beam current is gated on for one frame period every four frames. During the frame read-out of the vidicon, the frame memory is also gated to store new information into the memory as it is being read from the camera.

The gating signal for the vidicon is derived from the 1 output of the MCFF. A composite sync signal is combined with the MCFF signal by the AND circuit, as shown in Fig. 13 and the resultant signal is directly coupled to the vidicon cathode. Normal blanking signals are provided in this manner during the frame read-out.

XV. REPLENISHMENT SYSTEMS

In a replenishment system, only $(1/n)$th of the total amount of information stored in the frame memory is replaced with new information each frame period, a total of n frame periods being required to replenish all of the information stored in the memory. In each succeeding group of n frame periods, the same pattern of replenishment is repeated.

Six different replenishment patterns have been demonstrated. In five cases, total replenishment of the information stored in the frame memory is accomplished over four frame periods (1/15 second), one-quarter of the information being replenished each frame period according to a given pattern. For the remaining case, total replenishment is accomplished every two frame periods (1/30 second), one-half of the total information stored in the memory being replenished with new information each frame period.

The various replenishment patterns are shown in Fig. 14. The numbers represent the frame period relative to the total replenishment period during which a particular picture element is replenished in the picture format. The basic principles employed to implement these various patterns are described.

Logic is programmed to control the MCFF in such a manner that the data stored in the frame memory is replenished with new information according to the desired pattern. The MCFF is clocked at specified multiples of the sampling, line, and frame rates for replenishment patterns 1 through 5. The remaining pseudo-random pattern is dependent only on the order in which a sequence of pseudo-random

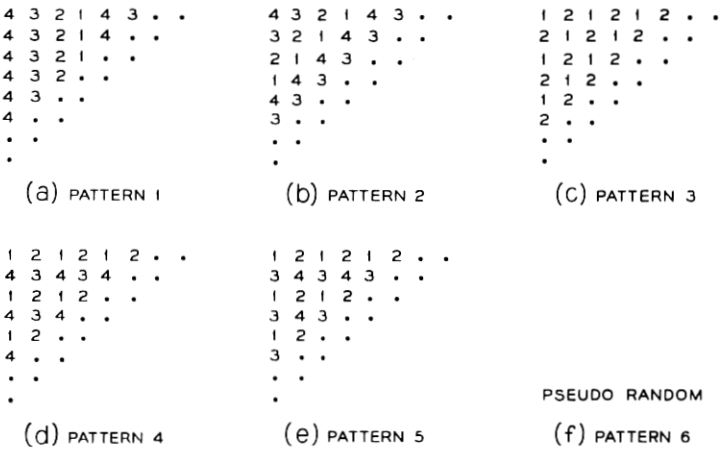


Fig. 14 — Various replenishment patterns implemented.

digits is generated at the sampling rate. This pattern is inherently locked to the frame rate.

The control logic requires clock pulses which occur at the sample, line, and frame rate. The clock pulses which occur at the line and frame rate are shifted in phase so as not to coincide with each other or with the clock pulses occurring at the sample rate. Pulse steering techniques are used in the control logic to direct the incoming pulses occurring at the sample rate to the set or clear inputs of the MCFF, depending on whether the write or repeat mode of operation for the memory is to be established. This allows a change of state of the MCFF to be clocked to the correct phase of the master clock independent of the line and frame rates which have been shifted in phase.

15.1 *Pattern 1*

The first replenishment pattern is shown in Fig. 14(a). For this pattern, the picture elements replenished each frame period lie in vertical lines spaced every fourth picture element. In each succeeding frame period, the replenishment pattern for a single frame is shifted horizontally one picture element in the picture format. Thus, in four frame periods, all information stored in the frame memory is replenished once. The pattern of replenishment then repeats itself. Logically, this may be accomplished as shown in Fig. 15.

The input sample rate is scaled down by a factor of four by using

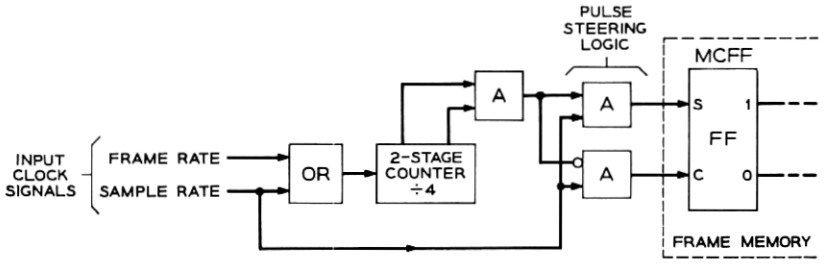


Fig. 15 — Control logic for replenishment pattern 1.

a 2-stage counter and a two-input AND to recognize the all 1's state of the counter. Each time that the counter is advanced through the all 1's state, the output of the AND assumes a 1-state. This condition causes the pulse steering logic to direct the next sample pulse to the set input of the MCFF. When this occurs, the write mode of operation is established for the frame memory and the counter is advanced to the all 0's state. The output of the AND which recognizes the state of the counter now assumes a 0-state. This condition causes the pulse steering logic to direct the sample pulses to the clear input of the MCFF, which establishes the repeat mode of operation for the frame memory. In this manner, the MCFF is set for only one sample interval corresponding to every fourth sample in the frame. Each frame period, the same corresponding picture elements of each line is replenished with new information, since the number of picture elements per line (160) is a multiple of four. Hence, this process establishes the vertical pattern of replenishment. At the end of each frame period, a pulse corresponding to the frame rate is used to advance the state of the counter one count. This is accomplished by the OR operation which is used to couple both the sample pulses and frame pulses to the input of the counter. This effectively shifts the single frame replenishment pattern horizontally one sample period each frame period. After four frame periods, the four frame replenishment patterns will be repeated.

15.2 *Pattern 2*

The second replenishment pattern is shown in Fig. 14(b). In this case, the picture elements replenished each frame period lie on diagonal lines spaced every fourth sample. Each succeeding frame period, the replenishment pattern for a single frame is shifted horizontally one picture element with respect to the previous frame. In four frame periods all information stored in the frame memory will be replenished

once. The pattern of replenishment will then repeat itself. Logically, this may be accomplished as shown in Fig. 16.

The logic required to generate this pattern of replenishment is the same as in the preceding case with one exception: means must be provided to shift the pattern horizontally one picture element each line period. This is accomplished by advancing the state of the counter one count at the end of each line period. Clock pulses corresponding to the line rate are coupled to the input of the counter through the OR operation which precedes the counter.

During each frame period the replenishment pattern repeats itself every four lines. Since this factor is a submultiple of the number of lines in a frame (160 lines/frame), the same corresponding picture elements would be replenished in every frame unless an additional horizontal shift in the replenishment pattern was employed at the end of each frame period. This is accomplished by advancing the state of the counter one count at the end of each frame period as in the preceding case. After four frame periods, all information stored in the frame memory will be replenished only once and the replenishment pattern will then be repeated.

15.3 *Pattern 3*

The third replenishment pattern is shown in Fig. 14(c). This pattern is equivalent to pattern 2 except the rate of replenishment is increased by a factor of two, thus requiring only two frame periods rather than four to replenish all information stored in the frame memory before the pattern repeats itself. The logic required to generate this pattern of replenishment is the same as for pattern 2 with one exception: a divide-by-two counter is used rather than a divide-by-four counter. All other logical functions and operations remain the same.

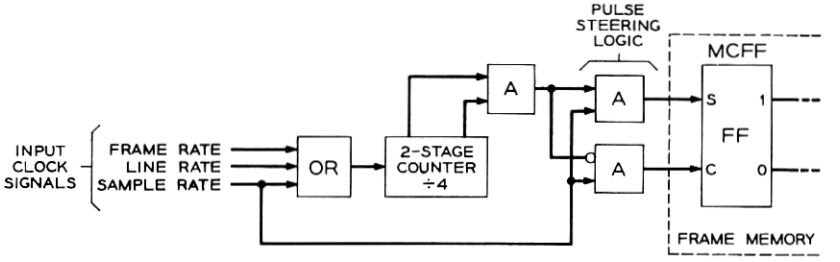


Fig. 16 — Control logic for replenishment pattern 2.

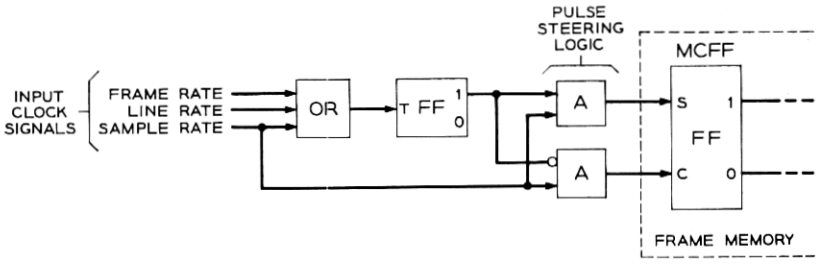


Fig. 17 — Control logic for replenishment pattern 3.

This change is accomplished by replacing the 2-stage counter and its associated AND, used to generate pattern 2, with a complementary flip-flop as shown in Fig. 17. The output of the OR is applied to the toggle input of the flip-flop and the output of the flip-flop is applied to the pulse steering logic in place of the AND output. This modification permits all picture elements to be replenished only once in two frame periods rather than the four frame periods required by pattern 2.

15.4 *Pattern 4*

The fourth replenishment pattern is shown in Fig. 14(d). With respect to the picture format, the basic replenishment pattern consists of replenishing alternate samples on alternate lines each frame period. A means is provided for shifting the position of the basic pattern each frame period in the desired sequence to insure that a different subset of picture elements is replenished each frame period. The sequence of shifting the position of the basic replenishment pattern is repeated every four frame periods after all picture elements stored in the frame memory have been replenished once. Logically, this may be accomplished as shown in Fig. 18.

A complementary flip-flop (labeled FF-S) is used to define alternate samples in a frame period. Using the OR operation, clock signals occurring at the sample rate are applied to the toggle (T) input of the flip-flop. When operating the flip-flop in this manner, the 1 output of the flip-flop assumes a 1-state every other sample interval. The 1-state signal condition is used to define alternate samples in the frame period. The same sequence of alternate samples will be specified for each line in a frame since the period of sample replenishment is a submultiple of the line period.

A second complementary flip-flop (labeled FF-L) is used to define alternate lines in a frame period in the same manner as above. The

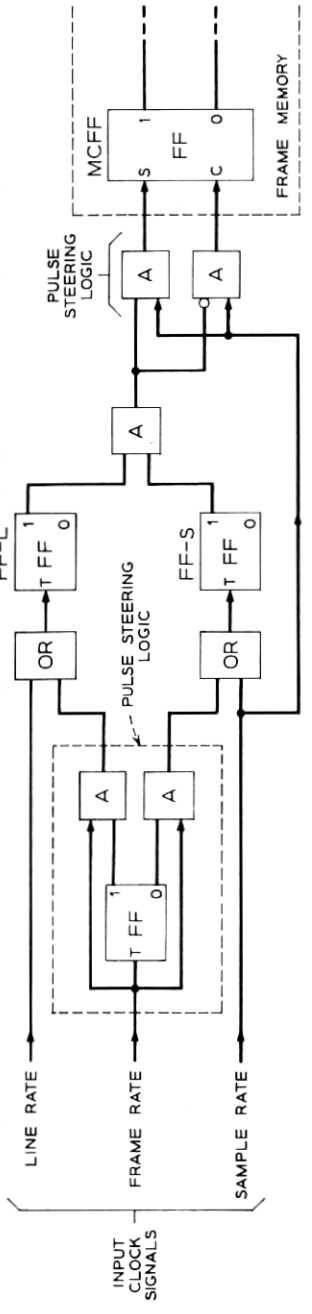


Fig. 18 — Control logic for replenishment pattern 4.

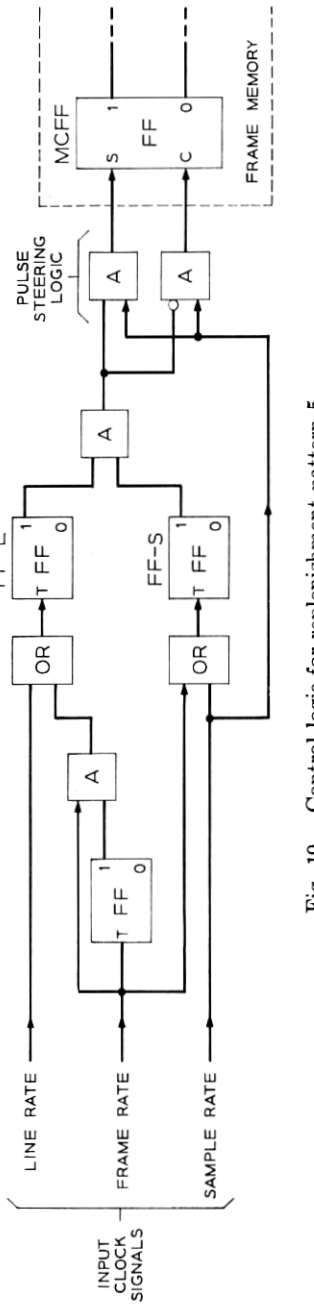


Fig. 19 — Control logic for replenishment pattern 5.

OR operation is used to apply clock pulses, occurring at the line rate, to the toggle input. The 1 output of the flip-flop assumes a 1-state every other line period which is used to define alternate lines in the frame period. Since the picture format is comprised of an even number of lines, the line replenishment pattern will normally repeat itself each frame period unless a shift operation is employed.

In order to replenish a different subset of picture elements each frame over a four frame period, in the required sequence, the basic replenishment pattern for a single frame is shifted one sample interval at the end of each frame period, alternating between a horizontal and vertical shift operation with respect to the picture format. Only one shift operation is performed each frame period. The horizontal shifting of the replenishment pattern's position is accomplished by reversing the state of FF-S at half the frame rate. The vertical shift operation is achieved by reversing the state of FF-L at half the frame rate but timed to occur in alternate frame periods in which the horizontal shift operation is not performed.

In each case, to reverse the state of the flip-flop, the OR operation is used to convey clock pulses, occurring at half the frame rate, to the toggle input of the flip-flop.

Pulse steering techniques are used to derive the clock pulses required for the shifting operations. Alternate clock pulses derived from the frame rate are steered to the respective inputs of the OR's in the correct sequence.

By performing the AND operation on the 1-output of both flip-flop's (FF-S and FF-L), alternate samples on alternate lines each frame period are specified in the required sequence when the output of the AND assumes a 1-state. This condition occurs only when both inputs assume a 1-state. The output signal of the AND is applied to the pulse steering logic which controls the MCFF. The write mode of operation will be established for the frame memory each time the output of the AND assumes a 1-state; otherwise the repeat mode of operation is established.

15.5 *Pattern 5*

The fifth replenishment pattern is shown in Fig. 14(e). The basic single-frame replenishment pattern for this system is identical with that of pattern 4. The sequence of shifting the basic pattern over a four-frame period differs from pattern 4 in one respect. The horizontal shifting of the replenishment pattern's position is performed every frame period rather than every other frame period. All other logical

operations remain the same as shown in Fig. 19. The OR operation preceding FF-S is used to convey clock pulses, occurring at the frame rate, to the toggle input of FF-S. The state of FF-S is thus reversed every frame period, as required, to generate the desired replenishment pattern over a four-frame period.

15.6 *Pattern 6*

The six replenishment pattern is not regular over blocks of four picture elements as in the other 4:1 replenishment systems described above, but is pseudo-random. The same average bit rate is maintained by replenishing one-quarter of the total amount of information stored in the memory each frame period. In four frame periods all information stored in the frame memory is replenished only once. The pattern of replenishment then repeats itself. Logically, this may be accomplished as shown in Fig. 20.

A quasi-random binary digit generator is used to generate a sequence of random binary digits at the system's sampling rate. The sequence is periodic with 2^{10} digits in each period. During each period of this sequence of random digits, every one of the 2^{10} possible strings of ten digits appears exactly once as a block of ten consecutive digits. The period of this sequence of digits is chosen to be a multiple of the system's frame period so that the same sequence of digits is generated each frame period.

A logical operation is performed on the output of the random digit generator to remap the sequence over four frame periods. In the process of generating the quasi-random sequence, each time that two consecutive digits in the random sequence corresponds with a specific

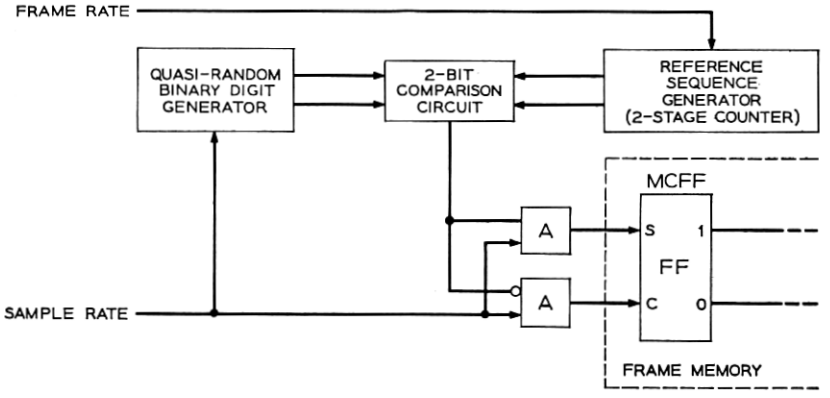


Fig. 20 — Control logic for pseudo-random replenishment pattern.

two digit reference sequence new information is inserted into the frame memory; otherwise, the previous information stored in the frame memory is recirculated. During four consecutive frame periods, a different two digit sequence is used as reference each frame period. The order of generating the reference sequence is then repeated.

Only four different two digit reference sequences are possible—00, 01, 10, and 11. Considering consecutive digits in the random digit sequence, each of these combinations of two digits occurs at random an equal number of times during each period of the random digit sequence. The replenishment pattern thus generated directs replenishment, in a random manner, of one-quarter of the total amount of information stored in the frame memory each frame period. All information stored in the memory is replenished only once during any four consecutive frame periods.

The pseudo-random digit generator consists of control logic and a ten-stage shift register advanced at the system's sampling rate. The output of all stages of the register is fed to the control logic as shown in Fig. 21. The output of the exclusive OR and its prime is coupled to the input of the first stage of the register. The control logic normally functions as an exclusive OR operation with the output of the tenth and seventh stages of the shift register coupled to the input except when the string of $000\cdots001$ digits appears. For this condition, the output of the seventh stage, coupled to the input of the exclusive OR by the OR operation, is temporarily over-ridden by the output of the AND which assumes a 1-state, permitting the string of $000\cdots00$ digits to be generated. For a ten-stage shift register, every one of 2^{10} possible strings of ten digits appears exactly once, as a block of ten consecutive digits each period of the sequence.

In spite of the fact that the nth digit is completely determined by the digits which precede it, the sequence of digits resembles, in some respects, sequences which are produced when the nth digit is chosen at random with probabilities $\frac{1}{2}$ for 0 and $\frac{1}{2}$ for 1 and independently of other digits.

The remapping operation is performed by comparing the output of the ninth and tenth stages of the shift register with the logical state of a 2-stage binary counter which serves as the reference sequence generator. The binary counter is advanced at the frame rate. When in agreement with each other, a 1-state exists at the output of the comparison circuit. This condition permits a sample pulse to be coupled to the set input of the MCFF by the pulse steering logic allowing new information to be inserted into the frame memory. If no agreement

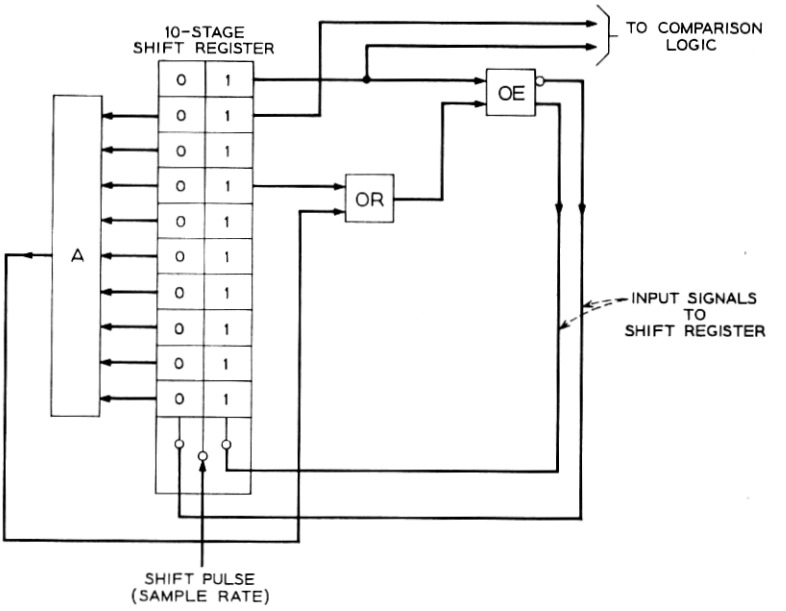


Fig. 21 — Quasi-random binary digit generator.

exists, the output of the comparison circuit assumes a 0-state causing the sample pulse to be steered to the clear input of the MCFF, thereby recirculating the information previously stored in the frame memory. Since the shift register is stepped along at the sample rate, the comparison operation is performed each sample period. Four frame periods are required to step the 2-stage binary counter through all possible states before recycling. Thus, four frame periods are required to replenish all information in the frame memory once. Each succeeding four frame periods, the same pattern of replenishment is repeated.

XVI. DISCUSSION

A description of an experimental low-resolution television system employing digital and storage techniques has been presented. The flexibility of this system permits subjective testing to be performed on a variety of bandwidth compression schemes processed in real-time to determine and evaluate the factors affecting the acceptability of such schemes.

A modified camera chain is used to generate a picture signal with a format consisting of 160 lines per frame sequentially scanned at 60

frames per second. The picture information is processed in real-time in a digital format. A digital memory is employed with sufficient capacity to store one complete frame of video information encoded as 8-digit PCM—a total of 204.8 kilobits at a rate of 1.536 MHz per second. Means are provided to introduce into the memory whole new pictures or selected picture elements at any interval which is a multiple of the frame rate. The information inserted into the memory is decoded and displayed on a monitor at a rate of 60 pictures per second in order to avoid flicker.

A number of frame repeating and replenishment systems have been demonstrated in real time using this equipment, however the system is in no way limited to those applications which have been discussed.

XVII. ACKNOWLEDGMENTS

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REFERENCES

1. Brainard, R. C., Mounts, F. W., and Prasada, B., Low-Resolution TV: Subjective Effects of Frame Repetition and Picture Replenishment, B.S.T.J., *45*, this issue, pp. 301–311.
2. Edson, J. O. and Henning, H. H., Broadband Codecs for an Experimental 224 Mb/s PCM Terminal, B.S.T.J., *44*, November, 1965, pp. 1887–1940.
3. Waldhauer, F. D., Analog-to-Digital Converter, U. S. Patent 3-187-325, applied for July 2, 1962; issued June 1, 1965.
4. Meitzler, A. H., Ultrasonic Delay Lines for Digital Data Storage, Trans. IRE Prof. Group Ultrasons Eng., *VE-9*, December, 1962, pp. 1–8.
5. Kovanic, E. F., A High Accuracy Nine-Bit Digital-to-Analog Converter Operating at 12 mc, IEEE Trans. Commun. Electron., March, 1964, pp. 185–191.
6. Fredendall, G. L. and Kennedy, R. C., Linear Phase Shift Video Filters, RCA Review, *11*, September, 1950, pp. 418–430.