A Phase-Locked Primary Frequency Supply for the L Multiplex

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The carriers and pilot tones of the L multiplex are all derived from a single source of 4 kc. The new primary frequency supply provides this primary frequency. It is designed to operate phase-locked to a pilot tone derived from an incoming carrier system and hence to have no frequency error with respect to that tone. The unit features a high degree of frequency stability, even in the absence of the pilot; it features more reliable performance and lower maintenance as well as marked size reduction compared with the older equipment.

I. INTRODUCTION

In single-sideband suppressed-carrier transmission systems, of which the L-type multiplex is a modern example, it is necessary to supply, at each terminal, sequences of harmonically related carrier frequencies to power the various modulators, and also to provide line pilot frequencies for system regulation. Because the accuracy requirements for these frequencies are severe, it has proven most economical and technically satisfactory to derive them all from a single highly accurate and stable source which, in the case of the L-type multiplex, has been named the primary frequency supply. The means by which the ensemble of carrier and pilot frequencies is derived therefrom are described in a companion article.[1]

II. REQUIREMENTS — GENERAL

To provide flexibility within and promote orderly growth of the communications plant, it is desirable that newly designed equipment operate compatibly with and serve as electrical replacements for older counterparts, where such exist. This compatibility must, however, be achieved without limiting the performance capabilities of the new equipment to those representative of the older. The predecessor of the primary fre-

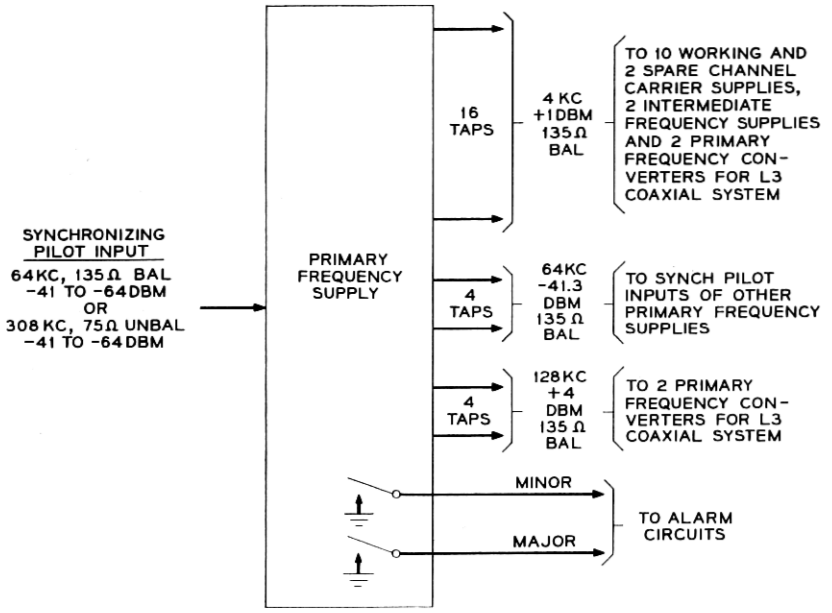

Fig. 1 — Primary frequency supply interfaces.

quency supply was the 4-kc supply of the L telephone terminal,[2] together with various physically separate, but functionally associated synchronizing and distributing circuits. Since it was evident that there were many installations where combinations of old and new equipment would occur, compatibility assumed great importance. Fig. 1 shows the electrical interfaces between a fully loaded primary frequency supply (as well as its functional predecessor) and the remainder of the multiplex equipment. Three output frequencies are provided, (*i*) the basic 4 kc, corresponding to the channel separation of the multiplex,* (*ii*) 128 kc, required for carrier generation in associated L3 coaxial system terminals, and (*iii*) 64 kc, which may optionally be used for synchronization, as described later. All carrier and pilot frequencies of both the L-type multiplex and the L3 coaxial system are integral multiples of the basic 4 kc.

With compatibility and replaceability postulated, *minimum* performance requirements, equivalent to those of the older equipment, are established. At this point, the execution of a prudent design requires consideration of probable future applications of the equipment which might increase the severity of these requirements, and, where economically

* Alternatively, some of the 4-kc output taps may be used to supply a reference frequency for carrier generation in other carrier systems.

feasible, provision either of performance consistent with these anticipated applications, or means for future improvement without complete redesign. Such anticipated applications include, among others, increasingly sophisticated systems for data transmission, stereophonic program transmission, and establishment of a system-wide frequency standard. In addition, the rapid growth of intercontinental toll facilities via submarine cable and, as seems likely, via satellite-borne systems, demands conformance with accepted international standards of performance.[3]

In addition to satisfying the performance requirements arising from the considerations outlined above, the design of the primary frequency supply must comply with constraints of space, environmental conditions, and available power supply, and, because of the large number of dependent message channels — as many as 3600 — must guarantee a very high order of reliability and provide easy access for maintenance and repair.

2.1 *Frequency Accuracy*

The frequency accuracy requirements of the primary frequency supply are of two kinds, absolute and relative. Absolute accuracy is a statement of the difference between the nominal and actual frequencies of a given supply measured in terms of real time; relative accuracy is a statement of the difference in actual frequencies of two supplies. Both requirements must be stated in terms of allowable drift per interval of time; for the moment this will be loosely defined as the normal maintenance interval, the duration of which will be determined later. Since all derived frequencies are generated by frequency multiplication, the fractional accuracy requirement for any carrier or pilot applies also to the primary source.

The absolute requirement stems from the necessity for a proper "fit" of the derived carrier and pilot frequencies to the transmission characteristics of the highly selective filters to which they are applied. Of these frequencies, the most critical is the 92-kc group regulating pilot,[4] not only because of the high selectivity of the corresponding filters, but also because of the serious effects of such errors on system performance. The tolerable error at this frequency has been established at one cycle per second. Rounded off, this is one part per 10^5 per maintenance interval.

Relative frequency accuracy is the measure of the difference between the primary frequency and its derivatives within a given multiplex terminal to those within its associated counterpart at the far end of a

transmission facility. The consequence of inaccuracy of relative frequency is frequency translation error, in which all components of a message are displaced in frequency by an equal number of cycles, with resultant destruction of their normal harmonic relationship and hence, loss of fidelity of the recovered information.

The channel most susceptible to this type of degradation is that which occupies the highest line frequency produced by the L3 coaxial terminal when it is used in conjunction with (and with its carriers derived from) the L multiplex. The corresponding "virtual" carrier frequency is 8.284×10^6 cycles per second. The more susceptible of present services, such as program and voice-frequency telegraph, suffer impairment due to frequency errors in excess of two cycles per second. These considerations lead to a relative frequency accuracy requirement of 2 parts per 8.284×10^6, or, rounded off, 2 parts per 10^7 per maintenance interval. Comparison of this requirement with that for absolute frequency accuracy reveals that the relative accuracy requirement is the more severe by more than an order of magnitude, and is therefore controlling.

In order to satisfy the relative accuracy requirement without correspondingly increasing the absolute requirement to values which were economically impractical at the time of the design of the older 4-kc supply, so-called "synchronous" operation was adopted. This was accomplished by designating a selected supply as the "master"* and transmitting, as a pilot, an integral harmonic (64 kc or 308 kc) of its output frequency. At controlled terminals the corresponding locally generated harmonic is compared with the incoming pilot, and correction automatically effected. In the older L-type telephone terminals, the correction is via an electromechanical servo loop. Although this system is theoretically capable of perfect correction, its sluggish nature, together with the effects of static friction, result in a usual relative error of about two parts per 10^7, which is marginal.

It is important to remark here that multiplex terminals often receive synchronizing and message information over different transmission paths. Increasing emphasis on system security points up the desirability of minimizing service degradation in those cases where the synchronizing path may be interrupted while the message path remains intact. In the older 4-kc supply, the static friction of the mechanical elements

* At present, the "master" supply is located in New York City; actually, it is in turn controlled by the Bell System Primary Standard of Frequency at Murray Hill, N. J., the accuracy of which is one part in 10^9, indefinitely (achieved by periodic correction).

From this master are controlled very nearly all of the multiplex terminals in the continental United States. As many as nine synchronizing links may be interposed between the master and the most remote terminal.

of the synchronizing servo has provided a useful "memory" to prevent any substantial change of frequency during such interruptions.

The new primary frequency supply is, therefore, required to have the capabilities both of synchronizing and of being synchronized by existing 4-kc supplies, and of satisfactory operation on a free-running basis for appreciable intervals of time. Despite the value of the frictional "memory" of the electromechanical servo of the 4-kc supply, maintenance problems led to its abandonment in favor of an all-electrical servo which, during normal operation, maintains a constant phase relationship between the locally generated and incoming pilots, and so completely eliminates relative frequency errors. The free-running accuracy requirement is satisfied by making the free-running frequency accuracy of each primary frequency supply sufficiently great (and, therefore, the required frequency-control range so small) that the requirements of the preceding section are fulfilled even though control is relaxed due to pilot interruption. This requirement becomes 1 part in 10^7 when allowance is made for two oppositely drifting supplies. Present state-of-the-art permits quite economical realization of this accuracy for one-month intervals; at somewhat greater cost the interval can be extended to six months. The requirement, therefore, was established as lying between the above limits, taking the following into account:

1. Relatively few supplies will be loaded with full 1800-channel systems; in these cases it appears most economical to shorten the maintenance interval, rather than burden all systems with the added cost of unneeded accuracy.

2. The probability of the most susceptible services' occupying the least favorable carrier frequency slot is small.

3. The possibility of "network" interconnection of synchronizing pilot is being studied. If adopted, this will make the probability of pilot failure almost negligible.

To meet this objective, two distinct phase-locked frequency supply circuits are provided, either of which supplies the useful output at any given time. A minimum of components — all passive — appear in the common path following the combining circuits. The latter employ hybrid circuitry, and are so designed that either input can be open- or short-circuited without materially affecting transmission from the alternative supply via the conjugate input. Failure of the working supply initiates a transfer to the alternate supply, and simultaneously provides a minor alarm and visual indication so that repairs can be effected. The phase-lock of the two supply circuits, together with proper phasing of the hybrid transformers in the combining circuits and the high switching speed all help to minimize transmission disturbances due to the

transfer. Minor alarms and visual indications are also provided to indicate failure of the non-working supply circuit, failure of the incoming pilot, and end-of-range of the automatic frequency and phase-control circuits. The latter function is performed by meter-relays, which also serve as indicators during adjustment of the centering of the phase control range. Complete failure of any of the three output frequencies results in a major alarm.

Routine maintenance consists of observing and adjusting to a minimum the voltage applied to the varactor diode to effect phase-lock. This has the effect of matching the natural frequency of the controlled oscillator to the frequency of the controlling master oscillator and hence minimizing the frequency deviation that would result were pilot control lost. One-month maintenance intervals are expected to be sufficient for newly-installed equipment, with increases to three or six months after aging of the oscillator crystals.

Test jacks are provided to permit the oscilloscopic examination of significant waveforms in the digital circuitry. To correct malfunctioning circuitry, the plug-in circuit containing the defective elements will be removed and replaced by a spare. Field repair of defective plug-in circuits will not be attempted.

2.2 *Mechanical, Environmental and Power Supply Requirements*

The primary frequency supply is designed to mount in a standard nineteen-inch relay rack, in a space $5\frac{1}{4}$ inches high by 15 inches deep. The ambient temperature limits are 38° to 120°F. Performance must be unaffected by a mechanical shock having 3-g acceleration. Available power supply is -21 to -28 vdc.

III. TIMING OSCILLATOR

The basic timing oscillator of the primary frequency supply is crystal-controlled and operates at a frequency of 1.024 mc. This choice of frequency is, as required, a binary multiple of 4 kc, and is high enough to permit use of a crystal cut which is favorable to stability, yet not so high as to require an inordinate number of frequency dividers. A modified Pierce circuit[5] is used, as shown in Fig. 2. The frequency of the oscillator is controlled, over a range of ± 25 parts per 10^7, by the capacitance of the varactor diode, which is effectively in series with the quartz plate. The capacitance of the varactor diode is, in turn, governed jointly

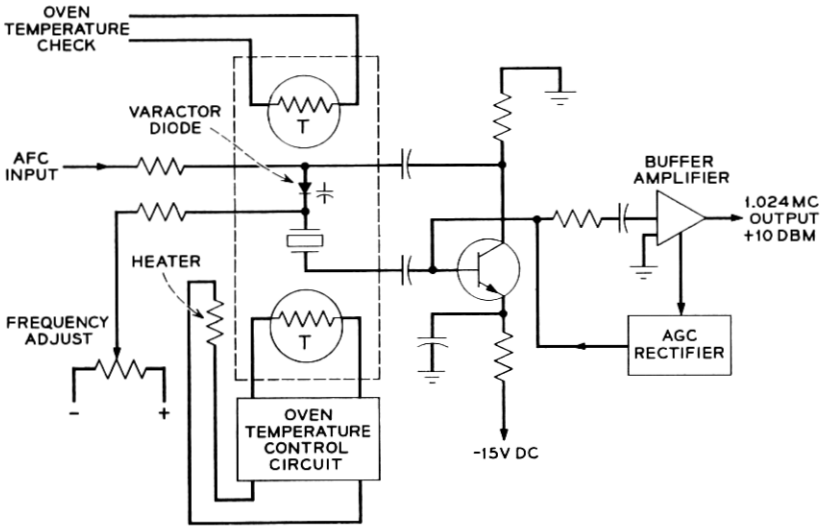

Fig. 2 — Timing oscillator.

by the frequency-control voltage and the setting of the frequency adjustment potentiometer. The five-stage buffer amplifier isolates the oscillator from the connected load, and permits the oscillator proper to operate at a low level, which is favorable to stability.

The crystal is a plano-convex AT cut quartz plate, operating in the fundamental mode. It is mounted in an evacuated cold-welded metal enclosure and, together with the varactor diode, is housed in an oven which is provided with a stepless oscillating closed-loop temperature control system which maintains the temperature constant within $\pm 0.15°C$ for all anticipated ambient conditions. A monitoring thermistor is provided so that the oven temperature can be checked at any time.

IV. DIGITAL FREQUENCY DIVIDERS

Although the inputs and outputs of the primary frequency supply are signals of sinusoidal waveform, the advantages of digital techniques for the necessary frequency division, switching, alarm, and frequency and phase comparison functions led to their adoption for the internal circuitry. Among these advantages are:

1. Economies resulting from the use of identical digital circuits for various logic functions.

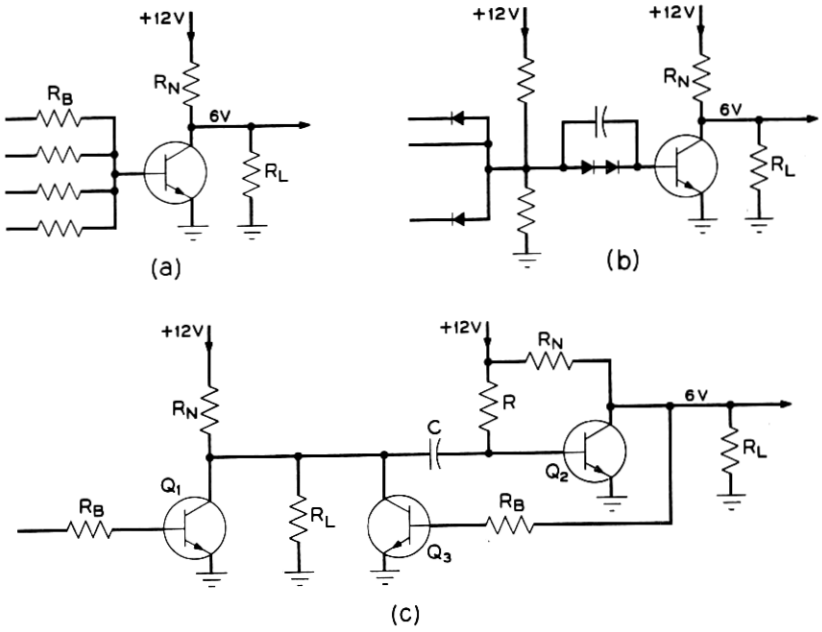

Fig. 3 — Logic circuits.

2. The relative ease with which the 77-to-1 division, necessary for operation with a 308-kc pilot, could be achieved.

3. The go-no-go nature of digital circuits, which contributes to ease of maintenance.

4. The inherently excellent time precision which can be realized with this type of circuitry.

The three basic transistor logic circuits used in the frequency divider units are shown in Fig. 3. A 12-volt supply with a transistor node resistance (R_N) of 2370 ohms is used for all logic functions. The value of the load resistor R_L is selected to limit the maximum collector-to-emitter voltage to 6 volts. The majority of logic functions are performed by the Transistor-Resistor-Logic (TRL) of Fig. 3(a). When an increase in switching speed is required from this circuit, a capacitor is used in parallel with the base resistor R_B . Since silicon transistors are used, reverse bias for the base circuit is not required. The Transistor-Diode-Logic (TDL), Fig. 3(b), is used to perform fast gating functions where as many as eight input signals are received. The two series diodes in the base circuit develop the required reverse bias to insure turnoff of the transistor.

This method of obtaining bias proves more efficient than providing a special power supply when relatively few TDL circuits are required as in this equipment. The Univibrator (U) logic circuit, Fig. 3(c), is used to generate a pulse of controlled length from a positive-going pulse of any duration greater than 0.1 microsecond. The length of the pulse is determined by the time constant of R and C.

The signals received by the digital frequency dividers from both the timing oscillator and the pilot amplifier are sine waves. It is necessary to convert these signals to logic type signals before they can be used. This conversion must be accurate within 0.1 microseconds. The sine wave to logic pulse converter used to perform this function is shown in Fig. 4. Q_1 is an emitter follower, with temperature stabilization of its bias circuit provided by CR_1 and CR_2. Q_2 provides high switching current to Q_3, which is operated as a common-base amplifier. The base voltage E on Q_3 is set to a value that yields a symmetrical square wave at the collector of Q_3 for a sine wave input at Q_1. The square wave is converted to logic level by coupling through C to Q_4 with a dc restorer diode CR_3.

The binary frequency division is performed by a three-stage transistor circuit (see Fig. 5). Q_1 and Q_2 form a flip-flop circuit with diode-capacitor steering for the input signal. The negative edge of an input square wave is used to change the state of the flip-flop circuit. A buffer amplifier, Q_3, is used to minimize the loading effects of associated logic circuits on the flip-flop counter stage. The maximum delay through the binary counter stage is 0.05 microsecond.

The method of using the divide-by-256 unit with the timing oscillator, pilot amplifier, and digital discriminator to obtain 64-kc pilot phase-

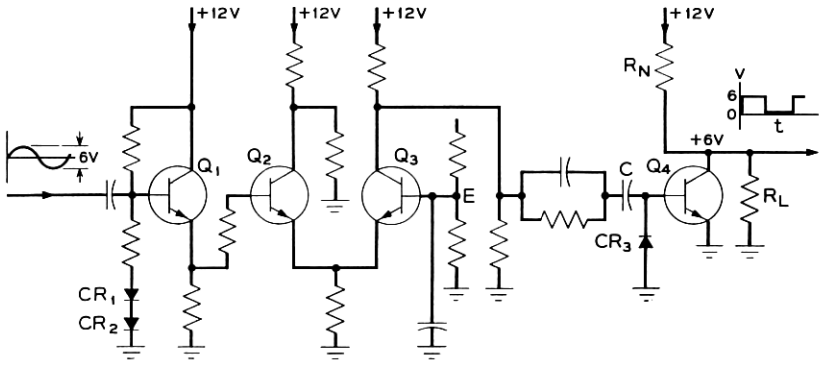

Fig. 4 — Sine-wave to logic pulse converter.

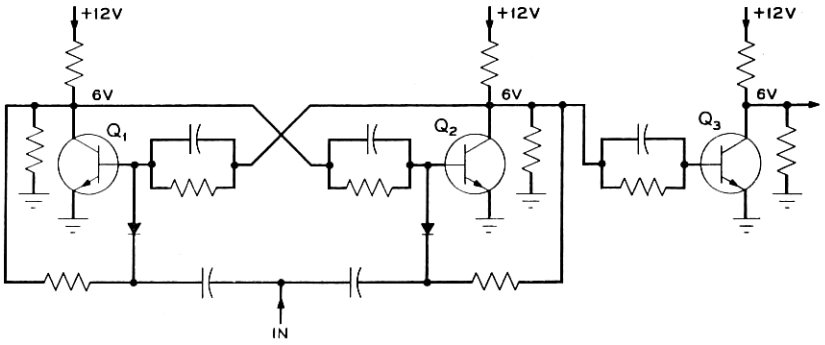

Fig. 5 — Binary counter circuit.

lock, and generate the basic frequencies for the carrier supply, is shown in Fig. 6. The 64-kc "clocked" pulses for the digital discriminator are generated by diode gate no. 1, which receives gating pulses from the first four binary counter stages, and the clocking pulses from the timing oscillator. The digital discriminator[6] compares the phase of the 64-kc clocked pulses with that of the 64-kc pilot and generates a dc voltage proportional to their phase displacement. This dc voltage is applied

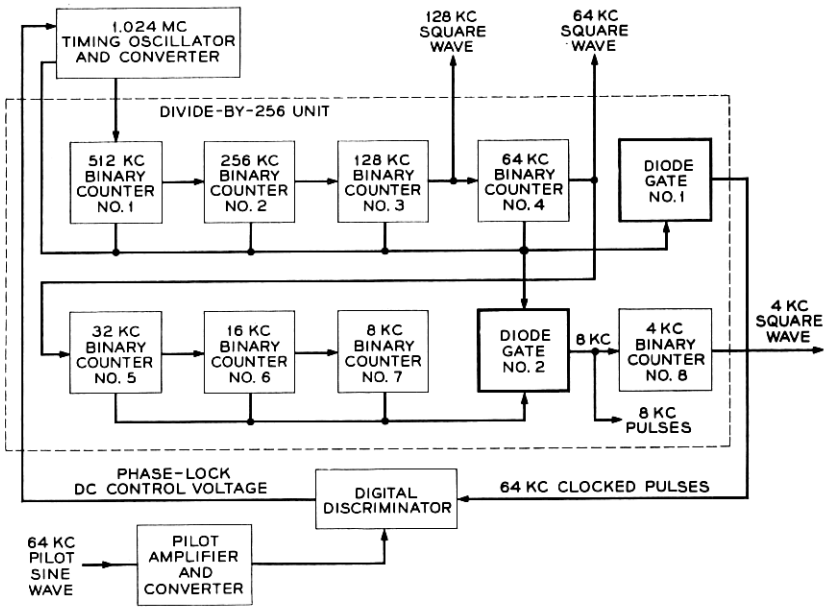

Fig. 6 — Divide-by-256 unit with 64-kc pilot phase-lock connections.

across the varactor diode in the timing oscillator to change the timing frequency for proper phase-lock. Diode gate no. 2 receives gating pulses from the first seven binary counter stages and the clocking pulses from the timing oscillator. The 8-kc clocked pulses generated by diode gate no. 2 are used to drive the eighth binary counter stage and the digital discriminator, when 308-kc pilot phase-lock is required. Driving the eighth binary counter with clocked 8-kc pulses to obtain a 4-kc square wave minimizes the delay variations that may occur through seven binary counter stages.

In those cases where the timing oscillator is to be phase-locked to a 308-kc pilot, it is necessary to use a divide-by-77 unit to generate an 8-kc frequency that can be compared in phase with the 8-kc frequency obtained from the divide-by-256 unit. The method of using the divide-by-77 unit with the timing oscillator, divide-by-256 unit, digital discriminator and 308-kc pilot signal is shown in Fig. 7. The diode gate in the divide-by-77 unit receives gating pulses from seven binary counter stages and a 616-kc clocking pulse generator.

The code for the diode gate to obtain a divide-by-77 is as follows: $64 + 0 + 0 + 8 + 4 + 0 + 1 = 77$. When the 77th pulse enters binary counter number 1, the diode gate detects an "AND" condition and sends a positive pulse to the univibrator. The univibrator immediately (within 0.2 microseconds) initiates the resetting of the seven binary

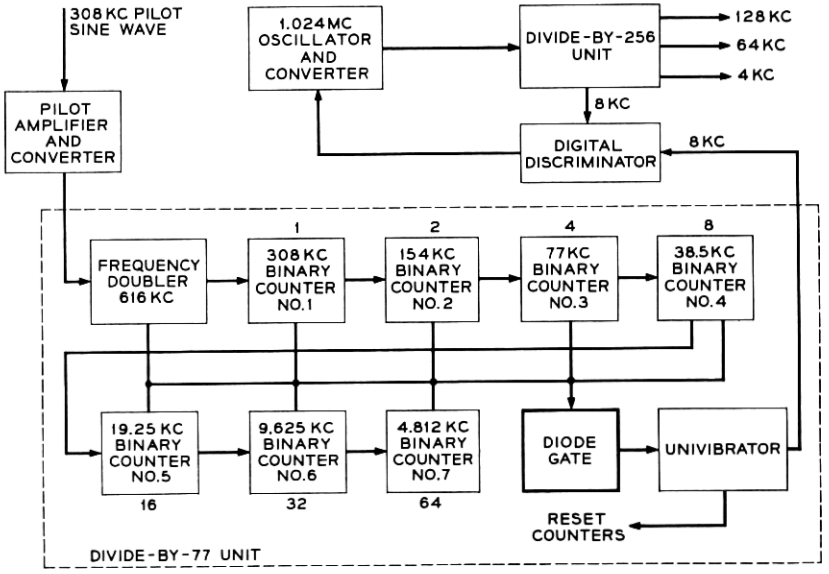

Fig. 7 — Divide-by-77 unit for 308-kc phase-lock.

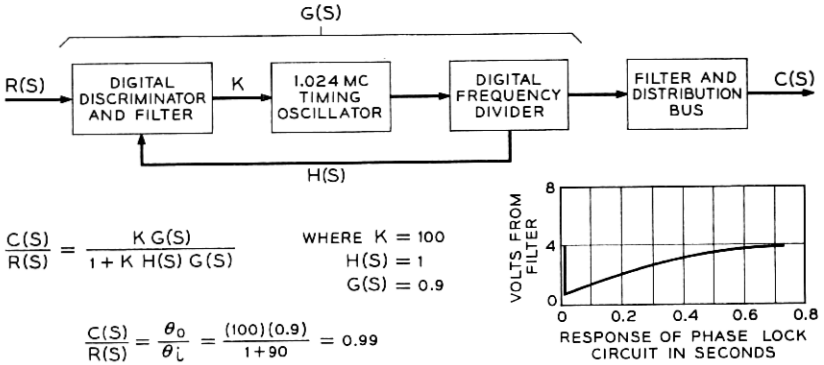

Fig. 8 — Phase-lock control loop.

counter stages to zero. This resetting operation is performed within one microsecond. The 8-kc output from the divide-by-77 unit is used by the digital discriminator to phase-lock the timing oscillator in the same manner described for the 64-kc pilot phase-lock system. Doubling the 308-kc frequency before dividing provides an 8-kc instead of a 4-kc frequency for the digital discriminator, doubling the effective sensitivity.

V. PILOT PHASE-LOCK

The characteristics of the pilot phase-lock circuit are given in conventional automatic control system terms by Fig. 8. The digital discriminator and filter perform the phase error detection and develop an amplified dc voltage proportional to the phase error. This dc voltage is applied across a varactor diode, causing its capacitance to change and, in turn, produce a change of timing oscillator frequency. The maximum rate of oscillator frequency change is 25 cycles per second. A dc voltage change of 0.15 volt across the varactor diode will cause the oscillator to change frequency one cycle per second.

The response of the digital frequency divider is enough faster than that of the crystal controlled oscillator that its characteristic may be omitted from the control circuit analysis. The sensitivity of the digital discriminator has been made as high as possible to eliminate the need for an additional dc amplifier between the filter and timing oscillator. The steady state error is less than 0.15 microsecond for 64-kc pilot operation and less than 1.2 microseconds for 308-kc pilot operation. The corresponding carrier phase error is dependent on the frequency of the carrier. A maximum time of 0.8 second is required for the timing oscilla-

tor to phase-lock with the pilot frequency. If the pilot is interrupted, the discriminator will generate an average dc voltage of 4.0 volts, corresponding to zero phase error and the timing oscillator will generate a frequency very close to its last calibrated free-running frequency.

The circuit of the digital discriminator, filter, and the varactor portion of the timing oscillator is shown in Fig. 9. The digital discriminator is very similar to the binary counter stage described in Fig. 5. An additional "set" circuit for the pilot is provided at the base of Q_2 and a metering relay is connected between the collectors of Q_1 and Q_2. When the symmetry of the square waves at the collectors of Q_1 and Q_2 deviates beyond a prescribed amount, corresponding to an oscillator frequency change of one part in 10^6, the meter relay provides an alarm signal.

The digital discriminator functions in the following manner. Assume the positive going edge of the pilot wave form (see Fig. 9) occurs at t_0; the pulse received from the divide-by-256 counter occurs at t_1, $x_1 = x_2$,

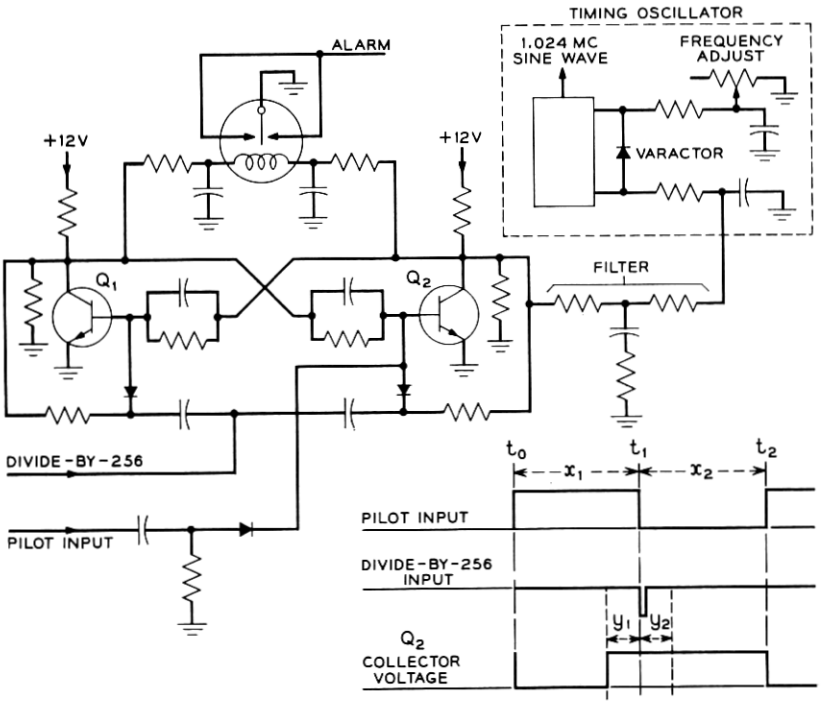

Fig. 9 — Digital discriminator and filter circuits.

and $y_1 = y_2 = 0$. In this condition the output of the discriminator is a symmetrical square wave developing an average of 4.0 volts, the potential used to calibrate the timing oscillator. If the pulse from the divide-by-256 unit arrives early, Q_2 is turned off early, resulting in an output voltage higher than 4 volts. The varactor circuit is arranged so that a higher discriminator voltage results in a lower voltage across the varactor. This lower varactor voltage results in an increased capacitance to the oscillator circuit, causing it to run slower. As it runs slower, the time y_1, approaches zero, and phase-lock is obtained. A similar set of events occurs if the pulse from the divide-by-256 arrives late with y_2 approaching zero.

VI. AUTOMATIC GENERATOR SWITCHING AND ALARM UNITS

Two separate frequency generators, with automatic switching to either, are provided in the primary frequency supply, as shown in Fig. 10. Either generator A or generator B may be selected manually to permit maintenance on the idle generator or selected automatically in case

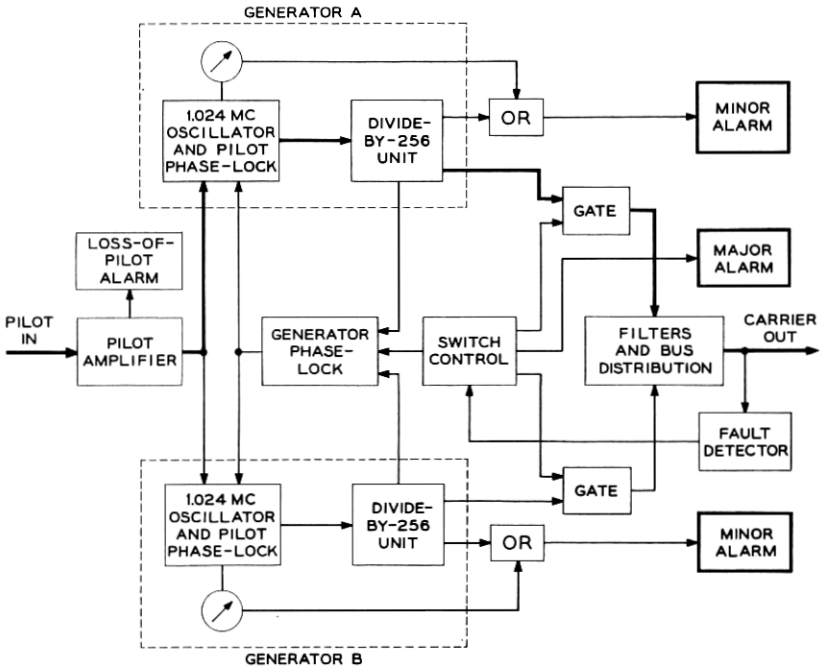

Fig. 10 — Generator switching and alarm units.

the carrier signal disappears at the distribution bus. The heavy lines in Fig. 10 show the signal path through generator A with a similar path available through generator B. Only one pilot amplifier with its own alarm is provided for the two generators, since the timing generator will hold adequate frequency for a short period of time. Two minor alarm circuits are provided with each generator. A meter-relay unit (Sensitrol) is used to monitor the oscillator frequency and a logic circuit is used to detect the operation of the divide-by-256 unit. If a fault is detected by either of these alarm circuits, a minor alarm is initiated but no action is taken by the automatic switching circuit. A fault detector circuit at the distribution bus monitors the presence of the 128-kc, 64-kc, and 4-kc signals. If any of these three signals disappears for longer than one millisecond, the switch control circuit will automatically effect a transfer to the idle generator. If the signals do not reappear at the fault detector within 0.1 second after a transfer, a major alarm is initiated. Transmission "hits" are minimized during manual transfer of generators by operating the two generators phase-locked to each other. A generator phase-lock circuit that detects which generator is in use and phase-locks the idle generator to the active generator is incorporated as part of the logic switching circuits.

VII. OUTPUT CIRCUITS

The outputs of the 4-kc AND gates are connected to a hybrid coil such that either can pass signals to the load and transmission from one side is not effected by either an open or a short circuit steady state condition of the gating transistor on the other side. Thus, 4 kc is supplied to the distribution bus despite failure of one side.

Combining of the 64 and the 128-kc outputs is done in the same way. The square-wave outputs of the combining circuits are reduced to sine waves by filters to insure compatibility with both old and new harmonic generating equipment to which these signals are supplied.

VIII. RELIABILITY

A calculation of the reliability of the primary frequency supply has been made, using failure rate estimates for the various components. Though this calculation is necessarily approximate in the absence of statistical data on the components, it has been useful in striking a balance between the common and redundant sections of the equipment. It also has been influential in determining the allocation of spare plug-in units.

The summation of component failure rate weightings for each section of the equipment results in a "mean time between replacements" for the redundant portion of the supply — oscillator counters and most of the alarm and control circuits — as well as the common equipment. These quantities were 23,000 hours and 250,000 hours, respectively.

Failure of one side of the supply, of course, does not result in interruption of any of the output signals except in the rare case where the other side had failed previously and had not yet been repaired. Thus, in order to combine these statistics and obtain a single statement of the reliability of the supply it is necessary to consider maintenance. Suppose, for example, that spare packages for the unit are available in each office so that only 1 hour is required to repair a defective oscillator. The mean time between coincident failures of the redundant sections is the square of the mean time between replacements ($23{,}000^2$) divided by the repair time or 530×10^6 hours. If spares are stocked in regional centers so that a week is required, a coincident failure would occur once in 3×10^6 hours on the average. Even under these conditions the reliability of the primary frequency supply is controlled by the common equipment and hence is equal to about 230,000 hours or 26 years.

The mean time between coincident failures is materially reduced when longer repair times are assumed. Thus, the plan for providing spares is based on keeping this interval less than a week.

It is of interest to note that had the primary frequency supply been designed without redundant sides the mean time between failures would have been approximately 3 years. Hence, an improvement of nearly 10 to 1 has resulted from the use of redundancy.

IX. EQUIPMENT FEATURES

Reliability has played a key part in the choice of equipment features. It has dictated that (1) certain functional units be plug-in for ease and expedition of replacement and to facilitate repair at maintenance centers, (2) special care be taken to minimize the operating temperature of the components. The number of circuits that had to be accessible as plug-in units made it desirable that a drawer structure be used. The use of a drawer also made it possible to provide thermal decoupling between the power regulators and the remainder of the components; further, it has minimized the chance of inadvertent removal of the plug-in units, since they are not accessible with the drawer in place.

Figs. 11 and 12 show the complete unit. In the area beneath the

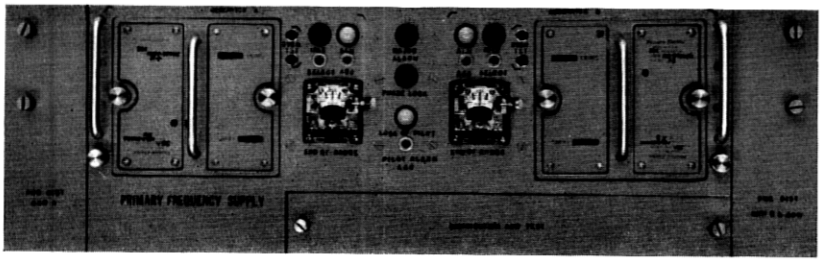

Fig. 11 — Front panel showing alarm and phase indicators and controls.

drawer are a terminal block for external connections and the bus equipment and the jacks. Power regulation units are outside the box. The unit is shown equipped for 308-kc synchronization.

Figs. 13 and 14 show the counter plug-in units. Each three-transistor binary cell occupies a $1\frac{1}{2} \times 5$ inch printed wiring board. Six of these are mounted in the frame of the unit; and soldered interconnections are made at the edges of these to a 4×5 inch board. The associated

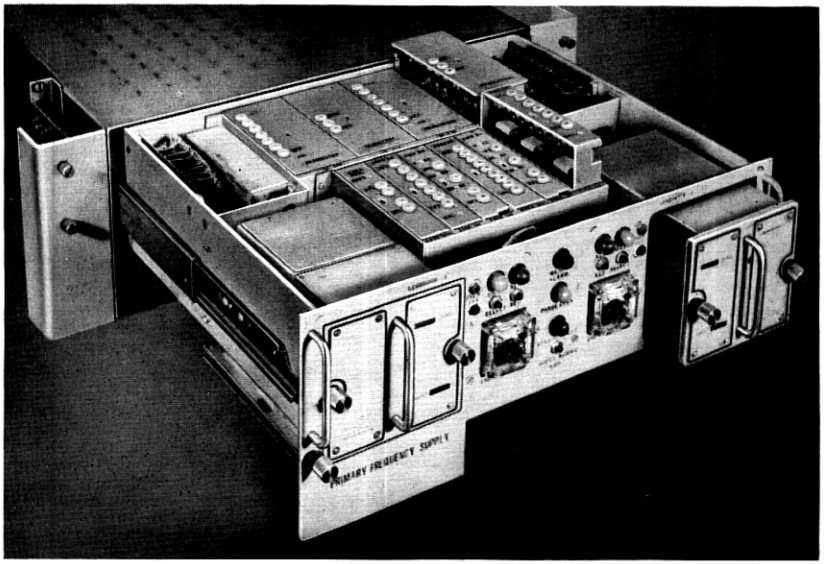

FIG. 12 — Drawer-type construction makes plug-in units accessible but conserves front panel space.

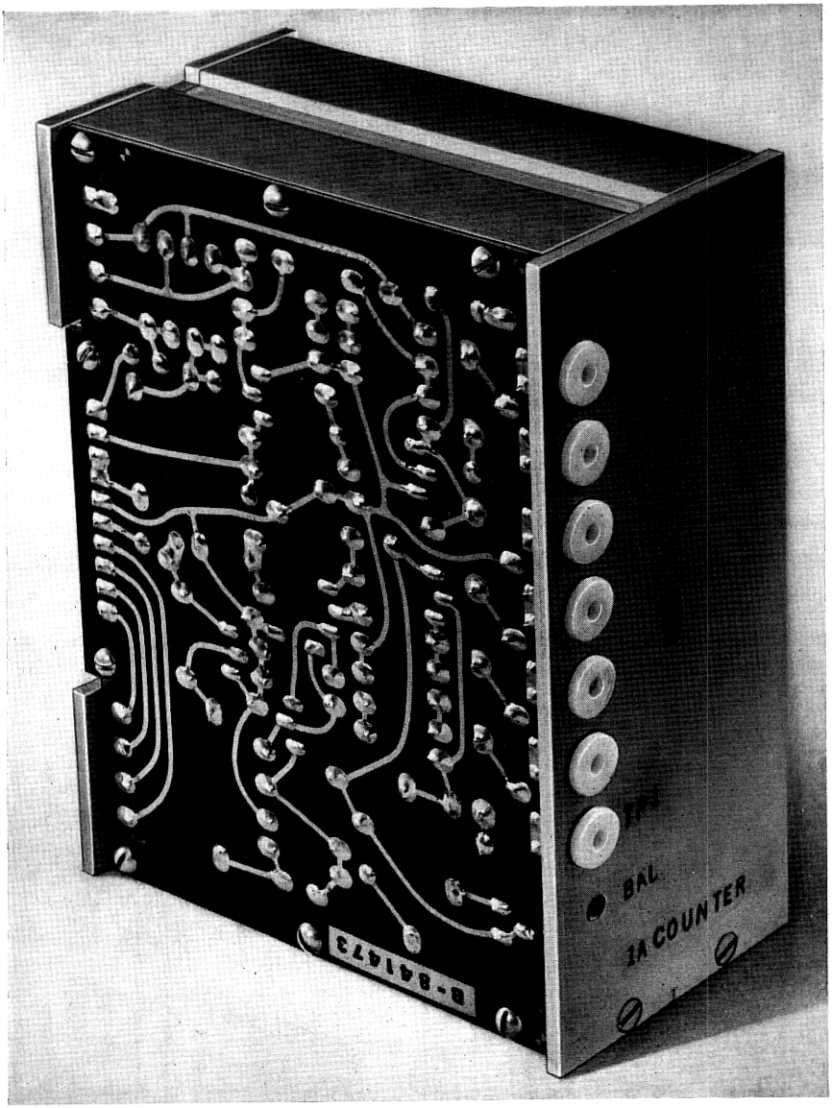

Fig. 13 — Keyway in edge of plug-in unit, location of plug and shape of unit insure proper positioning and orientation.

gate and reset circuits are included on another 4 × 5 inch board. When these eight boards are fastened in the frame no components are visible on the outside of the resulting package.

The various plug-in units are "keyed" so as to prevent their insertion

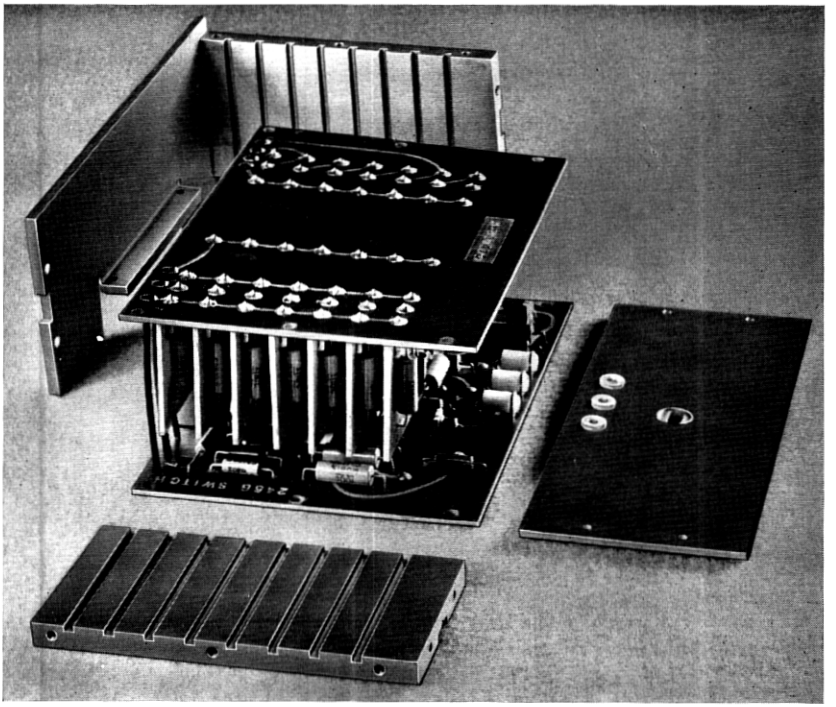

Fig. 14 — Counter units use sandwich-type construction.

in the wrong locations or orientations. Typical units are shown in Figs. 15 and 16.

X. CONCLUSION

Calculations, verified by tests, have indicated that a unit-to-unit delay range equal to 0.08 microsecond when synchronized to 64 kc, and 0.18 microsecond when synchronized to 308 kc, may be expected among accurately adjusted supplies. Any one unit is expected to display a delay variation less than 0.05 microsecond over a 24-hour period, and a gradual change due to crystal aging, not in excess of 0.3 microsecond for 64-kc synchronization or 2 microseconds for 308-kc synchronization. The total phase difference, at 64 kc, between the two sides of a supply is therefore less than 10 degrees.

The maximum frequency error that would result on loss of synchronization is not expected to exceed one part in 10^7. Routine adjustment of the oscillators not more frequently than once per month is expected to guarantee this accuracy.

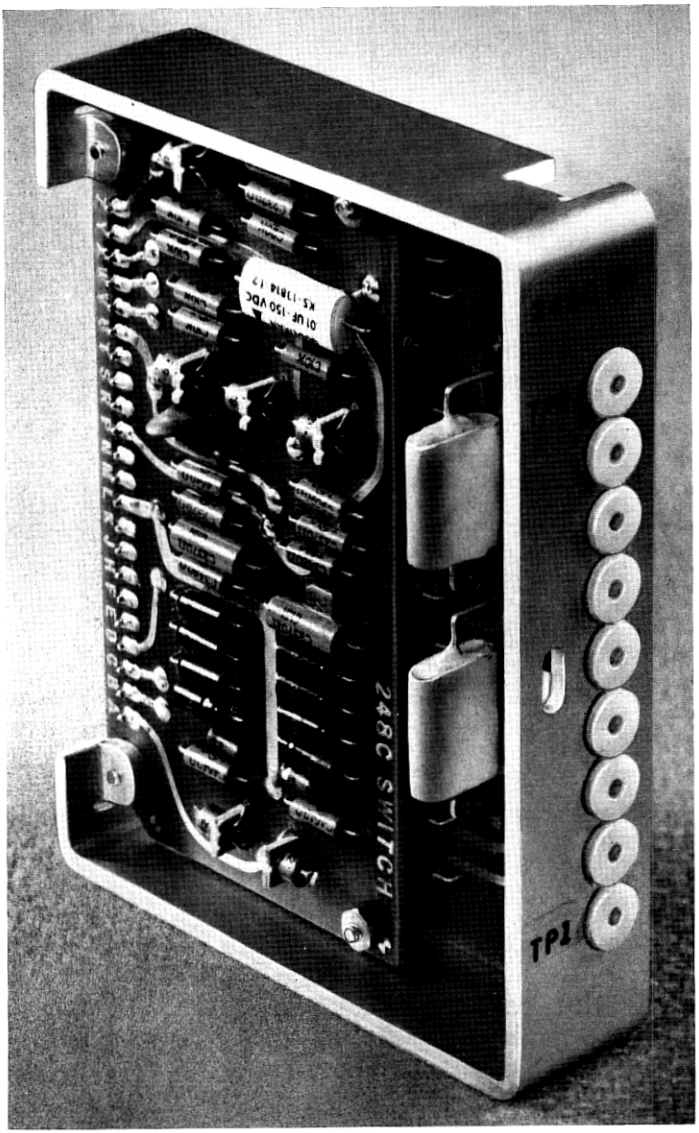

Fig. 15 — This unit contains two printed-wiring boards interconnected at the plug.

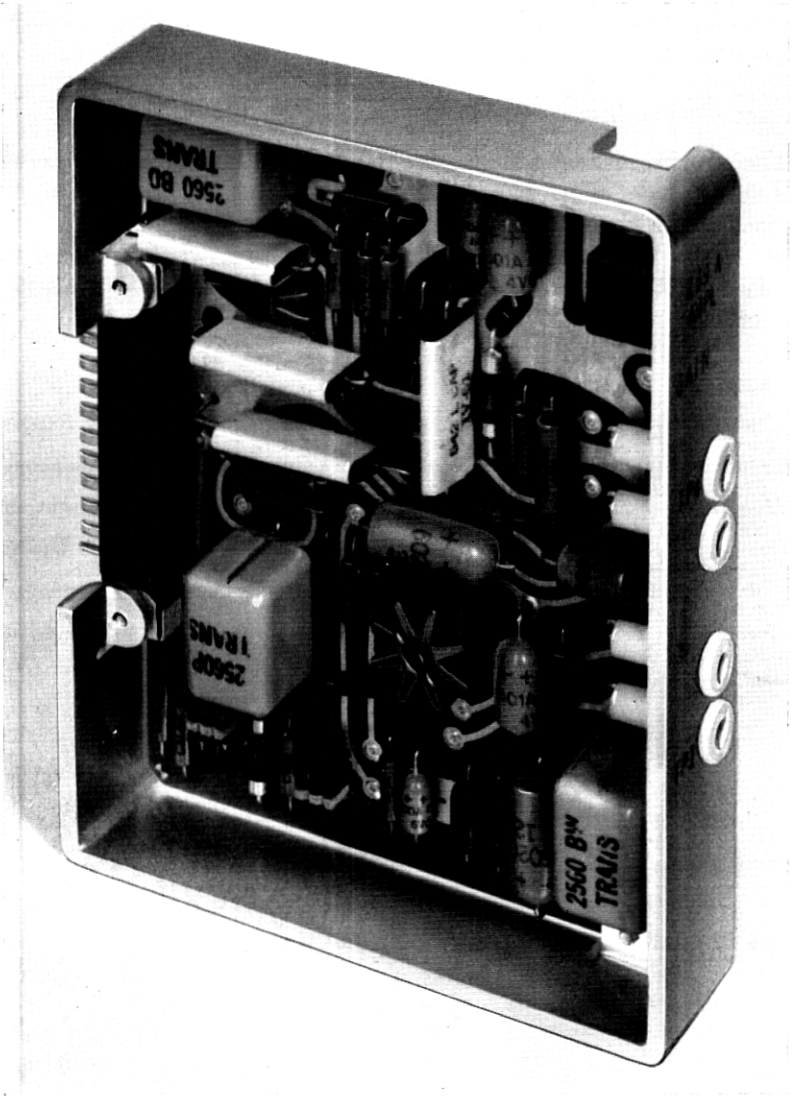

Fig. 16 — Each plug-in unit occupies an individual cell in the drawer. This affords good shielding between units so that individual covers are not required.

In addition to this indicated frequency and phase stability, the requirements outlined in Section II as to compatibility with old and new L multiplex and reliability have been met with margin. An over-all size

reduction of more than 6 to 1, compared with the equivalent units of the old system, was also achieved.

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