Integrated Magnetic Circuits for Synchronous Sequential Logic Machines

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The magnetic switching core is a small, reliable and inexpensive component for digital logic circuits, but conventional core circuits also include a large number of auxiliary semiconductor components. As a result, the cost and reliability of core circuits are not very different from those built entirely with semiconductors. The possibility of building logical systems that use a minimum of nonmagnetic components is examined. Except for the provision of clock-pulse sources, fully integrated magnetic machines are feasible in principle. Suitable circuits must contain provision for gain, memory and unilateral transmission of data. These requirements can be met by taking advantage of the threshold characteristics of ferromagnetic materials that have a rectangular hysteresis loop. Two approaches are selected for consideration. In the first, a binary digit is represented by the remanent state of magnetization of a ferrite core. Upon the application of clock pulses its state can be transferred to adjacent cores by means of electrical interconnections. In the second approach, a binary digit is represented by a discrete flux pattern in a continuous flux conductor. These patterns can be propagated in a step-by-step process through the flux conductor by means of clock pulses. Examples are given of experimental synchronous sequential circuits using commercially available multiapertured cores. The capabilities, limitations and organization of these circuits are discussed.

I. INTRODUCTION

The ferrite memory core has many attractive features as a switching element for digital computer circuits.[1,2,3,4,5,6] It combines a memory function with the circuit equivalent of a switch, and it is small and inexpensive. Furthermore, as a magnetic amplifier it can provide gain. It is also believed to be reliable, the only ambients to which it is susceptible being temperature, external magnetic fields and mechanical stress. In spite of this, its use in logical circuits has been mostly limited to access circuitry for magnetic memories.

295

Why is this? One reason is that the maximum rate at which present-day cores can be cycled is around 1 mc, the limitation being the rise in temperature produced by hysteresis losses. However, this speed is sufficient for many systems, and materials are being continually improved in this respect. A more pertinent reason is to be found in the circuit approaches that have been used. Additional circuit components, and diodes and transistors in particular, are usually included. The result has been that the total count of semiconductor components in some cases — for example, shift registers — is not materially reduced compared to the equivalent all-semiconductor circuits. Thus, the reliability and cost are set mostly by the semiconductor components. In addition, in order to provide a correct impedance match between the magnetic and semiconductor components, it is necessary to use multiturn windings on the cores, and this considerably increases the cost of assembly. Therefore, the more general use of magnetic core logic is dependent upon the design of new circuits that materially reduce or eliminate semiconductor components. This article describes the possibilities that have been examined, and it will be shown that an almost complete integration in terms of magnetic components may be possible. Means rather than applications will be stressed.

Section II is tutorial in nature, and is intended to introduce the reader to the basic tenets of magnetic core circuitry including the terminology and models used, and also to the requirements of a fully integrated circuit. In Section III the requirements of combinational and sequential logic machines are discussed, and possible approaches to the design of a magnetic machine are introduced. An approach based upon the use of multiapertured cores is described in detail in Section IV, and experimental data are presented. Section V describes approaches based upon the step-by-step propagation of flux patterns through a continuous flux conductor; there is little experimental information available in this case. Finally, the state of the art is summarized in Section VI. A full treatment of this nature may help elucidate the possibilities and limitations of this particular approach to an integrated computer technology. It is hoped that dividing the article into sections in the manner described will simplify the selection of points of interest.

II. GENERAL PROPERTIES OF CORE CIRCUITS

For completeness, an account will be given of the properties of memory cores and the requirements of an integrated circuit.

We shall be concerned with ferromagnetic materials that have the rectangular hysteresis characteristic shown in Fig. 1.[7,8] Note the sharp threshold for switching from an upper to a lower state of magnetization,
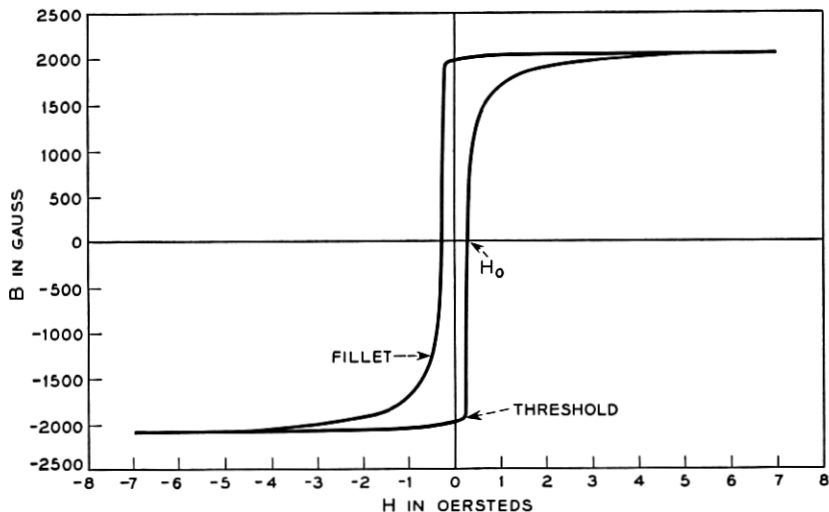
Fig. 1 — $B–H$ characteristic of a typical fast switching memory core ferrite.

or vice versa. An objectionable feature is the fillet, which is found in all of the ferrite materials and to a lesser degree in the permalloys, since it means that the switching threshold must be exceeded by an appreciable factor if a complete reversal is to be obtained. Sometimes it is perfectly satisfactory to operate on a minor loop, in which case the fillet is not troublesome, but for many of the circuits to be considered it would be better if the fillet were eliminated. It is to be hoped that materials will be developed to accomplish this.

In the majority of cases to be considered, lines of magnetic flux can be completed entirely within the material, and the effect of air leakage can be neglected. This means that the magnetic field H, in oersteds, produced by an applied drive NI, in e.m.u., is given approximately by the expression $H \cong 4\pi NI/L$, where L, in centimeters, is the mean peripheral length of the core, irrespective of the manner in which the winding is placed on the core. This approximation may be invalid in cases where portions of the magnetic path are saturated. If a constant-current drive is used to reverse the flux, the rate of change of flux as a function of time, $d\varphi/dt$, has the form shown in Fig. 2. The switching time, τ, is normally defined as the separation between the 10 per cent points of the $\dot{\varphi}$ versus t waveform, and is approximately inversely proportional to the applied switching field, as is shown in Fig. 3.[8] The resultant total flux reversal,

$$\int_{\tau} \dot{\varphi} dt,$$
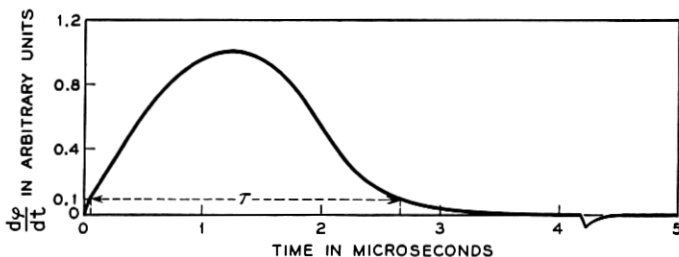
Fig. 2 — $d\varphi/dt$ as a function of time.

varies with drive in the manner shown in Fig. 4. At large drives the total flux reversal approaches a constant value Φ. The gradual rise to this value can be attributed to the fillet.

It is customary when analyzing core circuits to make the following approximations:[2] (a) $d\varphi/dt$ is constant during switching; (b) $\tau(H - H_0)$ = constant = s_w ; (c) the material has an ideal rectangular loop. In other words, it is assumed that it is possible to replace the waveform of Fig. 2 by one that is rectangular with the same enclosed area and time duration τ; that of Fig. 3 by a straight line having the same mean slope and axis crossing; and that of Fig. 4 by a step function having the same mean amplitude Φ and axis crossing H_0 . These assumptions lead to the useful approximation for large drives

$$\frac{d\varphi}{dt} \cong \frac{\Phi}{\tau} \cong \frac{\Phi(H - H_0)}{s_w} \cong \frac{4\pi\Phi}{s_w L} (NI - I_0),$$
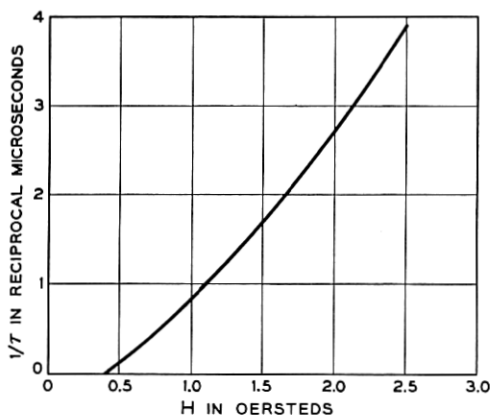

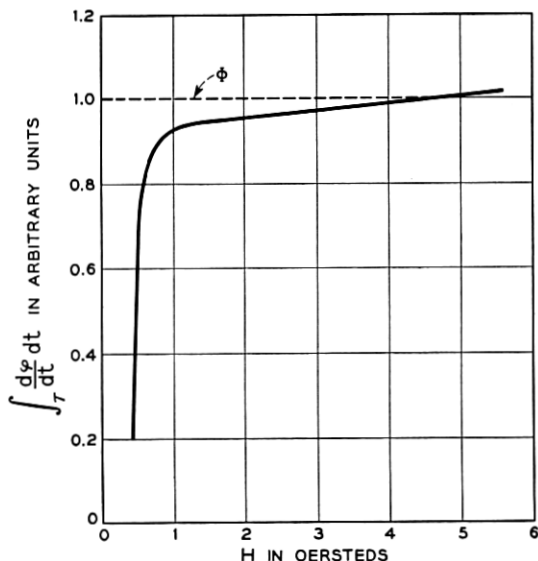Fig. 3 — Reciprocal switching time as a function of applied field.

Fig. 4 — Total flux reversal as a function of applied field.

where NI is the resultant constant-current drive and I_0 is the threshold current for switching using a single-turn winding. Units are in e.m.u. Typical values for existing ferrites are $s_w = 0.7 \times 10^{-6}$ oersted-second* and $\Phi = 4 \times 10^3 \times A$ gauss-cm², where A is the minimum cross section of the core. The model is a crude one, but it has been found to give quantitative values useful for designing circuits that use either simple toroidal cores or multiapertured cores.

It is customary to describe magnetic circuits schematically by means of mirror symbols.[2] Toroidal cores are represented by heavy vertical lines, which may be regarded as end view projections. Winding leads are represented by horizontal lines and the winding turns coupled to the cores are indicated by short diagonal line segments ("mirrors") at the intersections. A simple example is given in Fig. 5. The sense of the field produced in the core is obtained by "reflecting" the applied current at the corresponding mirror surface. Thus, in Fig. 5, I will set the first core downwards. The sense of the voltages produced in coupled windings by a flux change are obtained by reversing the applied field and "reflecting" it at each mirror surface. Thus, in Fig. 5 as the core is set

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* Switching time may also be defined as the time interval between 10 per cent Φ and 90 per cent Φ points. For this definition, $s_w \cong 0.2 \times 10^{-6}$ oersted-second. The relevance of either definition will vary with the application.
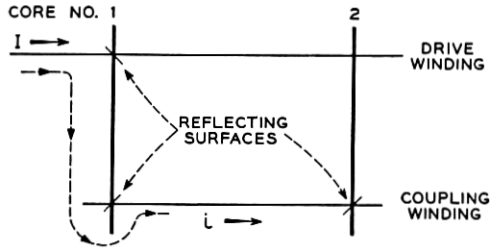
Fig. 5 — Example of the mirror representation of a core circuit.

downwards an emf is induced in the upper winding from right to left, that is, in a direction to oppose I. It will also induce an emf in the lower winding from left to right, that is, in a direction to produce a current i in the winding coupling the first and second cores. The current i is in a direction to set the second core upwards.

The wiring complexity of a core circuit can often be reduced, and its efficiency increased, by using more complicated magnetic structures in place of the simple toroidal cores.[9,10,11,12,13] In order to follow the operation of these structures, it is only necessary to keep in mind two facts. First, flux continuity must be preserved. Second, when an mmf exceeding threshold is applied, a flux reversal will first take place in the switching path presenting the lowest reluctance in preference to the remaining paths.[10] With few exceptions, the lowest reluctance path is the shortest path having flux available for the reversal.

Most multiapertured cores can be reduced to one of two types, or to a combination of the two. Representative of the first is the laddic structure,[10] which has the property that all important flux paths are flux-limited to the same extent. Representative of the second type is the transfluxor,[9] which has the flux capacity of one path equal to the sum of the flux capacities of the remaining paths. In a sense, the laddic can be considered as consisting of a number of toroidal cores interconnected in series by magnetic linkages, while in the transfluxor the toroidal cores are interconnected in parallel. The magnetic linkages make possible a transfer of flux from one core to another without the use of a coupling winding. The latter, because of added resistive losses, reduces the efficiency of circuits.

A modified mirror symbol representation will be used to describe circuits made with multiapertured cores. The procedure is illustrated in Fig. 6 for a two-hole transfluxor. Each leg of the core shown in Fig. 6(a) is represented by a heavy vertical line in Fig. 6(b), the notation at the bottom giving the flux capacity set by the minimum cross section

of the corresponding leg. The horizontal striated lines are included simply to draw attention to the fact that the legs are connected magnetically, so that a flux reversal in one must be balanced by an opposite reversal in one or both of the other two in order to maintain flux continuity. The preferred flux return will be through the closest available path. Apart from these last restrictions, each vertical may be treated as a separate core. As an example, assume that leg 1 is initially set up, legs 2 and 3 down. Application of a current I to the winding shown will drive flux downwards in leg 1, and maintain downwards saturation in leg 3. The result will be that one flux unit (Φ) will be reversed in leg 1 and returned through leg 2, which will be left set in the upwards direc-
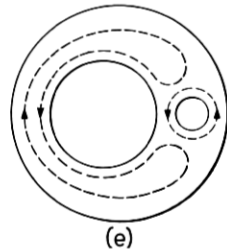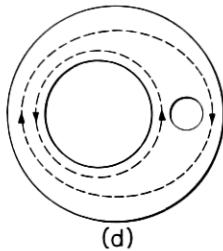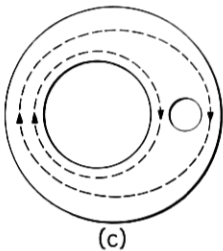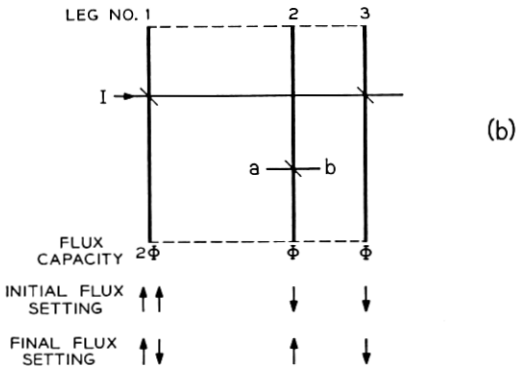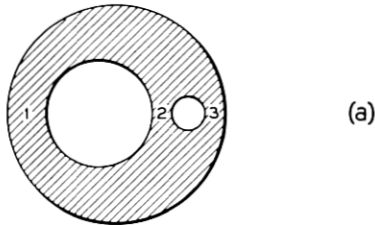
Fig. 6 — Transfluxor, its mirror-symbol equivalent, and flux patterns.

tion. Applying the normal mirror circuit procedure, it will be seen that the result of setting flux up in leg 2 will be to induce an emf in the winding ab in a direction to drive current from terminal a through the winding to terminal b. This notation simplifies the explanation of the more complicated circuits.

It is often helpful in describing the operation of these structures to represent the state of magnetization graphically by means of closed flux patterns. As an example, three of the possible states of magnetization of the transfluxor are shown in Figs. 6(c), (d) and (e). In this case, each of the flux arrows represents the saturation remanent flux capacity of each of the smaller legs. Thus, in Fig. 6(c) all legs are fully saturated; whereas in Figs. 6(d) and (e) legs 2 and 3 only are saturated, leg 1 having zero resultant magnetization—which, it should be remarked, is not arrived at by a sinuosidal demagnetization, but by a partial reversal from a saturated state. A further subdivision of the flux patterns may be introduced if necessary, provided that the condition of flux continuity is maintained. It should be kept in mind that such flux patterns are merely a convenient fiction, and that the actual domain structure will be considerably more complicated. Nevertheless, the model is helpful and adequate for most purposes. It is usually sufficient to represent the state of magnetization of the individual legs by upwards or downwards pointing arrows, each representing one unit of flux, as in Fig. 6(b).

Frequently, a multiapertured core can be replaced by an equivalent toroidal core circuit.[13] For example, the transfluxor shown in Fig. 6 can be replaced by the circuit shown in Fig. 7. The three magnetically linked legs of the transfluxor are replaced by three electrically coupled toroidal cores having appropriate flux capacities and thresholds. If the coupling
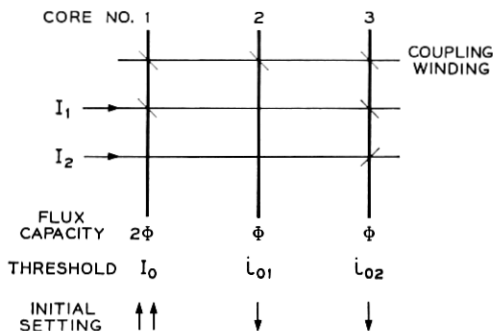

Fig. 7 — Equivalent core circuit of a two-hole transfluxor; $I_0 > i_{02} > i_{01}$, in order to allow for the difference in switching path lengths between the corresponding legs of the transfluxor.

winding has zero resistance, then flux may be transferred from core 1 to core 2 by I_1, and then from core 2 to core 3 by a current-limited drive I_2, as between the corresponding legs of the transfluxor. In general, however, the operation of the multiapertured core equivalent is simpler to explain. It is also inherently more efficient, because one part of the advance sequence is carried out by a flux transfer within the core itself, so that for this flux transfer there is no power dissipated in coupling windings. Furthermore, the use of multiapertured cores reduces the cost of assembly, since the cost of putting in coupling windings appears to be the most important single factor.

It is possible to obtain a flux gain between stages of a core circuit by using an adequate turns ratio in the coupling winding. In order to illustrate this point, consider the circuit shown in Fig. 8(a). Two cores are coupled by a closed winding of resistance R having n turns on core 1, but only one turn on core 2. Let core 1 be initially set up and core 2 set down by I_1. Now apply I_2 to reverse the flux in core 1. Simultaneously a current i will be induced in the coupling winding in a direction to reverse the flux in core 2. The distributed inductance and capacitance of the winding can be neglected in a practical instance. Thus, considering instantaneous electromotive forces in the coupling winding,

$$iR = n\frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt},$$

where the subscripts 1 and 2 denote core 1 and core 2, respectively. Accordingly,

$$\int_0^t d\varphi_2 = n\int_0^t d\varphi_1 - \int_0^t iR\,dt.$$

Clearly, when $R \to 0$ the flux change produced in core 2, if its flux
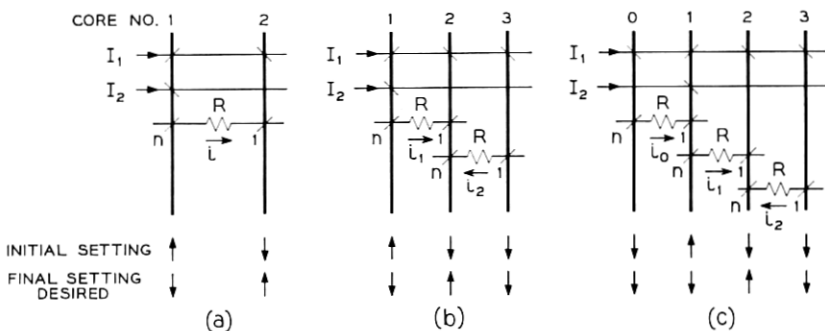

Fig. 8 — Core circuits to demonstrate the capability for gain and the need for decoupling.

capacity is sufficient, will be n times larger than that produced in core 1, and, for a finite value of R, it may be made at least equally large by a suitable choice of n.

However, the provision of a turns ratio is not in itself always sufficient for providing gain. To illustrate this point, consider the circuit shown in Fig. 8(b). Cores 1 and 2 are coupled together as previously, but in this case core 2 is also coupled to a following core by a similar winding. Core 1 is initially set up and cores 2 and 3 set down by I_1. Core 1 is now driven down by I_2 in order to transfer its setting to core 2, as previously. However, in this case, the resultant mmf acting on core 2 is reduced, because an opposing current i_2 is induced in the winding coupling core 2 to core 3. Considering instantaneous electromotive forces in the coupling windings:

$$i_1 R = n \frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt},$$

$$i_2 R = n \frac{d\varphi_2}{dt}.$$

Note that there is no $\dot{\varphi}_3$ term, because there is no flux reversal in core 3. Furthermore, according to the approximate model for the core circuit described previously,

$$\frac{d\varphi_2}{dt} \cong \frac{\Phi}{\tau_2} \cong \frac{4\pi\Phi}{s_w L} \left(i_1 - n i_2 - I_0 \right).$$

Therefore, introducing the values of i_1 and i_2 in terms of $\dot{\varphi}_1$ and $\dot{\varphi}_2$,

$$\frac{d\varphi_2}{dt} = \frac{n \dfrac{d\varphi_1}{dt} - I_0 R}{1 + n^2 + \dfrac{s_w L R}{4\pi\Phi}}.$$

It follows that, for $R > 0$, the maximum rate of switching of core 2 is less than one-half that of core 1. Thus, it is impossible to transfer even one-half of the flux setting of core 1 to core 2 for any value of n. Therefore, some method of decoupling forward coupling windings during the advance phase is necessary in addition to a turns ratio if flux gain is to be obtained.

An additional reason for including a decoupling feature is the need for preventing adverse backwards propagation of a flux setting. This situation can be explained by reference to Fig. 8(c), which again shows a series of interconnected cores. In this case flux is initially set up in core 1 and down in the remainder by I_1. During the advance phase

the flux in core 1 is to be driven downwards by I_2, in order to advance its initial setting to core 2, as previously. However, in this case a current i_0 is also induced in the back winding coupling core 1 to core 0. This current is in a direction to set flux upwards in core 1, and therefore there must also be provision for preventing this.

In conventional core circuitry the necessary decoupling is achieved by including a diode or transistor in the coupling windings. It is its function that must be replaced by magnetic components in a fully integrated circuit.

The question of decoupling and gain has been dealt with at some length because its understanding is crucial to the design of integrated magnetic circuitry. The need for gain to compensate for circuit losses and to permit fanout is obvious, but the failure to recognize the need for decoupling is a common pitfall. The analysis presented here is based upon a relatively crude model of a core circuit, and the behavior of an actual circuit may be somewhat worse or possibly better, depending upon the actual properties of the cores. It may be better if the core has a re-entrant hysteresis characteristic of the kind found in some of the permalloys.[14] In these materials once the static threshold (H_0) is exceeded and switching commenced, the threshold for continued switching decreases as shown in Fig. 9. This can result in an additional flux gain relative to that calculated from a model based upon the ideal rectangular characteristic. However, this possibility has not been studied extensively and so will not be considered further.

III. REQUIREMENTS OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

Simple logic machines, which must generate a unique Boolean function of a set of input variables that are coincident in time, are best constructed with combinational circuits for fastest performance. For these systems the situation is fairly satisfactory. For example, any switching function can be generated by a single laddic or a combination of other magnetic components. Semiconductor components may be required in the input and output circuits in many cases, but the total count relative to completely semiconductor circuits is small for complicated switching functions.

More complicated machines, particularly general-purpose machines, must be constructed with sequential circuits. The logical inputs in this case are presented sequentially in time, and the outputs obtained at any particular time are used to provide the inputs during the next phase of the sequence. In other words, the state of magnetization of a magnetic circuit set during a first phase must be capable of determining the setting
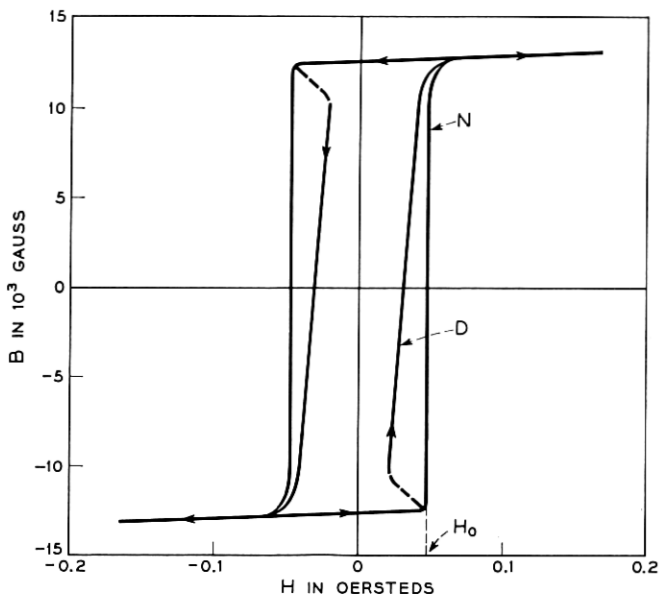
Fig. 9 — Example of a re-entrant hysteresis loop found in stressed 69-permal-loy. In order to initiate a flux reversal a field exceeding the static threshold, value H_0, must be applied. However, once switching has commenced it can continue under an applied field less than H_0. The normal loop (N) is measured in the conventional way. The dynamic loop (D) is obtained by first applying a field exceeding H_0 to initiate switching and then immediately reducing it.

of another during a second phase. There must, therefore, be provision for storage, gain and unidirectional transfer of a sequence of bits. The remainder of this paper will be mainly concerned with this kind of organization.

There are two basic approaches possible. The first, which is considered in Section V, is more in the nature of a true magnetic circuit concept in that it involves the step-by-step propagation of discrete flux patterns through a continuous magnetic structure. It is the more elegant approach because the bit information may be kept in magnetic form throughout an entire sequence of logical operations, being translated to electrical form only at the input and output terminals.

The second approach is more conventional; separate cores are used for each combinatorial phase of the operation and are interconnected by coupling windings. The core itself provides the required storage function, and, as discussed in Section II, a flux gain between stages can be obtained by means of a suitable turns ratio in the coupling windings,

provided that there is also provision for decoupling at the appropriate times and for preventing backwards propagation of the bit information. As mentioned previously, in conventional core circuits the decoupling is obtained by including a diode or transistor to block undesired currents. It is the function of these diodes that must be reproduced. It should be noted that only the nonlinear resistance property of the diode is important. Other nonlinear components could be used, but the present discussion will be limited to consideration of the use of the nonlinear property of the cores themselves. The fact that a current drive must exceed a certain amplitude before it can produce a flux reversal means that the core can be considered to have a current sensitive switch in series with its input. The function of the diode could be replaced by such a switch. All circuits proposed so far using both simple toroidal cores and multiapertured cores make use of this feature.[15,16,17] As mentioned in Section II, multiapertured core circuits have definite advantages. For this reason circuits using simple toroidal cores will not be considered. Rather, in Section IV the discussion will be limited to a consideration of a multiapertured core circuit that fulfills the basic requirements. Because a certain amount of flux steering can be accomplished within the multiapertured cores, their use actually represents a compromise between the two approaches.

For small systems it is possible to perform a limited amount of sequential logic using laddics and related devices as the circuit elements. These possibilities have been described previously.[10] It should also be noted that parametron and ferroresonant magnetic core circuits also fulfill the stated requirements.[18,19] Complete logical systems based upon the former have been reported. However, they do not enter naturally into the present discussion, which is concerned primarily with the use of cores exclusively. It should only be remarked that they appear to share similar speed–power limitations.

IV. CORE CIRCUITS

The problem of organization of a synchronous sequential machine is a complex one. For the present class of circuits, the most profitable starting point is to use a shift register having associated combinational components. As noted previously, all the operations for combinational logic at a given stage of the advance sequence can be performed on a single core, which might, for example, take the form of a laddic with a transfluxor output. This paper will mostly be concerned with the design of the shift register.

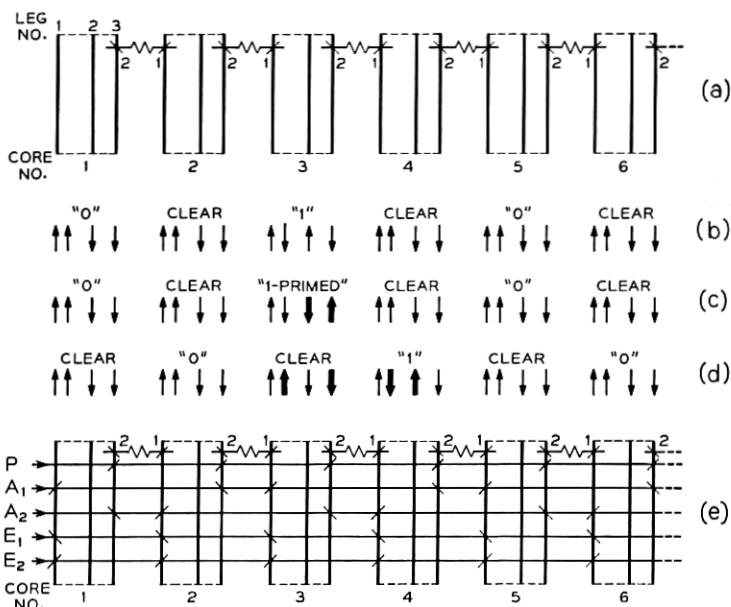The circuits to be described in this section are based upon the trans-

Fig. 10 — (a) Skeleton shift register circuit; (b) initial flux setting; (c) primed flux setting; (d) advanced flux setting; (e) complete circuit.

fluxor structure shown in Fig. 6. The framework of the shift register is shown in Fig. 10(a). Leg 3 of each core is coupled by a closed winding to leg 1 of the following one. The resistance shown in Fig. 10(a) is the resistance of the winding itself, normally a few tenths of one ohm. A turns ratio is used to give the flux gain necessary to make up for transfer losses.* In practice, it is convenient to make $n = 2$. The flux setting of each leg will be represented by arrows in Figs. 10(b), (c) and (d), each arrow representing one unit of flux (Φ).

Alternate cores are used as information cores at each stage in the advance sequence; the remainder are in a "cleared" state. In other words, at one stage in the sequence the bit information will be stored in the odd-numbered cores, at the next stage it will be advanced into the adjacent even-numbered cores, etc. As an example, in Fig. 10(b) the odd-numbered cores 1 and 5 are shown set in the "zero" state, core 3 being set

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* It should be possible to use a unity turns ratio in the coupling loop by taking advantage of the flux gain mechanism produced by a re-entrant B–H characteristic as mentioned in Section II. However, the materials property necessary is somewhat critical, and as a result the alternative complication of a turns ratio is preferred at present. Furthermore, the flux gain is then sufficiently large that the allowable tolerances are improved.

in the "one" state. The corresponding flux patterns are shown in Fig. 6(c) and Fig. 6(d) respectively. These two states correspond to the "blocked" and "unblocked" states of a transfluxor.[9] The "clear" state also corresponds to the "blocked" condition. Observe that it has been possible to change the flux pattern to insert a one into core 3 without producing a flux change in leg 3, which would induce an emf in the winding coupling core 3 to core 4. Therefore, it was possible to effect a full flux transfer from core 2 to core 3 without including the diode, which was required in the conventional toroidal-core circuit discussed in connection with Fig. 8(b).

The bit information may be transferred from the odd-numbered cores to the following even-numbered cores, leaving the former in the "clear" state, as follows:

The information cores are first "primed" by applying a drive to leg 3 of every core in a direction to switch flux upwards. This is the P (prime) drive shown in the complete circuit, Fig. 10(e). It is limited in current amplitude so that although it can switch flux between legs 2 and 3, that is, around the small hole of the transfluxor, it cannot produce a flux reversal around the longer path including legs 3 and 1. The P drive will not affect the zero or "clear" cores. However, in a core which contains a one it will set leg 3 up and leg 2 down. In other words, the flux pattern is changed from that shown in Fig. 6(d) to that shown in Fig. 6(e). As leg 3 is being set up, a current will be induced in the winding coupling cores 3 and 4. However, the direction of this current is such that it does not change the flux setting of core 4. The final setting of all cores following the P phase is shown in Fig. 10(c). Note that it was at this point that advantage was taken of the threshold characteristic of the core, in this case to prevent the improper conversion of a zero into a one. The closest corresponding situation in the conventional toroidal-core circuit was the adverse backwards propagation of a one.

Observe that the current that was induced in the winding coupling cores 3 and 4 was limited only by the winding resistance. This current acted in opposition to the applied drive, and therefore reduced the mmf acting on leg 3. It follows that leg 3 switched quite slowly during this phase, and that a full reversal will have taken place only if the P current was applied for a sufficient length of time. It is not necessary for the successful operation of this circuit to produce a complete reversal, because attenuation of flux by an incomplete reversal can be compensated for by the gain provided by the turns ratio of the coupling loop. However, the flux reversed must exceed a certain minimum, and so there is a corresponding minimum time for bit propagation.

The information cores are now to be "cleared" and the bits advanced. To do this, a drive is applied to the A_1 (advance) winding shown in Fig. 10(e). Cores 1 and 5 are already "blocked", so that there is no change in their flux patterns nor in those of the coupled cores 2 and 6. On the other hand, core 3 is driven from the "one-primed" to the "clear" state. This flux reversal induces a current in the coupling winding between cores 3 and 4 in a direction to reverse flux in leg 1 of core 4. The A_1 drive prevents a flux reversal in leg 3 of either core 4 or core 2. Therefore, the sum result is to set leg 2 of core 4 in the upwards direction to give the flux pattern shown in Fig. 10(d). The bit information has now been advanced into the even-numbered cores. Subsequently, the latter can be primed (by P), and then cleared (by A_2) to advance the bits one further stage back into the odd-numbered cores. In this manner by applying the sequence of drives P, A_1, P, A_2, the bits may be propagated from left to right through the register.

This circuit may be analyzed by means of the approximations described in Section II. In the Appendix, it is shown that the resistance, R, of the coupling winding has a maximum permissible value because of the requirement that there be a flux gain of at least unity between stages. The minimum switching time, τ_p, possible for a P phase is obtained by making the winding resistance equal to this maximum value. For a large ratio of the diameter of the large hole to that of the small hole $(\tau_p)_{\min}$ is approximately proportional to s_w/H_0. Since s_w cannot be reduced appreciably below existing practical levels, it is necessary to increase H_0 in order to decrease τ_p. Therefore, higher switching speeds can be obtained only at the expense of a corresponding increase in drive power.

It is not necessary for the resistance of the coupling winding to be exactly equal to the maximum value in order to obtain the maximum speed for the P phase, since, as noted previously, a partial flux reversal is permissible. Therefore, the time duration of the P phase may be set by the width of the drive pulse rather than by the actual switching time, permitting considerable latitude for the choice of the resistance of the winding. If speed is unimportant, there is no lower limit for R, since, given sufficient time, a flux reversal during the P phase can always be completed irrespective of the resistance of the coupling winding.

The switching time during an A phase is limited only by the amplitude of the current drive practicable. Therefore, the speed of the circuit is limited primarily by the P phase, and the cycle time required to advance a bit one stage is approximately equal to $2\tau_p$. Measured values of the minimum value of τ_p for three commercial multiapertured cores are

given in Table I. It will be seen that the 3665 core is capable of a bit handling capacity, $\frac{1}{2}(\tau_p + \tau_A)^{-1}$, of the order of 5×10^4 per second. By improving the design of the core as discussed, it should be practical to increase this figure by perhaps an order of magnitude, but a further increase in speed will probably depend upon the development of improved materials, since the drive requirements become excessive.

The peak power requirement occurs during the A phases, when a flux reversal must be produced around the large hole of each core containing a one. At the same time, current must be supplied to make up for that taken by the coupling windings. The total drive current required using single turn windings is approximately $I_t n^2/(n - 1)$, where I_t is the current required to produce a flux reversal around the large hole of an

TABLE I — MINIMUM SWITCHING TIMES AND OPERATING CURRENTS FOR SHIFT REGISTERS USING THREE COMMERCIAL CORES

Core number	E_1, ampere-turns	E_2, ampere-turns	$P_1 = P_2 = P$ (max.), ampere-turns	$P_1 = P_2 = P$ (min.), ampere-turns	$A_1 = A_2$, ampere-turns	$(\tau_p)_{min}$, micro-seconds
RCA XF-3665	0	0	0.56	0.46	9	8
	0.5	0	0.56	0.46	4	
RCA XF-3668	0	0	0.39	0.27	5	30
General Ceramic F-1023-S6	0	0	0.14	0.12	2.4	
	0	0	0.15	0.10	3	38
	0.1	0	0.14	0.12	1.2	
	0	0.1	0.21	0.12	3	

unloaded core in time t. Thus, for $n = 2$, the advance current is $4I_t$. The peak back emf developed in a single turn for each bit is approximately equal to Φ/t. Therefore, the peak power requirement is equal to $4I_t \times \Phi/t$, or approximately $s_w \Phi L/\pi t^2$. In a typical situation, this peak power is approximately 0.4 watt/bit for $t \sim 1$ microsecond. The average power needed is less by a factor t/T, where T is the total cycle time for advancing a bit. The power required for the P phase is less, since switching takes place at a slower rate. The average power dissipation in watts/bit is approximately 10^{-6} times the bit rate for the commercial cores. It is interesting to note that almost exactly the same figure has been reported for parametron and ferroresonant shift register circuits.[18,19]

The A drive current has wide margins. It is only necessary that it be sufficient to clear the cores within a few microseconds. On the other hand, the magnitude of the P drive currents must be kept within fairly

well defined boundaries, as shown by Fig. 11. Curve A shows how the total flux switched around the small hole of an "unblocked" core varies with the applied drive, and curve B shows the same relation for switching around the large hole of the core when "blocked." The P drive must lie within the boundaries delineated by the hatched region. If it exceeds the right-hand boundary it will produce unwanted switching in a core containing a zero, so that zeroes may gradually be converted into ones. On the other hand, if it falls below the left-hand boundary insufficient flux will be switched in a core containing a one, so that the one will become attenuated even though there is provision for a small flux gain between stages. The boundaries shown in Fig. 11 are the measured values obtained from experimental re-entrant registers. They can be considerably improved by suitable design of the geometry of the core.

Additional drive windings can be incorporated to increase margins, to increase speed and to reduce the drive current amplitudes. For ex-
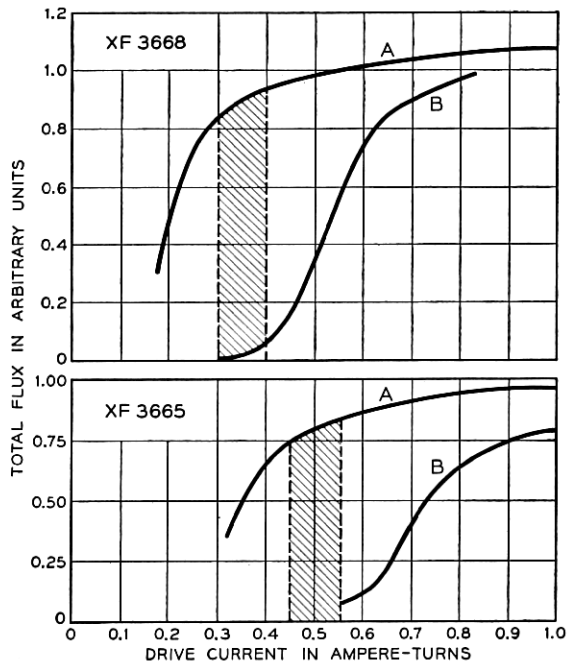

Fig. 11 — Threshold characteristics for two commercial cores: curve A indicates total flux switched between leg 3 and leg 2 versus the drive current applied to leg 3 of an initially "unblocked" transfluxor; curve B indicates total flux switched between leg 3 and leg 1 versus the drive current applied to leg 3 of an initially "blocked" transfluxor.

ample, in Fig. 10(e) an additional winding, E_1, is shown. It may be used during each A phase to bias cores, which are receiving bit information, up to the threshold needed to switch flux between legs 1 and 2. It therefore reduces the current required in a coupling winding to switch a one into a core and, therefore, the magnitude of the A drive necessary to complete switching in a prescribed time. A second winding, E_2, can be used during the P phase. It provides an mmf around the large hole that acts counter to the P drive, making possible an increase in the upper limit of the P drive and the corresponding maximum bit rate. Other windings of this nature can be incorporated. However, all such windings can at best only increase the speed by a factor of two. These additional windings can normally be driven in series with the corresponding major drive windings, so that additional current sources are unnecessary. In this connection also, the P drive can conveniently be supplied by a dc source, so that only two pulse sources are necessary, one for A_1 and another for A_2. Thus, in a sense, only a two-phase drive circuit is needed, but there must be adequate spacing between A_1 and A_2 pulses to allow for the slow priming operation, due to the use of a dc source for the P current.

The circuit can be modified in various ways to reduce the peak current amplitudes required. As an example, consider the circuit shown in Fig. 12(a). It uses a core that has small holes between legs 1 and 2 and between legs 3 and 4, and a large hole between legs 2 and 3. Each leg in this case has a flux capacity, Φ, of one unit. The additional small hole makes it possible to clear the information cores in the back direction during the P phases, thereby eliminating the additional current that
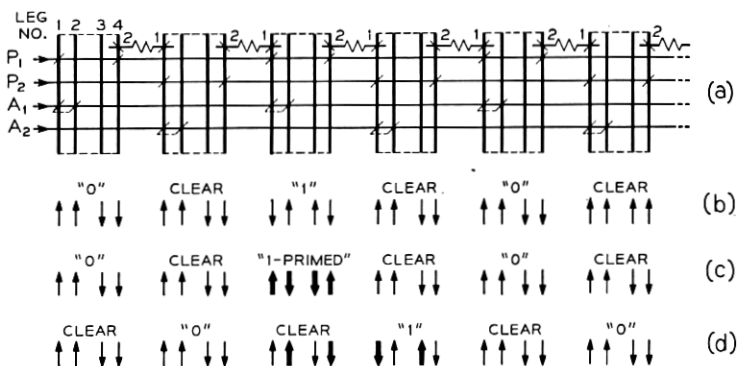

Fig. 12 — (a) Modified circuit; (b) initial flux setting; (c) primed flux setting; (d) advanced flux setting.

the A drive must provide in the circuit of Fig. 10(e) to compensate for that dissipated in the coupling loop in the back direction. The operation of this circuit can be followed by studying the sequence of flux patterns shown in Figs. 12(b), (c) and (d). The cycling pattern in this case is P_1, A_1, P_2, A_2, P_1, $\cdots$. A dc source can again be used for both P_1 and P_2.

Experimental shift registers have been built based on both the circuits of Figs. (10(e) and 12(a) using each of the cores listed in Table I. They have been operated in re-entrant circuits, i.e., with the output of the final core in the chain coupled directly to the input of the first without intermediate amplification. Fig. 13(a) shows the output that was obtained from one of the cores in a re-entrant three-bit chain using XF3665 cores in the circuit of Fig. 10(e) when a one, zero, zero was be-
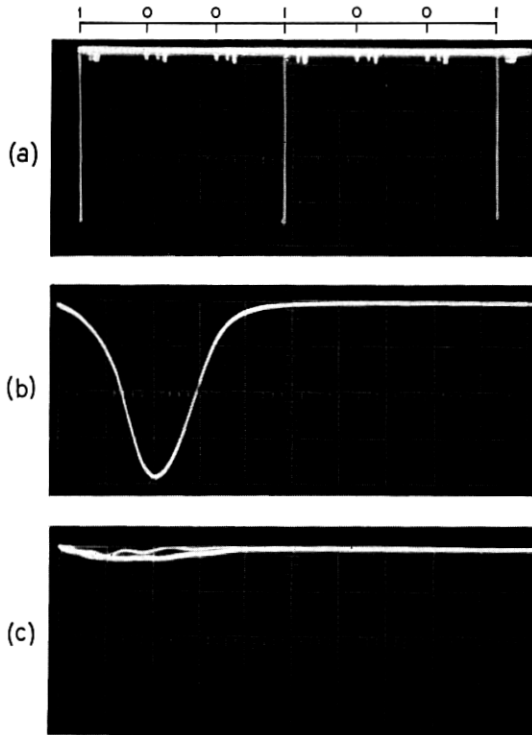

(a)

(b)

(c)

Fig. 13 — (a) Waveforms appearing across the output of one transfluxor in a re-entrant register circulating a 1, 0, 0 pattern. Vertical calibration = 0.15 volt/turn/division; horizontal calibration = 500 μs/division. (b) Output waveform for a one. Vertical calibration = 0.15 volt/turn/division; horizontal calibration = 0.1 μs/division. (c) Output waveform for a zero. The maximum noise signal is also shown superimposed. The calibration is the same as that for (b).

ing continuously circulated. Figs. 13(b) and (c) show the corresponding waveforms for a one and a zero on an expanded time base. The operating currents are shown in Table I. The values given for $A_1(=A_2)$ are the minimum values needed for reliable operation using the corresponding minimum values for $P_1(=P_2)$.

The ampere-turns required to drive these circuits are large, but not beyond the capabilities of transistors. For example, the 2N417 and the 2N580 can be used to give pulses between 1 and 2 amperes in amplitude. In addition, components such as the General Electric controlled-rectifier C35F can provide pulses up to 150 amperes peak amplitude. They have been used as switches to discharge pulse-forming network drivers. Relay contacts have also been used. The waveform of the drive pulses is not critical. A rise time of 0.5 microsecond is adequate.

It should also be remarked that it is a simple matter to introduce multiturn drive windings in order to reduce the current for a given ampere-turn drive. The cores can be mounted in such a manner that each turn consists of a single wire threaded straight through an in-line assembly of alternate cores. Multiple turns can then be obtained by interconnecting the individual wires of a multiconductor cable at the ends of the register. A photograph of an experimental 10-bit register module is shown in Fig. 14. The cores were assembled and wired upon the two jig rods shown in (a), and then pushed together for close packing. The circuit was then mounted on a printed circuit card and potted, as shown in (b). It was unnecessary to preselect the XF3665 and F-1023-S6 cores used in re-entrant registers, except to reject those that were obviously mechanically damaged. However, this was not the case for the XF3668 cores. Registers up to 800 bits (1600 cores) capacity have been operated.[20]

The register can be interrogated nondestructively at each stage of the shift, since the flux patterns for a one and a zero correspond to those of a transfluxor in the "unblocked" and "blocked" states. Thus, each core can be interrogated nondestructively in the normal manner.[9] It is convenient to use an additional small hole in the structure for this purpose. Fig. 15 shows the waveforms obtained upon nondestructively interrogating two register cores containing a one and a zero respectively.

Because of the gain feature, fanout is practical. In other words, one or more inputs may be driven in parallel by each output. Each fanout will reduce the maximum bit rate, because each added coupling winding will increase the total counter mmf produced during a P phase by the induced currents. If there are N fanouts, the switching speed during a P phase is reduced by a factor a little less than N. The A drive on the core must also be increased by a corresponding factor in order to
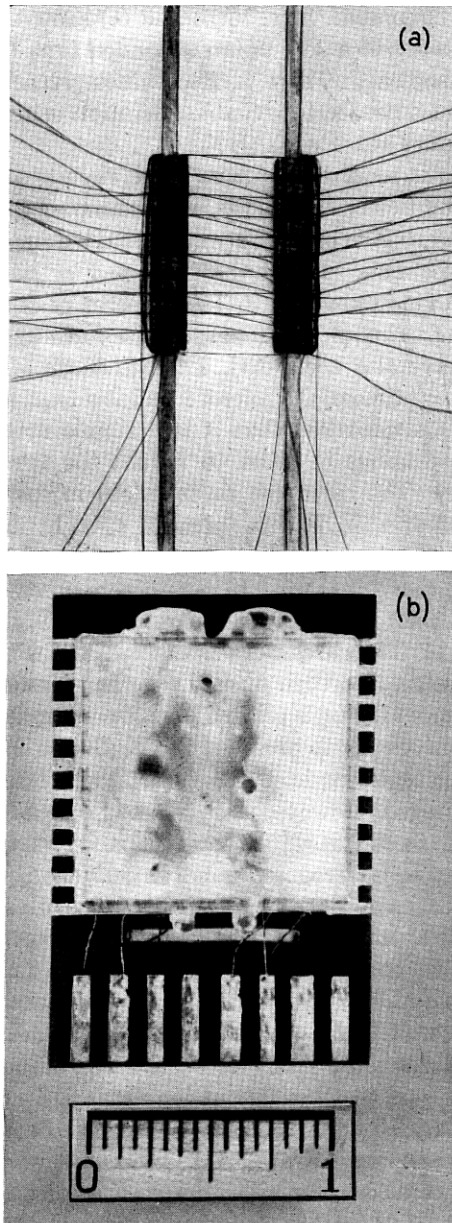
Fig. 14 — (a) Ten-bit shift register cores assembled on jig. There are ten parallel inputs on the left-hand side, and ten parallel outputs on the right-hand side. The clock windings run parallel to the jig rods. (b) Register mounted on printed circuit card and potted.
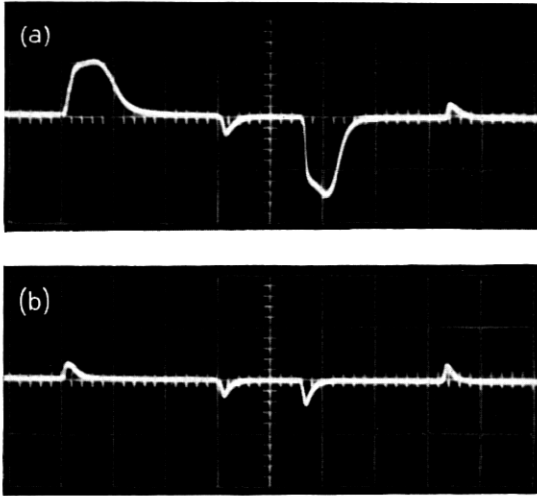
Fig. 15 — (a) Output waveform obtained by nondestructive interrogation of a core containing a one. (b) Output waveform obtained when the core contained a zero. Vertical calibration = 0.1 volt per division; horizontal calibration = 2 μs per division.

compensate for the increased total of coupling currents loading the core. Experimentally, a fanout of three has been demonstrated.

As an example of the use of fanout and the incorporation of an additional simple combinational operation, consider the circuit shown schematically in Fig. 16, and in its entirety in Fig. 17.[21] Outputs x and y are inserted into an exclusive-OR circuit. The output of the latter provides the input for the register. It can easily be shown that this circuit will successively generate all combinations of four bits except four zeroes. For if the register initially contains 1000, during the next advance the exclusive-OR circuit will insert a zero into the input of the register, which will now contain a 0100; subsequent advances will give 0010, 1001, etc., for a total of 15 terms before the initial setting is repeated.
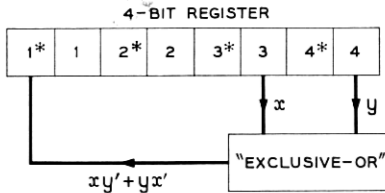

Fig. 16 — Example of a synchronous sequential machine that can be constructed entirely with multiapertured cores.
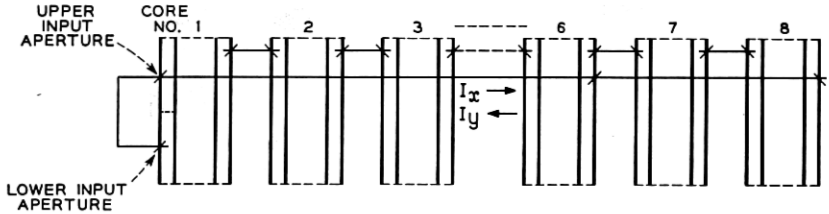
Fig. 17 — Complete circuit for the machine shown in Fig. 16. The P and A drive windings are omitted for clarification, since they are exactly the same as those shown in Fig. 12, with the exception of core 6, which must have a doubled A_1 drive winding because of the fanout at that point.

The three-hole core circuit of Fig. 12(a) was used for the register. The exclusive-OR function was derived by connecting the outputs from the third and fourth bit position of the register, cores 6 and 8 respectively, in series opposition to drive the input core, core 1, as illustrated in Fig. 17. Core 1 has an additional small input aperture, obtained, as indicated in the mirror circuit representation, by segmenting the first aperture with a magnetic interconnection. When I_x alone is present, a one is inserted into core 1 by means of a flux reversal around the path including leg 3 and the lower input section of leg 1. When I_y alone is present, the reversal path includes leg 3 and the upper input section of leg 1. When both I_x and I_y are present, or both are absent, the resultant drive is zero, and there is no switching in core 1, i.e., a zero is inserted. The output from a single core in this circuit shows the repetitive pattern of 15 settings as the bit patterns circulate, Fig. 18.

In summary, it appears that, with sufficient ingenuity, core circuits can be designed that should satisfy the stated objectives. This can be done at the expense of a considerable reduction in the maximum system speed possible compared to a core-diode system using the same cores,
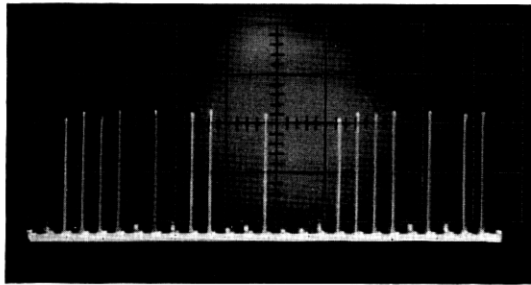

Fig. 18 — Output obtained from an experimental model showing the repetitive pattern of fifteen bits that was generated, i.e., 001111010110010.

but for many applications in the telephone system speed is not a primary requirement. For elementary systems, the operating conditions have been shown to be reasonably practical and can be improved by designing the device with this application in mind.

As mentioned previously, two other circuits based upon the transfluxor have been described in the literature,[16,17] and there are a number of variations possible. Their operation differs in detail, but an analysis shows that their performances with respect to drive requirements and speed are generally similar. A detailed analysis giving the design parameters of these circuits is presented in the Appendix.

The idea of performing logic by a step-by-step transfer of a flux pattern through a continuous magnetic structure is an appealing one for the reasons given previously. Known methods of this kind, unfortunately are especially reliant upon the threshold characteristics of the materials, and all advance drives must be amplitude-limited. Furthermore, there is no provision for gain. However, the techniques are of interest and there are some potentially useful applications, so that a detailed consideration is justified.

Two complementary approaches will be considered. The first makes use of the threshold characteristics of multiapertured structures,[6,13] while the second adds the influence of the depolarizing fields produced when the structure is open, i.e., when the flux pattern is closed by airflux outside the structure.[22,23,24] A third possibility is based upon the use of flux summation structures. However, the latter can usually be reduced to toroidal core circuits, which have been described in the literature[6,25,26] and do not appear to fulfill all the requirements for a synchronous sequential machine. Therefore, this approach will not be considered.

An elementary example illustrating the propagation of flux in a multiapertured structure is shown in Fig. 19. A laddic structure is used, its feature being that the flux capacities of the rungs, and preferably that of the side-rails also, are all equal. To begin with, the flux pattern shown in Fig. 19(a) is established. The flux around alternate windows is magnetized in an anticlockwise sense to the left of rung 5, and in a clockwise sense to the right. Rung 5 is left in a neutral state of magnetization. A first advance pulse, A_1, is now applied. It produces an mmf in a direction to drive flux downwards in rungs 3, 5, 9, 11, 15, 17, $\cdots$, as shown in Fig. 19(b). Of these, only rung 5 has flux available for a reversal. There are two possible return paths for this reversal: to the left of rung 5 through rung 1, or to the right of rung 5 through rung 7. The first
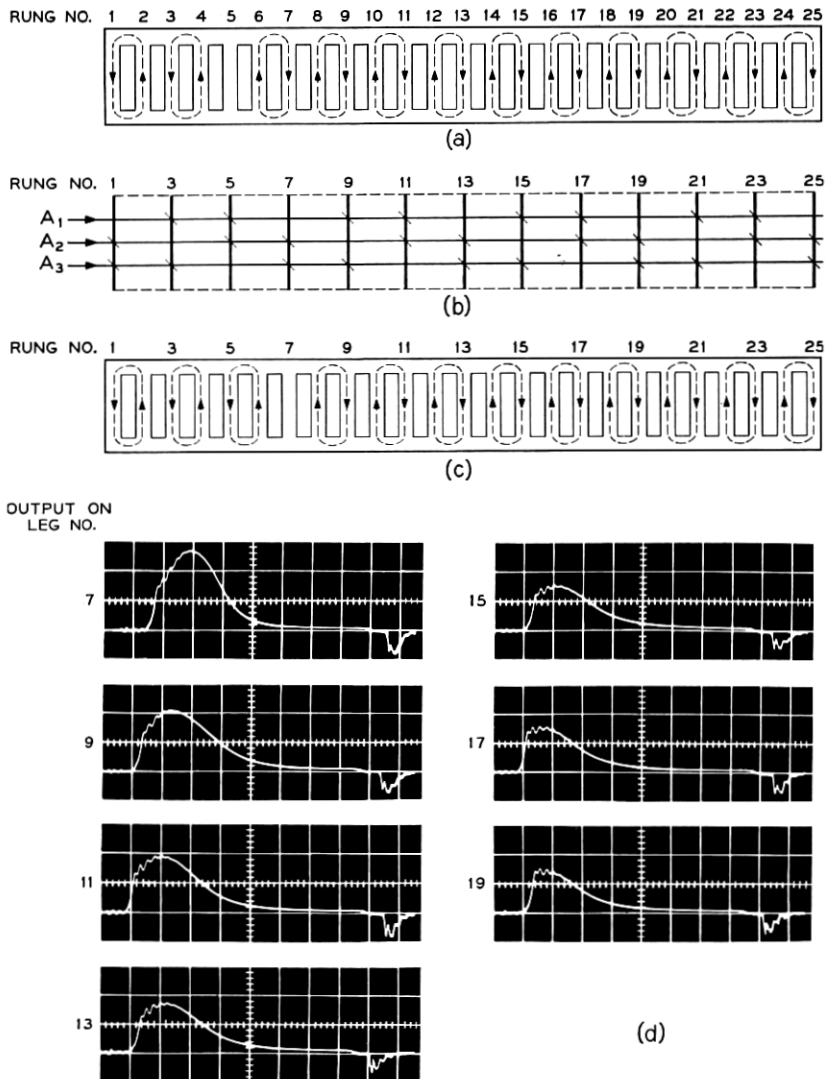
Fig. 19 — (a) Initial flux pattern in laddic stepping switch; (b) circuit diagram; (c) flux pattern following one advance step; (d) successive outputs obtained from an experimental structure as the bit pattern was propagated through successive odd-numbered rungs.

path is almost twice as long as the second. Therefore, if the A_1 current is limited, so that it is below the threshold required for switching between rungs 5 and 1, only the reversal between rungs 5 and 7 can take place. Thus, following the A_1 drive the flux pattern becomes that shown in Fig. 19(c). It will be seen that the initial flux pattern has been displaced two rungs to the right to rung 7. Similarly, the flux pattern will be displaced an additional two rungs to the right following each of the successive drives A_2, A_3, A_1, $\cdots$. In this manner, the bit information represented by the neutral magnetization of a rung can be propagated step-by-step from left to right. By adding a fourth phase, it is possible to use the same structure as a self-clearing shift register.

Many alternative arrangements are possible, making use of modified advance windings or structure, or both. However, they are all subject to the same limitations, depending very much on the threshold characteristics of the materials, and require amplitude limited drives throughout. As a result at each step, a little flux may be transferred beyond the required point, (or left behind), because of an inferior threshold characteristic. In addition, any departure from the correct geometry — e.g., an overlarge rung — will also result in a deterioration of the flux transfer. These effects are cumulative, so that the result is a continuous attenuation of the flux pattern. For example, in an experimental model the flux transferred to the correct rung was reduced by approximately 7 per cent at each step. As an example, the successive outputs obtained as the bit pattern was propagated through the successive odd-numbered rungs, 7, 9, 11, 13, 15, 17 and 19 respectively, are shown in Fig. 19(d).

The second method is best introduced by considering the example of a magnetic tape, which has an easy direction of magnetization parallel to its long axis. Let it be fully magnetized in this direction, say from right to left. Now let a field be applied in a direction to reverse the magnetization in a small segment, ab, as illustrated in Fig. 20; for example, by means of a small solenoid. In this case, flux closures must be completed by air-flux (not shown). Under these conditions, the segment ab is subjected to demagnetizing fields, which increase as the length ab is decreased, and, in fact, if ab is too small the reversed setting will be unstable once the applied field is removed. In consequence, it will be possible to produce a stable zone of reversed magnetization only if ab exceeds a critical length, which is dependent upon the thickness, width and magnetic properties of the tape.

Once a stable reversed segment is produced, it can be extended if a pulsed current is applied to an adjacent solenoid that is less than the critical length. This solenoid would not be capable of establishing a
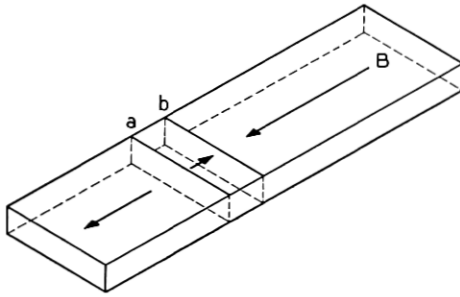
Fig. 20 — A reversed segment in a magnetic tape.

permanent reversal in the absence of an adjacent reversed segment, but it can do so if the latter is present, because the demagnetizing field is reduced. Therefore, it is possible to propagate a bit, which, in this case, is represented by the presence or absence of a reversed segment bounded by a 180° butt domain wall, in a similar manner to that used for propagating the bit pattern in the laddic. The corresponding circuit is shown in Fig. 21, which uses mirror symbols to show the sense of the windings, A_1, A_2 and A_3. Each winding acts upon every third segment, e.g., ab, de, etc., and each segment is less than the critical length but greater than one-half of it. Assume that the tape is initially magnetized from left to right on the left of a, and in the opposite direction on the right. Now apply the A_1 drive. It acts to reverse magnetization in every third segment — ab, de, etc. — but, because each is less than critical in length and alternate segments are spaced by more than one critical length, it will succeed in producing a permanent reversal in ab only, thereby advancing the wall from a to b, as discussed. Similarly, as the successive drives A_2, A_3, A_1, $\cdots$ are applied, the wall is advanced step-by-step from left to right.
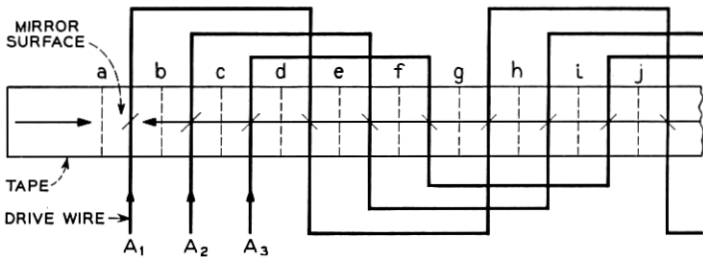

Fig. 21 — Circuit diagram of a magnetic strip stepping switch.

As for the laddic structure, the threshold characteristics of the material must be well defined, and the drives must be amplitude-limited, since the effective length of each segment of the reversal field depends upon both the current amplitude and the length of the solenoid. Both the laddic and tape devices operate in a similar fashion, and synchronous sequential circuits using either can be designed. However, the latter are simpler to describe and also appear to be the more promising from a practical viewpoint. Therefore, they will be used as the basis for further discussion.

The function of the circuit shown in Fig. 21 is that of a stepping switch or counter, since an emf will be induced in turn in output windings placed at intervals along the structure. This must be reset every time the butt wall reaches the terminal output winding. The uses of such a device are limited, but, by a slight modification of the advancing circuits, it is possible to restore the magnetization of the strip to its reset direction to the rear of the reversed segment as the latter is being propagated. In this case, it becomes possible to propagate a series of reversed segments simultaneously, and the device can be used as a shift register.[22,23] A minimum of four advance phases is necessary.

This circuit could be used as the basic building block of a synchronous sequential machine, as discussed for the core circuits. However, if the register must provide parallel outputs for the electrical input to a similar device, the transferring drive current should not be limited to the same extent as are the advance currents. In other words, the transfer drive should be capable of supplying the additional ampere turns required in the output winding, in addition to the drive required for the operation of the unloaded register. This requirement can best be met by designing the circuit so that the output winding is coupled to the tail end of the bit segment at the appropriate clock time. The output emf is then produced by the drive, which serves the primary purpose of restoring the magnetization of the end section of the bit segment to the reset direction, thus clearing the tape to the rear. This drive need not have the same amplitude limitation that was imposed upon the advance currents.

A shift register circuit, which uses electrically interconnected short tapes in much the same way as cores were used in Fig. 10, is illustrated in Fig. 22. A stable reversed segment, ab, representing a one in the first tape can be advanced into the adjacent segment, bc, which is smaller than the critical length, without modifying the setting of the adjacent tape, which is in the "cleared" or zero state. This comprises the priming operation. The first strip is then reset to the "clear" state (by an unlimited amplitude drive), thereby inducing a current in the coupling

winding in a direction to set a one into the following tape in its *ab* segment. Reverse propagation can be inhibited as before. The interesting feature of this circuit as compared to the core circuit is that the magnetic structure is threaded through the windings, rather than vice versa. This could simplify the assembly advantageously.

It will be clear that the strip register meets the requirements of a basic building block for a synchronous sequential machine. Fanout can be achieved by electrical interconnections between tapes, as in the transfluxor circuits. However, in this case an interesting and reasonably practical possibility is to obtain a fanout by an actual physical branching. In practice, this can be achieved by replacing the single tape with a number of separate flux conductors, which are driven in common up to the branch point but individually beyond there, where necessary. Fan-in can be similarly obtained. The total number of branches is limited, since each fanout will reduce the magnitude of the flux quantity representing a bit. However, this is not a serious limitation.

In principle at least, it should be possible to make quite extensive synchronous sequential machines by these techniques. Thin magnetic film or wire technologies appear particularly suitable for their fabrication. Unfortunately, experimental work in this field has been very limited, so that the actual capabilities are unknown. However, there has been sufficient experimentation to demonstrate the feasibility of these proposals.[22,23] The critical length of a stable reversed segment is of the order of one millimeter in nickel-iron films and wire. The actual range and uniformity of the critical length for different materials have not been studied extensively, but an examination of the shape of a reversed segment suggests that there is going to be a practical minimum limit. To
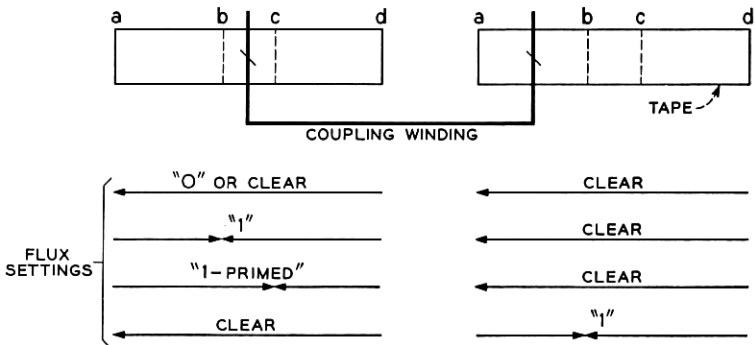

Fig. 22 — A magnetic strip shift register circuit that is analogous to the core circuit of Fig. 10.
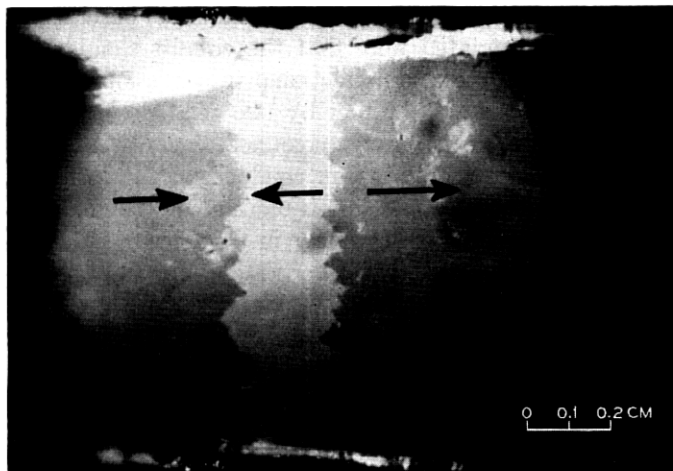
Fig. 23 — Photograph of a 180° butt wall domain.

illustrate this point, a photograph of the structure of a reversed segment in a thin nickel-iron film is shown in Fig. 23. The photograph was taken through a polarizing microscope, which delineated the region of reversed magnetization by the different rotation of the plane of polarization that it produced. It will be seen that the domain wall is very irregular, varying in position by approximately 0.25 mm. The critical length must, of course, be much larger than this irregularity, or its threshold will be poorly defined.

The question of speed is an interesting one. The limiting speed of an unloaded continuous-tape shift register is set by the time required for an unstable reversed segment to revert to normal magnetization when an advancing field is removed. This time will decrease as the length of the segment is decreased, so that the greatest speed is obtained by making each segment equal to its minimum value, which is one-half of the critical length for the four-phase shift register. The reversal time can be decreased by using a material having a higher threshold field, all other parameters being kept unchanged, but at the same time the drive current must be increased. Thus, in this case also, increased speed can only be obtained at the expense of an increased drive.

VI. DISCUSSION

An attempt has been made to coordinate the known ways to exploit the properties of rectangular loop magnetic materials in order to build

synchronous sequential machines using a minimum of other components. The requirements stipulated were that the circuits should have a capacity for gain, memory and unidirectional transmission of data. These requirements were shown to be met by two related systems, the first using an assembly of electrically interconnected cores, and the second using an assembly of continuous-flux conductors; the latter must use electrical interconnections where gain is required, and a modicum of flux steering can reduce winding complexity in the former. Of the two, the first is immediately practical, at least for simple subsystems such as shift registers, and commercially available devices are suitable if system requirements are not excessive. In principle, neither system is limited in speed, but increased speed can be obtained only at the expense of an increase in drive power. It cannot be proved, but it appears at the present time that this limitation applies generally to all magnetic logic systems. Circuits of this nature may have a constant power–speed product analogous to the constant gain–bandwidth product of vacuum tube circuitry.

As matters stand, circuits using electrically interconnected cores appear to be satisfactory when bit-rate requirements are not excessive. They are expected to be reliable and economical. Fully integrated magnetic systems are feasible, in principle, with the exception of a few nonmagnetic components which must be included to provide the primary pulse sources. Such a machine should be designed at the very beginning in terms of magnetic components, rather than attempting to use magnetic subsystems as replacements for parts of an existing design. The replacement approach very often suffers because of the complications afforded by an impedance mismatch, as well as a mismatch of the relative capabilities of different technologies. The balance of parallel versus serial organization of a subsystem also should be kept in mind when speed is a consideration. The apparent reliability and low cost of magnetic devices may make practical an increased use of parallel organization. Questions of this nature will always be somewhat controversial, and indeed can only be settled for quite specific applications.

The question of interrogation of the outputs of a machine has been touched on only briefly. A magnetic device can be interrogated in a number of ways, both destructively and nondestructively. Most of these have been discussed in detail in the literature.

The number of magnetic devices for memory and logic is continually increasing, so that it would not be justified to assume that the devices selected for consideration in this paper represent the optimum. However, it does appear likely that alternatives will make use of similar techniques. No doubt more difficult, and occasionally simpler, approaches will be-

come evident. Few devices more complicated than shift registers have been constructed in this technology, and the practicability of more complex systems has yet to be established. The objective is to construct suitable function packages, which can be interconnected for specific applications. Because of the low input and output impedances, it is desirable to make individual packages considerably more complex in logical performance than has been done in other technologies. For example, in the case of the elementary shift register, let us not ask for a single-bit package to replace those now available, but rather for a multibit package. This is quite practicable; indeed, it is the most economical approach, and gives the most compact assembly. The further development of these circuits may open up some interesting possibilities for computer design.

VII. ACKNOWLEDGMENTS

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APPENDIX

The limiting parameters of the circuit described in Section IV can be determined by means of the approximate model for a core discussed in Section II.

First, to determine the properties required of the coupling winding consider the part of the shift register circuit shown in Fig. 24, let core 1
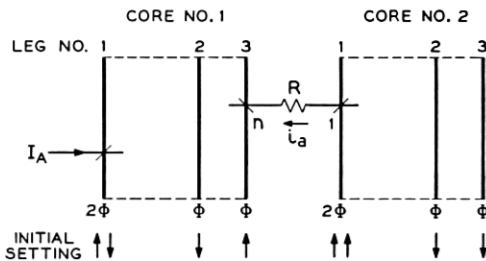

Fig. 24 — Shift register circuit, A phase.

contain a "one-primed" setting which is to be advanced into the second core as the A drive clears the first. In order that the maximum amount of flux be transferred, core 2 must switch at least as fast as core 1 at this time; i.e., $\dot{\varphi}_2 \geqq \dot{\varphi}_1$. Otherwise, core 2 will not have completed switching by the time core 1 is fully switched, and, therefore, the transfer will be incomplete. This requirement can be expressed as

$$i_a \geqq I_A - ni_a. \tag{1}$$

Equation (1) expresses the fact that the resultant mmf acting on core 2 must equal or exceed that acting upon core 1. The assumption is made that i_a remains constant during switching, this following from the model — i.e., $\dot{\varphi} = $ a constant — when a constant-current drive, I_A, is applied to produce the reversal.

Furthermore, considering emf's around the winding

$$i_a = \frac{n(\dot{\varphi}_1)_a - (\dot{\varphi}_2)_a}{R},$$

where the subscripts 1 and 2 refer to cores 1 and 2 respectively. For the limiting case where $(\dot{\varphi}_2)_a = (\dot{\varphi}_1)_a$,

$$i_a = \frac{(n - 1)(\dot{\varphi}_1)_a}{R},$$

or, inserting the expression for $\dot{\varphi}$ given by the model, i.e., $\dot{\varphi} = \Phi/\tau$,

$$i_a = \frac{(n - 1)}{R} \frac{4\pi\Phi}{s_w L} (I_A - ni_a - I_0), \tag{2}$$

where I_0 is the threshold current for switching between legs 1 and 3.

Thus, combining (1) with (2) to eliminate i_a and assuming that $I_A \gg I_0$, we obtain as a necessary condition

$$R \leqq \frac{4\pi\Phi}{s_w L} (n - 1). \tag{3}$$

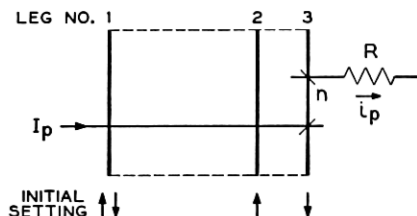We must now consider the requirements of the P phase. In this case

Fig. 25 — Shift register circuit, P phase.

I_p, Fig. 25, must be limited to below the threshold for switching between legs 1 and 3:

$$I_p < I_0. \tag{4}$$

The current induced in the coupling winding during switching in this phase is limited only by the resistance of the winding

$$i_p = \frac{n(\dot{\varphi}_1)_p}{R}$$

$$= \frac{n}{R} \frac{4\pi\Phi}{s_w l} (I_p - n i_p - i_0), \tag{5}$$

where i_0 is the threshold for switching between legs 2 and 3, and is equal to $I_0 l/L$, l and L being the lengths of switching paths around the small and large holes respectively. Combining (4) and (5), and noting that the reciprocal switching speed $1/\tau_p = 4\pi(I_p - n i_p - i_0)/s_w l$, it follows that

$$\frac{1}{\tau_p} < \frac{I_0 \left(1 - \dfrac{l}{L}\right)}{\dfrac{s_w l}{4\pi} + \dfrac{\Phi n^2}{R}},$$

or, taking into account the limitation on R, in (3), the limiting speed obtained by making $L \gg l$ is given by,

$$\tau_p > \frac{s_w}{H_0} \frac{n^2}{n - 1}, \tag{6}$$

where $H_0 = 4\pi I_0/L$ is the threshold field for the material. Thus, for a large length ratio, L/l, increased speed is obtained by decreasing the switching time constant or increasing the threshold field, both characteristics of the material only. The turns ratio, n, should be kept as small as compatible with the gain requirements. The minimum value for τ_p estimated in this way has the order of magnitude 10 microseconds for available materials in agreement with the measured range. As noted previously, a further increase in switching speed can be obtained by using an enabling winding.

It is of interest to determine, in a similar manner, the minimum switching speed during the slow phase of a related circuit described recently by Prywes.[17] (The reader is referred to the original article for a full description of the operation of this circuit.) For the present purposes, we need only consider that phase of the operation shown in Fig. 26. Core 1 contains a one. When drive I is applied to produce a reversal between legs 3 and 4 in core 1, the induced current i produces a reversal between legs 1 and 3 in core 2, advancing the one.
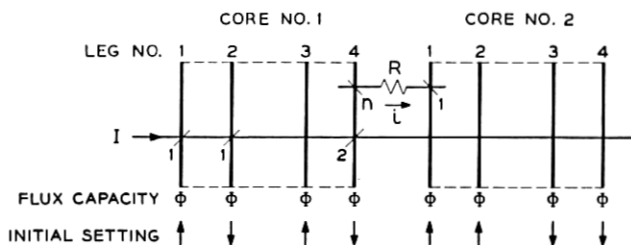
Fig. 26 — One phase of operation of circuit described by Prywes.[17]

As noted previously, it is necessary that $\dot{\varphi}_2 \geqq \dot{\varphi}_1$. However, in this case the fastest transfer of flux to core 2 is obtained by letting $R \to 0$. In this case,

$$\dot{\varphi}_2 \to n\dot{\varphi}_1 \quad \text{and} \quad i \to \frac{2nI + I_0}{1 + n^2}.$$

Therefore,

$$\frac{1}{\tau^2} = \frac{4\pi}{s_w L} (i - I_0)$$

$$< \frac{4\pi}{s_w L} \left(\frac{2nI + I_0}{1 + n^2} - I_0 \right).$$

In this circuit, in order to prevent an improper conversion of a zero into a one at this stage, it is necessary that $I \leqq I_0$. Therefore,

$$\tau_p > \frac{s_w}{H_0} \left(\frac{1 + n^2}{2n - n^2} \right).$$

Consequently, this arrangement is subject to similar speed limitations. In addition, in this case it is necessary that $n < 2$, thereby limiting the practical possibilities for fanout.

There are a number of alternative ways to organize these circuits. For example, the output of an information core containing a one can be used to inhibit rather than produce switching. However, the alternative arrangements are subject to essentially the same speed limitations.

At the beginning of Section IV it was pointed out that a combinational function could be generated at a given stage of the advance sequence by modifying the input structure of the core. One possibility is illustrated in mirror image form in Fig. 27. Legs 2 and 3 correspond to those of the same numbers in Fig. 10(e). However, the input leg [leg 1 in Fig. 10(e)] is replaced by a number of variable rungs V_N, there being as many legs,

N, as there are product terms in the Boolean function in its conjunctive canonical form. Each variable leg has the same flux capacity, Φ, as legs 2 and 3. In addition, a bypass leg B having a flux capacity equal to $(N - 1)\Phi$ must be added, and a closure leg C (capacity Φ) must also be added to complete the required flux path. There is a large aperture between legs B and 2, small apertures between the remainder. The "clear" flux setting of the structure is as shown in Fig. 27. Information is advanced into this core by N input pulses, each provided by the output of a preceding information core during an advance phase A_1. Each pulse switches flux down in each of the variable rungs. If all N inputs are present simultaneously, a full flux reversal will be produced in both legs B and 2. Each input pulse should be of duration longer than the longest switching time in order to prevent back-switching. The core can be "primed" and then "cleared" by I_{A_2} to advance a one out of the core as in the circuit of Fig. 10(e). On the other hand, if one or more of the inputs are missing, leg B will absorb all flux reversals and rung 2 will remain set downwards. In this case, the core cannot be "primed", and so a zero will be advanced during the A_2 phase. It will be clear that the input structure performs an AND function. Any OR terms necessary can be obtained by combining the outputs of separate cores. Thus, to the gain feature provided by the transfluxor output there is added provision for generating any combinational function. The same function can be generated by combining a number of the regular two-aperture cores, but a modified structure may offer a more convenient arrangement. Modified structures of this nature have been included in experimental circuitry, and have been shown to perform satisfactorily.
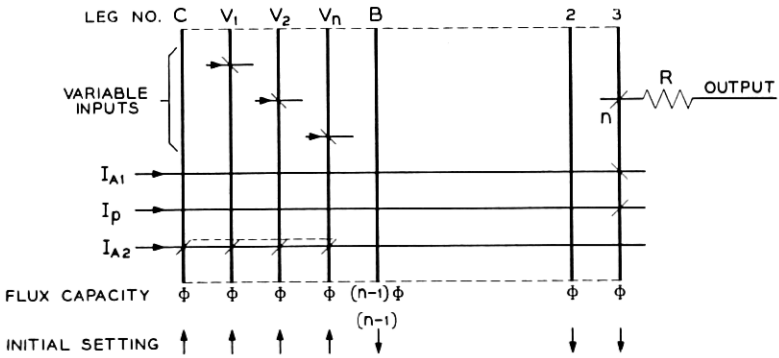

Fig. 27 — Structure for generation of combinational function at a given stage of the advance sequence by modifying input structure of core.

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