Application of Breakdown Devices to Large Multistage Switching Networks

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(Manuscript received July 15, 1958)

Electronic switches have been applied in designs for multistage space-divided electronic switching networks. The electrical characteristics of the gas diode switch are discussed from the viewpoint of its utilization in switching networks, with emphasis upon the circuits employed in an experimental electronic switching system. A general method of calculating voltage margins for the reliable operation of multistage switching networks is illustrated by the description of two techniques for establishing a switching path, the end-marking and internal-marking methods. In conjunction with these operational methods, the uses of network controls and auxiliary network cricuits, such as mark propagator and junctor circuits, are described. The transmission aspects of the electronic switching network determine to a large degree the circuit requirements and compromises. This is in contrast with the situation in electromechanical switching, where switching and transmission characteristics are largely independent.

I. INTRODUCTION

Switching networks, as discussed in this paper, comprise the interconnection facility for call traffic in a telephone switching system. This definition serves to exclude from consideration the numerous other components in the switching system, including the memory, logic, sensing and controlling elements that are required. This paper is concerned primarily with that large aggregation of switches which provides the desired voice frequency communication channels among telephone customers. Moreover, the discussion is limited to space-division electronic switching networks, excluding both electromechanical switching in its many forms and time-division electronic switching.

Since the advent of machine switching, a rapid evolution has taken place in the organization and control of multistage switching networks. This has led to the development of a succession of switching systems, each of which depended upon the nature of the chosen switching ele-

ment. In the Bell System these include step-by-step, panel and crossbar systems; the system name in each case being derived from the type of switch employed. The electronic switching system currently under development is keyed by its title to that branch of technology which is so important a characteristic of the present era. Nevertheless, the properties of a new switch, the breakdown diode, again determine to a considerable degree the structure of the new system.[1] In this paper are described the breakdown characteristics of gas diode switches and the dc-coupled logic circuitry that is employed in the establishment of switching paths in a multistage breakdown electronic switching network. These techniques are general in their application. Also described are the control circuitry and transmission aspects of an electronic switching network.

II. GENERAL

The space-divided switching network is first of all a mapping problem. It takes the form of a network of nodes and branches, including nodes designated as terminals. In the branches of the network are switches which are closed in sequences to provide paths among designated sets of terminals. Many paths exist simultaneously, but at a given time no node (or branch) is associated with more than a single set of designated terminals. The last requirement is a statement that unrelated paths are not coupled with one another but that n-way connections among more than two terminals may be permitted.

The economics of switching network design have been studied in terms of minimization of the number of switches required.[2] The boundary conditions include the number of terminals and the amount and kinds of traffic offered. Resulting configurations assign switch sizes, number of switching stages, wiring patterns and methods of operation — everything intended to produce the best traffic performance for the least cost over a defined range of office sizes. Electronic switch elements permit the fullest exploitation of such studies since they may be organized into groups with a minimum regard for regularity or "natural size" of the group. Considerations which, in other switching systems, set the optimum size ranges for stepping switches, crossbar switches or panel assemblies have little relevance in electronic switching, where the switches are available as discrete units.

The structure of large networks has taken the form of multistage arrays of rectangular switch modules. In crossbar systems, for example, the switch module is a unit of 10 or 20 verticals (inputs) connecting

TABLE I — RELATIVE ECONOMY OF SEVERAL NETWORK CONFIGURATIONS

Number of Stages	Switch Module Size	Terminals Each Side	Number of Diode Switches	Erlangs (Blocking = 1%)	Diode Switches per Erlang
3	75 x 75	5,625	1,265,625	4,280	296
4	22 x 22	10,648	937,024	4,550	206
5	20 x 20	8,000	800,000	4,930	162
6	10 x 10	10,000	600,000	4,250	143

with 10 horizontals (outputs). These 10-by-10 or 20-by-10 grids of crosspoints are organized into primary and secondary groups in an orderly wiring pattern, regularized for ease of control and administration. The electronic switching network may be organized in a similar structure. The basic switch module is a 10-by-10 grid with 100 crosspoints, each of which is supplied with a gas breakdown diode. The 10-by-10 switches are organized into primary, secondary and tertiary "frames" with a wiring pattern designed to maximize the fanout. The resulting "superframe" provides network building units with 1000 inputs, each of which reaches 1000 junctor terminals. Junctor links are employed to interconnect as many as ten originating superframes with an equal number of terminating superframes. The over-all switching network at maximum capacity has 10,000-by-10,000 terminations in six stages of 10-by-10 switch units, and contains 600,000 switch elements.

Further study to optimize network structures of this scale may indicate different choices for switch unit size, different number of stages and nonuniformity in structure. The study of structure is not the topic of this report, however, and it is mentioned only to establish the multistage fanout framework which constitutes the electrical circuit problem. Table I tabulates the calculated cost and performance for several large uniform grid networks in the region of 5000 erlang capacity. Lower cost in switches is achieved as the number of stages is increased.

III. THE BREAKDOWN DIODE SWITCH

Fig. 1 shows the significant voltage-current characteristics of the gas diode breakdown switch. It has been assumed that the device is to be operated in one dc polarity only, biased when conducting at a suitable sustaining value of dc, and that it will transmit speech signals which produce variations in the sustain current. It has been assumed further that a path may be extinguished from a single connected termi-

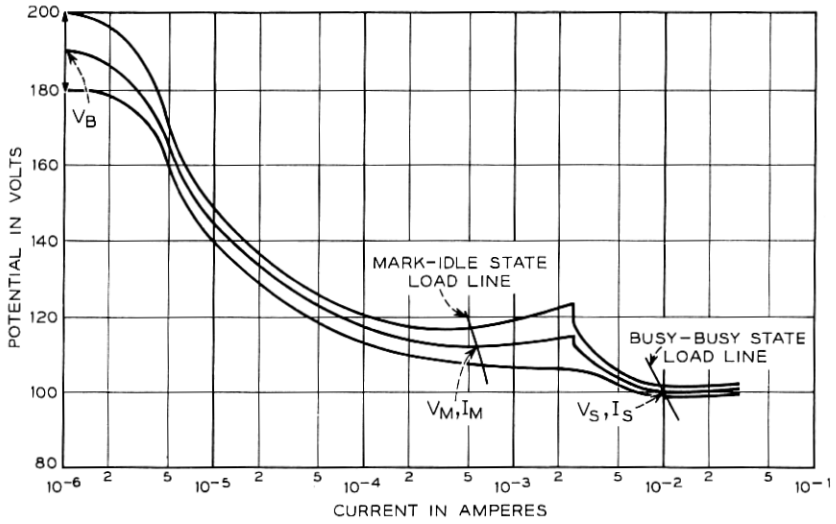

Fig. 1 — Breakdown characteristic for the A1624 gas diode switch in a multistage switching network application showing the range of product.

nal without a prior identification of the nodes which are associated in the particular path. This last assumption provides that the path will be extinguished if the normal sustain current is interrupted at any place in the path. Residual currents which might continue to flow through biasing impedances at the nodes must not sustain the switches.

The switch is made conducting by the application of a voltage at its terminals which exceeds the breakdown voltage, V_B with its range of values, $\pm\Delta V_B$. The circuit impedances establish the mark-idle load line shown in Fig. 1. The intersection of the load line with the switch characteristic established the value of current, I_M , which flows when the switch is marked. The voltage at this point, V_M , is lower than the marking voltage required to break down the switch. The voltage difference $V_B - V_M$ is the useful switch output signal which provides the mechanism whereby a marking potential, applied at the end of a switching network, propagates inward from stage to stage. The marking current, I_M , is held to a minimum practicable value since, in large switching networks, as breakdown propagates from the terminal to the interior nodes, this value is multiplied by fanout. Fanout ratios in large networks may exceed 1000-to-1, so that the total marking current requirement becomes impracticably large unless the current required to sustain the individual switch is maintained at a low value.

Those switches which are marked but not used in establishing a new connection must extinguish when the marking potential is again reduced to the idle value V_I, which is below the breakdown value. This also imposes restrictions upon the value of the marking current. The load line, when marking, must lie wholly above the switch characteristic; when idle, it must lie entirely beneath. Fig. 1 illustrates both situations for a typical switch. A third reason for minimizing the marking current is to maintain the load impedance as high as possible, since this is a shunt placed across busy paths in the talking condition and introduces audio losses. The final consideration bearing upon the value of the marking current is the negative impedance of the switch at this current: the lower the current, the higher the negative impedance. This impedance, together with the parasitic capacitance of the circuit, tends to produce sustained oscillations at marked nodes. Depending upon parasitic circuit capacitance to ground, marking currents in the order of 0.2 to 0.6 milliampere are typical. The V-I characteristic of the switch illustrates a typical discontinuity at $I = 2.5$ milliamperes. It is in this current region that the glow discharge of the gas tube moves from the outer surfaces of the cathode into its cavity.[3] Above this current, the tube continues to display a negative impedance—in this case, a useful transmission parameter. At the normal operating bias I_S, negative resistance of the order of 200 to 300 ohms is exhibited. The current in the chosen path is adjusted to the busy state (path-holding) value by changing simultaneously the load impedance and the source potential to path-holding values. The path-holding potential is below the voltage necessary to maintain conduction in the remaining marked switches, which are not required for the talking connection, and they extinguish. More will be said in a later part of the paper concerning the transmission properties of the gas diode switch and resulting network performance. At this point one other aspect is pertinent — the variabilities of all the switch parameters heretofore discussed. These ultimately determine the switching margins against false breakdown behavior. Successful design of a multistage network depends upon adequate limitation of the variabilities because, in ways which will become clear, they produce cumulative uncertainties in the process of propagating the marking potential into the fabric of a multistage switching network.

IV. BREAKDOWN SWITCHING NETWORKS

The crosspoint breakdown network exploits two useful characteristics of the switch element. One of these is that the path selection and con-

trol may be carried out over the path itself. The control voltages are applied to path nodes and directly operate the connecting switches. The second property of the switch is its utility as a memory cell. Its conducting or nonconducting state is read nondestructively in the path-finding process, thereby providing the mechanism for discerning idle nodes. No auxiliary path memory is required for these switching networks. Busy paths are avoided in the connection process without prior knowledge about the existing nodal busy or idle states. The nodal voltages shift potential when the node becomes busy, biasing the unconnected adjoining switches so that they cannot be broken down.

A node, q, in a multistage network may be in one of several states: busy, idle, marked or primed. The idle state potential is derived through shunt-bias impedances connected at the nodes. The prime-state potential is similarly derived but is applied in the marking sequence to designated nodes when directing the new paths to specified switch units, frames or switch levels is desired. The busy and marked potentials are derived from the various terminal circuits and transmitted through the switches to all the nodes in the respective marked or busy paths.

A marked node is expected to break down switches which connect with primed nodes in the succeeding stage. However, busy nodes are expected to be inaccessible from the adjacent nodes, excepting, of course, those which are associated with it in a busy path. These expectancies are met by a combination of properly chosen state potentials operating successfully with the voltage-current characteristics of the switches.

V. SWITCHING NETWORK BREAKDOWN MARGINS

One of the major design considerations in the construction of multistage switching networks is the provision of adequate voltage margins against false connections. A voltage margin may be defined as the minimum breakdown voltage of a switch less the maximum voltage that appears across it when it is in proper operation and should not break down. The following sections will illustrate a general method of calculating such margins in large networks and give some specific applications to several marking techniques. To facilitate the description of the network operation and margin conditions, the following list of terms, abbreviations and symbols is used:

n = number of network stages,

q = a general node in the network,

M_q^x = an x-type voltage margin between node q and a succeeding connecting node $(q + 1)$,

RM_q^x = an x-type voltage margin between node q and a preceding connecting node $(q - 1)$,

VI_q = voltage at node q during idle condition,

VK_q = voltage at node q during busy condition,

VM_q = voltage at node q during marking condition.

Fig. 2 shows two paths through an idealized n-stage network where there is no associated link circuitry. Only a general node q will be discussed. To provide adequate margins for the reliable operation of the network, it is necessary to select the worst possible condition contributing to false breakdown which exists between adjacent nodes, and then to optimize that condition. At a given time, a general node q may be in idle, busy or in some form of marking or priming condition. These potentials are indicated by the symbols VI_q, VK_q and VM_q, respectively. In addition, the busy node potential includes an ac component V_a, which represents the peak speech voltage transmitted through network paths. It is then possible to define the following set of margins to prevent breakdown of the switch in the forward direction.

(a) Margin M_q^a, which will prevent breakdown of a series switch when node q is busy, and node $(q + 1)$ is idle:

$$M_q^a = (V_B - \Delta V_B) - (VK_q - VI_{q+1}) - V_a . \tag{1}$$

(b) Margin M_q^b, which prevents a series switch from breakdown when node q is busy and $(q + 1)$ is busy:

$$M_q^b = (V_B - \Delta V_B) - (VK_q - VK_{q+1}) - V_a . \tag{2}$$

(c) Margin M_q^c, which will prevent breakdown when node q is busy and node $(q + 1)$ is in the marking condition:

$$M_q^c = (V_B - \Delta V_B) - (VK_q - VM_{q+1}) - V_a . \tag{3}$$

(d) Margin M_q^d, which prevents breakdown of a switch when node q is idle and node $(q + 1)$ is also idle:

$$M_q^d = (V_B - \Delta V_B) - (VI_q - VI_{q+1}). \tag{4}$$

(e) Margin M_q^e, which prevents a switch breakdown when node q is idle and node $(q + 1)$ is busy:

$$M_q^e = (V_B - \Delta V_B) - (VI_q - VK_{q+1}) - V_a . \tag{5}$$

(f) Margin M_q^f, which will prevent a switch breakdown when node q is idle and $(q + 1)$ is in a marking condition:

$$M_q^f = (V_B - \Delta V_B) - (VI_q - VM_{q+1}). \tag{6}$$

(g) Margin M_q^g, which will prevent breakdown when node q is marking and $(q + 1)$ is idle:

$$M_q^g = (V_B - \Delta V_B) - (VM_q - VI_{q+1}). \tag{7}$$

(h) Margin M_q^h, which prevents a series switch breakdown when node q is in the marking condition and node $(q + 1)$ is busy:

$$M_q^h = (V_B - \Delta V_B) - (VM_q - VK_{q+1}) - V_a . \tag{8}$$

(i) Margin M_q^i, which prevents a switch breakdown when nodes q and $(q + 1)$ are in the marking condition:

$$M_q^i = (V_B - \Delta V_B) - (VM_q - VM_{q+1}). \tag{9}$$

This list of margins may be reduced if it be assumed that two adjacent nodes in the same condition do not provide sufficient potential across the intervening switch to cause a breakdown. This eliminates margins M_q^b and M_q^d as trivial. It should be noted that, when there is more than one form of marking involved in the operational technique, the number of margins will increase. Under conditions which depend upon the particular network configuration, certain members of the preceding list may become the necessary conditions for the desired breakdown of the switch. In these cases, the voltage differences become negative, indicating the assured breakdown of the switch. An example of this would be condition M_q^i, which assures forward breakdown along the path of the desired connection.

A similar number of margins may also be defined in the reverse direction, i.e., voltage conditions which operate the switch in their reverse breakdown condition. As an example, RM_q^a may be defined as the margin preventing a reverse breakdown of a device when node q is in the busy condition, and node $(q - 1)$ is idle, i.e.:

$$RM_q^a = (V_{RB} - \Delta V_{RB}) - (VK_q - VI_{q-1}) - V_a . \tag{10}$$

Combining (1) and (10) gives a comparison of forward and reverse margins:

$$RM_q^a - M_q^a = (V_{RB} - V_B) - (\Delta V_{RB} - \Delta V_B) + (VI_{q-1} - VI_{q+1}). \tag{11}$$

It is characteristic of the gas diode network that the margins in the reverse direction exceed the forward margins. In gas diode networks the

sustaining voltage drop of the device is substantial (approximately 100 volts). To permit the breakdown of successive switches in establishing a connection, it is necessary to have a stage-to-stage increment in the idle node voltage bias about equal to the sustaining voltage drop. In (11) the term $(VI_{q-1} - VI_{q+1})$ is then approximately 200 volts, assuring a large reverse breakdown margin.

For devices having a very low sustaining voltage drop in the forward direction, the term to be considered in (11) is $(V_{RB} - V_B)$. To achieve a positive excess reverse breakdown margin, it is necessary that the switch reverse breakdown voltage, V_{RB}, safely exceed the forward breakdown, V_B.

Comparisons may be made among the other pairs of forward and reverse margins as was done in (11). Such comparisons lead to the same result, namely, the reverse margins to prevent breakdown exceed corresponding forward breakdown margins. The poorest of the reverse margins sets the requirement for the switch reverse breakdown voltage. Except for this calculation of reverse breakdown requirement for the switch, consideration now need be given only to the margins in the forward direction.

The list of margins may now be reduced by inspection. Assume, as a reference voltage, the busy condition at q to be VK_q. Then the idle and marking conditions may be either positive or negative with respect to this reference potential. Combining equations (1) and (5) gives, for example,

$$M_q^a - M_q^e = (VI_q + VI_{q+1}) - (VK_q + VK_{q+1}).$$

Then, depending on the relative polarity of the idle condition, M_q^e is greater than or less than M_q^a. In a particular network only one condition will exist, and consequently only one of M_q^a or M_q^e need be considered. Similarily, it can be shown that only one of M_q^c or M_q^h and only one of M_q^f or M_q^g need be considered. If the list of possible potentials for the idle and marking conditions is then considered with respect to the busy voltage as a reference, Table II may be drawn up (for convenience, the subscript q is dropped).

The worst marginal set now being known, it is necessary to optimize within the set in order to determine the best values of the circuit parameters. As previously indicated, the negative margin M_q^i, which assures forward breakdown along the desired path, is combined with the set of worst margins and provides a system of simultaneous equations in the bias voltages which may be solved for the particular case.

This will be more clearly understood if an example is considered. As

TABLE II — NETWORK MARGINAL SETS

VK	VI	VM	$\lvert VM \rvert > \lvert VI \rvert$	$\lvert VI \rvert > \lvert VM \rvert$	To Be Considered	To Be Eliminated
Reference	+	−			$M^f\ M^e\ M^c$	$M^a\ M^g\ M^h$
Reference	−	+			$M^g\ M^a\ M^h$	$M^e\ M^f\ M^c$
Reference	+	+	Yes	No	$M^h\ M^e\ M^g$	$M^a\ M^c\ M^f$
Reference	+	+	No	Yes	$M^e\ M^h\ M^f$	$M^a\ M^c\ M^g$
Reference	−	−	Yes	No	$M^c\ M^a\ M^f$	$M^e\ M^h\ M^g$
Reference	—	—	No	Yes	$M^a\ M^c\ M^g$	$M^e\ M^h\ M^f$

an application of margin calculations, consider a network employing a technique of end, or terminal, marking[4] to establish a connection.

VI. END-MARKING TECHNIQUE

This technique is a method of controlling the establishment of connections in a switching network where voltage (or impedance) marks are derived by translation of address information and applied to network terminals only.

The propagation of the marks into the fabric of the network can be described briefly as follows. In the idle condition, all nodes are biased negatively. To establish a connection, a terminal is selected and a marking potential, VM_0, is applied to the zero, or terminal, node. This is a positive potential and, combined with the negative idle voltages appearing at the connecting first nodes, it is sufficient to switch the first-stage devices to their low-impedance state. Associated with a switch in its busy state is a potential drop, V_S, and its variation, ΔV_S. The potential drop, $V_S \pm \Delta V_S$, now occurs across one of the first-stage crosspoints which switches to the low-impedance state, and a voltage $VM_0 - (V_S \pm \Delta V_S)$ appears at the first nodal position. This, combined with the negative idle potential at the second nodes, is sufficient to break down

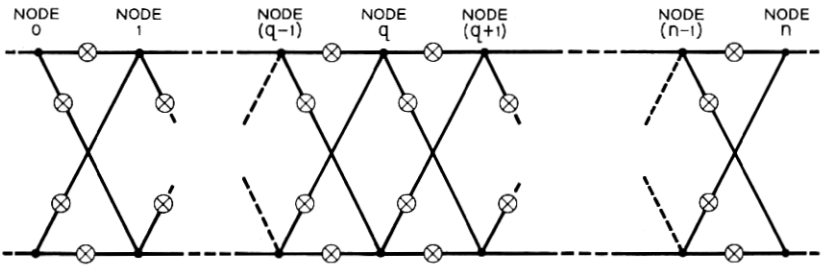

Fig. 2 — Two paths through an n-stage switching network.

the connecting second-stage switches. Multipled at each node are several paths leading through second-stage switches to secondary nodes; two such paths are shown in Fig. 2. The idle potential at any such multipled second nodes will cause breakdown of additional second-stage switches, permitting the marking potential to fanout to several switches in the second stage. It is this fanout of the marking potential which provides the ability of the network to seek out idle paths. The marking potential at one node tries to break down all multipled switches; those which do break down form elements of possible paths. By this method, the terminal mark produces progressive breakdown towards the outgoing terminal. Since sufficient current must be provided to maintain the multipled switches in the second (and ensuing) stages in their low-impedance states, it is readily seen that an important inherent drawback of the end-marking technique is the very large current drain. (In three stages of 10 x 10 switches, this fanout ratio is 1,000-to-1.)

As a result of the voltage drops across switches in the busy condition, the busy voltage, VK_q, at a node q depends upon the position in the network at which the reference voltage in the busy path, V_R, is introduced. For simplicity in discussion, assume that the dc reference voltage, $-V_R$, is applied at the outgoing terminal, and has associated with it a small variation, ΔV_R. The busy voltage at node q is then given by the relation

$$VK_q = -(V_R \pm \Delta V_R) + (n - q)(V_S \pm \Delta V_S). \tag{12}$$

Experimentally, it has been found that, to switch a breakdown diode to its low-impedance "on" state, it is necessary to provide a voltage greater than the nominal breakdown voltage and its variation, $(V_B + \Delta V_B)$. This overvoltage is given by the symbol Δ. Then, for the end-marked network, the marking potential at a node with idle potential at the next adjacent node must turn the switch "on," i.e.

$$VM_q - VI_{q+1} = (V_B + \Delta V_B + \Delta). \tag{13}$$

Equation (13) represents condition (g) of the preceding margin list, where the voltage difference is negative, assuring the breakdown of the switch. Moreover, the difference in the marking potentials at adjacent nodes is merely the sustaining voltage (and variation) of the intervening switch, i.e.,

$$VM_q = VM_{q+1} + (V_S \pm \Delta V_S), \tag{14}$$

or, in general,

$$VM_q = VM_{q+x} + x(V_S \pm \Delta V_S). \tag{15}$$

A tentative assignment of potentials can now be made for VM_q and VI_q. As indicated in (15), the marking potential changes from node to node decreasing as q increases, and cannot be set to a universal value. The idle potential at all nodes may, as a practical matter, be set to a single value. The marking potential has its least value at node $(n - 1)$. Then, to satisfy (13),

$$VM_{n-1} + VI_n = (V_B + \Delta V_B + \Delta), \tag{16}$$

and VI_n will represent the largest idle potential in the network. All other idle potentials will be less than this, and any universal idle potential must at least equal this value of VI_n. Choose, then, all idle potentials to be the same as VI_n, and set

$$VI_n = VI_q = -(1 - \alpha)(V_B + \Delta V_B + \Delta), \tag{17}$$

where α is a fraction less than, or equal to, unity. From (16) and (17),

$$VM_{n-1} = \alpha(V_B + \Delta V_B + \Delta).$$

From (15),

$$VM_q = VM_{n-1} + (n - q - 1)(V_S \pm \Delta V_S).$$

Combining these two yields

$$VM_q = \alpha(V_B + \Delta V_B + \Delta) + (n - q - 1)(V_S \pm \Delta V_S). \tag{18}$$

Then, for the end-marked network, (15), (17) and (18) give the values of the busy, idle and marking voltages. To determine the worst marginal conditions, the busy voltage is taken as a reference voltage, and these equations then represent the conditions in the second row of Table II. The margins which must be considered are M_q^a, M_q^g, and M_q^h. The conditions given by M_q^g have already been considered in obtaining (13). The two remaining conditions which must be studied are

$$\begin{aligned} M_q^a &= (V_B - \Delta V_B) - (VK_q - VI_{q+1}) - V_a \\ &= \alpha V_B - (2 - \alpha)\Delta V_B + V_R - \Delta V_R \\ &\quad - (1 - \alpha)\Delta - (n - q)(V_S + \Delta V_S) - V_a, \\ M_q^h &= (V_B - \Delta V_B) - (VM_q - VK_{q+1}) - V_a \\ &= (1 - \alpha)V_B - (1 + \alpha)\Delta V_B - V_R \\ &\quad - \Delta V_R - \alpha\Delta - 2(n - q - 1)\Delta V_S - V_a. \end{aligned}$$

Both these margins exhibit the worst conditions at the same node,

$q = 0$. To optimize conditions, these two margins may be equated, yielding, at $q = 0$,

$$2V_R = (1 - 2\alpha)(V_B + \Delta V_B + \Delta) + nV_S - (n - 2)\Delta V_S . \quad (19)$$

From this equation it may be seen that the reference voltage, V_R, is most independent of device parameters if $2\alpha = 1$. Under these conditions,

$$2V_R = nV_S - (n - 2)\Delta V_S . \quad (20)$$

The worst margin may then be expressed as

$$M_0^a = M_0^h = \frac{1}{2} V_B - \frac{3}{2}\Delta V_B - \frac{1}{2}\Delta - \Delta V_R - \frac{n}{2} V_S - \left(\frac{3n - 2}{2}\right)\Delta V_S - V_a . \quad (21)$$

The overvoltage, Δ, may also be considered as one of the necessary margins in the network operation. Then, setting Δ equal to the other margin, the worst margin becomes

$$M = \frac{1}{3} V_B - \Delta V_B - \frac{2}{3}\Delta V_R - \frac{n}{3} V_S - \left(\frac{3n - 2}{3}\right)\Delta V_S - \frac{2}{3} V_a . \quad (22)$$

To determine the number of stages of switching through which the marking potential may be propagated, M is equated to zero, and (22) is solved for n. This gives

$$n = (V_B - 3\Delta V_B - 2V_R + 2\Delta V_S - 2V_a)/(V_S + 3\Delta V_S). \quad (23)$$

As a numerical example, suppose that the switch used is a neon gas diode whose characteristics are:

$$V_B = 190 \pm 10 \text{ volts},$$

$$V_S = 101 \pm 1 \text{ volt at 10 milliamperes sustain current},$$

$$\Delta V_R = 1.0 \text{ volt}.$$

This network would operate in a 2000-ohm impedance circuit in order to transmit 10 milliwatts of audio power, and $V_a = 6.3$ volts. Substituting these values in equation (23) yields

$$n_{\text{neon diode}} = (190.0 - 30.0 - 2.0 + 2.0 - 12.6)/(101.0 + 3.0)$$
$$= 1.3.$$

That is, the marking potential may be transmitted reliably through just

one stage of switching; with two stages of switching, the margins become negative and false breakdowns will occur.

Various means for improving the margins for a gas diode network have been proposed. An obvious improvement is to bisect the network, so that it is marked at both terminals and these marks produce progressive breakdown toward the central nodes. At the center, a matching facility is necessary which will recognize the arrival of a clear path to both terminals and connect these paths. This matching device also permits the establishment of one connection only, which provides a lock-out function against redundant parallel paths. Such a bisection should approximately double the number of stages for which the use of a given switch is applicable. The network is symmetrical about the central node (junctor) and, consequently, the operation of only one-half the network need be studied. It is also possible to regulate the holding voltage, V_R, at the central position in the network, thereby minimizing the variation of the worst busy link voltage.

The busy voltage at a general node q is given by the relation

$$VK_q = -V_R + \Delta V_R + \left(\frac{n}{2} - q\right)(V_S \pm \Delta V_S). \tag{24}$$

The propagation of the marking potential through the network is still represented by (13) to (15) and the marking potential has its least value at node $(n/2) - 1$. Then, to satisfy (13),

$$VM_{n/2-1} + VI_{n/2} = (V_B + \Delta V_B + \Delta).$$

The potential $VI_{n/2}$ represents the largest idle voltage, and all others may be chosen equal to it, i.e.,

$$VI_{n/2} = VI_q = -(1 - \alpha)(V_B + \Delta V_B + \Delta). \tag{25}$$

Thence,

$$VM_{n/2-1} = \alpha(V_B + \Delta V_B + \Delta),$$

and, from (15),

$$VM_q = VM_{n/2-1} + \left(\frac{n}{2} - q - 1\right)(V_S \pm \Delta V_S).$$

Combining these two yields

$$VM_q = \alpha(V_B + \Delta V_B + \Delta) + \left(\frac{n}{2} - q - 1\right)(V_S \pm \Delta V_S). \tag{26}$$

Then, for the bisected, end-marked network in which the reference voltage supply is placed at the junctor, the busy, idle and marking potentials are given by (24) to (26). These represent the conditions in the second row of Table II and, as in the previous example, the margins M_q^a, M_q^g and M_q^h must be considered. Once again, M_q^g represents the condition for the desired forward fanout of the marking voltage. The other margins may be written as:

$$M_q^a = (V_B - \Delta V_B) - (VK_q - VI_{q+1}) - V_a = \alpha V_B - (2 - \alpha)\Delta V_B + V_R - \Delta V_R - (1 - \alpha)\Delta - \left(\frac{n}{2} - q\right)(V_S + \Delta V_S) - V_a,$$

$$M_q^h = (V_B - \Delta V_B) - (VM_q - VK_q + 1) - V_a = (1 - \alpha)V_B - (1 + \alpha)\Delta V_B - V_R - \Delta V_R - \alpha\Delta - 2\left(\frac{n}{2} - q - 1\right)\Delta V_S - V_a.$$

Both these margins exhibit their worst condition at the node $q = 0$. To optimize conditions, these margins are equated at $q = 0$, yielding

$$2V_R = (1 - 2\alpha)(V_B + \Delta V_B + \Delta) + \left(\frac{n}{2}\right)V_S - \left(\frac{n}{2} - 2\right)\Delta V_S. \quad (27)$$

As before, V_R is most independent of device parameters if $2\alpha = 1$ and, under these conditions,

$$2V_R = \left(\frac{n}{2}\right)V_S - \left(\frac{n}{2} - 2\right)\Delta V_S, \quad (28)$$

and the margins become

$$M_0^a = M_0^h = \tfrac{1}{2}V_B - \tfrac{3}{2}\Delta V_B - \tfrac{1}{2}\Delta - \Delta V_R - \frac{n}{4}V_S - \left(\frac{3n + 4}{4}\right)\Delta V_S - V_a. \quad (29)$$

If the overvoltage is considered a necessary margin and is equated to the margin in (29), the worst margin is

$$M = \tfrac{1}{3}V_B - \Delta V_B - \tfrac{2}{3}\Delta V_R - \frac{n}{6}V_S - \left(\frac{3n + 4}{6}\right)\Delta V_S - \tfrac{2}{3}V_a. \quad (30)$$

Then, to determine the number of stages of switching through which the marking potential may fan out without a negative margin, (30) is equated to zero, and

$$n = 2(V_B - 3\Delta V_B - 2\Delta V_R + 2\Delta V_S - 2V_a)/(V_S + 3\Delta V_S). \quad (31)$$

This equation gives n as exactly twice the value for a nonbisected network in which V_R is supplied at the outgoing terminal, as indicated in (23).

Then, for a gas diode switch, the bisected network can permit the propagation of the marking potential through two stages of switching before false breakdowns will occur.

Although there will be no change in the margin equations just derived, it is possible to obtain a more symmetrical arrangement of the network. The switches in each half of the bisected network may be polarity-oriented towards the junctor. This symmetrical arrangement exhibits better transmission properties for the network than did the preceding "straight-through" case. Gas diodes of the type presently available are used in a region of nonlinear negative resistance. In the straight-through network, instability and distortion arise from this nonlinearity.

For a bisected network, then, it would appear that a maximum number of stages would be two, unless additional control of the circuitry were added.

VII. PROPAGATORS

Such an additional circuit is the propagator. This is an auxiliary link circuit which, in a multistage network, would appear at intermediate nodes. The propagators correct for the variations in switch characteristics by requantizing the voltage mark as it is transmitted towards the junctor. This regenerated potential can then fan out through two additional stages and still maintain positive margins.

A propagator circuit, for use with a gas diode switch, is shown in Fig. 3. A marking signal, in the form of a positive pulse, ionizes the gas diode, X_1, in the stage of switching preceding the propagator. An idle input bias and link resistor provide that, when X_1 ionizes, current flows from X_1 to the idle input bias terminal. When X_1 breaks down to its low-impedance state, the voltage at the cathode of X_1 will increase by the difference in the sustaining and idle voltages of the diode switch. The increase is ac-coupled through a resistor-capacitor combination, R_1-C_1, to the anode of the propagator gas diode. The diode D_2 is reverse-biased, and the voltage coupled through R_1-C_1 will add to the idle voltage already appearing at the propagator anode. When the positive pulse at the cathode of X_1 rises above the potential of the idle output bias, the diode D_1 becomes forward-biased and a small part of this pulse is reflected through D_1 to the cathode of the propagator tube. Despite the appearance of part of the pulse at the propagator cathode, the main

part of the pulse arrives at the propagator anode. The pulse reaching the anode of the propagator has an exponential decay with a time constant $C_1(R_1 + R_2)$.

To assure breakdown of the propagator tube, this pulse must remain above a given breakdown voltage for a time greater than the longest ionization time of the tube. Simultaneously with the application of marking voltages, a propagator mark voltage pulse appears at all propagators. This rises to the same potential as the idle propagator bias, thereby giving this supply a low-impedance path on the anode side of the propagator tube. In the busy paths the propagator gas diodes are not ionized by the propagator mark voltage. This voltage is coupled into the circuit through diode D_2 at a magnitude which does not exceed the propagator idle bias, so that the marking pulse will not be coupled into busy nodes through the R_1C_1 network. The source impedance of the propagator mark voltage is low so that, upon ionization of the propagator gas diode, a new source of marking potential is effectively coupled to the output node. The cathode voltage rises to the clamping potential, the mark limiting voltage. This is the newly regenerated marking potential which propagates forward into the succeeding switching stage X_2.

The propagator also reduces the fanout current for the X_1 stage of the distribution network during the marking cycle. This, of course, reduces the current requirement of the voltage-marking source at the network terminal.

With propagators, a six-stage network may be constructed to operate

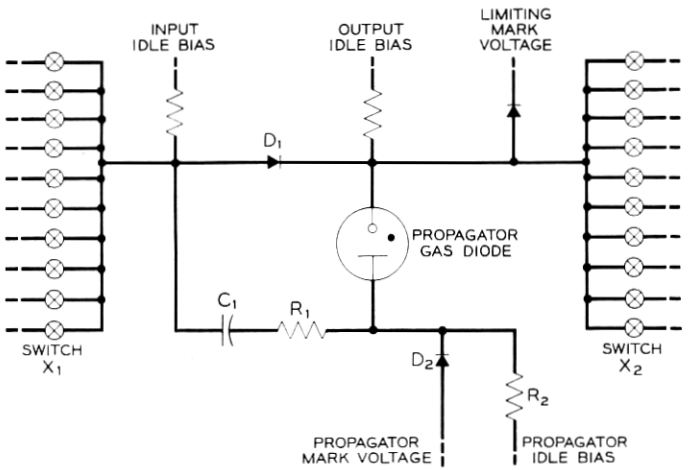

Fig. 3 — Active mark propagator circuit.

with positive voltage margins. The four inner stages, bisected as already described, now operate as two two-stage networks. Between these and the two outer stages are inserted propagator circuits. In this arrangement each half of the network is marked as a one-stage network and a two-stage network and is held, in the busy condition, as a three-stage network. The margins lie between those of a two- and a three-stage network; examination shows them to be positive and close to those of the two-stage network alone.

The propagator just described operates to connect additional marking energy into a switching node and provides the dual results of requantizing the mark potential and supplying the fanout current. When current fanout is not a consideration, the following passive circuit (Fig. 4) may be employed at less cost. This circuit is useful, for example, between stages two and three and between stages four and five of the six-stage network as an additional margin improvement circuit. No additional mark voltage source or active device is required.

In the idle condition, diode D_3 is reverse-biased, and a charge appears across capacitor C_2. When a connection is being established, a marking signal appears at the anode of the second-stage switch X_2. This, combined with the input idle bias, is sufficient to ionize X_2, and the voltage at the cathode of X_2 rises by the difference in the sustaining and idle voltages of the gas diode. This voltage pulse is not transmitted through D_3 to the anode of the third-stage switch X_3. The pulse is, however, ac-coupled through the R_3-C_2 resistor-capacitor network. The pulse combines with the output idle bias to produce a pulse which is limited by

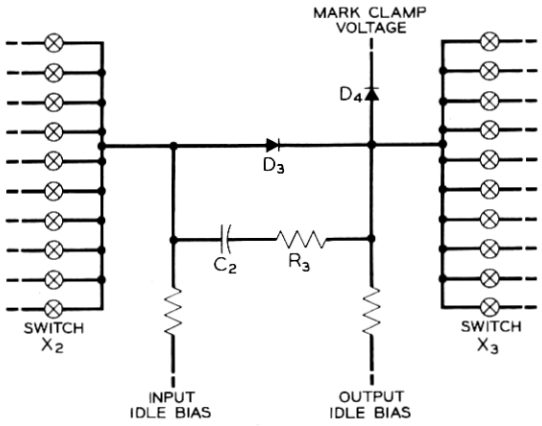

Fig. 4 — Passive mark propagator circuit.

conduction of diode D_4 to the clamp mark voltage. This voltage is subject to less variation than the original marking signal appearing at the anode of the second-stage switch.

The requantized marking voltage is supplied to the anode of the third-stage switches X_3 and, combined with the third-stage output idle bias, it is sufficient to ionize the X_3 switches. The discharge time of the R_3-C_2 network must be less than the time required to ionize the X_3 switches, so that the potential appearing at the input node to stage three does not come out of the clamp before the X_3 switches ionize. When the X_3 switches conduct, the potential at the X_3 node falls, and diode D_3 then conducts in the forward direction, completing a dc path from the second to the third stage of the network.

VIII. NETWORK CONTROLS

To this point the discussion primarily has been concerned with the distribution switching network; there has been a description of the end-marking process, the switch characterization and circuits such as the propagator which implement the marking process. There are, however, several types of orders which must be carried out by the network.[1] Information must flow between the memory elements of the system and various network controls which carry out these orders. There must also be a sequence circuitry for programming these orders through the network. The following sections will briefly discuss network controls and their operation such as those which will be used in the experimental electronic switching system.

Connections are set up in the distribution switching network by marking, or changing the voltage, at the particular end terminals between which a transmission path is desired. This change of voltage is propagated through the network from each side toward the center on all idle paths. At the junctor only one of the many paths that can handle the call is permitted to connect itself to the hold supply.

To establish a connection through the network, the binary address of the desired terminal is sent from the central control of the system to the input of a selector circuit. The selector contains two stages of magnetic core circuitry. It translates in two stages the given address to a two-digit address, one 20-valued and one 50-valued. Seventy leads then are wired through a maximum of 1000 terminals. Each terminal has a resistor and a selector gas diode, which act as the last stage of selection. These elements are wired to the 20-by-50 crosspoint matrix. A negative pulse on one of the 50 X-coordinate leads and a positive

pulse on one of the 20 Y-coordinate leads will cause one, and only one, of the network terminal selector gas diodes to ionize. This transmits the marking potential to the anodes of the first-stage switches.

Associated with the selector is a sequential pulsing circuit. A pulse into this circuit clears both stages of the selector core circuitry. The input cores then are set according to the voltage pattern on the address leads. Finally, the information is read through the two stages of cores and fires one selector diode in the output stage.

At the end of this operation, three pieces of information are returned to the central control of the system: (a) the completion of the operation, (b) its success or failure, and (c) for an unsuccessful connection, whether a failure was caused by encountering a busy terminal or by failing to make a connection. This latter case may be caused by a fault in the system or by inability to find an idle path from an available junctor to the desired terminal, i.e., blocking.

When the desired terminal address is sent to the selectors, other operations are also begun. The propagator pulsers are turned on, and the "time-out" pulser is set. This pulser is a clock which measures the interval permitted in which to establish a connection.

The busy-check delay circuit is also set in operation. This is a monostable flip-flop which times the check of end terminals for busy connections. If either of the end terminals is busy within the check period, the junctor enabler is not started and the operation is concluded.

If both terminals are idle, the junctor enabler circuit, which sequentially tests junctors for the presence of mark signals, is set in operation. A junctor circuit and control are shown in Fig. 5. A junctor latch tube receives marks from both sides of the network and, with the enabling signal, it ionizes and completes the paths from the marked terminals through the two halves of the network to the holding potential. A match pulse is generated by the resulting holding current which indicates the successful completion of the connection.

If, at the end of the permitted "time-out", neither a "successful match" nor "busy" signal is received, the time-out pulser reports this to the central control and the network controls are cleared.

The controls are cleared after each operation of a sequential circuit. A pulse from the match (or release) detector, from the connect (or release) time-out pulser, or from the central control system can initiate such a clearing sequence. In the connect sequence, a pulse from any of these sources stops the junctor enabler and resets the time-out pulsers. Deionization of the gas tubes in the output stages of the propagator

pulsers and selectors begins, and the control voltages are removed from the network.

After sufficient time has elapsed to clear the network and its controls, a pulse is transmitted to the central control which signals the readiness of the network to accept the next command.

To disconnect a path, the address of either terminal of the connection is fed from the central control to the appropriate terminal selector. This translates the address in the same way as for the connect order and reapplies the mark voltage at the specified terminal. Associated with the release order is a delay circuit which, upon operation, initiates the "release time-out" clock. The mark voltage is transmitted via the connection to the junctor. This, in conjunction with a release pulse applied in common to all junctors, fires a release tube in the junctor which removes the hold current from the latch tube. When the current in the latch tube has decreased below its minimum sustaining current, deionization takes place. The release tube then is extinguished by removal of the common release pulse, and the network release is complete.

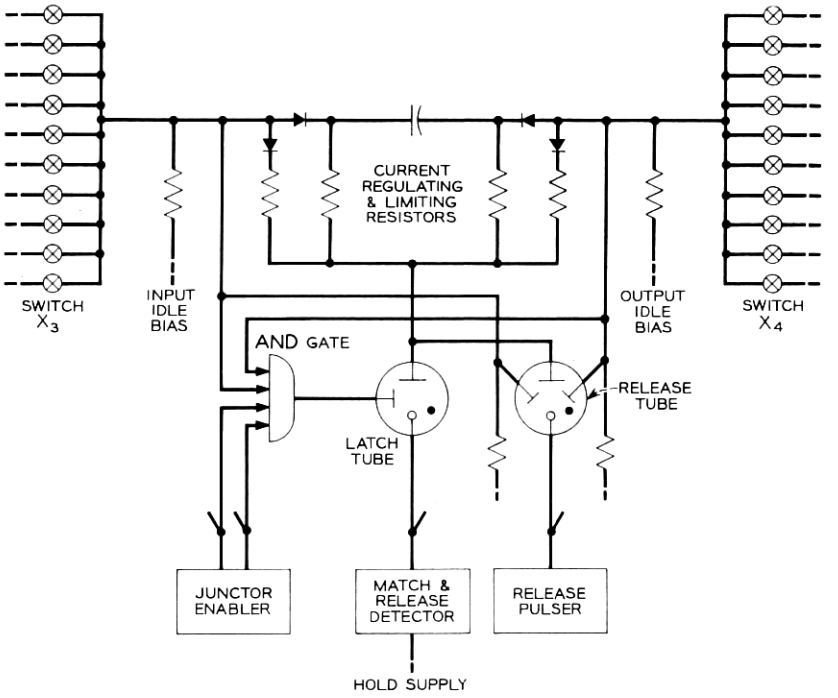

Fig. 5 — Junctor circuit and control.

Network control circuits include one more group, called "identifiers." These are the inverse of selectors; they detect at network terminals changes in current which are produced by marking or release actions and translate the specific action location into its binary address. This function serves two important purposes in network operation. First, the operation of the selectors which translate the input binary address into action at a specific terminal is checked by the simultaneous inverse translation of the action back to binary address form. The selector address is compared with the identifier address. If the two binary numbers match, it is certain that marking potential was connected to the specified terminal. Mismatch is a valuable trouble indication and a signal to operate with the duplicate set of network control equipment.

The second use of the identifier is to permit a trace through the network. When a disconnect is initiated at one terminal in a connection, the equipment number of the opposite terminal is recovered in its corresponding identifier. Progressive disconnect is thereby facilitated without the need for large amounts of call memory.

IX. INTERNAL MARKING

An alternative to the end-marking scheme is to program the marking of each stage of switching according to the terminal addresses involved in the particular connection. The network terminal address is a binary word which may be divided into several sections. For the six-stage network, these sections specify the appropriate superframe, frame and switch components of the address. Each section of the address is used to control a sub-selector and a full selector marks the terminal. The switch selector has access to the first nodal circuits; the frame section of the address has access to the second set of nodes. The superframe section of the address is used to partially control the junctor enabler, limiting its access to junctor nodes in the selected superframe. This technique applies marking potentials to the selected nodes in the network, directing the establishment of connections.

The system is characterized by the addition, at each node, of an auxiliary marking circuit which includes a shunt breakdown switch. It is through these shunt switches that individual nodes are marked, permitting the establishment of a unique path in both halves of the network. A selective choice of matching devices at the junctor then will permit the establishment of a unique path through the entire network. This procedure is similar to that used in the crossbar systems. The ability to determine a single switching path eliminates the problem of

fanout that occurs in the end-marked network, giving a considerable saving in marking-current drain.

Two paths through one half of such an internally-marked n-stage network are shown in Fig. 6. The network is bisected and the reference voltage in a busy path, $-V_R$, is introduced at the central node. The operation of the system is symmetrical about the junctor, and only that of one half need be considered.

As for the bisected end-marked network, the busy voltage at a general node, q, is given by the relation

$$VK_q = -(V_R \pm \Delta V_R) + \left(\frac{n}{2} - q\right)(V_s \pm \Delta V_s). \tag{32}$$

The sequence employed for establishing a connection is now detailed. In the idle condition the nodes are permanently biased through a resistor, R_q, at a negative potential, E_q. When a node has been selected to participate in the establishment of a connection, a positive potential, V_q, is applied through the shunt switch in series with another resistor, r_q. The voltage, $V_q - E_q$, is sufficient to operate the shunt switch at a sustaining current, $I_p \pm \Delta I_p$, somewhat in excess of its minimum sus-

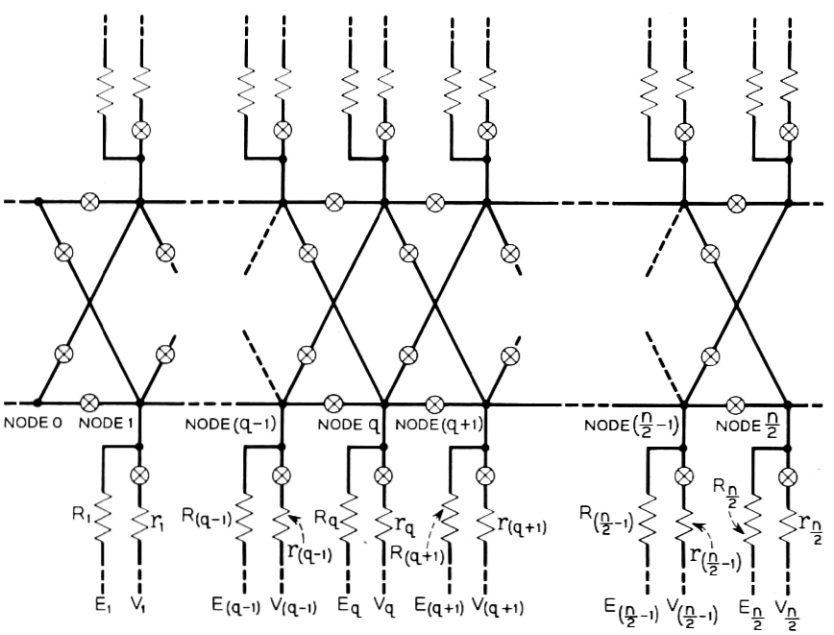

Fig. 6 — Two paths through $n/2$ stages of internally marked switching network.

taining current, i.e.,

$$V_q - E_q = (V_B + \Delta V_B + \Delta). \tag{33}$$

If the node is already busy, the application of V_q will not operate the shunt switch. Thus, busy paths are not disturbed by the marking of nodes in the process of setting up new paths. This change of state at the node will be called priming, and the potential at q during this condition is VP_q.

The junctor node, in the idle condition, is permanently primed at a value $VP_{n/2}$ through the resistor $R_{n/2}$. If an idle junctor node is selected, a negative potential $V_{n/2}$ is applied through $r_{n/2}$ to turn on the shunt switch at the node $n/2$. This places a negative potential $VMI_{n/2}$ at the node, where $VMI_{n/2}$ is called the first marking potential at node $n/2$. If now a connecting preceding node is in the primed condition, the series switch between these nodes will turn on, i.e.,

$$VP_{(n/2)-1} - VMI_{n/2} \geqq (V_B + \Delta V_B + \Delta). \tag{34}$$

The potential now appearing at node $n/2 - 1$ is $VMI_{n/2-1}$. This negative potential is such that, combined with the priming potential at the next preceding connecting stage, it will turn on the intervening switch. To assure this condition, $r_{n/2} \ll r_{n/2-1}$. In this manner, the marking potential is propagated outwards towards the terminals and, in general,

$$VP_{q-1} - VMI_q \geqq (V_B + \Delta V_B + \Delta). \tag{35}$$

The resistances, r_0 and $r_{n/2}$, are such that $r_0 \ll r_{n/2}$. Consequently, when the mark has reached the zero node (terminal), nodal potentials again reverse, and a positive potential now appears at each node in the first half of the network. This positive potential, given by $VMII_q$, is called the second marking potential.

A similar succession of potentials appears at the nodal positions in the second half of the network. If a clear path for the connection has been encountered in both halves of the network then, during the junctor enabling, the potential $VMII_{n/2}$ coupled with the enabling voltage will cause the junctor switch to break down and conduct in the forward direction. This permits a large current to flow in the series switches. The detection of this current surge sets in motion circuitry to extinguish the shunt switches and supply a holding current and voltage in the busy path.

The priming voltage, VP_q, at a node q is determined by the bias voltage applied to the node, V_q, i.e.,

$$VP_q = V_q - r_q(I_p + \Delta I_p) - V_s - \Delta V_s . \tag{36}$$

Combining (35) and (36) yields

$$-VMI_q = V_B + \Delta V_B + \Delta + r_{q-1}(I_p + \Delta I_p) + V_s + \Delta V_s - V_{q-1} . \tag{37}$$

A tentative assignment of potentials may be made for V_q. This may have the same value at all nodes, and so may be set to

$$V_q = \beta(V_B + \Delta V_B + \Delta), \tag{38}$$

where β is a fraction less than, or equal to, unity. Then, to satisfy (33),

$$E_q = -(1 - \beta)(V_B + \Delta V_B + \Delta). \tag{39}$$

The network operation involves three forms of marking and, as a consequence, the number of margins to be considered is increased threefold over the number considered when one form of marking was employed, as in the end-marked case. That is, VM of Table II now has three possible values, VP, VMI and $VMII$. The potential at node q under differing conditions is given by equations (32) to (39). Using the busy potential at node q as a reference, the idle and priming voltages represent the conditions of line two of Table II. The idle, busy and first marking voltage give the conditions of line five of Table II. Since there is some freedom in the choice of the junctor enabling potential, $VMII_{n/2}$ may be chosen so as to give better-than-minimal margin conditions. For example, $VMII_{n/2}$ may be chosen to be $\frac{1}{2}(V_B + \Delta V_B + \Delta)$. Then the idle, busy and second marking voltage give the conditions on line two of Table II. These conditions, however, are less restrictive than those represented by the idle, busy and priming voltages. The marginal conditions to be considered, then, are (a), (c), (f), (g) and (h) of Section V.

Marginal conditions (f) and (g) are merely restatements of the conditions necessary for the proper network operation. An examination of the remaining margins shows that $M_q{}^a$ may be eliminated as being less restrictive than $M_q{}^c$ and $M_q{}^h$. Then the two worst conditions are given by:

(i) Margin $M_q{}^c$, which prevents the breakdown of a series switch when node q is busy and node $(q + 1)$ is in the first stage of marking, i.e.,

$$M_q{}^c = (V_B - \Delta V_B) - (VK_q - VMI_{(q+1)}) - V_a .$$

From (32), (37) and (38), this becomes

$$M_q{}^c = \beta V_B + (\beta - 2)\Delta V_B + (\beta - 1)\Delta + V_R - \Delta V_R - r_{q-1}(I_p + \Delta I_p) - \left(\frac{n}{2} - q + 1\right)(V_s + \Delta V_s) - V_a . \tag{40}$$

(ii) Margin M_q^h, which prevents the breakdown of a shunt switch when node q is in the busy condition and is subsequently primed, i.e.,

$$M_q^h = (V_B - \Delta V_B) - (V_q - VK_q) - V_a .$$

From (32) and (38) this becomes

$$M_q^h = (1 - \beta)V_B - (1 + \beta)\Delta V_B - \beta\Delta - V_R - \Delta V_R + \left(\frac{n}{2} - q\right)(V_S - \Delta V_S) - V_a . \tag{41}$$

Margin M_q^c exhibits its worst conditions at node $q = 1$; M_q^h has its worst conditions at $q = n/2$. To optimize conditions, M_1^c is equated to $M_{n/2}^h$, yielding,

$$2V_R = (1 - 2\beta)(V_B + \Delta V_B + \Delta) + \left(\frac{n}{2}\right)(V_S + \Delta V_S) + r_0(I_p + \Delta I_p). \tag{42}$$

As before, V_R is most independent of device parameters if $2\beta = 1$ and, under these conditions,

$$2V_R = \left(\frac{n}{2}\right)(V_S + \Delta V_S) + r_0(I_p + \Delta I_p), \tag{43}$$

and the worst margin becomes

$$M_1^c = M_{(n/2)}^h = \tfrac{1}{2}V_B - \left[\tfrac{3}{2}\Delta V_B + \tfrac{1}{2}\Delta + \Delta V_R + \tfrac{1}{2}r_0(I_p + \Delta I_p) + \frac{n}{4}(V_S + \Delta V_S)\right] - V_a . \tag{44}$$

If the overvoltage is considered a necessary margin and is equated to the margin in (44), the worst margin is

$$M = \tfrac{1}{3}V_B - \left[\Delta V_B + \tfrac{2}{3}\Delta V_R + \tfrac{1}{3}r_0(I_p + \Delta I_p) + \frac{n}{6}(V_S + \Delta V_S)\right] - \tfrac{2}{3}V_a . \tag{45}$$

As a numerical example, consider such an internally marked network employing neon gas breakdown switches. For such a device,

$$r_0 = 5000 \text{ ohms},$$

$$I_p = 10 \pm 3 \text{ milliamperes}.$$

Using the previously given values for the other parameters, the margin M vanishes when $n = 1.5$ stages. This would then appear to be no im-

provement on the end-marked network. For an internally-marked network using devices with smaller values of V_S and I_ρ, full benefit may be taken of the principal advantage of the internally-marked system — the saving in current fanout between successive stages.

From the foregoing discussions, it is possible to arrive at certain conclusions from a switching margin viewpoint concerning desirable switch characteristics. These are listed below.

(a) All margins would be considerably improved if the ac breakdown voltage used in the calculations were equal to the nominal dc value. This would require the switch to take all transient voltages without exhibiting any loss in V_B.

(b) The margins improve as the variations in the switch parameters, ΔV_B and ΔV_S, are reduced. This requires a close supervision of the acceptable limits placed on switch characteristics during manufacture, together with minimum deterioration in the lifetime of their application.

(c) The overvoltage, Δ, required to assure breakdown of the switch either subtracts from the margins or may be considered to be a margin in itself. For gas diodes the speed of switching depends on the overvoltage, and so a compromise must be made between margin and speed. For the p-n-p-n switch the speed limitations due to overvoltage limitations are inconsequential, so that the overvoltage requirement is small.

(d) The power consumed in maintaining a switch in its "on" state depends on the minimum sustaining current, I_0, and the sustaining voltage, V_S. Consequently, a low value of I_0 and V_S will save considerably on the holding power drain.

(e) The forward and reverse impedance of the switch in "off" condition should be as high as possible. Then the impedance at idle nodes consists of the bias resistor connected to the idle bias potential in parallel with the impedance of multipled switches connected to other busy or idle nodes. If the multipled switches terminate at nodes that are not in the idle condition, leakage currents will flow into the node and alter the value of the idle potential. To prevent excessive variation of the idle bias voltage at a node (and hence deteriorate the margins) it is necessary that the "off" switch impedance be very much greater than the bias resistor. Both gas diode and p-n-p-n switches are expected to exhibit adequately high "off" impedance.

X. TRANSMISSION ASPECTS OF A BREAKDOWN CROSSPOINT SWITCHING NETWORK

The busy state of network nodes directly affects the switching margins. This is due to variabilities in the switch sustain potential accumu-

lating from stage to stage and to the amplitude of the speech signals which are transmitted through the paths. These and other interactions between switching and transmission states, as well as transmission factors *per se*, have largely determined the design choices. This fact distinguishes networks of this type from the electromechanical systems, where the switching and transmission factors are separate to a far greater degree and are of relatively minor importance as design limitations.

Discussion of transmission through the gas diode switching network starts with the *V-I* characteristic, Fig. 1. The intersection of the busy-state load line with the switch characteristic sets the operating sustain current at 10 milliamperes. At this current, the ac resistance of the switch is negative. The magnitude of the resistance, about 200 ohms, varies with the current, temperature, age of the switch and, in a way related to the temperature behavior, it varies with time over the first several minutes from the moment the path is made busy.

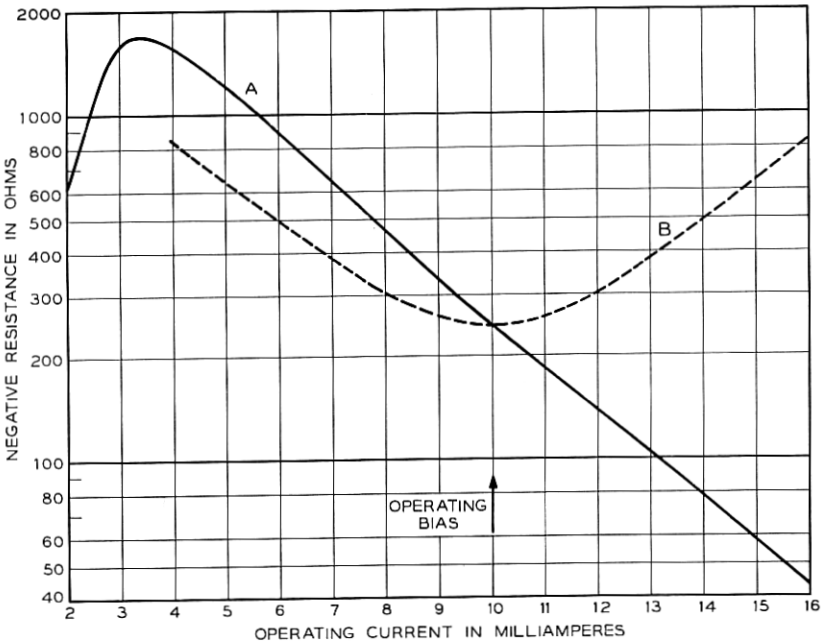

Fig. 7 — Variation of the A1624 gas diode negative resistance with operating current.

Curve A of Fig. 7 illustrates variation of negative resistance with current. The steepness of the characteristic at the operating point affects the design in two ways. First of all, it indicates that the source of holding current must be closely regulated, or variations in the negative resistance will occur from time to time as the power supply varies. These variations produce over-all gain variations which result, in one direction, in high transmission loss through the network and, in the other direction, in oscillations. The switch is useful as a series negative-resistance transmission element for compensation of the incidental series transmission losses elsewhere in the switching network, principally the copper loss of the coupling transformers. Gain compensation in this manner is analogous to the use of negative-impedance two-wire repeaters for trunk circuit loss compensation. The wide variability of the external terminations for the switching network indicates that the network transmission paths should be unconditionally stable between open or short circuit terminations. Excess positive resistance loss is designed into the transmission path to account for the maximum variations in positive and negative resistance and assured network stability. The greater these variations are, the greater must be the residual transmission loss. In an experimental six-stage gas diode switching network, the design value for the transmission loss is 1 db. This value also produces an optimum over-all return-loss characteristic, since the residual shunt and series losses are about equal and together represent a pad properly matched to the 2000-ohm network circuit impedance level.

The dependence of the impedance of the gas diode switch upon current passing through it has a second deleterious effect. Signal current variations produce distortion and, more importantly, if sufficiently large, they swing into the low-current high-gain region of the switch, with consequent instability. Both effects have been minimized in the six-stage network. A potential introduced at the center of the network supplies parallel-feed hold current to each pair of three oppositely poled stages of switching. Signal current flows through all six switching stages in series. Thus, as the signal current increases in three tubes it simultaneously decreases in the remaining three tubes. Compensating negative resistance variations are thereby introduced into the signal path. The resistance of a single tube may be expressed as $R(I) = R_0(I_0) + \Delta r(\Delta i)$, where $R_0(I_0)$ is the resistance at the bias current I_0, and $\Delta r(\Delta i)$ expresses the change in resistance produced by deviations in current from the bias value. The resistance of six tubes in a center-fed path is given by:

$$\sum_{6} = 6R_0(I_0) + 3\Delta r(\Delta i) + 3\Delta r(-\Delta i)$$

$$= 6[R_0 + \tfrac{1}{2}\Delta r(\Delta i) + \tfrac{1}{2}\Delta r(-\Delta i)].$$

To the extent that tubes are alike, an even-order balance is achieved. The effective resistance per tube is plotted as curve B of Fig. 7, which is a construction from curve A assuming a mean bias of 10 milliamperes and signal excursions about this operating point. The characteristic, parabolic in shape, results in an over-all increase in gain at the peaks of signal excursions and forces operating range limits of about ±3.5 milliamperes from a 10-milliampere bias. These current limits at the 2000-ohm network transmission impedance permit a maximum sine wave transmission amplitude of 12 milliwatts. The current limiting circuit in the junctor is biased to limit the current excursions to the ±3.5-milliampere value. This current swing produces a corresponding maximum signal voltage swing of ±7 volts at the terminals. The voltage clipper diodes in shunt with the transformer winding are designed to conduct at ±9 volts, just above the maximum signal. These diodes limit input signal amplitudes to values which can be transmitted. Their basic purpose is protection. In combination with the current-limiting feature, they prevent lightning and power faults from breaking down switches into existing network connections and from extinguishing paths which are present. Without this protection, early networks were sensitive to excessive signals; the paths were easily extinguished by extreme speech signal peaks.

Another significant characteristic of the gas diode switch is its transmission behavior as a function of temperature. Ambient temperature acts directly to change the negative resistance. In addition, temperature variations produce changes in the sustain voltage of the switch. These voltages, in turn, react to produce changes in the bias current of the held path, with resulting resistance changes already discussed. In addition to the effects of ambient temperature, the tube when operated dissipates about 1 watt, to produce a relatively large temperature rise in the first several minutes of operation. Both temperature effects were overcome by at all times maintaining about the switches a stream of air held at fixed temperature (±5 Fahrenheit degrees) and moving about 500 feet per minute. By this expedient the temperature of the tube is held within narrow limits. Fig. 8 shows the variation in the over-all six-stage network input resistance with time, with and without the benefit from moving air, from the moment of establishing a path. Curve B illustrates an increasing impedance with time corresponding to a decrease in the

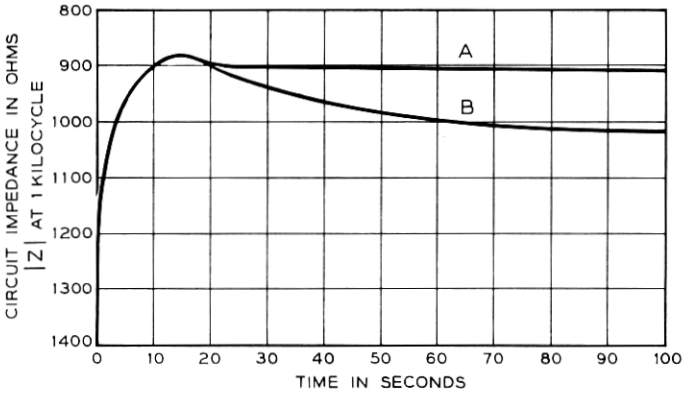

Fig. 8 — Starting circuit impedance transient due to the thermal properties of the A1624 negative-resistance characteristic: (a) air flow of 500 feet per minute across tubes; (b) tubes in stagnant air.

negative resistance of the gas diode switches as they heat in still air. Curve A corresponds with curve B but, in this case, with the use of a moving air environment. The expedient taken in this case to overcome the temperature characteristic is costly and was employed in view of the short time available. A promising longer range approach includes a better gas discharge characteristic and better packaging from a thermal point of view.

XI. CROSSTALK

The 2000-ohm network impedance level for the gas diode switching network is a compromise choice between insertion loss and capacity-coupled crosstalk among busy paths. Coupling among the busy paths is a special problem, since the switching network is unbalanced to ground. The ground plane within the equipment provides a common return circuit for all the path-terminating transformers. The coupling impedance of the common ground connection has not been a serious limitation. Mutual capacitance between adjacent circuits is the limiting source of coupling. It is minimized by switch designs which attempt to secure a maximum separation between adjacent circuits. The links between stages of switching necessarily are several feet in length and their large number necessitates relatively close spacing. In the present

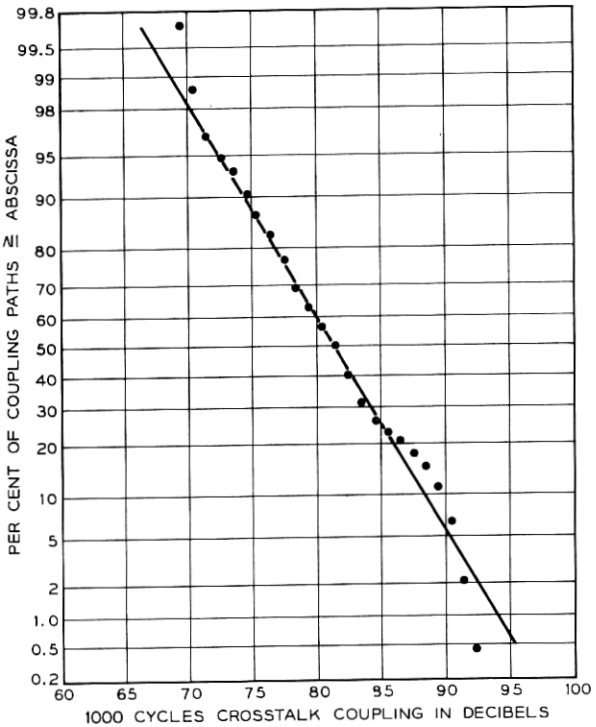

Fig. 9 — Distribution of crosstalk loss values for an experimental six-stage gas diode switching network.

design, direct coupling was reduced by the shielding effect of ground wires interspersed with the active leads. Factors of improvement of 3 to 10 are readily obtained with no more shielding than this.

At the 2000-ohm circuit impedance level, the mean path-to-path crosstalk loss achieved in the present design is about 80 db. Fig. 9 shows the distribution among paths to be nearly normal, with a sigma of 5 db. This performance is considered to be just tolerable and an improvement of 5 db is to be sought in subsequent designs. Higher circuit impedance would further aggravate the crosstalk problem and lower impedances will be beneficial. However, from the standpoint of insertion loss variations due principally to gas diode negative resistance variations, the situation is reversed. Higher circuit impedances will better absorb the switch impedance variations and lower impedance circuits would be more susceptible. For the experimental gas diode switching network, the impedance was set at 2000 ohms, as high a value as seems possible in terms of crosstalk performance.

XII. ACKNOWLEDGMENTS

The development of a multistage switching network is the result of the cooperation of many persons. The authors wish to express their appreciation for the contributions to this project by their many co-workers. In particular we wish to thank R. J. Andrews, R. Biddulph, K. S. Dunlap, L. W. Hussey, G. E. Jacoby, W. Peil, R. L. Simms and E. A. Woodin for their circuit contributions. Although the mechanical aspects of the experimental electronic switching system have not been discussed in this paper, the system itself would not have been possible without the mechanical design considerations of R. A. Billhardt, W. Hopf, J. H. Mogler, R. B. Mutke and L. J. Trimnell. The authors are also indebted to R. W. Ketchledge for his guidance and many valuable suggestions.

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