A High-Speed Barrier Grid Store

By T. S. GREENWOOD and R. E. STAEHLER

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This paper describes a high-speed random access memory developed to serve an experimental electronic telephone switching system. The memory uses a barrier grid type electrostatic storage tube which is incorporated in a complete general-purpose store with a capacity of 16,384 bits. Random access to any bit together with a full storage cycle of reading and writing is complete in 2.5 microseconds, permitting a 400-kc repetition rate.

Experience with this store indicates that barrier grid storage can provide stable, compact, economical memory for data handling systems.

I. INTRODUCTION

The last two decades have seen a phenomenal growth in the field of digital data handling systems of large capacity. Prior to 1940 the telephone central office contained the only large-scale systems to be found. Since that time the number of special and general-purpose computers has mushroomed and, at the same time, the demands on special data handling devices for such systems have become more severe. One of the more thorny problems has been that of providing adequate storage for the large amounts of information received and generated by the systems. Early systems effectively used electromechanical relays for information storage, but the demands for speed and economy have forced the system designer to go far afield in his search for satisfactory memory devices.

While many devices have been developed for memory purposes, each particular system has requirements which limit the choice to relatively few of them. Those systems having most severe choice limitations required a random access memory with very high-speed reading and writing. Prior to 1950 the choice was limited to some form of electrostatic storage tube. With the introduction of magnetic core storage the field was widened. Because of the discrete nature of its storage unit and the convenience for individual experimentation, the core became the focus of considerably more attention in recent years. In contrast, the

bulk nature of storage in tubes and the complex technology of such tubes required more extensive group efforts.

While widespread use of storage tubes has declined, the development of storage tubes and related techniques has continued and these tubes have retained a competitive position with cores. Storage tubes appear to have some advantage in speed and economy, while cores have a slight advantage in size and power consumption. Because these differences are small, the specialized requirements of a contemplated system may exert a profound influence on the choice of memory medium.

The form of electrostatic storage tube now most widely used is the barrier grid tube. Such tubes have been described by Jensen,[1] and Hines, Chruney and McCarthy.[2] They are fast, reliable and economical. This paper describes an unusually high-speed memory utilizing such a tube and is indicative of the barrier grid tube's present speed and capacity.

II. SYSTEM REQUIREMENTS

This store was developed to provide the erasable memory of the experimental electronic telephone switching system described in detail in a companion paper.[3] To serve this system, the memory was required to perform a complete memory operation (a random access plus a reading and writing operation) in 2.5 microseconds. Because of the nature of the system, large numbers of single-bit words were used and a serial memory was adequate for longer words. For this reason, the memory was designed to read or write a single bit at a time.

The limited nature of the system experiment and the use of large amounts of nonerasable memory reduced the erasable storage requirement to a few thousand bits. However, since a working telephone system would require considerably more memory with no essential change in other requirements, the store was designed to have as large a capacity as possible consistent with other requirements.

Because an inherent feature of barrier grid storage is the need for periodic regeneration of information, the store imposed some restriction on the system. A requirement of the barrier grid tubes used was that every bit in the memory be regenerated at least once each second. Because of interaction between adjacent storage locations, a somewhat higher rate of regeneration was required in most areas of the memory. This rate depends upon the performance level of the storage tube and the specific pattern of memory consultation. For the particular system using the barrier grid tubes available, a study indicated that no more

than 10 per cent of the working time of the system was needed for this regeneration. Since the system is a real-time data processer in which the full system time is used only during infrequent periods of maximum input data rate, the effect of regeneration time is very small.

Since the switching system did not provide common power supplies for its various units, the store was designed as a self-contained unit including power. Thus, the resulting store was a general-purpose memory which could be applicable to other data processing systems of a similar type.

III. DESIGN OBJECTIVES

The storage capacity of a barrier grid tube depends upon the combined analog resolving power of the tube and the deflection circuitry. With high-speed random access, the settling time of the deflection system usually sets the limit on resolving power. Since the desired memory required the deflecting of only one barrier grid tube, it was decided to devote sufficient effort to the deflection system design to achieve nearly the ultimate resolution of the tube. At the performance level needed, the capacity of the tubes was around 16,000 bits; accordingly, the capacity objective was a square array of 16,384 (128 × 128) bits.

Within the 2.5-microsecond cycle time imposed by the system, three separate store operations were required: beam deflection, reading and writing. The reading and writing durations were set by the tube design and at the capacity desired were 0.8 microsecond. With a 10 per cent design margin, the time remaining for deflection was 0.7 microsecond. Because of other requirements, it was necessary to deflect in somewhat less time and the design objective was from 0.4 to 0.5 microsecond. It is clear that any significant decrease in cycle time for the system requires faster barrier grid tubes; a 2.5-microsecond cycle is near the present practical upper limit.

To avoid excessive deviations in the duration of store operations, precise timing pulses were required within the store. The objective for these pulses was a single cycle of a squared 5-mc sine wave, which would give a pulse rise time of 0.05 microsecond. Since the inputs from the system were expected to be slower, input buffer circuits were provided. The pulse amplitude was set at a nominal 15 volts, with satisfactory operation at a 10-volt minimum.

At any designated location it was desired to have four alternative modes of operation. Each operation required the store to read and subsequently either (i) write a zero (WRITE 0); (ii) write a one (WRITE

1); (iii) write the same binary state as was read (REGENERATE); or (iv) write the binary state opposite to that read (REVERSE). Operations (i) and (ii) are the minimum necessary to provide storage. Because of the frequent occurrence of operations (iii) and (iv), it was observed that much system time could be saved by including the necessary logic for these operations within the store.

The functional block diagram of the store is shown in Fig. 1. The memory section contains the barrier grid tube and its associated dc control circuits. The deflection system contains all circuits necessary to direct the beam to the selected location and assure its proper focus. The control section contains the circuits which issue the proper sequence of pulses to execute the desired storage operation. The readout section provides gain and quantization of the readout pulses.

The implementation of the store operations requires pulses from the system on a selected set of 15 leads. The pulses on 14 of these leads define the binary state of a 14-digit binary number specifying the location of the bit. The remaining pulse, on one of four leads, specifies the storage operation to be carried out at the selected location. In normal operation, all 15 pulses arrive at the store simultaneously. However, proper operation of the store is achieved as long as no address pulses arrive in the 2.5-microsecond period following an operation order pulse. Each address digit is retained in the store until changed, so that the operation order will be carried out at the location specified by the complete set of most recent address pulses. Approximately 1.5 microseconds after the operation order, a readout 1 or 0 lead is pulsed by the store.

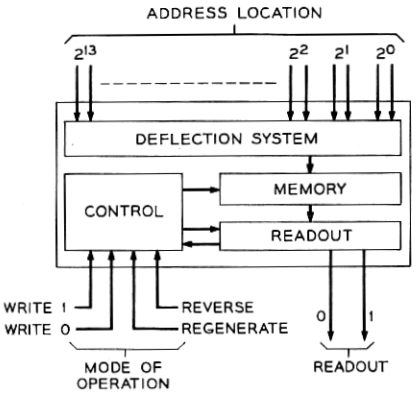

Fig. 1 — Barrier grid store system block diagram.

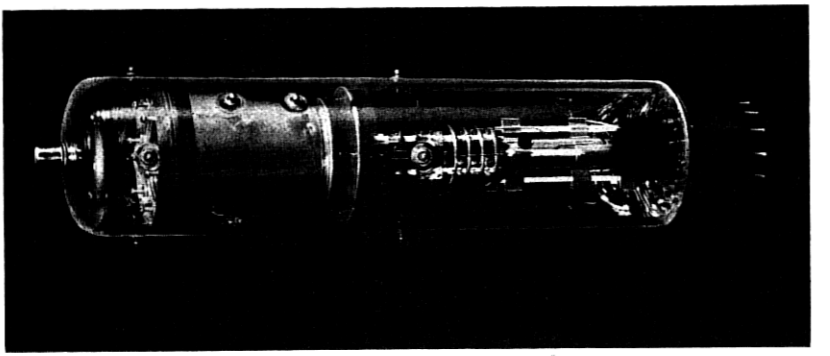

Fig. 2 — Barrier grid tube.

IV. SECTIONS OF THE BARRIER GRID STORE

4.1 *The Memory*

The storage tube used in the memory is similar to that described in detail in Ref. 2. It uses electrostatic deflection and focusing and operates at an acceleration potential of 1000 volts, but it differs from that tube in having a double focusing lens. The two control apertures of the lens have elliptical instead of circular shapes and are placed with their major axes at right angles. The lens is aligned with the deflection plates so that each aperture corrects, more or less independently, for the defocusing caused by a particular set of deflection plates. This type of structure facilitates the application of dynamic correction for deflection defocusing. A photograph of the tube is shown in Fig. 2.

The target structure of the tube consists of a mica sheet approximately 0.001 inch thick placed between a 500-mesh barrier grid on the gun side and a conductive back plate on the opposite side. The space between deflection plates and target is occupied by a conical electron collector assembly.

When the beam is directed at a point on the mica, the area under the beam charges to an equilibrium potential approximately equal to the fixed barrier grid potential. The potential thus obtained represents the storage of a binary 0. Writing a binary 1 is a similar process, except that a positive potential is applied to the back plate during the mica charging process. When the back plate potential is restored to zero after the charging, the capacitive coupling to the mica causes it to finally assume a potential more negative than the barrier grid, representing a 1.

Reading is accomplished by the same operation as writing 0. During

this process, the current flow away from the mica will depend upon whether the spot is already at equilibrium. Thus, there will be a different current flow for a 1 or a 0. This flow may be observed either at the collector or at the target (barrier grid plus back plate). The first method is called collector reading, and is used in this store. The second method is called target reading, and offers distinct advantages in signal uniformity and detection. Unfortunately, the current required to charge the back plate to barrier grid capacity for the write 1 process also flows in the target leads. This current is about one-half ampere, while the signal current is about one microampere. To maintain the desired cycle time of the store it is necessary for the readout amplifier to completely recover from the large writing pulse on the previous spot in about one-half microsecond. Ref. 2 describes a method of driving the back plate through a transformer wound with coaxial wire, which would reduce the interference from 500,000 to about 20 times the readout. Although this method holds considerable promise for the future, the residual recovery time problem was still a deterrent to its use in the present store.

With collector reading, both the 1 and 0 signal are of the same polarity and the 1 is 30 to 50 per cent larger than the 0. To decide whether a given readout is a 1 or a 0 requires an amplitude discriminator. With a fixed discrimination level, variation in the 0 amplitude over the surface represents a noise component. This is discussed by Hines under the subject "shading". In the tubes used, the construction was carefully controlled to minimize shading.

A figure of merit used for these storage tubes is the read-around-number (RAN). This refers to the number of complete storage operations* that can be carried out at a storage location without causing erroneous readout from an adjacent location. For any particular tube, the RAN figure of merit is the smallest such number obtained by testing all locations and all combinations of interfering and adjacent spots. Such a figure of merit gives an indication of how many times a spot may be used before its neighbors must be regenerated. In the tubes used the RAN was greater than 50 at full storage density.

The interaction effect of spots more distant than one unit may be expressed by a similar RAN, but it is found that this interference very rapidly becomes independent of distance. Thus, in the tubes used it was found that approximately one million operations in spots more than

* A compiete storage operation is any of those defined in Section III. This definition gives RAN's which are approximately one-half of those obtained using the definition given by the IRE Standards Committee on Electron Tubes.

three or four units removed from a given spot could be tolerated before errors occurred. These errors are caused by very small scale effects, such as reflected high-speed secondary electrons and positive ions.

To prevent errors from this cause, a requirement was imposed on the system to insure that each spot was used or regenerated at least once each second. At a 2.5-microsecond cycle time, this limited the maximum number of distant interferences to 400,000. In addition, the system was required to regenerate more frequently any spots that had high adjacent-spot interference.

4.2 *Deflection System*

The deflection system receives at its input a 14-digit binary number. It must convert this number into two analog voltages whose values are proportional to the binary numbers obtained by dividing the input number into two 7-digit numbers. These two voltages, applied to the deflecting plates of the tube, provide 128 discrete levels of beam position in each orthogonal axis. Since the adjacent spot interference depends upon accurate beam positioning, a high order of accuracy must be maintained in the conversion process. An error greater than 0.1 spot is deemed inadmissible for maintaining high RAN in the store. This means that in a jump from the lowest level to the highest level (128 spots) a positioning accuracy of better than 0.1 per cent is required.

The maximum regeneration interval of one second eases the accuracy requirement on slow drifts, since the regenerated array can move on the surface of the target. However, to avoid the necessity of extra target area, long-term drift must be minimized.

The requirement of 0.1 per cent accuracy has an important bearing on the attainable deflection speed, since the beam cannot be turned on until the deflection voltage has settled to within the 0.1-spot limit. To meet the design objectives, this must occur within 0.5 microsecond. If the voltage approaches its final value exponentially, this is equivalent to a 0.2-microsecond rise time in conventional terminology. Because of unavoidable overshoots, the amplifier must, in practice, be at least twice as fast. At the opposite end of the frequency spectrum, the response must extend to dc because, with random access, the store may operate almost continuously at any place on the storage surface.

Since accurate focusing of the beam is required for high RAN, the deflection system must have a minimum effect on focus. This requires, first, that the deflection plate voltage be applied in balance across the deflection plates to assure constant average potential between them.

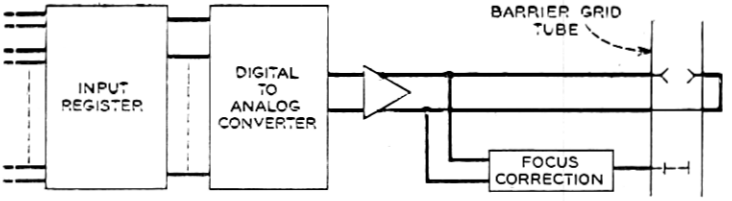

Fig. 3 — Deflection system functional diagram (one axis).

This alone is insufficient, and correction must be made for the remaining defocusing caused by the lens action of the deflecting plates, using circuitry which develops a voltage proportional to the square of the off-axis deflection. This voltage is then applied to the appropriate focusing electrodes. With the independent control in each axis offered by the double-focus lens, spot size can be held to a 30 per cent increase in the corners.

The circuit of each axis of the deflection system consists of four main parts, as shown in Fig. 3. The input register consists of flip-flops which convert the incoming pulse into binary dc levels. These levels actuate the digital-to-analog converter to produce a low-level analog signal proportional to the input binary number. These analog signals are amplified and applied to the deflecting plates and the focus correction circuit.

The register flip-flops are identical to those shown in a later section

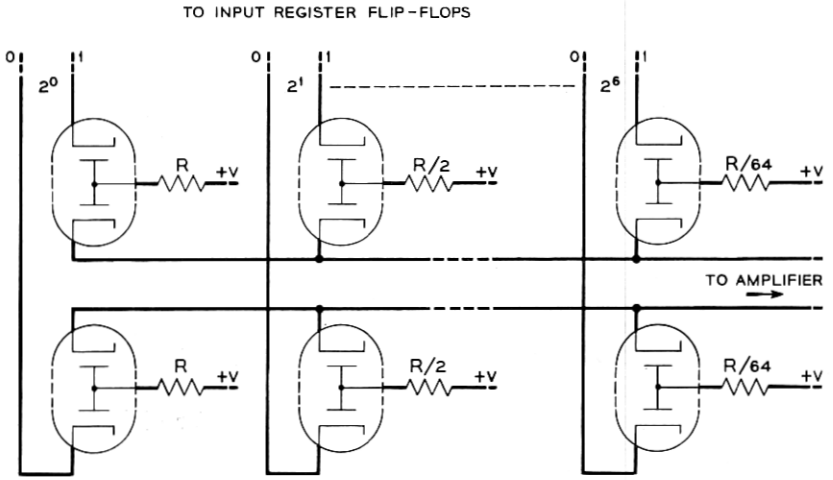

Fig. 4 — Digital-to-analog converter schematic diagram.

and are conventional Eccles-Jordan type with cathode follower outputs. They each drive an input of the digital-to-analog converter whose circuit is shown in Fig. 4. This is a well-known circuit in which there is a current established by each resistance from a common supply. The current may flow into the low-impedance lead to the amplifier or back into its respective flip-flop. The potential at the junction of each diode pair is held to within a volt or so of ground, while the supply voltage, $+V$, is approximately 100 volts. This means that there is essentially a constant current in each resistance and residual inductance effects are minimized. The action of the converter is to switch a number of these binary-weighted currents into the input leads to the amplifier, where they add to produce the desired analog voltage across the input resistance of the amplifier. To meet the required balanced output voltage, both sides of the flip-flops are used to create complementary currents in the two output leads.

The accuracy of the converter depends on the accuracy of the resistors and the power supply. The latter must be well regulated, to at least 0.05 per cent over a one-second period and better than 1 per cent over longer periods. The resistors, chosen for good high-frequency performance, are carbon film types and are not a factor in short-term drift. However, their long-term drift is important, particularly if they do not all drift equally. This could cause crowding of lines and columns of the storage array and serious degradation of RAN.

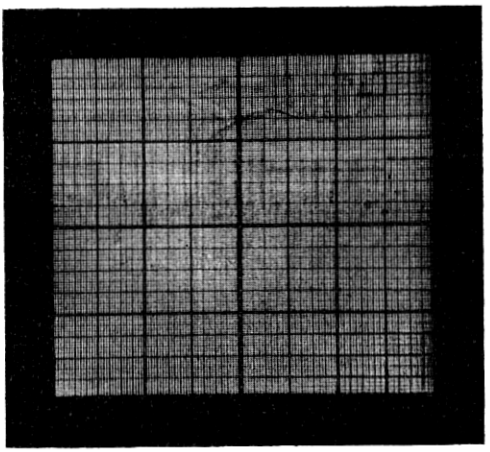

Fig. 5 — Barrier grid tube storage raster showing "plaid" pattern for drift protection.

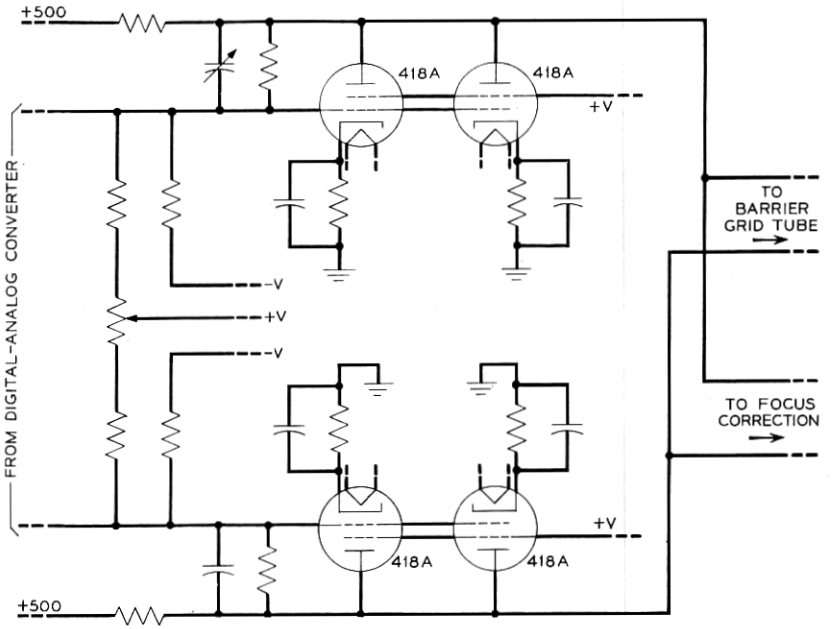

Fig. 6 — Deflection amplifier schematic diagram.

In order to permit some drift, the resistors were chosen with a weighting ratio of 2.02 between digits instead of 2.0. These result in a plaid pattern, as shown in Fig. 5, which occupies a square approximately 8 per cent larger than a linear-spaced array with the same minimum spacing. However, a ± 1 per cent drift in the resistors is allowed before the minimum spacing is exceeded. Generally, this much protection is more than adequate, since the resistors tend to drift in the same direction.

The output of the converter drives an amplifier whose simplified schematic is shown in Fig. 6. To stabilize the gain of this amplifier, feedback from grid to plate is used. This also provides the necessary low-input impedance required by the converter circuit. The output of the amplifier drives the deflection plates of the barrier grid tube directly. To allow for differing deflection sensitivities, the effective converter supply voltage is variable. Centering is accomplished by differential current injection at the amplifier grid. The total swing at each deflection plate of the tube is about 75 volts, centered at 145 volts. To achieve optimum focus, the average value of the plates is adjustable by means

of the bias supply voltage ($-V$). This supply, like the converter supply, must be well regulated.

To achieve an over-all deflection rise time of 0.1 microsecond with negligible overshoot requires careful layout of the output circuit to minimize stray capacity. It was for this reason that size and centering were placed in the grid circuit. Careful adjustment of the feedback capacitors permits the overall deflection system to achieve rise times of 0.08 microsecond and to settle to within 0.1 per cent of final value in 0.5 microsecond.

The defocusing caused by the full beam deflection requires correction at the focus electrodes. Ideally, the correction should vary as the square of deflection deviation; in practice, a power term whose exponent lies between 1.5 and 2.5 is equally satisfactory. For this reason, the correction is developed by using the approximate multiplicative action of grids on beam current in multigrid tubes. The circuit of Fig. 7 has input pentodes whose control and suppressor grids are driven by the same signal. Each deflection plate drives such a stage and outputs from corresponding plates are added. The result is very closely parabolic and

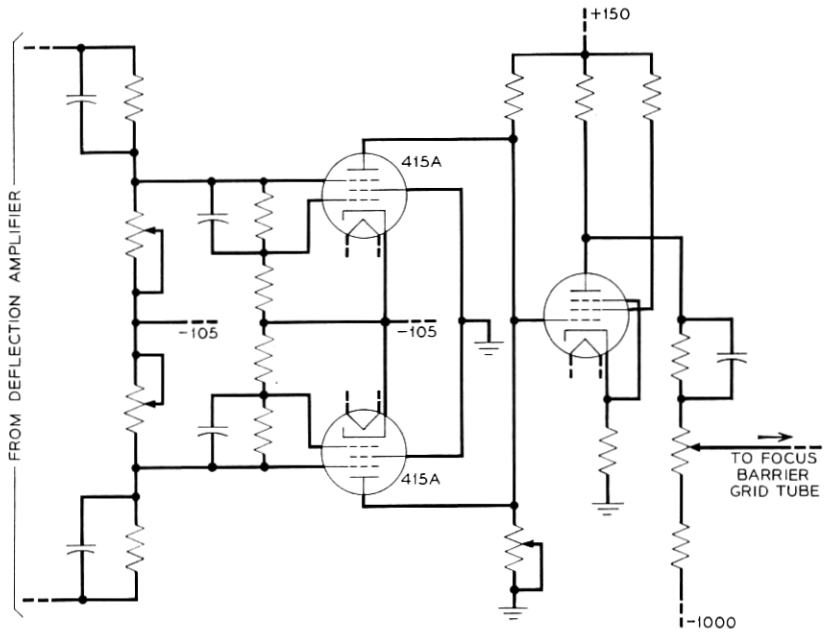

Fig. 7 — Focus correction schematic diagram.

symmetric about the center of deflection. Further amplification is necessary to provide the required correction amplitude.

4.3 *Control System*

During a storage cycle the change of deflection plate potential and focus correction must be completed before the beam is turned on. As previously indicated, a 0.7-microsecond period is allowed for this action. When this interval has elapsed the beam is turned on, with the back plate at its lower potential (the backplate is normally held at this potential). This action (see Fig. 8) constitutes both a reading and a writing of a 0 and occupies 0.8 microsecond. During this period, the output current from the collector is sampled to determine the value of the spot stored and, at the end of the period, the spot has been written to a 0. Up to this point, the action is identical for all operational modes. During the succeeding 0.8 microsecond the action depends on the particular polarity required in the write operation. The circuit may either remain idle and leave the 0 just written, or the beam may be turned on and the backplate potential raised, writing a 1.

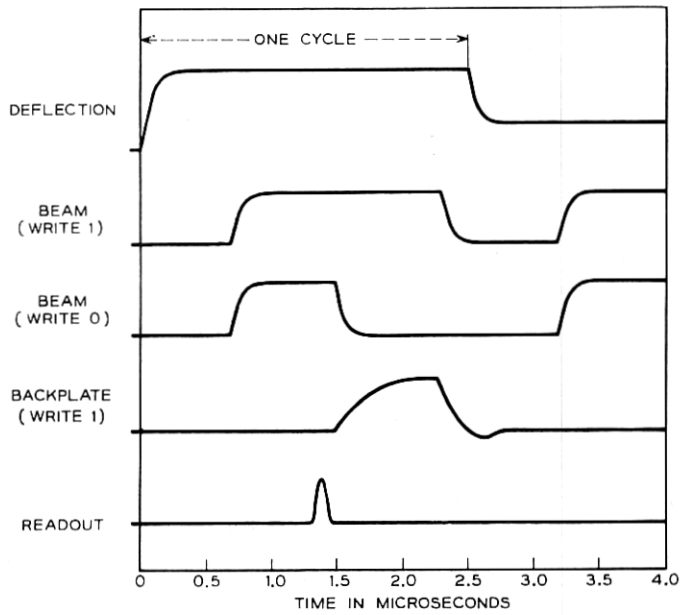

Fig. 8 — Timing sequence.

It is the function of the control circuit to time and initiate these actions, using the circuit whose simplified schematic is shown in Fig. 9. The circuit is constructed of logical gates, passive delay lines and flip-flops. Delay-line losses are made up by gate circuits (which have gain stages) either in conjunction with their normal logical function or, in some cases, specifically for gain purposes. Gates in the latter class have been omitted from the schematic.

There are two basic gate units providing the logical "or" and logical "and" functions; their circuits are shown in Fig. 10. They consist of a basic-pulse gain stage preceded by a logic stage. The basic output pulse is of 0.1-microsecond duration and uses 100-ohm terminated pulse cables with low-impedance delay lines. The output transformer of each unit acts as a reshaper and provides a uniform pulse shape throughout the system.

The flip-flop circuit is shown in Fig. 11. This same circuit is used in both the deflection registers and the control circuit.

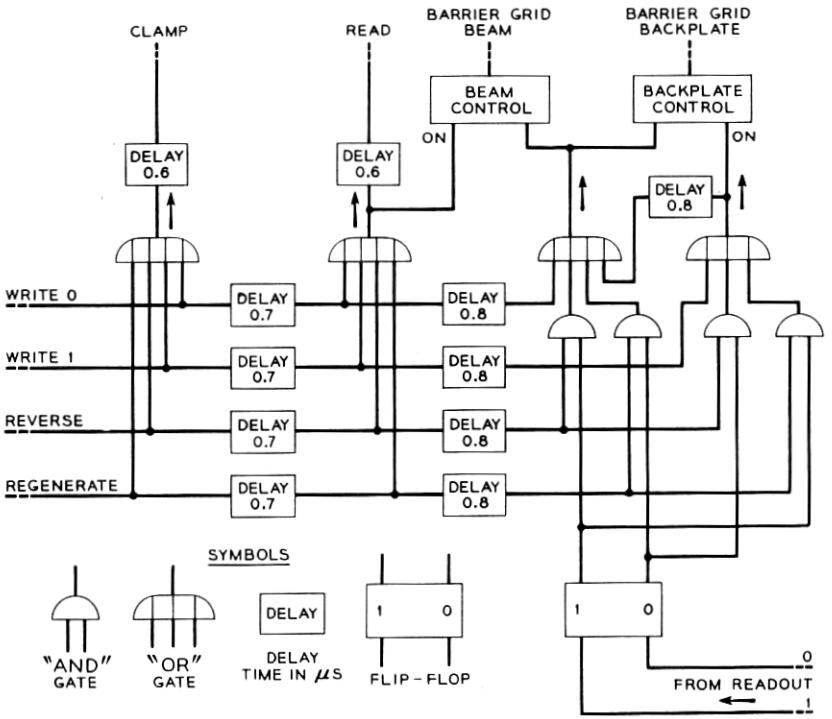

Fig. 9 — Logic of control section.

There are two special circuits in the control circuit which are used functionally as flip-flops but whose special requirements dictate a circuit different from that just given. These are called drive circuits. A common simplified schematic is shown in Fig. 12.

These circuits are required to drive an essentially capacitive load from one voltage level to another. The change must be rapid and operate on the receipt of a "set" or "reset" pulse. Normally the circuit is in its lower voltage state and is driven to its upper level for only short periods of time. Due to the essentially nondissipative character of the load, current is required from these circuits only during the transition from one level to another. However, to achieve the required rise and fall times (typically, 0.3 microsecond for a 50-volt transition across 2500 micromicrofarads at the back plate) the peak currents required are of the order of one-half ampere.

Tube V_3 acts as a cathode follower and in response to a "set" pulse provides a large pulse of current to cause a positive-going transition. Because the load is capacitive, it remains at its upper potential after

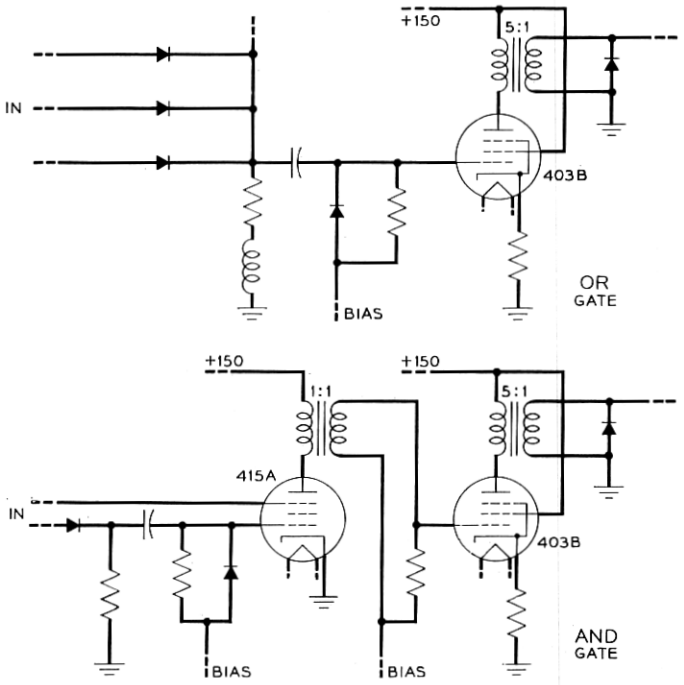

Fig. 10 — Logic circuit schematics.

V_3 is biased off. When a return to the normal lower potential is desired, V_4 is pulsed to discharge the load. This tube must discharge the load sufficiently to allow V_3 to become biased on and assume control of the output voltage.

To assure that the output current does not drift upward during periods of idleness, a constant drain current is provided by V_5. The width of the system pulses are insufficient to insure current flow during the entire transitions, so these pulses are stretched by the input diodes and grid capacity and are clipped and amplified by V_1 and V_2.

In the specific circuit for driving the back plate, the load is sufficiently large to require doubling V_3 and V_4. In the case of the grid-drive circuit, single tubes are adequate, but the lesser capacitance results in considerably more droop along the top of the pulse. Since proper operation of the barrier grid tube requires this top to have very little droop, the actual output is severely clipped by the circuit of Fig. 13 before it reaches the

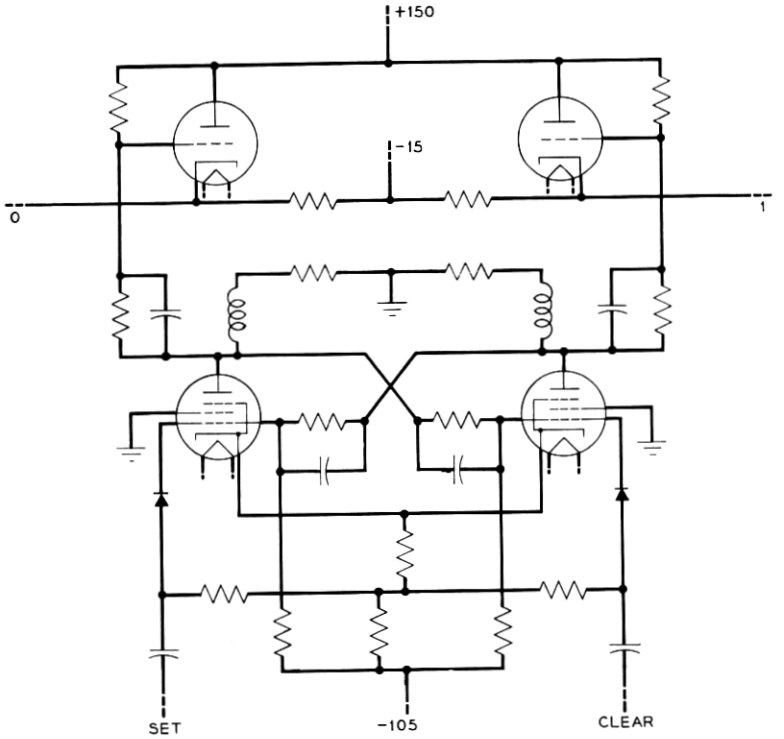

Fig. 11 — Flip-flop circuit schematic.

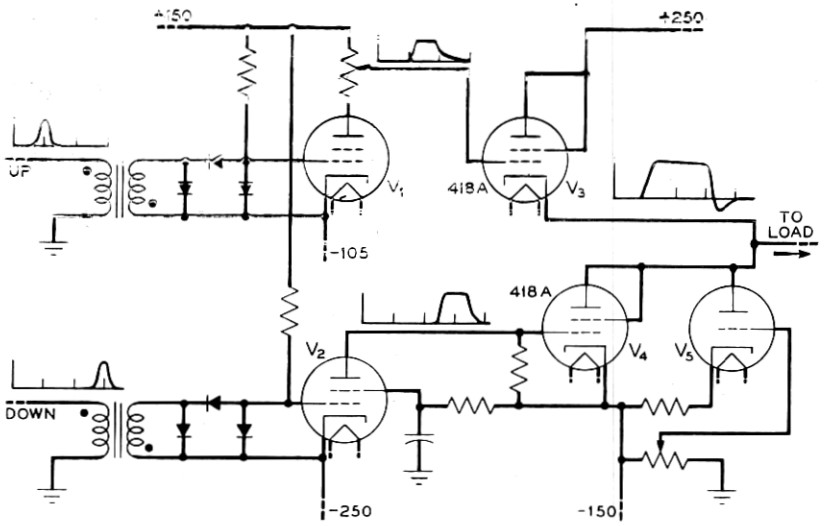

Fig. 12 — Driver circuit simplified schematic.

grid. This circuit clamps the grid to either -1000 volts or to $-V$ volts. The cathode bias is adjusted so that when the grid is at -1000 volts the beam current is at the desired value. The supply, $-V$, is adjusted to insure the tube is cutoff when the grid is at $-V$ volts. This method of clipping provides a fairly simple circuit, but a change in operating beam current requires a change in cathode voltage, with a resulting change in accelerating voltage and deflection sensitivity. In practice, the usable range of beam currents can be achieved by a change in accelerating potential of less than 2 per cent. For most adjustments of current this does not require readjustment of deflection.

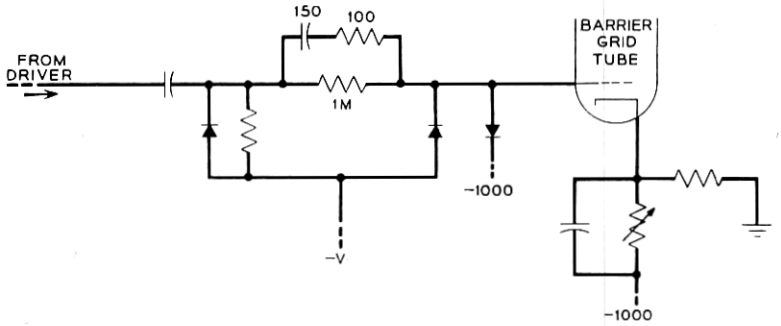

Fig. 13 — Beam drive clamp circuit.

4.4 *Readout Section*

The output current of the collector is of the order of 1 microampere. Since the required rise time of the output voltage and the collector and wiring capacity limit the load resistor to 2 kilohms, a voltage of 2 millivolts represents the available output signal. Of this, only about one-third represents the difference between 1's and 0's. Amplification must be provided to achieve satisfactory discrimination between these two states.

Unfortunately, both 0 and 1 signals have a dc component which depends upon duty factor. To make the proper discrimination, this dc component must be preserved in the amplification process. At these input levels and bandwidths (the amplifier rise time is 0.3 microsecond) stable dc amplification is not achieved simply. Fortunately, the waveform is such that an ac amplifier followed by dc restoration may be used. The schematic of the amplifier is shown in Fig. 14. The signal output of the amplifier for several conditions is shown in Fig. 15.

Each figure shows the superimposed readouts from all spots in the store. Since the pattern of 1's and 0's in the store formed a checkerboard, half of the readouts represent 1's and half represent 0's. The central 2.5 microseconds of each sweep represents a complete storage cycle

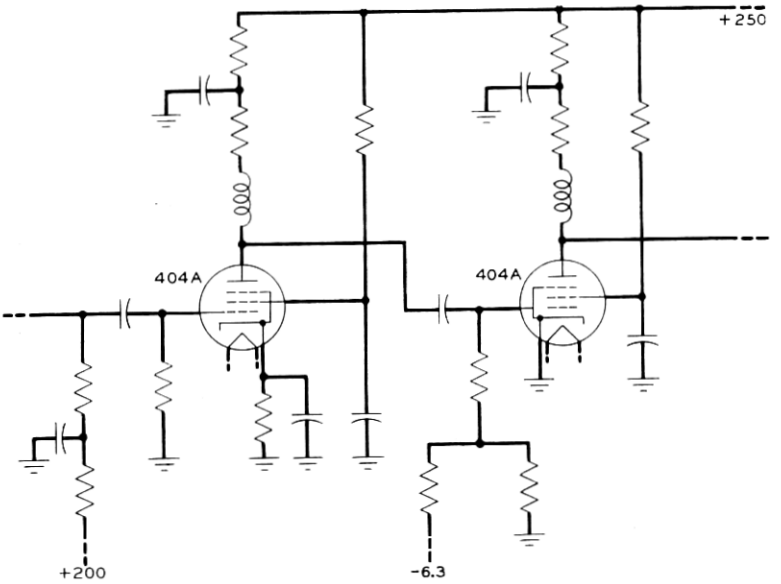

Fig. 14 — Readout circuit input section.

consisting of deflection (D), reading (R), and writing (W). This is most clearly seen in Fig. 15(a), where the store is operated at a low repetition rate. In Figs. 15(b) and 15(c) the repetition rate is 400 kc and the noise from the writing in one cycle extends into the deflection period of the next cycle.

During the period R the differing traces represent the 1 and 0 readouts and the amplitude must be sampled during this period. The store delivers a 1 output pulse only if the signal is more negative than approximately −3 volts. In Fig. 15(b), where no dc restoration is provided, the effect of the higher repetition rate can clearly be seen to be essentially a shift in the dc level of the readouts, and the preceding discriminator would not indicate the presence of 1's. Since all traces in Fig. 15(b) coincide just prior to readout, the voltage at this point may be clamped to the same value (0 volts) it has in Fig. 15(a), and the result is shown in Fig. 15(c). Here it can be seen that the discriminator will give the correct

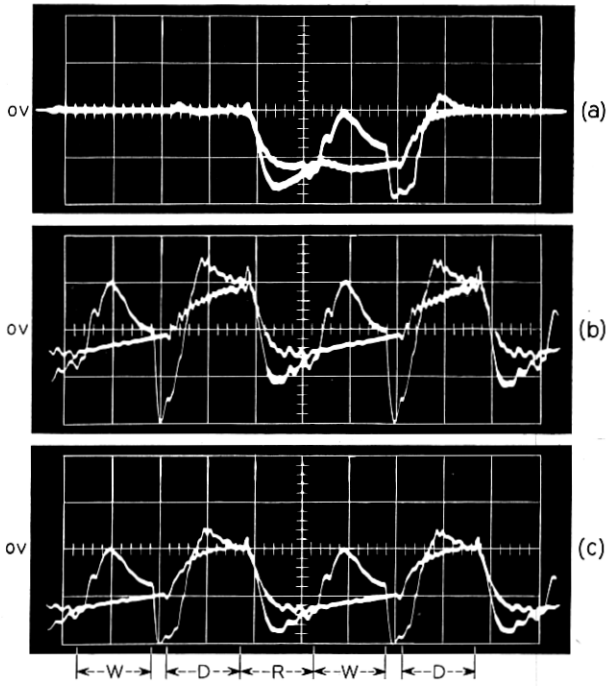

Fig. 15 — Signal outputs from readout amplifier: (a) low repetition rate; (b) high repetition rate without clamp; (c) high repetition rate with clamp. Horizontal scale, 0.5 microsecond per division; vertical scale, 2 volts per division. D = deflection; R = read; W = write.

readout. The actual sample of the readout is taken at the center of the trace and is about 0.1 microsecond in duration. The apparent improvement in the separation at this point in Fig. 15(c) relative to Fig. 15(a) is due to a favorable interference pattern and, in practice, the levels are essentially identical between low-frequency and high-frequency operation.

These views of the readout indicate that a more favorable sample might be taken earlier than at the time indicated. Unfortunately, it is difficult to reproduce marginal 1 signals photographically, and these do not show the large separation from the 0's early in the readout period. The optimum time in an actual store is determined by adjusting for best RAN, and it is close to the indicated time in all tubes.

The clamping circuit and amplitude discriminator are shown in Fig. 16. Vacuum tube diodes were used to achieve fast clamping with minimum loading. The amplitude discriminator consists of a cathode follower driving a grounded grid amplifier through a series diode. This configuration has proved to be very accurate, stable and fast, and it has a large overload capacity. However, since it is not regenerative it must be

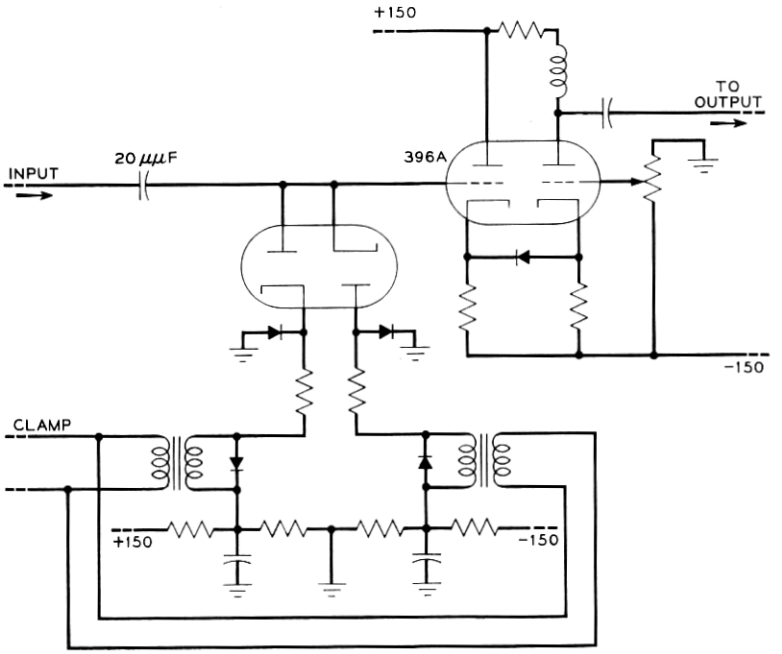

Fig. 16 — Readout circuit clamp and discriminator section.

followed by considerable gain. This is shown in Fig. 17. The first stage is straightforward voltage gain, followed by a regenerative phase splitter. This circuit has characteristics similar to a Schmidt trigger circuit,[4] but, since the feedback is ac coupled, there tends to be a small amount of turn-off delay. This is minimized by limiting the amplitude of the feedback. This stage drives a pair of diode AND gates which are sampled at the appropriate time by the control circuit to generate a 1 or 0 output.

4.5 *Equipment*

In packaging the various circuits which constitute the store several objectives were sought. It was desired to evaluate the problems existing in an actual telephone system where continuous operation is mandatory. Clearly, continuous operation requires the system to have standby

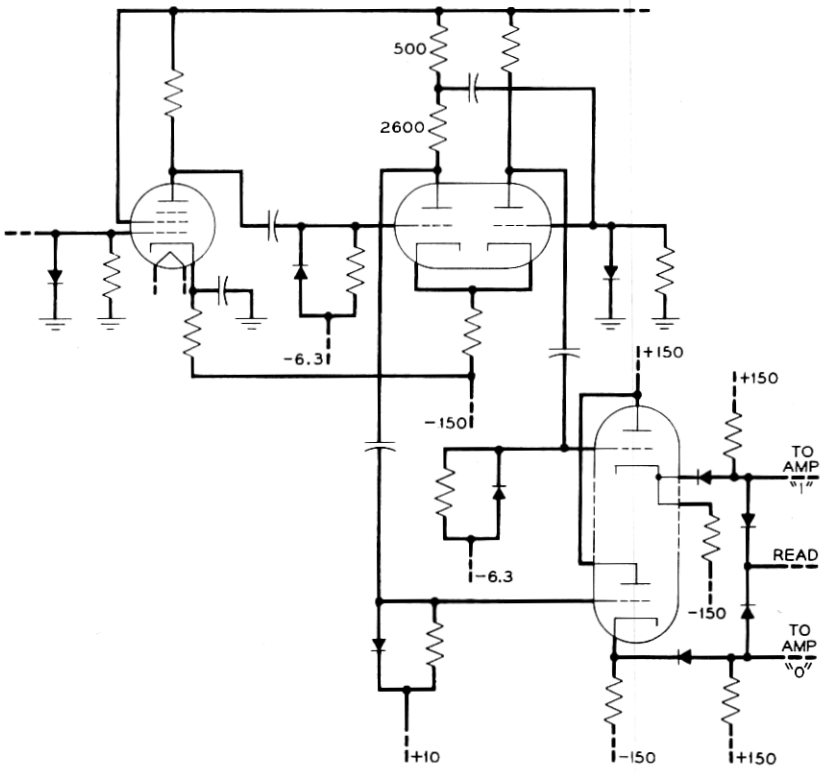

Fig. 17 — Readout circuit output signal generation.

storage facilities. Since the amount of such storage depends upon the expected out-of-service time of faulty stores, the stores must be arranged for simple and rapid maintenance and repair. To assure this, practically all components were included in plug-in packages. Exceptions to this rule were made in the case of highly reliable elements such as delay lines, but in general the only fixed elements in the store cabinet were wiring and connectors.

The control section and part of the deflection system readily divide into small functional units which may be packaged conveniently, but the other sections of the store cannot be so readily separated. If their breakdown is into rather small units, stray capacitance due to extra inter-unit wiring presents a problem in keeping within the cycle time. Too large a unit imposes a mechanical problem and tends to require excessive spare equipment. However, what proves to be the governing consideration is the need for grouping all alignment controls and their circuits on a single plug-in unit so that store realignment is not necessary when a package is replaced. The alignment controls in the store include adjustment for deflection size and centering, focusing correction and level, beam current, output gain and discrimination level and a few dc parameters of the storage tube. The number of these adjustments requires this one package to be relatively large.

This package, called the barrier grid tube unit, is shown in Fig. 18. It includes the barrier grid tube and its dc circuitry, the deflection amplifiers, the focus correction unit and the readout section. Fig. 18(a) shows the partially assembled unit with the barrier grid tube centrally mounted in a Mu-metal box for magnetic shielding. Electrostatic shielding is obtained from the copper mesh placed directly around the tube. The deflection amplifiers are mounted on either side of the tube outside of the shields, and they are wired directly to the deflection plates. In the forward left-hand corner is the focus correction unit. In Fig. 18(b) is shown the unit with the Mu-metal cover and complete readout section in place. Fig. 18(c) shows the fully assembled unit. For installation, the unit rests on drawer-type slides in the center of the store.

A view of the full store is shown on the left side of Fig. 19. Below the barrier grid unit is the remainder of the deflection section. The individual flip-flop units are on the sides, while the digital-to-analog converter is in the center. The latter is a single unit that plugs into the rear of the store. Above the barrier grid unit is the control section. The uppermost unit is the combined grid and back plate drivers.

The small functional packages in the control circuit and deflection

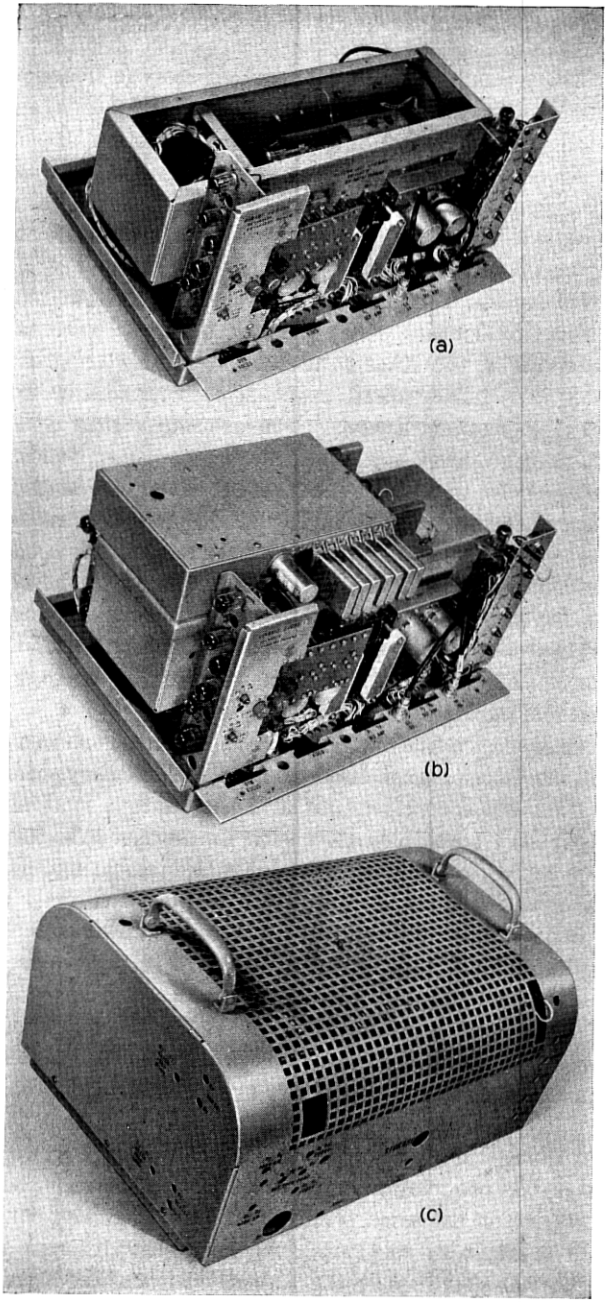

Fig. 18 — Barrier grid tube unit: (a) mounting of barrier grid tube; (b) unit without cover; (c) fully assembled unit.

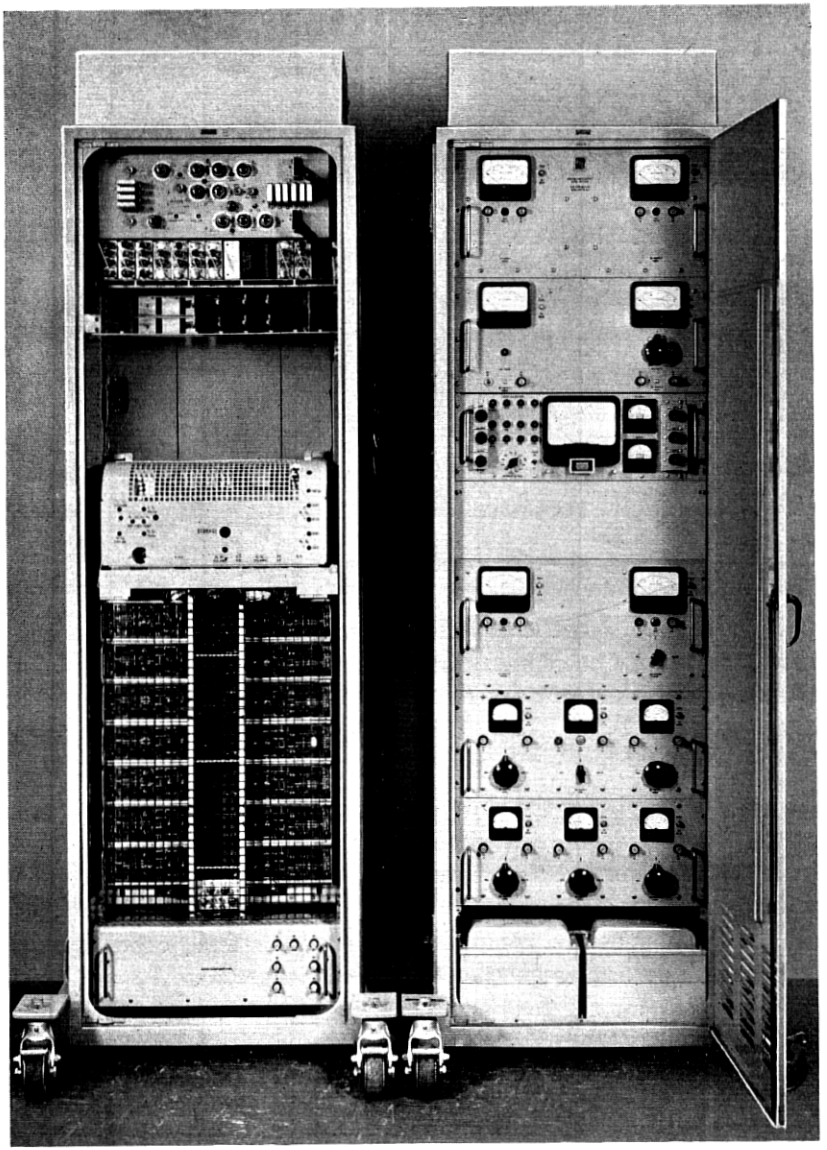

Fig. 19 — The barrier grid store, left, and its power supply, right.

input register are shown in Fig. 20. These are the gates and flip-flop circuits. Three types of mechanical designs were used for evaluation purposes. All used printed wiring, but various amounts of mechanical

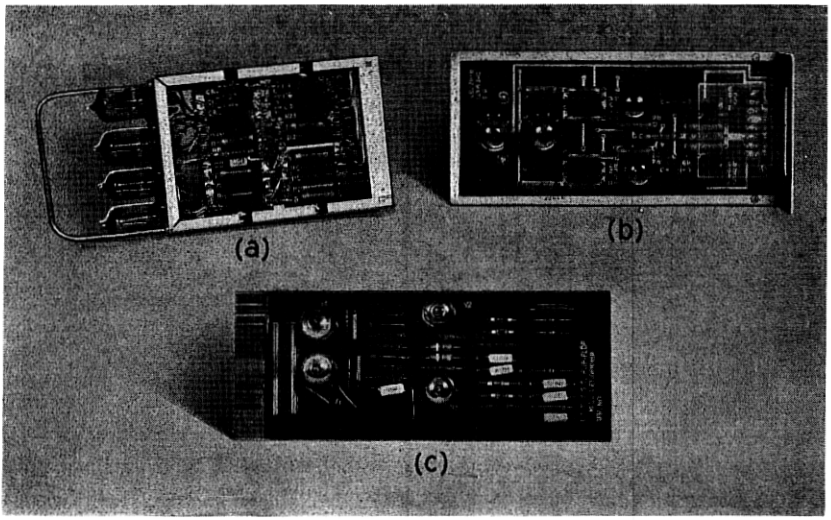

Fig. 20 — Construction of small packages.

support were used. Experience has indicated that in the relatively non-severe type of usage encountered in this type of system a self-supporting card of type (c) is entirely satisfactory.

4.6 *Power Supplies*

The power supply for the store is shown on the right side of Fig. 19. Twelve voltage levels are used. Eight of these, which supply 75 per cent of the dc power, are simple rectifiers achieving ± 2 per cent regulation through line voltage regulation of ± 1 per cent in resonant regulators. The remaining power is supplied by electronically regulated supplies meeting ± 0.5 per cent regulation for periods longer than 1 second and ± 0.05 per cent for shorter periods. The total dc consumption of the store is 500 watts.

In addition to the dc power, a filament supply of 220 watts is required. Although these power requirements are quite modest, a largely transistorized version of the store would offer significant power economy. Such a version appears to be feasible with transistors now available.

V. OPERATING EXPERIENCE

The laboratory operating experience with two stores over a combined time of 10,000 hours has been very favorable. The most difficult operating

aspect has been that of initial alignment. The operator has under his control about a dozen parameters which he must initially optimize for system operation. The general alignment procedure which has evolved is first to adjust size, shape and centering of the deflection raster. This presents some problems because the raster is not directly viewable and the effective edge of the storage area is not exactly definable. The usual procedure is to define the edge by, say, a 20 per cent reduction in a 1 readout. This permits the deflection sensitivity to be measured and the shape and centering and approximate size to be set. The "correct" size may be set later during more sensitive tests.

For setting focus and discrimination it is necessary to have test equipment available which will evaluate RAN (or an equivalent figure of merit) both at a point (or over a small area) and over the entire storage surface. The focus correction can then be determined by optimizing small-area RAN at the center and four sides. For setting the actual dc level of focus, it is preferable to use an over-all RAN, since focus should be optimized at the point of lowest RAN. Likewise, the discrimination level should be set for optimization of over-all RAN. The actual alignment procedure can be mechanized. However, the alignment procedure was an important consideration in the original store design since an unwanted interdependency of adjustments might have seriously complicated the procedure.

Once aligned, the store requires little further adjustment. The stability of alignment has proven very good with respect to both continuous operation and package replacement. Prealignment of a spare barrier grid unit is entirely practical, although a slight amount of touch-up alignment is usually done after replacing this package. The only drift effects that have proved noticeable have been from changes in storage tube beam current. These, however, are easily corrected by periodic observation and minor adjustment. No other drifts of important magnitude have been apparent. Observations on one store over 2500 hours showed a drift in raster position of only one spot.

The RAN's that have been obtained for the store are in the range of 50 to 60 at the worst areas of the surface. These are generally the edges and corners, and RAN's of 150 are more common for most spots. No changes in storage characteristics have been noted over periods of several thousand hours. While cathode life would thus seem to be the main factor in limiting the life of the tubes, the small numbers of tubes used and the short periods involved have not permitted a complete evaluation of expected life.

For the store as an entity, a measure of reliability would be desirable. Such measures are difficult to obtain and are often of nebulous meaning,

but, to the degree that they establish bounds, they are nonetheless useful. For the store described, tests were carried out in which known storage patterns were regenerated for long periods of time. From such tests, the store, its power supplies and its test equipment appear to have an error rate of approximately 1 to 2 errors every 24 hours, or about 1 error in 10^{11} operations. At this low rate, protection of important information which must be held for long periods can be assured by single error-correcting codes.

VI. SUMMARY AND CONCLUSIONS

Using a single barrier grid tube, a complete self-contained data storage unit has been achieved. The unit has a 16,384-bit capacity, and an access to any bit, including reading and writing, may be made every 2.5 microseconds. While the specific unit was designed for serial operation, its high input impedance makes paralleling of stores straightforward. Regeneration is necessary, but the interaction between spots is low and not more than 10 per cent extra system time is required.

The store has a volumetric efficiency of 4 cubic inches per bit (inclusive of power) and a power efficiency of 45 milliwatts per bit. As a measure of economy, the component count (tubes, resistors, condensers, diodes, transformers, switches, sockets) indicates a usage of approximately 0.1 unit per bit, of which only 10 per cent are active elements. Actual operation has indicated good stability and reliability.

In the field of random access memory for data handling systems, barrier grid tubes can provide high-speed memory with moderately large capacity per tube. The resulting stores are economical and offer considerable promise for future electronic telephone switching systems.

VII. ACKNOWLEDGMENTS

As with any project of this nature, many persons have been involved. We especially acknowledge the efforts of C. F. Ault, S. J. Dudek, R. M. Genke and J. A. Ruff for circuit contributions and E. Ley for mechanical design. The encouragement of R. W. Ketchledge has been invaluable.

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