Semiconductor Circuit Design Philosophy for the Central Control of an Electronic Switching System

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The advent of electronic switching has necessitated a considerable number of changes in the circuit design philosophy employed in the electromechanical switching art. The invention of the transistor and the refinement of other semiconductor devices have made possible new techniques. This paper discusses the philosophy of circuit design for the central control of an electronic switching system. Primary emphasis in the designs has been low cost consistent with good margins, reliability and the meeting of systems requirements.

I. INTRODUCTION

The proper selection of semiconductor switching circuits to be employed in electronic switching systems is influenced by a large number of different factors. Some of these are the result of systems philosophy,[1] while others are concerned with device availability, required reliability, economy and ease of design, manufacture and maintenance, etc. We do not propose to go through an exhaustive design analysis of the circuits described herein, but we shall present the techniques which were developed.

The particular experimental electronic switching system of interest here operates with a stored program in real time and in a generally synchronous serial mode, utilizing direct-coupled (dc) logic. The largest concentration of semiconductor circuitry is in the central control of the system, which is the data and information processing center of the telephone central office. It is with the circuits in the central control that this paper is mainly concerned.

In most present-day electromechanical switching systems many operations take place in parallel, due to the speed limitations of relay circuits. Electronic switching systems also can be built using the parallel

building block approach, but significant savings in quantities of apparatus are possible if serial operation is employed. The serial mode, however, makes it necessary for the processing equipment to operate at much higher speeds. In fact, for the particular electronic system under consideration, it is necessary for a program order to be executed in a few microseconds if the office is to handle the telephone traffic properly.

Although most parts of the electronic switching system operate in a serial mode, the central control itself operates in a parallel mode. The speed limitations of available semiconductor devices and circuits are a contributing factor to this choice. However, the program order structure, the manner in which information is stored in the system and the way in which the central control affects the operation of the other major system blocks in the office are of even greater importance in the selection of the parallel mode. It should be noted, however, that in receiving address words from the barrier grid store some serial-to-parallel conversion equipment is required, since this memory furnishes information only one bit at a time.

The central control operates in a generally synchronous manner, using a single-phase clock having a frequency of several hundred kilocycles. However, the synchronous circuit actions are controlled by some asynchronous logic circuits which can stop the clock when certain delays are encountered in system functions, and then restart it. After the clock has been restarted, it runs at a constant rate. The design of synchronous circuits is somewhat more economical in equipment and lends itself more readily to the automatic checking features employed in this system.

The logic circuitry of the central control is direct-coupled (dc), that is, signals are represented by steady-state voltages. Two levels are employed, one representing a binary 1 and the other a binary 0. The memory elements used are flip-flops with double-rail output signals to drive the logic circuits. A double-rail output is one in which both the logical 1 and 0 conditions are represented by active signals on separate leads. Only one of the two leads, however, has an active signal at any time. The use of dc circuitry avoids a design problem implicit in ac circuitry. In order to obtain the AND function in an ac system, precise coincidence is required of pulses applied to an AND gate. Since delays are encountered as a pulse progresses through the logic, the design of circuits which will cause all pulses to be propagated to the right place at the right time can be quite complex. In order to make signals coincide exactly in time, extensive use of precision delay apparatus and multiphase clocks is generally required. The ac system also lacks a certain amount of flexibility, since the addition of any function generally requires the overhauling of

other sections of the logic in order to maintain the proper signal coordination. With dc circuits, on the other hand, unequal chains of logic may exist with no particular problems. Since both flexibility and economy are of importance in an electronic switching system, the dc mode was chosen.

To a major degree, the advent of electronic switching was made possible by the invention of the transistor and the refinement of other semiconductor devices. The required logical functions are highly complex and necessitate thousands of active devices in the central control. Before the development of the transistor, hot-cathode vacuum tubes were the only available active elements for use in high-speed switching systems. The inherently high-power-consuming vacuum tubes require relatively high-cost circuits for adequate reliability, and this makes the vacuum tube unsuitable for large-scale electronic switching applications. However, semiconductor devices of moderate cost have the high reliability, high speed and low power consumption required for large-quantity use in such systems. It is believed, from the evidence so far available, that the reliability of the transistor and semiconductor diode will be orders of magnitude better than that of vacuum tubes performing comparable functions.

After deciding upon the use of semiconductor devices and synchronous dc circuitry in the central control, several other general decisions remain to be made. It is possible, if one is not concerned with the amount of equipment involved, to reduce all information-processing circuits to two tandem stages, an AND and an OR. However, two-stage logic is generally nonminimal. The use of multistage logic results in a reduction in the equipment needed for simple circuits and in even greater savings in complex circuits. However, a longer time is required for the logic operation, since information is passed through more stages and the delay time of the signals will increase with the number of stages. Greater attenuation of the signals also will occur. Therefore, in multistage logic an economic balance must be achieved between equipment savings and the cost of additional time. This balance limits the minimization of the logic circuits.

Another approach which leads to a less costly design, although perhaps to more circuit elements, is the development of universal circuit packages. The use of such universal packages in the central control is made possible by distributing amplification throughout the logic. These subjects are more fully covered in Sections III and IV.

The use of these packages has allowed a separation between logical and circuit design. The building blocks can be treated as black boxes by

following a few simple interconnection rules, thus considerably reducing the over-all design time. The circuits have also been designed to be consistent with marginal and diagnostic testing techniques developed for the system.

II. SEMICONDUCTOR DEVICES

Transistors and semiconductor computer diodes were specifically developed for this electronic switching system. While the central control is the major user of these devices, they are also employed in large numbers in other portions of the system, such as the switching network and scanner. In order to develop units of high reliability and to obtain the economic benefits of high-level production, it was felt necessary to minimize the number of designs and codes for the system. Therefore, the device characterizations represent a compromise among all possible uses in the system and, as such, are not necessarily the best for any individual application. The over-all benefits obtained from a smaller number of codes, however, more than compensate for this disadvantage.

The transistors employed in this electronic switching system are a complementary pair — an n-p-n and a p-n-p designed for medium power and relatively high-speed switching applications. The transistors are capable of dissipating 450 milliwatts in free air at 25°C without the use of an external heat sink. In general, the logic circuits use the tran-

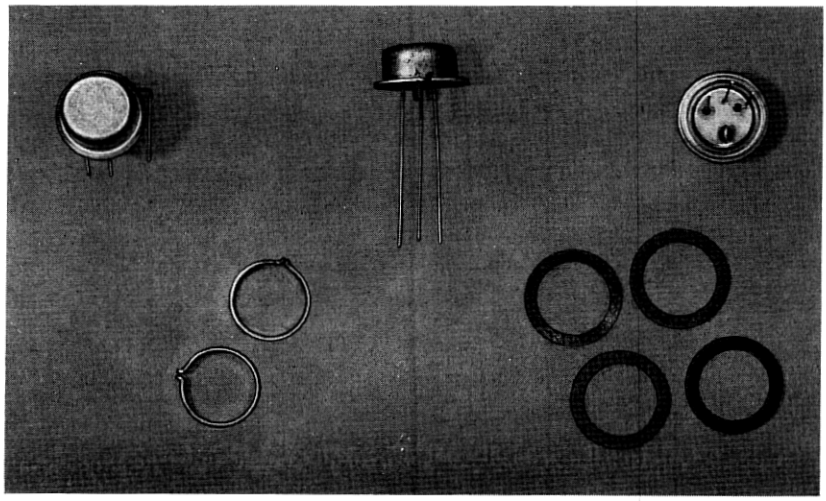


Fig. 1 — Germanium alloy junction transistor for electronic switching system central control.

TABLE I— TRANSISTOR CHARACTERISTICS

Parameter	Limits	
	n-p-n Transistor	p-n-p Transistor
Collector breakdown voltage	30 volts min.	30 volts min.
Emitter breakdown voltage	25 volts min.	25 volts min.
I_{co} at 15 volts (25°C)	35 μa max.	15 μa max.
Punch-through voltage	25 volts min.	25 volts min.
Common emitter current gain		
I_c = 25 ma; V_c = 1 volt dc	50 min.	50 min.
I_c = 150 ma dc; V_c = 1 volt dc	25 min.	25 min.
Collector capacitance at 4.5 volts	45 $\mu\mu$f max.	45 $\mu\mu$f max.
Inverse gain bandwidth (IGB)	0.25 μsec/cycle max.	0.25 μsec/cycle max.
Power dissipation, free air 25°C ambient	450 mw	450 mw

sistors well below their power rating in order to obtain satisfactory system reliability. Fig. 1 is a photograph of the transistor, and Table I lists its important electrical characteristics, for both n-p-n and p-n-p.

These characteristics are self-explanatory except for inverse gain bandwidth (IGB). This is a measure of switching speed and is related to the normal $f\alpha$ measurement for transmission applications. The main difference between the transmission and switching fields lies in the conditions of operation. In the transmission field (for other than power amplifier applications) a bias point is chosen and small excursions are made around this point. In the switching field, the whole operating region is traversed, and the effective values of the parameters are obtained by integration over this region. Although the parameter $\alpha_n\omega_n$, the gain-bandwidth product of the transistor, is useful in both fields, in transmission this parameter is a function of the chosen bias point, while in switching this parameter is a weighted average taken over the whole range of bias points traversed, and properly should be labeled $\overline{\alpha_n\omega_n}$.

A corresponding method of measurement must be chosen, such as putting the transistor in a standard switching circuit and arranging to measure $\overline{\alpha_n\omega_n}$. One way this can be done is to compare the output waveform in a sufficiently low-impedance circuit with a waveform derived from a simple RC integrating circuit. The low-impedance circuit eliminates effects of collector capacitance; the use of the same voltage supply cancels the effect of voltage variations.

It can be shown that the quantity $\overline{\alpha_n\omega_n}$ is inversely proportional to the RC product if the initial slopes of the rise portions of the pulses at the outputs of the transistor and RC circuits are matched. In the actual measuring apparatus, a further factor of 2π has been introduced and

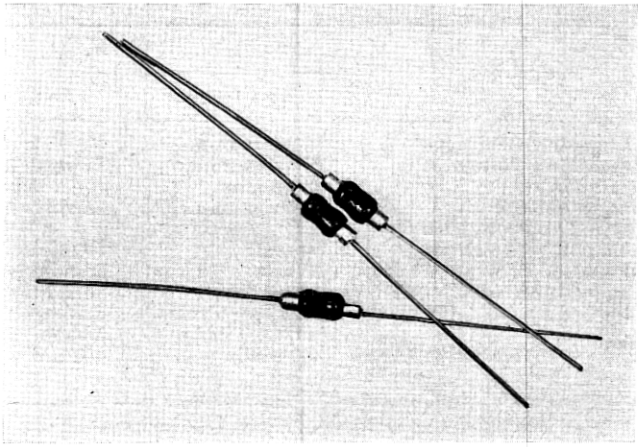


Fig. 2 — Germanium point-contact diode for electronic switching system central control.

the quantity $1/\alpha_n f_\alpha$ is read directly. This is called the inverse gain-bandwidth product or IGB and is measured in microseconds per cycle. Where $\alpha_n \cong 1$, as it is for these transistors, IGB is approximately equal to $1/f_\alpha$. Therefore, the upper limit of IGB, 0.25 microsecond per cycle, roughly corresponds to an average f_α over the active region of 4 mc minimum.

Two codes of semiconductor computer diodes have been developed for the logic and switching circuits. Both are glass-enclosed, hermetically sealed, point-contact germanium diodes (Fig. 2). One of these units has a higher forward conductance and is used in AND gates, where the series voltage drop is of more importance. The other diode has better reverse characteristics and is used in OR gate applications, where the effect of leakage currents has a greater effect on circuit operation. Both diodes have maximum ratings of 100 ma steady-state (dc) forward current with a peak surge-current limit of 500 ma. The maximum inverse working voltage is 100 volts. Maximum power dissipation at an ambient temperature of 25° C is 200 mw, with a derating factor of 3 mw per degree C for ambient temperatures above 25°C The other relevant characteristics of these diodes are given in Table II.

III. TYPES OF SEMICONDUCTOR LOGIC CIRCUITS

There are two general requirements which must be placed on a logic gate. The first is that the state of the output of the gate must depend in

TABLE II — DIODE CHARACTERISTICS

Electrical Requirements at 25°C	Code 1	Code 2
Max. forward voltage drop at 20 ma	1.5 volts	1.2 volts
Max. reverse current at −5 volts	2.2 μa	4.5 μa
Max. reverse recovery time	0.06 μsec.	0.06 μsec.
Max. inverse voltage	100 volts	100 volts

some logical sense on the states of the inputs. The second is that each of the inputs must remain free to change state independently of the states of the other inputs, i.e., the logic gate must maintain isolation between the inputs.

It is convenient to classify the various methods of constructing physical embodiments of logic gates in terms of the devices used to obtain the isolation of inputs. These devices constitute a very large percentage of the equipment required for a logic system, since at least one device is required per input. There are two common methods of obtaining this isolation in semiconductor logic circuits, one using diodes and the other using transistors. These are referred to as diode logic and transistor logic circuits.

Diode logic circuits have been chosen for use in the central control. This decision was reached because semiconductor diodes at the present time are considerably less expensive than transistors, are capable of operating at higher speeds, and have achieved better reliability. The use of transistors in the central control has been restricted to amplification and memory functions, so that approximately seven times as many diodes as transistors are used.

IV. DIODE GATES

Two-input conventional diode AND and OR gates are illustrated in Fig. 3. Additional inputs could, of course, be added. The logical function performed by each of these circuits depends on whether the high signal voltage (V_1) or the low signal voltage (V_0) is considered to be the active,

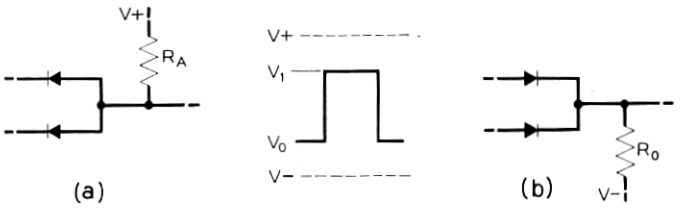


Fig. 3 — Conventional diode gates: (a) AND gate; (b) OR gate.

or 1 condition. These conventions are referred to as "positive" logic and "negative" logic respectively. In the central control, positive logic is used, i.e., the higher voltage condition is considered the 1 state. It is obvious that, if this convention is adopted, the circuit in Fig. 3(a) performs an AND function, since the output will be clamped to the lowest input voltage and, hence, a coincidence of high signals is necessary at the inputs to give a high signal at the output. The circuit in Fig. 3(b) can be seen to perform an OR function, since the output voltage will be high if any input voltage is high. Note that the inputs in both circuits can be at either level, independent of the states of the other inputs, because of the nonlinear characteristics of the diodes.

For reasons of economy, the central control uses multistage logic, i.e., many gates occur in tandem between the input and output of the system. Furthermore, the complicated logical functions to be performed often make it necessary for a gate to drive several other gates in parallel. This "branching" is commonly referred to as "fanout." As will be seen below, these features of the central control greatly complicate the use of diode gates.

A diode gate in a multistage logic circuit normally has its inputs driven by gates and its output used to drive a load consisting of other diode gates. In order to provide the desired output voltage and current levels when a gate is activated, it is necessary to select a resistor which will be the correct value for the particular load impedance which this gate must drive. In complex circuits such as the central control the selection of the proper resistor for each gate becomes a very complicated procedure. Also, many different types of gate designs are usually necessary.[2] This means that many different types of packages must be manufactured and many varieties of spare packages must be kept on hand for adequate maintenance. In addition, a single change may require redesign of substantial parts of the logic. Thus, such a system is difficult to design and has serious economic disadvantages.

Another factor makes the use of a multistage diode logic system undesirable. Since diode gates contain only passive elements, the logic signal is attenuated as it proceeds through tandem stages. To minimize this attenuation and to account for the signal power lost due to fanout, the impedance levels of the stages must be increased in successive stages. Thus, the problems of signal crosstalk and loss of high-frequency response due to stray wiring capacitance will increase in the later stages and can seriously limit the operating speeds of the system.

The use of transistor amplifiers in conjunction with the diode gates alleviates many of these problems. Such amplifiers are used in the central control and make possible the use of standard gates (gates whose resistor

values need not be tailored to the application) to construct relatively low-impedance, high-fanout, multistage logic circuits.

Amplification can be inserted into the logic chains at various points. It is possible to provide amplifiers either for each logic stage or only at other selected locations. In the central control, amplifiers are provided after every OR gate. In this particular system, many more AND gates than OR gates are required and thus fewer amplifiers are necessary if they are associated with OR gates. The use of amplifiers with every OR gate, rather than only in selected spots, makes possible the design of very flexible diode gates, as will be described below. This choice of amplifier location results in two stages of logic (one AND-OR cycle) between amplifiers, although several AND gates can be used in series, as can several OR gates.

The electronic switching system's versions of the conventional diode gates of Fig. 3 are shown in Fig. 4(a). The resistor R_0 on the conventional OR gate has been included in the amplifier which always follows an OR gate. The resistor R_A of the conventional AND gate has been removed and has been replaced by individual resistors on each OR input. These

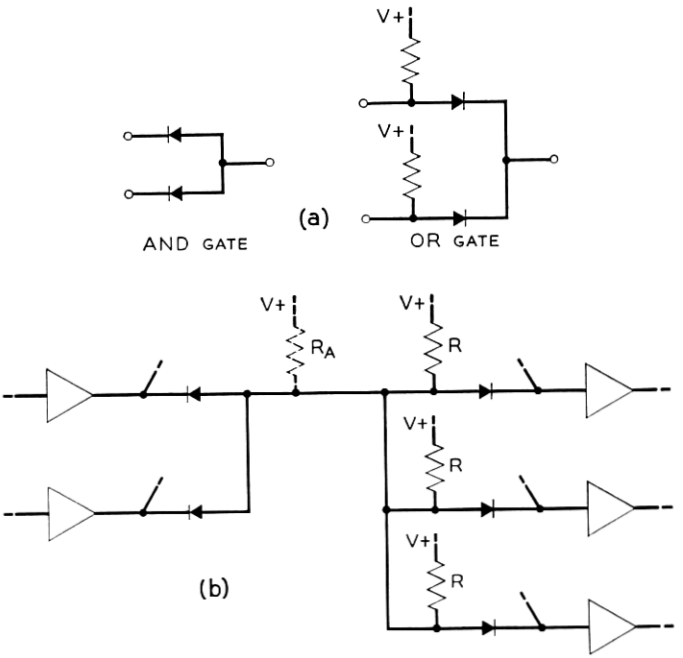


Fig. 4 — (a) Diode gates for central control; (b) interconnection pattern for diode gates.

individual resistors perform the same function as R_A but automatically give the correct equivalent resistance value for driving the load regardless of the degree of fanout. This is illustrated in Fig. 4(b). If a single resistor R_A were used, its value would necessarily be changed for different numbers of loads on the AND gate in order to provide efficient amplifier operation. The slight extra cost of the added resistors is more than compensated for by the increased ease of design, the reduction in the number of types of packages and the increased efficiency of the amplifiers.

The use of the individual OR input resistors also makes possible the use of a very efficient decoupling gate. The necessity for such a gate can be seen by considering Fig. 5(a). When two or more OR gate inputs are activated from a common point, the input current which each load will receive depends on the relative input impedances and threshold voltages of these loads. For instance, if $R_A < R_B$ and $V_A < V_B$, load A will receive most (or all) of the current from both input resistors A and B. The use of the decoupling gate [see Fig. 5(b)] prevents the flow of current between the input gate resistors A and B, and thus insures that each load will get the total output current of its associated gate resistor regardless of its input impedance or threshold voltage. The OR gate loads are al-

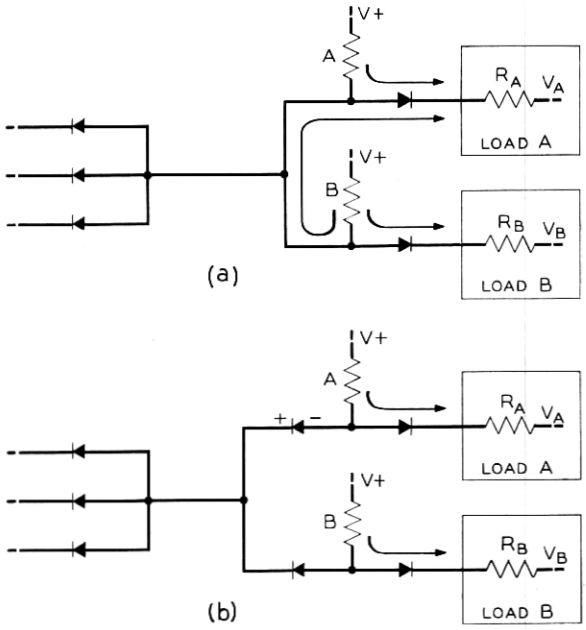


Fig. 5 — (a) Drive distribution problem; (b) use of decoupling gates.

ways transistorized packages in the central contol. The use of the decoupling gate allows the design of low-input impedance transistor circuits for maximum efficiency of operation and also allows the use of different input thresholds if desirable.

From Fig. 4(b) it can be seen that AND gates can be used in series without affecting the correct operation of the system. Also, OR gates can be used in series if input resistors are used only on the first stage. The use of gates in this fashion is often desirable to save diodes and is permitted in the central control, although it increases the logic signal voltage loss and, therefore, increases the voltage gain required of the amplifier.

The operating currents and voltages for the circuits must be determined before a decision can be made on the maximum number of OR inputs to be allowed. To be able to select operating currents and voltages, it is necessary to make engineering estimates of the effects of these levels on device and circuit reliability, operating speed and economy. In this system, the characteristics of the transistors and diodes are quite influential in the selection of operating levels. The OR gate currents are roughly 5 ma and the maximum transistor currents are 100 ma. The maximum reverse voltages applied to devices are less than 20 volts for diodes and well below the breakdown voltages for transistors. These levels allow the devices to be operated well within their ratings to insure long life. The resulting impedance levels are low enough to obtain sufficient switching speeds and tolerable crosstalk levels.

A limit of 20 inputs has been placed on the OR gate. This is necessary because the leakage currents through the diodes of all inactivated inputs will subtract from the current supplied to the amplifier by the activated

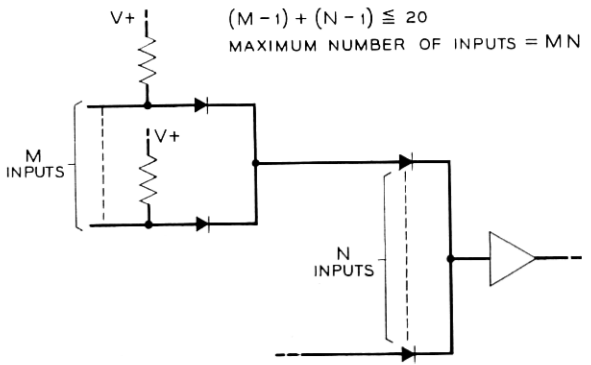


Fig. 6 — Use of series OR gates to extend the number of inputs.

input. By the use of OR gates in series, larger numbers of inputs can be obtained without increasing the number of shunting diodes. An example of how this can be done is shown in Fig. 6.

V. FACTORS IN THE DESIGN OF TRANSISTOR CIRCUITS

In the design of dc transistor amplifiers for logic circuits, it is convenient to use the transistors as switches. By utilizing the nonlinear characteristics of a transistor switch, many of the adverse effects of device parameter variation on correct amplifier operation can be greatly reduced. Before proceeding with the description of the actual circuit designs, some of the basic large signal properties of junction transistors will be summarized.

The use of a transistor as a switch[3] is illustrated in Fig. 7. From the characteristic curves it can be seen that the transistor can operate in one

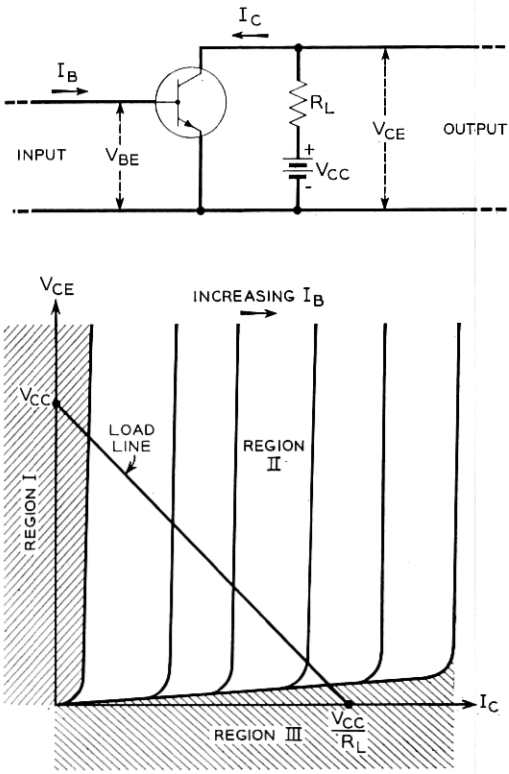
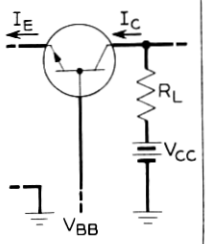
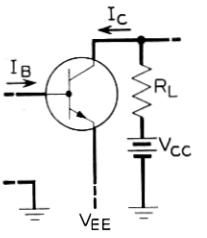
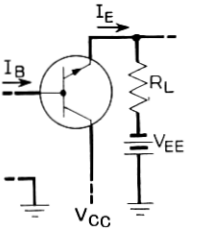


Fig. 7 — Transistor switch.

TABLE III — LARGE-SIGNAL PROPERTIES OF JUNCTION TRANSISTORS

	Common Base	Common Emitter	Common Collector
Circuit			
Current in Region II	$I_C = \alpha I_E + I_{C0}$	$I_C = \frac{\alpha}{1-\alpha}\left(I_B + \frac{I_{C0}}{\alpha}\right)$	$I_E = \frac{1}{1-\alpha}(I_B + I_{C0})$
Current gain	No	Yes	Yes
Voltage gain	Yes	Yes	No
Inversion	No	Yes	No

of three distinct regions. The region can be controlled by changing the input signal applied to the base. In region I, both collector and emitter junctions are reverse-biased and the transistor will be cut off, i.e., the impedance from collector to emitter will be very high. In region II, the active region, the emitter junction is forward-biased and the collector junction is reverse-biased. In region III, both junctions are forward-biased and the transistor switch will be closed. In this region the transistor is said to be in saturation and the impedance from collector to emitter will be very low.

The transistor switch described above is an example of the common emitter configuration. In this configuration the transistor exhibits both current and voltage gain and for this reason it is the most commonly used connection. The common emitter connection also provides signal inversion.

The general properties of the two other possible configurations are shown in Table III. The direction of currents and the polarity of the biasing voltages in Fig. 7 and Table III are for n-p-n transistors and should be reversed when p-n-p transistors are being considered.

In the design of dc transistor circuits, it is often useful to know the general relationships between the input voltage levels necessary to switch a transistor from cutoff to saturation and the resultant output voltage levels. These characteristics for the three configurations are shown in Fig. 8 for both n-p-n and p-n-p transistors. The waveforms represent the

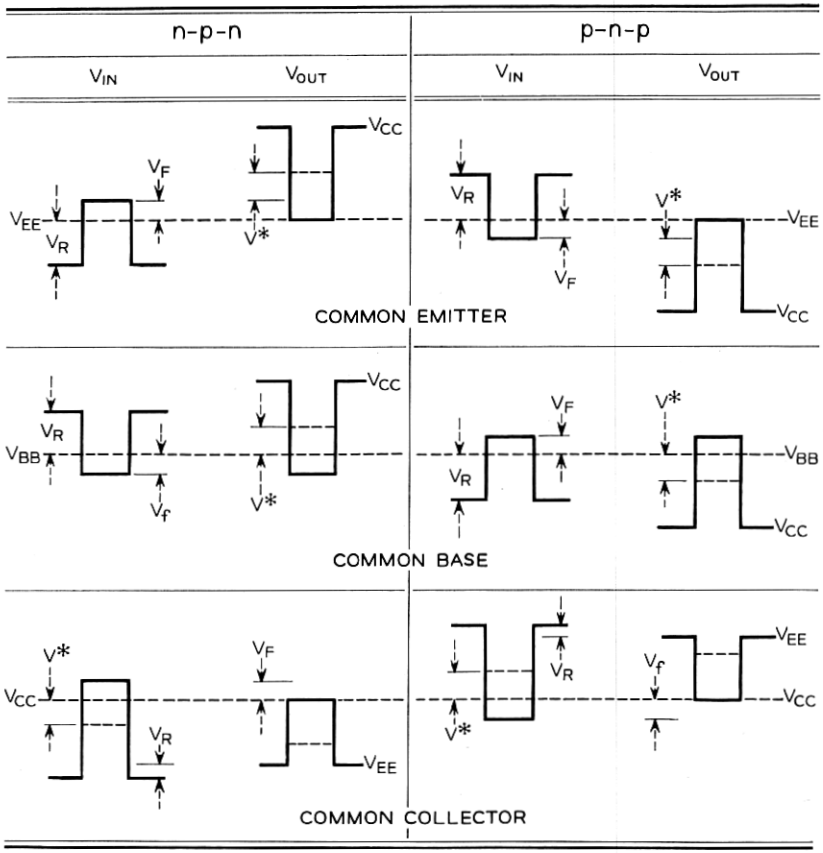


Fig. 8 — Input-output voltage relationships of various junction transistor configurations.

voltages which appear directly on the transistor terminals; V_R and V_F are the reverse and forward biases on the base-emitter junction and V^* is the reverse bias voltage which will appear across the base-collector junction if the transistor is not allowed to saturate. The usefulness of these characteristics is illustrated in the design of the gate amplifier in Section VI.

The switching speeds of transistors are important in nearly all applications, especially in the circuits for the central control. While these speeds depend mainly on the transistor parameters, it is possible to maximize them by suitable circuit design. Analytical studies of the switching times of junction transistors have been made by Moll[4] and have been extended

by Easley[5] to include the effect of collector capacitance. The results of these studies are quite useful in determining the relative effects of transistor and circuit parameters on speed. The discussion here will be limited to the common emitter configuration, but the results are quite similar for all configurations.

The basic common emitter circuit analyzed by Moll and Easley is shown in Fig. 9, together with waveforms illustrating the currents and switching times of interest. Here, T_0 is the rise time and T_2 is the fall time. The delay caused by carrier storage if the transistor is allowed to saturate, T_1, will be discussed below in more detail. The maximum value of the collector current, I_{C1}, will be approximately equal to V_{CC}/R_L if the transistor is driven into saturation.

The above-mentioned studies[4, 5] show the expression for the rise time to be

$$T_0 = \frac{1}{1-\alpha}\left(\frac{1+\omega_\alpha R_L C_C}{\omega_\alpha}\right) \ln\left[\frac{I_{B1}}{I_{B1} - 0.9\left(\frac{1-\alpha}{\alpha}\right) I_{C1}}\right], \qquad (1)$$

where

α = common base short-circuit current gain,
ω_α = alpha cutoff frequency in radians/sec,
C_C = collector junction depletion layer capacitance.

This equation is plotted in Fig. 10 to illustrate more graphically the ef-

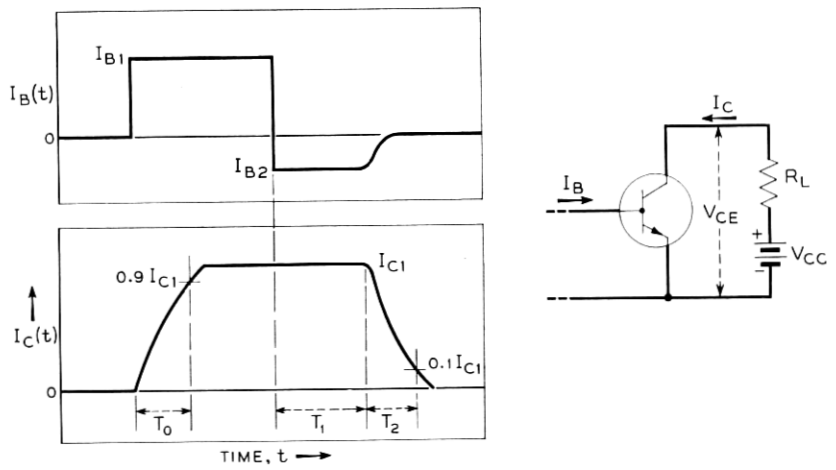


Fig. 9 — Transient behavior of common emitter junction transistor stage.

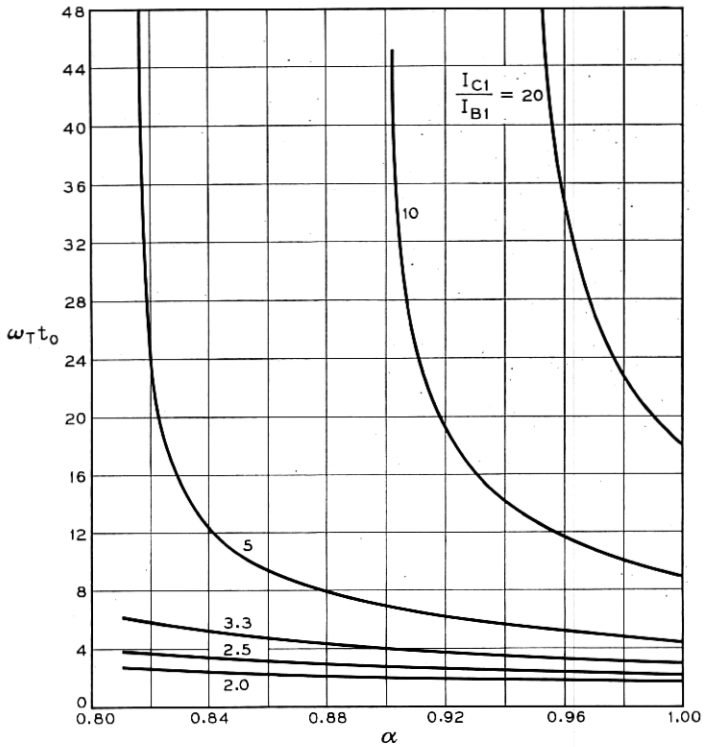


Fig. 10 — Plot of equation (1).

fects of variations in device and circuit parameters. The quantity ω_t in Fig. 10 represents the reciprocal of the effective time constant of the circuit, i.e.,

$$\omega_t = \frac{\omega_\alpha}{1 + \omega_\alpha R_L C_C}. \tag{2}$$

From Fig. 10, it can be seen that the rise time can be improved by increasing ω_t and α and by decreasing the actual circuit gain, I_{C1}/I_{B1}. Thus, given a specific transistor, the rise time can be improved by sacrificing circuit gain and by operating the circuit at low enough impedance levels to make $\omega_t \cong \omega_\alpha$. A further advantage of operating with low circuit gain is that the rise time will be little affected by changes in α which occur due to transistor aging. For circuit gains which are small compared to the possible gain, (1) can be reduced to

$$T_0 \cong 0.9 \frac{I_{C1}}{I_{B1}} \frac{(1 + \omega_\alpha R_L C_C)}{\omega_\alpha}. \tag{3}$$

Refs. 4 and 5 give the following expression for the fall time:

$$T_2 = \frac{1}{1-\alpha}\left(\frac{1+\omega_\alpha R_L C_C}{\omega_\alpha}\right)\ln\left[\frac{I_{C1}-\left(\frac{\alpha}{1-\alpha}\right)I_{B2}}{0.1I_{C1}-\left(\frac{\alpha}{1-\alpha}\right)I_{B2}}\right]. \quad (4)$$

A plot of this equation would be quite similar to that in Fig. 10, where the forward current gain I_{C1}/I_{B1} is replaced by the reverse current gain

$$\frac{I_{C1}}{I_{B2}+I_{C1}\frac{(1-\alpha)}{\alpha}}.$$

Thus, the fall time can be improved in the same general way as the rise time. For the case where the transistor is heavily overdriven, equal rise and fall times are obtained when I_{B1} and I_{B2} are approximately equal.

When a transistor is operated in region III (saturation), more minority carriers are present in certain regions of the transistor than the number which must be present in these regions when the transistor is operated in region II. Before the transistor can be switched from region III to region II, these excess carriers must be removed. While they are being removed the transistor will continue to operate in region III and the output current will change only slightly. This effect, called storage, results in a true delay between the time the input current is changed and the time when the output current begins to respond. For transistors such as those described in Section II, this delay may be as long as microseconds—much too long to be tolerated in most circuits. Special antisaturating circuits have been developed which prevent the transistor from saturating but still permit overdrive for fast rise and fall times. These techniques are illustrated in Section VI.

VI. BASIC BUILDING-BLOCK CIRCUITS

In the earlier sections the philosophy of using as few types of circuits as possible has been explained. The basic AND-OR diode circuits, which constitute a large percentage of the total number of circuits used, have already been discussed. The need for transistorized circuits to perform the memory function and to provide gain was also established. In this section transistor circuits will be discussed.

6.1 *Gate Amplifier*

The exact nature of the circuit used to provide the gain within the logic is determined by requirements and limitations imposed by the

type of logic and the parameters of the available transistors. The major requirements of the amplifier are:

1. The amplifier must have sufficient current gain to satisfy the fanout occurring at most OR gates. To provide enough gain to satisfy the worst case would be costly, since the number of large fanout points is relatively small. An available gain of six is sufficient to satisfy approximately 85 per cent of the applications. This rather modest current gain requirement can drive fanouts which appear much larger, as can be understood by reference to Fig. 11. In Fig. 11 amplifier G is shown driving inputs to n AND gates which control, in turn, m OR gates (m being greater than n). Since the amplifier shares the load of any AND gate with all the other passive (low-voltage state) inputs, the load on G is not equal to the sum of the currents in the AND gates. Therefore, where large fanout situations arise, known functional relationships between the inputs to the AND gates often make it possible to have effective fanouts of much greater than six. The nature of the logic in the system favors this condition.

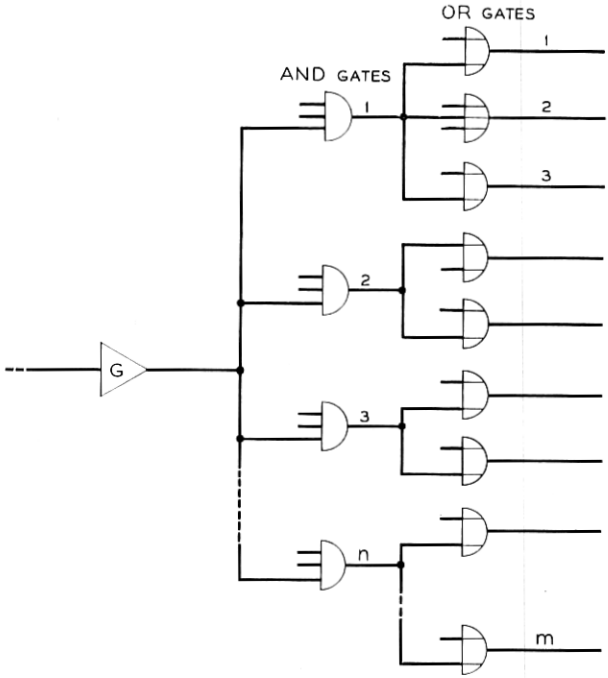


Fig. 11 — Fanout from an amplifier.

TABLE IV — PROPERTIES OF ONE- AND TWO-STAGE dc-COUPLED AMPLIFIERS

Amplifier Requirement	Circuit Configuration								
	One Stage			Two Stages					
	CB	CC	CE	CB-CB	CB-CE	CB-CC	CE-CC	CE-CE	CC-CC
Current Gain	No	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Voltage Gain	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No
No Inversion	Yes	Yes	No	Yes	No	Yes	No	Yes	Yes
Voltage "Straddling"	No	Yes	No	Yes	Yes	Yes (?)	No	Yes	Yes

CB = Common base
CE = Common emitter
CC = Common collector

2. The amplifier must have sufficient voltage gain to cancel the loss in the AND and OR gates and thus re-establish voltage levels. The AND gate diodes attenuate the passive-state signal level, while the OR gate diodes attenuate the active-state signal level. For these reasons the amplifier must provide gain about the center line of the dc input in both the positive and negative directions. Thus, the output voltage levels must "straddle" the input voltage levels.

3. The amplifier must be noninverting and dc-coupled.

4. The amplifier must be fast enough to allow the use of up to three amplifiers in a series logic chain. For the transistors employed, this requires nonsaturating, low-gain circuits.

In order to select the best circuit configuration to meet these requirements the properties of the three basic transistor configurations must be considered. These were discussed in Section V. The relatively modest current and voltage gain requirements of the amplifier make it evident that no more than two transistor stages should be necessary. The pertinent dc properties of all possible configurations of one- and two-stage amplifiers are listed in Table IV. From this table it may be seen that no one-transistor configuration meets the dc requirements of the amplifier. Of the two-transistor configurations only the common-base-common-collector and the common-emitter-common-emitter combinations meet all the requirements. A closer examination of the common-base-common-collector configuration reveals that some sort of passive voltage-shifting network would be necessary to meet the straddling requirement. In addition, in this configuration the common base transistor would have to furnish all the voltage gain and the common collector all the current gain. The two common emitter stages constitute the best configuration, since

each provide both current and voltage amplification and the combination satisfies the remaining requirements. From Fig. 8 it can be seen that one transistor must be an n-p-n and the other a p-n-p to obtain voltage straddling. Since the signal is inverted in each stage, the two transistors will be either both ON or both OFF. An input to the first transistor of a polarity to turn it ON, for example, will, when inverted, turn ON the second stage of the amplifier.

The only decision remaining in determining the configuration is to establish the order in which the transistors should appear. The diode logic demands that the amplifier output provide a current path to approximately ground potential in the passive state and a high impedance in the active state. Two possible types of amplifiers exist, corresponding to the two possible methods of connecting the transistors. In the positive logic system, placing the n-p-n first and the p-n-p second leads to a "make" type amplifier; the reverse order produces a "break" type amplifier. These two types are shown symbolically in Fig. 12, along with the corresponding transistor circuit configurations which realize them. In the break amplifier both transistors would be ON in the passive state

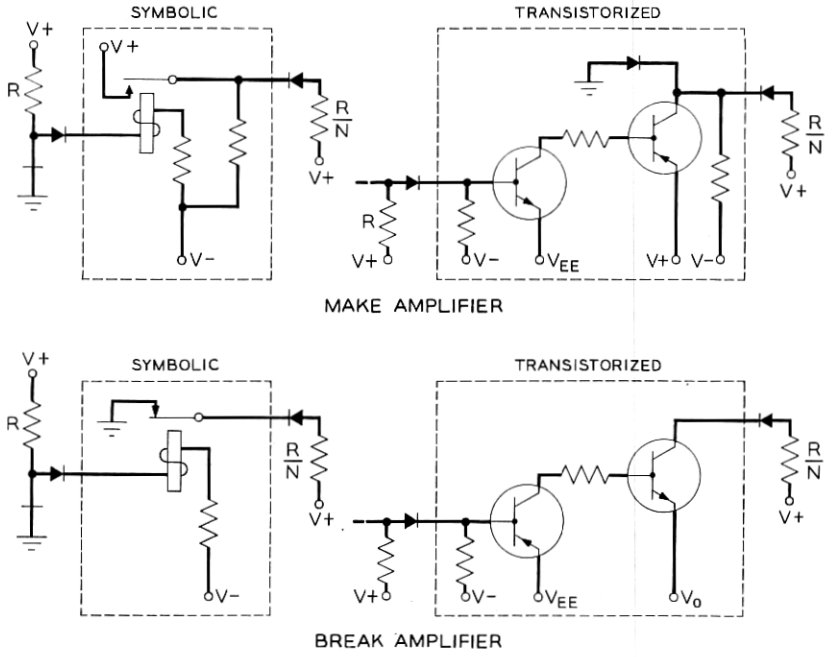


Fig. 12 — Possible amplifier configurations.

and OFF in the active state. The conditions would be reversed in the case of the make amplifier.

The choice between the two basic types of logic amplifiers above is not a simple one. The few apparent advantages of one over the other almost vanish when detailed final designs are approached. For example, the make amplifier appears much less efficient. In addition to supplying the full passive load current in the resistor to $-V$ at the output of the amplifier it must supply enough extra current to raise the output voltage to the active signal level. However, the need for dummy loading the break amplifier to compensate for stray wiring capacity in the system, as will be discussed below, almost nullifies this apparent advantage.

The decision as to which amplifier to choose must rest upon more subtle differences. The more important of these, leading to the choice of the break-type amplifier, are:

1. To stabilize the passive voltage level at the output of the make amplifier a diode clamp is required. This is a factor in reliability and introduces delay, since the current in the clamping diode must be replaced by current from the amplifier before any change in output voltage can occur during a transition from the passive to the active condition.

2. The make amplifier has a definite maximum current capacity and must switch this amount regardless of the load. (The diode clamp compensates for varying load conditions.) This necessitates an exact calculation of the maximum load on a particular amplifier. No such limitation exists in the case of the break amplifier, as will be developed later.

In addition to meeting the initial requirements in the system, the gate amplifier must have sufficient margin to function reliably as the components age. The most critical components in the circuit, and those for which the least aging information is presently available, are the transistors and diodes. A brief summary of the expected behavior of the most significant parameters is given below:

Transistors

1. Frequency cutoff of α, (f_α): This parameter is related almost exclusively to the internal geometry of the transistor and the physical constants related to transistor action. Therefore, no significant change should occur.

2. Transistor α: Experience has shown that α tends to age downward initially after which time it stabilizes. In all the designs an α of 0.94 was assumed as a reasonable minimum.

3. Transistor saturation current, I_{c0} : Almost without exception, I_{c0}

in transistors ages upward. In circuits which are sensitive to this parameter a maximum of 200 microamperes was assumed.

Diodes

1. Diode forward voltage drop: Previous experience with germanium point-contact diodes similar to those to be used in the system indicates little or no change with time.

2. Diode reverse leakage current: Diode reverse current behaves similarly to I_{c0} in transistors except that its behavior is somewhat dependent upon the voltage at which it is measured. At low voltages (5 volts or less) it often ages downward. At higher voltages the trend is upward.

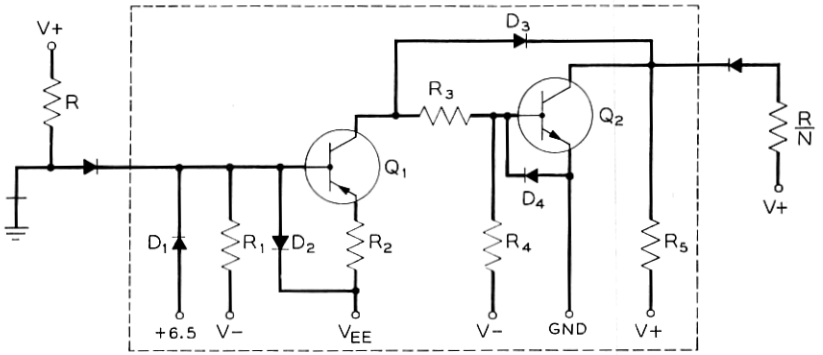


Fig. 13 — Nonsaturating amplifier.

In the discussion of the AND and OR gates in Section IV the current level in OR gates was stated as approximately 5 ma. In the passive state this current is shunted through one or more AND gates by one of the several types of amplifiers in the system. In the active state the shunt path through the AND gates is interrupted by the amplifier going OFF. Under this condition the OR gate current drives forward to turn OFF the succeeding amplifier stage. To operate properly the amplifier must, therefore, have an input voltage threshold higher than the total voltage drop in the AND gates preceding the OR gate plus any drop in the preceding amplifier in its passive state. From these considerations, the input threshold of the amplifier has been set at +6.5 volts. Having already established the output of the amplifier to be approximately ground in the passive state, we can choose the other voltages to provide the desired impedance level and current drives.

In Fig. 13 the break amplifier is redrawn with some complexity added

to prevent the transistors from saturating and to establish the proper threshold. With no input to the amplifier (the input OR gate shunted down) the amplifier must assume its passive condition (both transistors ON). This requires that V_{EE} be greater than the +6.5 volts which establishes the input threshold. The output current of Q_1 and thus the drive to Q_2, will be approximately

$$\frac{V_{EE} - 6.5}{R_2} \alpha_{Q_1} .$$

This current can be set by considering the input drive available and the required output current. Since the input must rise above V_{EE} in the active state to turn off Q_1, the quantity $(V_{EE} - 6.5)$ should be kept small. This leads to the choice of $V_{EE} = +8$ volts in the system.

In order to establish the internal current drives of the amplifier, the actual transistor gains must be calculated. The 5 ma current level in the OR gate is not all available to turn OFF the first transistor, Q_1. When the drive is removed from the input, the amplifier must return to its passive condition. Since both the active and passive states are equally important in the dc double-rail logic, this transition must be as fast as the transition from passive to active. A bias current drive is provided to establish the passive state when the input drive is removed. This bias reduces the forward drive when the amplifier is driven active. For equal turn-on and turn-off times, the bias current must be approximately one-half the input drive. This situation exists in both stages of the amplifier and, by itself, requires the combined transistor gain to be four times the apparent terminal gain of the amplifier.

Because of the large physical size of the central control, an amplifier often must drive loads located a considerable distance away from it. Stray capacity on these leads delays the transition from the passive to the active state. This effect can be reduced by the addition of R_5. Current in this dummy load is available to charge stray capacity at the expense of demanding more gain from the amplifier. A dummy-load current of 8 ma was chosen as a reasonable compromise. The dummy load also provides a well-defined active voltage level at the output of the amplifier.

By taking into account the current transfer loss of OR gates, the leakage currents of idle OR inputs and the dummy load, the combined transistor gain must be nearly 60 to realize the necessary terminal gain of six. This is accomplished by assigning a transistor gain of approximately 7.5 per stage, making the switching speeds relatively independent of α over the design range. (See Fig. 10).

By combining the information outlined above, the current level in R_4 can be set as $(I_{out\ max}/7.5) \doteq 5$ ma. This requires approximately 10 ma from Q_1 and a bias current to Q_1 of $(10/7.5) \doteq 1.3$ ma. From these basically simple considerations, the resistors R_1, R_2 and R_4 can be specified in terms of $-V$. The magnitude of $-V$ can be set by considering the breakdown voltage ratings of the transistors and the current transfer efficiency in R_1 and R_4. A value of -4.5 volts was selected.

The remaining components of the amplifier of Fig. 13 are D_2, D_3, D_4 and R_3. Diodes D_2 and D_4 limit the voltage swings at the transistor inputs and reduce the effect of collector capacity by lowering the transient

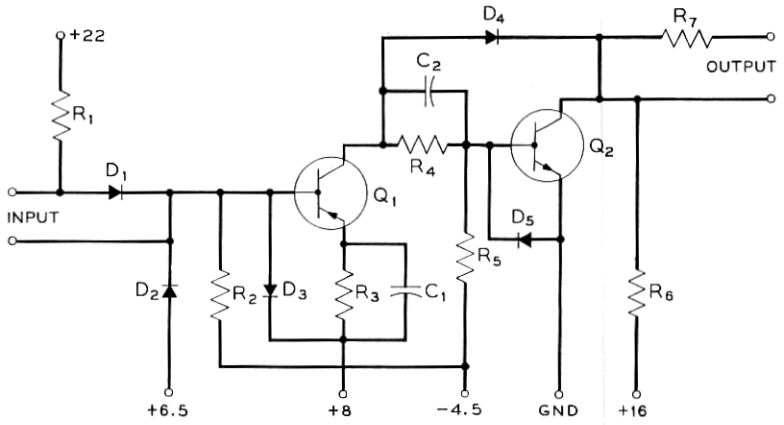


Fig. 14 — Gate amplifier.

base impedances. Resistor R_3 and diode D_3 combine to prevent saturation in transistor Q_2. Having established the currents in Q_1, R_4 and Q_2, and knowing the range of values of α and I_{C0} in Q_2, we can determine the currents in R_3 and D_3 under all conditions. If R_3 is chosen so that its voltage drop is always greater than the voltage across D_3 when Q_2 is ON, Q_2 will never saturate. The advantage of this method of preventing saturation is that diode D_3 shunts the excess drive to Q_2 only after the output voltage has completed its transition to the passive state.

The final design of the amplifier is shown in Fig. 14. It differs from the previous drawing, Fig. 13, in the addition of capacitors C_1 and C_2 and resistors R_1 and R_7. The capacitors C_1 and C_2 do not affect the dc conditions but do improve the transient response. In particular, the delay in the amplifier is reduced.

Resistor R_1 and diode D_1 constitute a single input OR gate. This

allows the gate amplifier to be driven by AND gates if desired. An option is also provided at the output of the amplifier for connecting loads to the collector of Q_2 directly or through R_7. Loads drawn through R_7 cause the voltage at the output to increase with load. Thus, if amplifiers are sharing a load (as in the case of AND gates), the load currents of the individual amplifiers will tend to equalize. This is an essential condition for realizing large fanouts, as was explained in conjunction with Fig. 11.

One of the advantages claimed for the break-type amplifier should be noted. Depending upon the α's of the transistors and the delay which can be tolerated in a particular logic chain, an amplifier may carry considerably more current than the design maximum of 30 ma. In engineering the logic of the central control, it becomes quite difficult to estimate the load current of each amplifier under all conditions of fanout. The break-type amplifier has margin for error when circuits are engineered to the design limit. This margin can also be of importance in locating a faulty amplifier under trouble conditions. Because of load-sharing between amplifiers, the failure of one causes the load on associated amplifiers to increase. If the associated amplifiers are capable of absorbing this added current, the trouble condition can be traced to the particular faulty amplifier. Amplifiers of the make type, however, by virtue of their inability to absorb current above a designed maximum, could indicate multiple troubles where only one actually existed.

6.2 *Flip-Flop and Associated Circuits*

The transistorized memory element of the central control must meet requirements which cannot be stated as explicitly as were those of the gate amplifier. The requirements can be generally stated as:

1. Stability: The flip-flop must maintain its bistability under all conditions of load, temperature and voltage encountered.

2. Compatibility: The flip-flop must trigger from pulses readily available in the system, must not respond to noise in the system and must be capable of driving into the standard dc double-rail diode logic.

The configuration of the transistorized flip-flop differs only slightly from the conventional Eccles-Jordan type. The development of the design is similar to that of the gate amplifier and the same considerations regarding gain, speed, etc., also apply. For this reason, the details of design will not be considered. Instead, emphasis will be placed upon how the flip-flop fits into the general system and upon some of its major characteristics.

The flip-flop used in the electronic switching system is basically a four-transistor circuit. The dc bistability is provided by two of the tran-

sistors, which are combined on a single package designated the flip-flop. The other transistors comprise two single-stage amplifiers which afford buffering between the 1 and 0 outputs of the flip-flop and the external dc logic that the composite flip-flop must drive. These amplifiers are designated the flip-flop to gate amplifiers. Special buffer amplifiers are provided for the cases where the flip-flop does not drive diode logic. All the amplifiers clamp the flip-flop output, this being essential in preventing saturation.

Fig. 15 shows the details of the flip-flop, with the buffer amplifiers simulated by resistor-diode clamps to ground. We shall consider the more important features of the circuit in turn.

The use of separate terminals to introduce the collector supply voltage (-16 volts) provides a method of predetermining the state a flip-flop will assume when power is applied. By connecting the terminals to separate supply buses and momentarily connecting one to $+16$ volts and then to the normal -16 volts, the system will assume the state represented by the wiring pattern.

The degeneration produced by the common emitter resistor stabilizes the voltage at the emitter node and the output current of the ON transistor. This voltage stabilization of the emitters (and therefore of the base of the ON transistor), combined with the clamping action of the amplifiers in the collector circuit of the ON transistor, prevents satura-

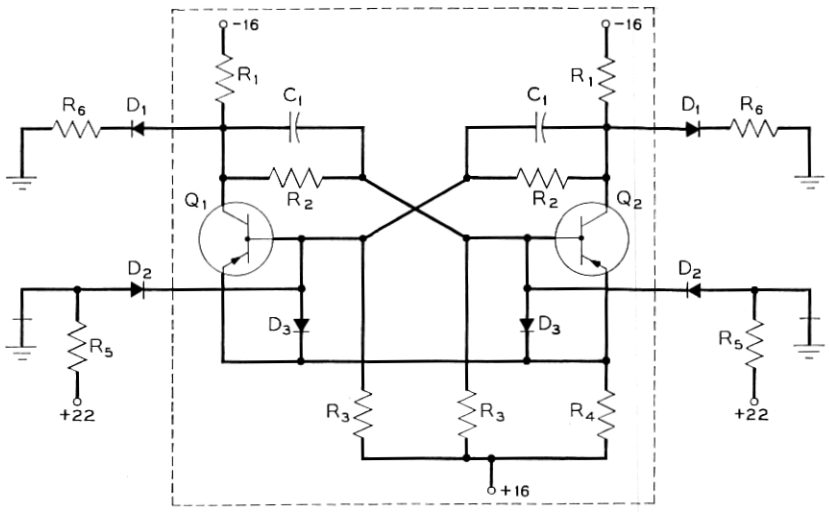


Fig. 15 — Flip-flop with simulated amplifier loads.

tion in the flip-flop. The voltage and current levels are designed to provide the same input voltage threshold as in the gate amplifier. By designing the output current to equal that of Q_1 in the gate amplifier, it was possible to make the flip-flop to gate amplifier essentially the same as the output stage of the amplifier of Fig. 14. Thus, when viewed from its terminals, the flip-flop and its amplifiers together are exactly equivalent to the gate amplifier insofar as dc conditions are concerned.

Fig. 15 shows the use of standard OR gates for triggering. To prevent race conditions from occurring in the system, all inputs to the flip-flop are gated by the master clock. This requires that a clock signal be an input on all AND gates preceding OR gates driving a flip-flop. A single-input OR gate is provided on each side of the flip-flop to allow driving from AND gates if desired.

Another feature of the flip-flop is the use of diodes between the bases and emitters of the transistors. These diodes limit the reverse bias on the transistors to a fraction of a volt, clamp the driving OR gate output and, most important, lower the transient impedance in the base circuit. The lower base impedance reduces the effect of collector capacity and improves triggering sensitivity.

The circuits of the two buffer amplifiers are shown in Fig. 16. The amplifier used to drive logic gates, the flip-flop to gate amplifier, needs no explanation since it is almost identical to the output stage of the gate amplifier previously described. The flip-flop to relay amplifier is designed to drive the highly inductive loads of wire-spring relays. The transistors are allowed to saturate in this circuit because of the slow speeds involved.

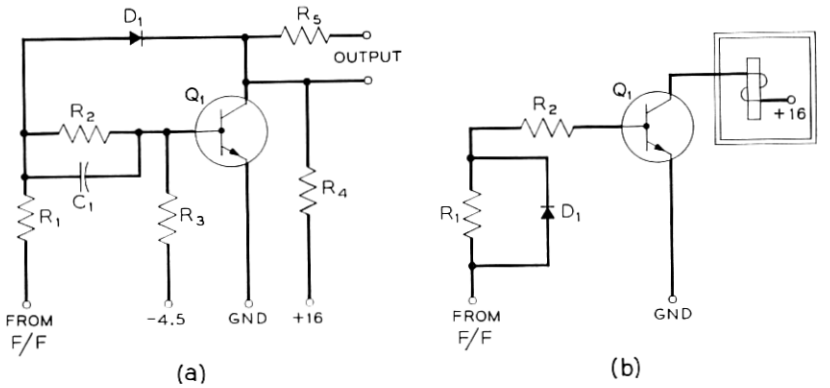


Fig. 16 — Flip-flop buffer amplifiers: (a) flip-flop to gate; (b) flip-flop to relay.

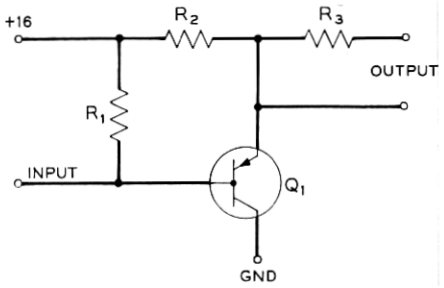


Fig. 17 — Emitter follower circuit.

6.3 *Emitter Follower*

In an earlier section, it was stated that the gate amplifier and the flip-flop to gate amplifier were not designed to have sufficient current gain to satisfy the points of largest fanout in the system. A special package, the emitter follower, is provided to supply this extra gain. One gate amplifier can drive a maximum of four emitter followers in parallel. For even greater fanouts, emitter followers can be cascaded. The inclusion of an emitter follower adds almost no delay to a logic chain. The circuit of the emitter follower is shown in Fig. 17.

6.4 *Inverter Amplifier*

An additional circuit, shown in Fig. 18, which saves equipment in many applications in the system is the inverter amplifier. The terminal conditions of the inverter amplifier are similar to those of the gate amplifier except for the logical inversion and a lower load capability.

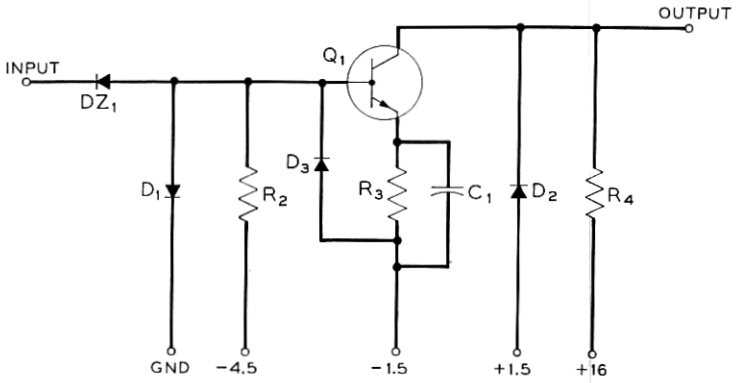


Fig. 18 — Inverter circuit.

The circuit is similar to the first stage of the gate amplifier, except for the use of an n-p-n transistor and different voltage levels. A Zener diode, DZ_1, raises the input voltage threshold to the same level as that of the other transistor circuits. Diode D_2 clamps the output of transistor Q_1 to prevent saturation.

6.5 *Cable Pulser*

The need for the central control to communicate with the electron tube circuits in other parts of the system requires special buffering amplifiers for transmitting high-speed signals over coaxial cable. These signals originate from OR gates in the central control. In addition to driving the cable, the OR gates must activate local flip-flops in the central control to retain a record of the information transmitted. The OR gate neither has sufficient current output to perform these two functions nor is its impedance compatible with that of the cable. The cable pulser circuit shown in Fig. 19 provides the required gain and achieves compatibility between the units.

The cable pulser is a two-stage amplifier. The first stage is a common collector configuration which provides sufficient current gain to drive a flip-flop and the second stage of the cable pulser. The second stage is a common emitter configuration which provides voltage and current gain to drive the cable. The output is coupled to the cable through an impedance-matching transformer. The input to the cable pulser is gated by the master clock.

6.6 *Special Circuits*

Although every attempt has been made to minimize the number of types of packages in the system, in some cases the use of special packages

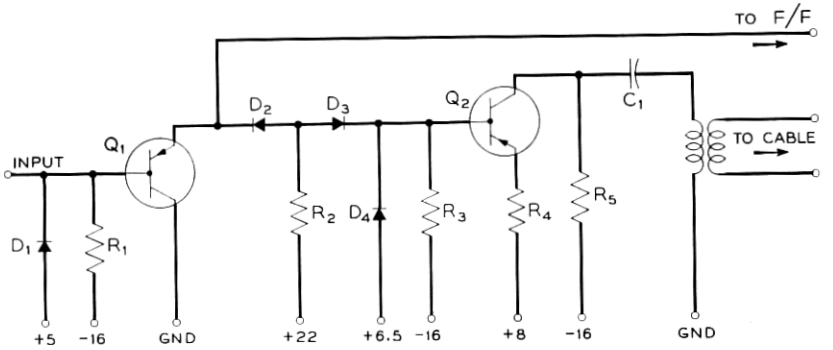


Fig. 19 — Cable pulser circuit.

is economically justifiable. In this system these special packages take the form of modifying networks which are used in conjunction with standard packages to realize special circuit functions. The circuits are shown in Fig. 20.

6.6.1. *Feedback Network*

Monostable flip-flops are required for timing applications in the system. This need has been satisfied by the design of a simple feedback network for use with the standard gate amplifier, consisting simply of a resistor and a capacitor in series. When connected between the output and input of a gate amplifier, the network provides positive feedback for a time determined by the values of the resistor and capacitor. The purpose of the extra resistor in the feedback network is to provide a voltage step at the output of the amplifier at the beginning of the timing cycle. If the load on the circuit is coupled through an AND gate, this step is sufficient to decouple the load during the timing cycle and, therefore, make the timing independent of load.

6.6.2. *Pulse-Shortening Network*

Occasionally the need arises in the system to derive a narrow (approximately 1-microsecond) pulse from the output of one of the standard amplifiers. This has been accomplished by a simple network consisting essentially of a shorted 0.5-microsecond delay line which can be connected to the output of an amplifier. As shown in Fig. 20(b), a resistance divider network is needed to derive a clamping voltage level approximately 2 volts above ground to prevent saturating the driving amplifier.

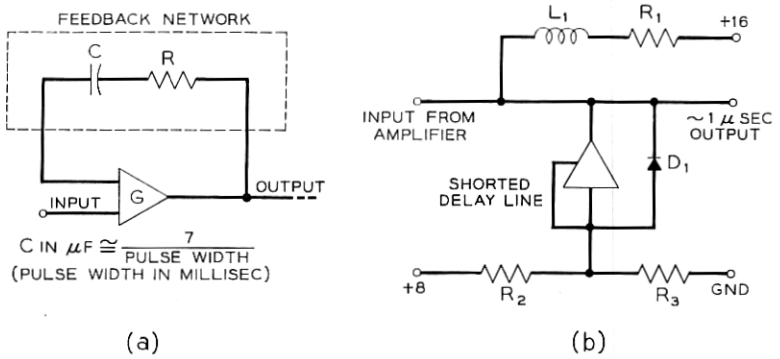


Fig. 20 — Special network circuits: (a) monostable feedback network; (b) pulse-shortening network.

The resistor R_1 and inductor L_1 provide a current step to the network, thus giving a better-shaped pulse in the output.

VII. MECHANICAL DESIGN

In the semiconductor circuitry of the electronic switching system, a modular approach to mechanical design is used. This is in keeping with the universal building block approach to obtain economy in both manufacture and in the number of spare packages required in the telephone central office. It is also consistent with the marginal and diagnostic trouble-detecting techniques developed for the system, whereby faulty equipment can be easily replaced.

The semiconductor circuits used in this model of the electronic switching system are placed on printed wire boards. A board may contain one or more circuits, depending on the degree of complexity and the number of components employed in the individual circuits. Fig. 21 illustrates the basic board assemblies. On both sides of the transistor end of the board (and only on those boards containing transistors) is a series of terminals designated shorting plug terminations. These are provided so that the transistors may be tested, external to the circuit environment, without unsoldering any leads or physically disturbing the transistor in any way. In normal use the transistor is connected into the

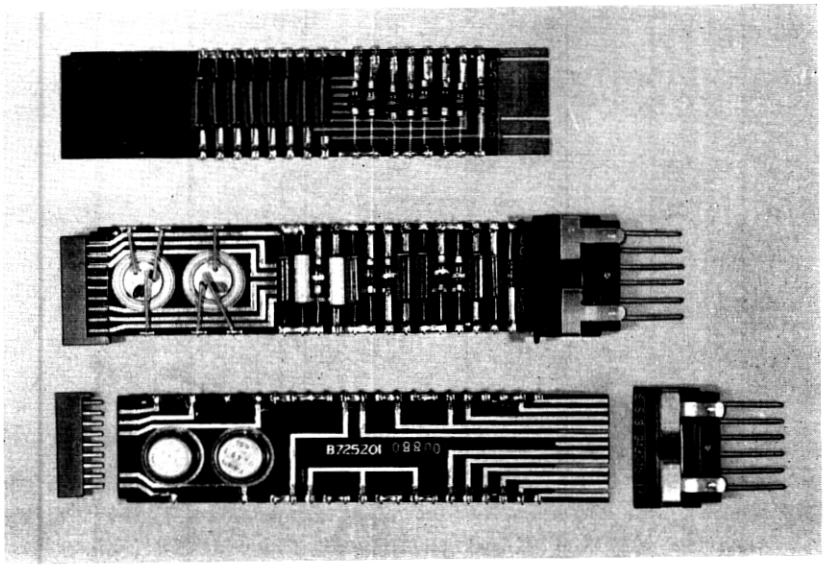


Fig. 21 — Printed circuit boards and components.

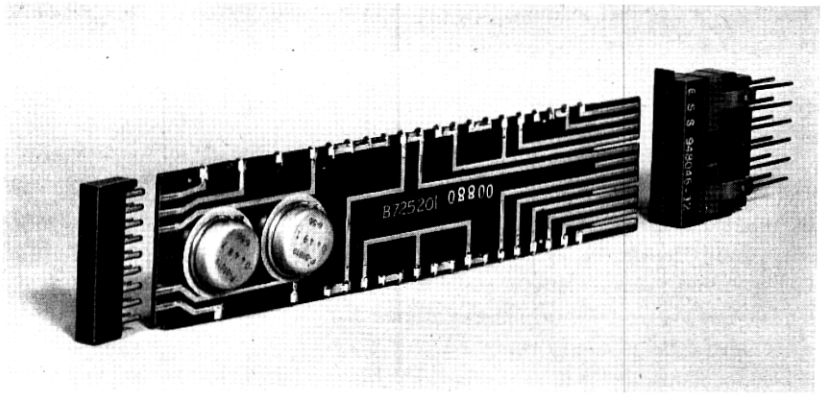


Fig. 22 — Printed board, shorting shoe and connector.

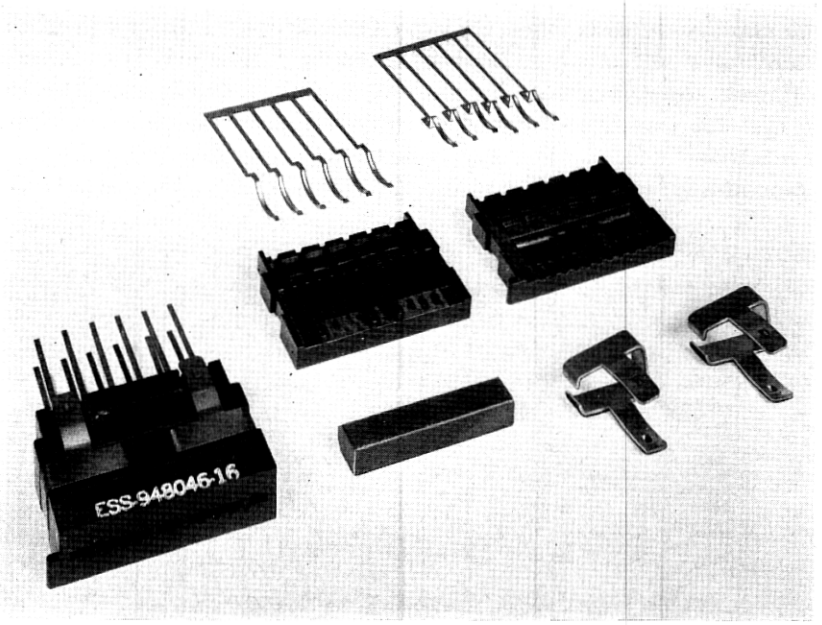


Fig. 23 — Coded connector for semiconductor package.

circuit by means of a shorting plug. Fig. 22 illustrates the use of the shorting plug and also shows the board terminations and connector. One can also see in Fig. 22 that each card assembly is coded on a 3-slot-out-of-a-possible-11 basis. The connector is similarly coded with barriers or teeth so that one particular type of card will fit into a companion coded

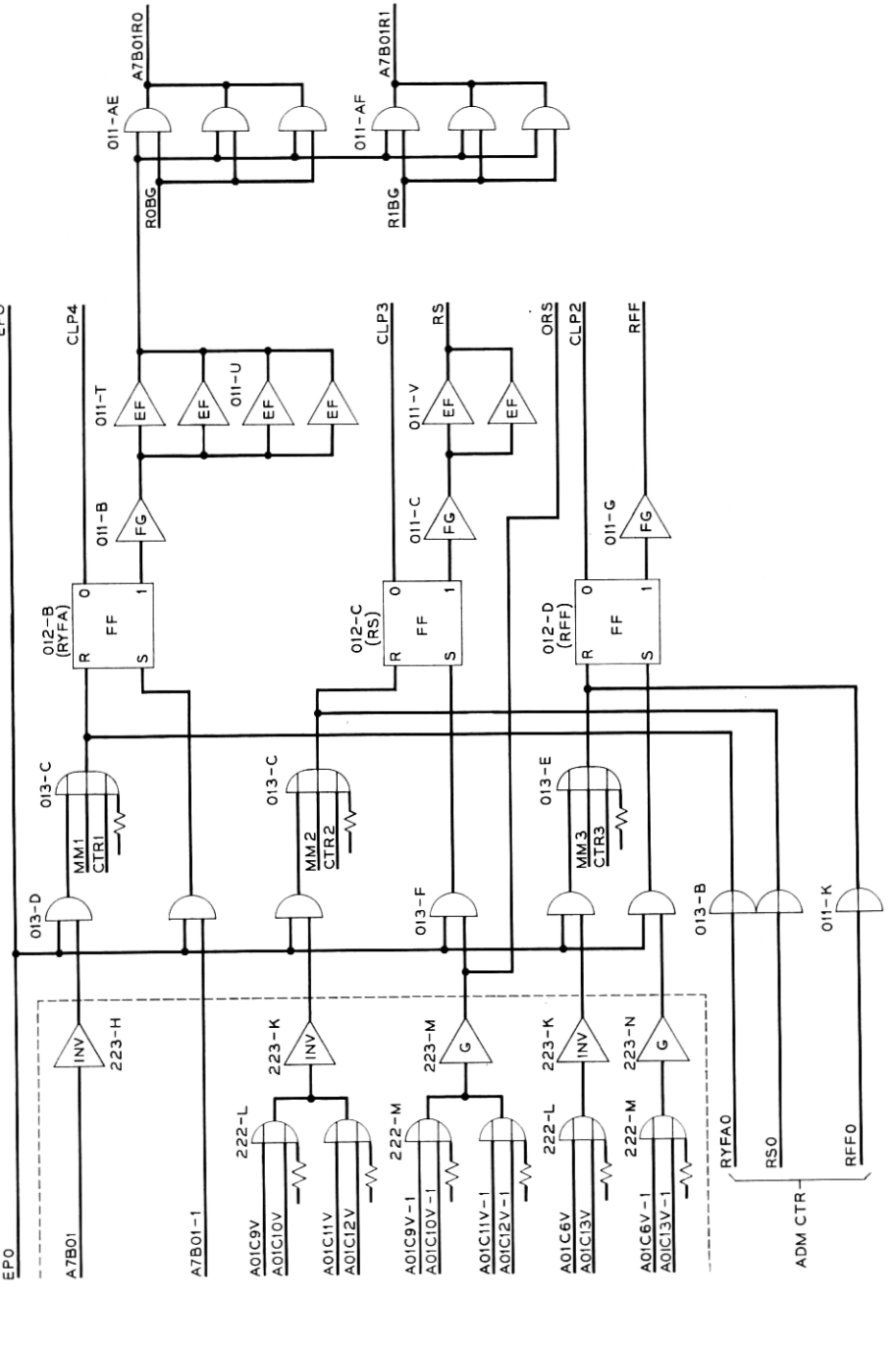


Fig. 24 — Representative portion of circuit schematic.

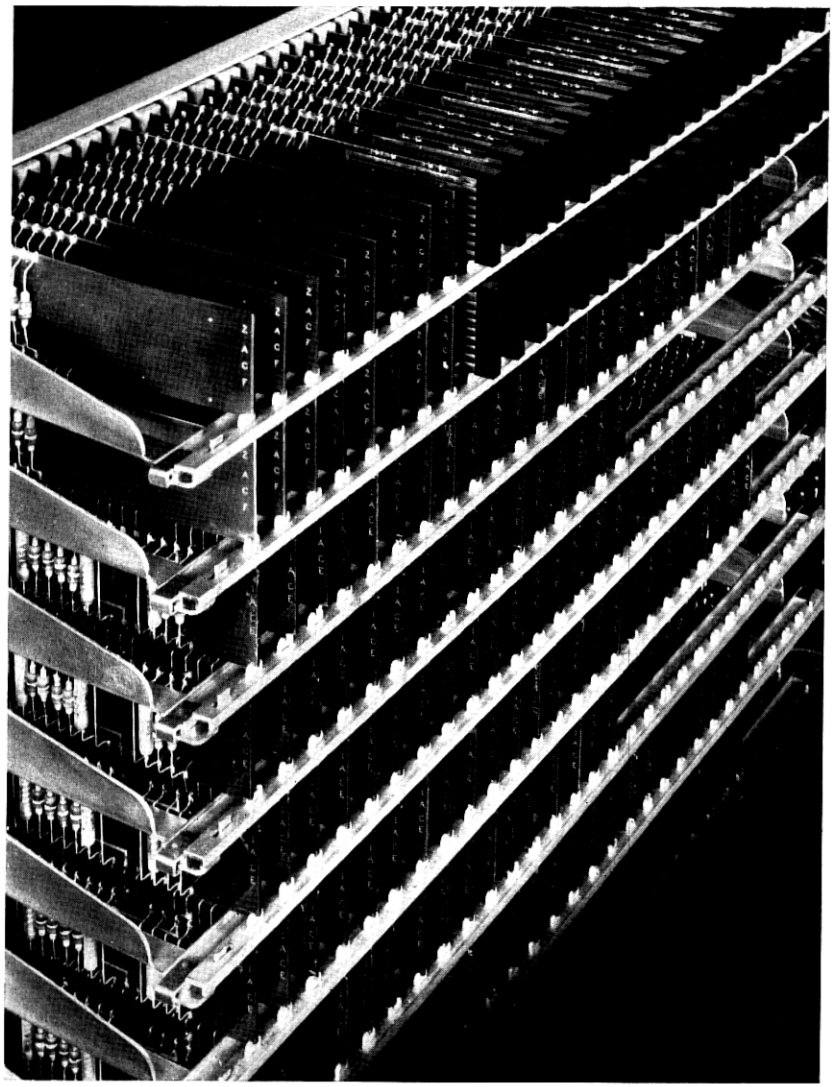


Fig. 25 — Equipment unit (front).

connector. This will prevent improper interchange of packages during assembly or maintenance.

As shown in Fig. 21, each component is fastened over the edge of the card by a clinch which mechanically holds it in position. A subsequent solder dip secures the mechanical clinch and at the same time makes the electrical connection to the printed wire circuit. The component lead

makes an edge connection from one side of the board to the other if this is required. This method of mounting the components lends itself to low-cost automatic manufacturing techniques.

The connector shown in Fig. 22 is a reliable contact connector that can be produced and assembled by automatic or semi-automatic machinery. It is held together by spring clips, which also hold the connector in the mounting plate. Fig. 23 shows the connector and its component parts in more detail.

Fig. 24 is a portion of a circuit schematic showing the use of AND and OR gates, amplifiers and flip-flops. Circuitry of this type is developed into equipment as shown in Fig. 25. The gates, amplifiers and flip-flops are arranged for ease of maintenance, ease of manufacture and for proper circuit operation. In this equipment connectors are placed in the mounting plates and the mounting plates are arranged in groups and wired. The printed wire board assemblies are plugged into the connectors. The fronts of the boards are supported and aligned by means of a bar ar-

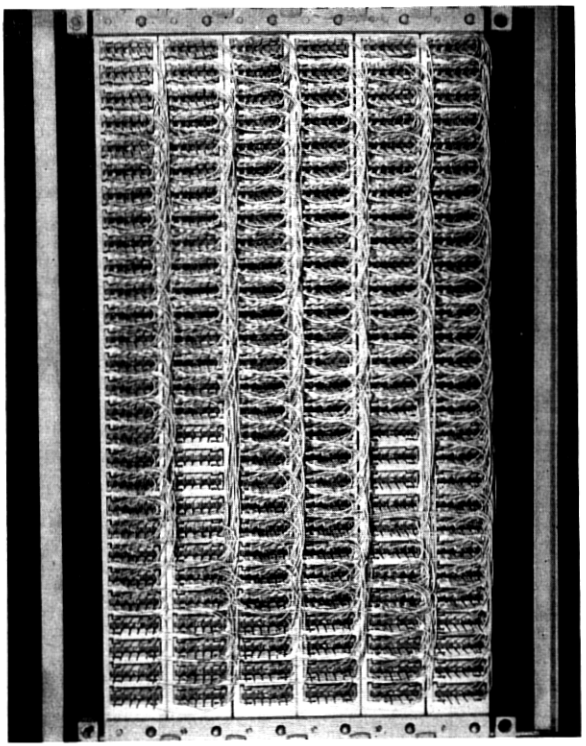


Fig. 26 — Equipment unit (rear).

ranged across the front of the framework, with the front edge of this bar also serving as a designation strip. Fig. 26 shows the rear of the equipment. Solderless wrapped connections are used exclusively, and the equipment can be automatically wired by programmed solderless wiring machines.

VIII. CONCLUSION

The philosophy of semiconductor circuit design for the central control of an electronic switching system has been described. The primary emphasis in the design has been on low cost consistent with good margins, reliability and the meeting of all systems requirements.

The general-purpose nature of the building blocks affords great flexibility to the logic designer in implementing complex system functions. The ability of the circuits to handle widely varying loads allows the system to be engineered quite simply. An effort has been made to minimize the number of package types consistent with the many different functions to be performed. This results in economy in manufacture and maintenance.

The use of antisaturating low-gain circuits, clamping techniques and careful equipment design has resulted in operating speeds sufficient for the desired rate of information processing. Throughout the designs, generous allowances have been made for aging and variations in device and component parameters to assure high reliability consistent with economy. It is too early to give an accurate evaluation of the true reliability of the circuits, since this can only be obtained by relatively long field experience. However, present indications are that these circuits will result in a system furnishing service at least comparable with present-day electromechanical systems.

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