Transistor Pulse Regenerative Amplifiers

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(Manuscript received April 5, 1956)

A pulse regenerative amplifier is a bistate circuit which introduces gain and pulse reshaping in a pulse transmission or digital data processing system. Frequently it is used also to retime the pulses which constitute the flow of information in such systems. The small size, reliability, and low power consumption of the transistor have led naturally to the use of the transistor as the active element in the amplifier. It is the purpose of this paper to describe some of the techniques that are pertinent to the design of synchronized regenerative amplifiers operating at a pulse repetition rate of the order of one megacycle per second. An illustrative design of an amplifier for use in a specific digital computer is presented.

1. INTRODUCTION

A basic building block of many modern digital data processing or transmission systems is a pulse regenerative amplifier. The particular high speed transistor regenerative amplifiers to be discussed in this paper are intended for use in systems where the logic operations on the digit pulses are performed by passive circuits and the amplifiers are inserted at appropriate intervals to amplify, reshape, and retime the pulses. The design of these amplifiers for any specified system involves a knowledge of the environment of the amplifier in the system, a study of possible functional circuits which are combined to form an amplifier circuit, and the selection of a combination of these functional circuits to achieve the desired amplifier performance. Although a study of the functional circuits constitutes the major portion of this paper, the design of an amplifier for a particular digital computer is presented to illustrate the general design procedure.

One important way in which these amplifiers differ from many pulse amplifiers is that they must function properly under adverse conditions. That is, instead of merely expecting superior performance most of the

Fig. 2. In the following sections the relation between each of the above functional features and amplifier performance is discussed, various circuit configurations to achieve each function are investigated, and the interactions between the functional circuits are examined. The design of any particular amplifier then consists of a suitable selection of a transistor and functional circuits to achieve the desired amplifier performance.

2. TRANSISTOR PROPERTIES

In a regenerative amplifier the transistor operates as a switch with power gain. The "on" and "off" state usually are characterized, respectively, by high and low collector current levels, and changes of state are initiated by applied control signals. The performance items of interest are the power dissipation in the two states, the speed with which the transistor changes state, the amount of power gain available, and the attainable margins against false operation. The transistor parameters related to these items, as discussed below, are listed in Table I with typical values for several classes of transistors. Desirable and satisfactory values have been indicated in italics.

The power dissipated in a transistor in the "off" state is proportional to I_{co}, the collector current with the emitter open circuited, and to the collector supply voltage. This is wasted power and, since the minimum collector supply voltage usually is dictated by other considerations, a low I_{co} current is desirable to reduce standby power. Point contact units are relatively poor in this respect. In junction units the I_{co} power is almost negligible compared to other circuit standby power.

The power dissipated in a transistor in the "on" state is proportional to the saturation voltage between the collector and the common terminal.

TABLE I — TRANSISTOR SWITCHING PROPERTIES

Switching Features	Point Contact Transistors (Low Resistivity Ge)	Junction Triode Transistors		
		Ge Grown	Ge Alloy	Si Grown
I_{co} at V_c = 10v	1500 μa	*5 μa*	*5μa*	*0.01 μa*
Collector to emitter saturation voltage at I_c = 10 ma	0.8 V	0.5 V	*0.05 V*	4 V
fα cut-off	*15 mc*	2 mc	4 mc	4 mc
Base resistance	*50 ohms*	500 ohms	*100 ohms*	500 ohms
Collector capacitance at V_c = 10V	*0.5 UUF*	10 UUF	20 UUF	10 UUF
Collector breakdown voltage	*40 V*	*100 V*	*35 V*	*100 V*
Punch through voltage	*no punch through*	*100 V*	*35 V*	*100 V*
Emitter breakdown voltage	*40 V*	5 V	*35 V*	1 V
Ratio of alpha at I_e = 10 μa to alpha at I_e = 1 ma	*3*	0.8	0.8	0.6

Again, this represents wasted power, but also important is the fact that it places an upper limit on the output power available from the transistor. Hence, it is desirable to have as low a saturation voltage as possible. Alloy junction transistors are especially good in this respect.

The speed with which a transistor changes state is principally a function of the alpha cut-off frequency (which should be high), base resistance, and collector capacitance (both of which should be low).[3, 4] Both the rise and fall times of the transistor response are greatly influenced by the associated circuitry; generally a blocking oscillator circuit yields the fastest response.

The amount of effective power gain available from a regenerative amplifier is influenced by two transistor properties. One property is the breakdown voltage, which may be the collector to base breakdown voltage or the collector to emitter punch through voltage (whichever is lower). This limits the output power by limiting the collector supply voltage. The other factor is the variation of alpha with emitter current, especially at low emitter currents. The minimum average emitter current required to initiate self-sustaining positive feedback determines the minimum input power. Point contact units are especially good in this respect in that alpha may approach ten at emitter currents as low as five microamperes. Junction units are poor since alpha generally decreases rapidly at emitter currents below one hundred microamperes.

Even though the attainable margins against false operation are largely a matter of circuit design, two transistor properties occasionally become important. In point contact units trouble with lock up in the "on" state may occur due to internal base resistance. Although this property of base resistance is exploited in negative resistance feedback circuits, it is undesirable in circuits where the feedback is obtained by external coupling. In grown junction units the emitter to base reverse breakdown voltage may limit the voltage margin against false triggering caused by noise or crosstalk. Normally it is desirable to have a one or two volt margin.

From the above discussion it can be seen that no one type of transistor is outstanding in all features. The choice of which unit to use in a specific amplifier depends upon the repetition rate, gain, and power requirements desired of the amplifier. Although the point contact type has the best overall performance of the types shown in Table I, it is quite possible that new types (such as PNIP or diffused triodes[13]) and improved designs of the present types will change the picture.

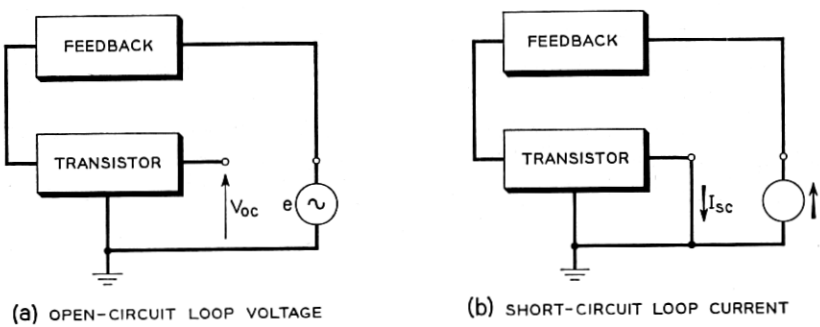
3. FEEDBACK CIRCUITS

The use of positive feedback in an amplifier results in high gain and short rise time. If the input circuit is isolated from the feedback loop by

a diode or large resistor, these effects are enhanced and the shape, duration, and amplitude of the output signal become independent of the input signal. These results are possible because once the circuit has been triggered and the feedback loop gain is greater than unity, the response proceeds independently of input conditions and is determined solely by the transistor and circuit parameters.

By definition a regenerative amplifier must have positive feedback sufficient to cause instability during the transition period between the "off" and "on" states. When investigating various circuits, it is necessary to eliminate circuits which are never unstable when a pulse is applied to the input circuit. If the circuit is unstable under either of the conditions shown in Fig. 3, sufficient instability is possible. However, if the circuit is stable, linear, and either the small signal open circuit voltage gain or the short circuit current gain is less than unity or negative at all frequencies, it is impossible to have instability. These latter conditions for instability often can be easily checked by inspection without tedious computation or experimentation.

This use of positive feedback requires that attention be given to its control. To be useful, the amplifier must be stable in one state and at least quasi-stable in the other state. The change from instability in the transition period to stability in the end states is accomplished by a nonlinear change in the gain or impedance of some element in the feedback loop. Usually the "off" state is made stable by causing the voltage and current conditions in the input circuit to reverse bias the transistor input. The "on" state may be made stable (or quasi-stable when there are reactive coupling elements in the loop) in several ways. For example, the transistor may be permitted to saturate when the desired pulse voltage is reached; a "catching" diode may be used to clip the pulse voltage at an appropriate level; or a current switch may be used to



(a) OPEN-CIRCUIT LOOP VOLTAGE

(b) SHORT-CIRCUIT LOOP CURRENT

Fig. 3 — A check for instability.

introduce an impedance in the feedback loop at a predetermined current level.

The degree of stability of the amplifier in the "on" state may be thought of as the amount of power required to initiate the transition to the "off" state. During the early portion of the output pulse duration the degree of stability should be large, but near the end of the pulse duration it should be relatively small to make turn-off easier. Also, the degree of stability should not change over the range of output loading expected for the amplifier and should be effected without excessive wastage of pulse or supply power. These conditions are difficult to fulfill when the range of output load current may be as large as 20 to 1.

Three methods of obtaining positive feedback in transistor circuits will now be considered: (a) negative resistance feedback; (b) capacitor coupled feedback; and (c) transformer coupled feedback. Of these, transformer coupled feedback appears to be the best for most applications. It will be assumed that the type of feedback under discussion is the dominant or only type present; circuits employing more than one feedback mechanism generally violate the premise of simple circuitry and will not be discussed.

3.1 *Negative Resistance Feedback*

With the advent of point contact transistors a novel form of negative resistance was offered to circuit designers for use in positive feedback applications.[5] This negative resistance property occurs when the current gain of a transistor is greater than unity and the emitter and base small signal currents are in phase.* At first sight this property appears to lead to attractively simple regenerative amplifiers. However, as systems become more complex and, consequently, amplifier requirements more severe, the original simplicity often is lost due to the additional circuitry required to control the negative resistance. An example, shown in Fig. 4, is similar to a regenerative amplifier described by J. H. Felker.[2] The functional circuits are indicated by dashed outlines.

This amplifier operates at a one megacycle pulse repetition rate with one-half microsecond, three volt pulses. It is capable of driving from one to six similar amplifiers. The output pulse rise time is 0.05 microsecond, the average dc standby power is 33 milliwatts, only a few components operate at as much as half of maximum ratings, and the supply voltage margins† are greater than ±15 per cent. Seven hundred of these ampli-

* Although point contact transistors are noted for this property, certain types of junction transistors also exhibit it. For example, see Reference 7.

† Supply voltage margins, the amount by which the supply voltage may be

fiers operated in a system for over 17,000 hours with a failure rate of slightly less than 0.07 per cent per thousand hours.

These features, however, are obtained at the expense of relative complex circuitry. This negative resistance type of high speed regenerative amplifier has the following inherent limitations.

1. The degree of stability in the "on" state depends critically on the collector current. In the example a dummy load must be strapped in when the amplifier drives less than four logic circuits.
2. A steering diode (D3) and a timing circuit diode (D1) have critical reverse recovery time[6] specifications.*
3. The requirements on transistor parameters (primarily the dynamic alpha versus emitter current and base resistance characteristics) are relatively critical.
4. A relatively large amount of synchronizing power is required.
5. With transformer output coupling (as discussed in Section 5.1) a large amount of the total standby power is absorbed by a circuit required to protect the transistor in case the timing voltage fails (In the example 21 milliwatts, or 64 per cent of the standby power, is absorbed by R3.)

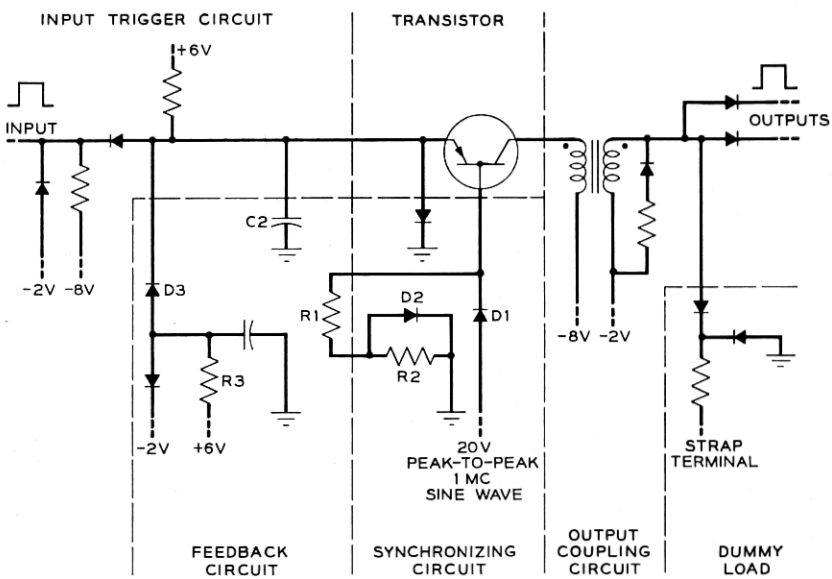


Fig. 4 — Negative resistance feedback amplifier.

varied without causing an operational failure, are an indication of the sensitivity of the amplifier to changes in component values.

* At lower pulse repetition rates this property may not be critical.

The use of an inductor, instead of a resistance, in the base lead does not appear to mitigate the limitations.

3.2 *Capacitor Coupled Feedback*

A second method of obtaining positive feedback is by external coupling through a capacitor or capacitor-resistor network. This method is seldom used for the principal feedback for reasons to be mentioned. Occasionally, in conjunction with some other type of feedback, it may be used to provide additional feedback during the rise time of an amplifier.

Since the voltage and current gain of a capacitor can not exceed unity, the open circuit voltage gain and the short circuit current gain of the rest of the loop (Fig. 3) must be greater than unity for instability. This criterion indicates that capacitor feedback is limited to point contact, or other transistors with an alpha greater than unity, or to a junction transistor in the common emitter configuration.*

A circuit with capacitor feedback around a short-circuit stable point contact transistor might take the form shown in Fig. 5. Although this type of circuit has the merit of simplicity, it has the following limitations:

1. The initial feedback current is highly dependent upon the incremental output load impedance. This may result in a failure to trigger when the load approximates a short circuit, as in the case of diode gates or a large stray capacitance.

2. The degree of stability in the "on" state is critically dependent on the load current and the collector supply voltage. Variations in either may cause a foreshortened output pulse or require an excessive timing signal current for turn-off.

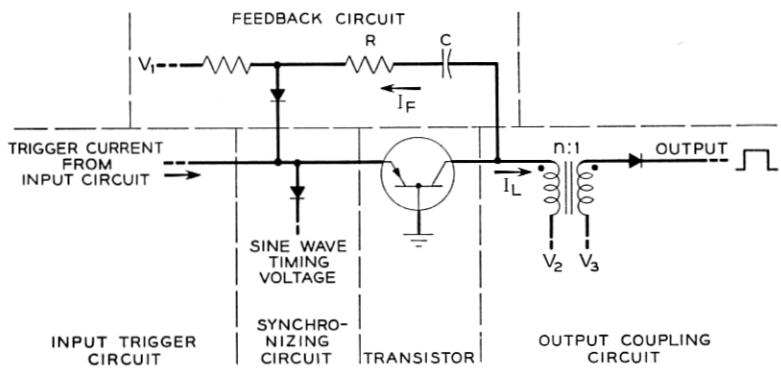


Fig. 5 — RC feedback amplifier.

* An inverting transformer is necessary with the junction transistor.

3. The necessity of a feedback circuit time constant equal to or shorter than the output pulse length results in a relatively low output power efficiency.

Due to the above considerations, capacitor feedback appears to be the least attractive type of feedback.

3.3 *Transformer Coupled Feedback*

A transformer appears to be the most convenient and versatile component for feedback coupling in a regenerative amplifier. The pertienent features* of a transformer are:

1. Current or voltage gain (impedance matching.) This feature permits full use of the power gain of the transistor, even if such gain be in the form of voltage or current gain only.
2. Bias isolation between circuit parts and the possibility of supplying dc voltage bias without the use of additional elements.
3. Phase inversion, if desired.

All of these features, conveniently combined in a transformer, provide great design freedom to meet specified circuit objectives. Since positive feedback is possible with any type of transistor (with power gain, of course), the choices of transistor and connection are determined by other circuit requirements.

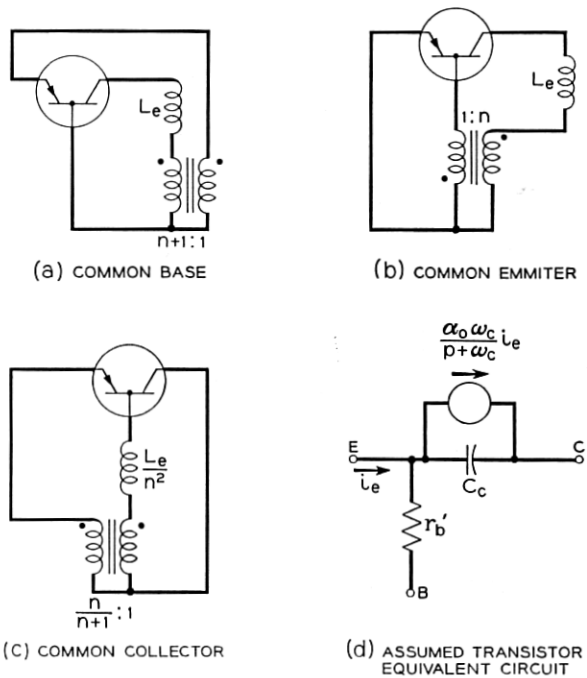
The use of transformer coupled feedback yields the familiar blocking oscillator circuit. An important feature of this circuit is the fast rise time that is obtainable. Linvill and Mattson[4] have shown that a junction transistor with an alpha cutoff frequency of two megacycles may exhibit a rise time of 0.1 microsecond in an unloaded blocking oscillator with collector to emitter coupling, Fig. 6 (a). It can be shown that the same response may be expected with collector to base or base to emitter coupling, provided that the transformer turns ratio is modified, Figs. 6 (b) and 6 (c). When the circuit is providing useful output power into a load, a slightly different turns ratio would be used for optimum rise time, which may be appreciably slower than in the unloaded case. However, it should be noted that the foregoing gives no information about the initial response of the circuit from the time that the input trigger is applied until the output reaches ten per cent of its final value. In some instances this initial time, which is a complicated function of the transistor non-linearities, may be comparable to the output rise time.

In a blocking oscillator circuit with a fixed output load, the degree of stability in the "on" state decreases with time. The reason is that the

* The operation of a transformer over the non-linear portion of its magnetization characteristic is outside the scope of this paper.

voltage across the coupling transformer, which is approximately constant during the pulse duration, causes an increasing magnetizing current to be subtracted from the initial feedback. When the feedback current can no longer support the required output current, the circuit turns off. In a synchronized amplifier the value of the feedback transformer mutual inductance may be specified to give the desired degree of stability at the end of the predetermined pulse length. Thus, the least stable condition occurs at the end of the pulse duration and is under the circuit designer's control. At other times during the pulse duration the circuit is more stable, which reduces the possibility of premature turn-off.

Other considerations, such as stability variations with output current, power dissipation, and output voltage regulation, depend upon whether the output load is in series or in shunt with the feedback loop. Therefore, these considerations are discussed in connection with output coupling in



L_e = LEAKAGE INDUCTANCE OF TRANSFORMER
n = TURNS RATIO FOR COMMON EMMITER CONNECTION
α_0 = LOW FREQUENCY VALUE OF COMMON BASE SHORT CIRCUIT CURRENT GAIN
ω_c = CUTOFF RADIAN FREQUENCY OF α

Fig. 6 — Transformer coupled blocking oscillator circuits.

Section 5.2. For constant voltage, variable current loads, transformer coupled feedback with the output load in series with the feedback loop results in low power dissipation, relatively small degree of stability variations versus output current variations, and non-critical components. The possible limitations are that transformers generally are more expensive than other passive components and are not as readily available in a variety of stock values.

4. INPUT TRIGGER CIRCUITS

The primary function of the input trigger circuit is to initiate the transition from the "off" to the "on" state when there is an input signal. At all other times the input circuit must provide a threshold or margin against false triggering due to noise or spurious disturbances.

Although the input circuit must supply sufficient energy to establish regeneration, it is unnecessary and undesirable that any additional energy be supplied. To do so reduces the gain of the amplifier, since gain may be defined as the ratio of the output power to the input power during one cycle of operation. Because regeneration makes the input and output power independent of each other, any reduction in input power results in greater amplifier gain.

In an amplifier with external feedback coupling it is possible, but not always practical, to have the input circuit trigger the transistor at the collector, base, or emitter terminal. The collector terminal seldom is selected because then the input circuit must supply energy to the output load as well as to the transistor. Also, the base is usually not used (except occasionally with negative resistance feedback) because extra components are required to steer the triggering energy into the transistor and it is diffiult to apply a timing signal.* However, the following discussion and the dc input characteristic of Fig. 7 (a) are equally valid for triggering at the base or emitter terminal of junction or point contact transistors which are short-circuit stable.

One of the simplest types of triggering circuits is shown in Fig. 7 (b). The voltage and current increments assumed necessary to initiate regeneration are designated V_t and I_t. Therefore, the required input signal voltage V_s and current I_s are:

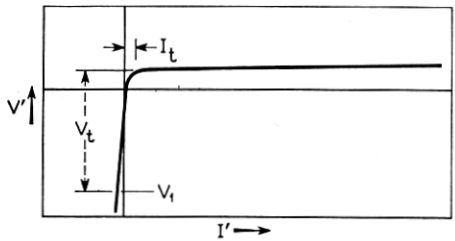
$$V_s \geqq V_t + I_t R_1 \tag{1}$$

$$I_s \geqq I_t \left(1 + \frac{R_1}{R_2}\right) + \frac{V_t}{R_2} + \frac{V_1 - V_2}{R_2} \tag{2}$$

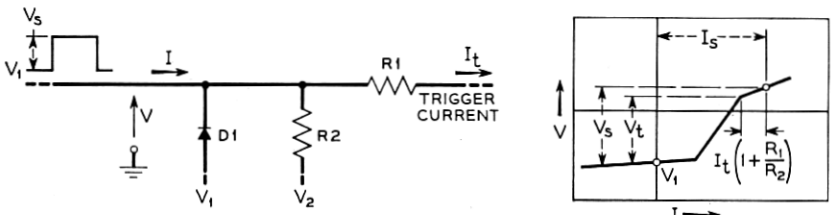
* Also, for junction transistors, about twice as much energy is required to trigger at the base as at the emitter.[4]

The purpose of diode D_1 is to provide a low impedance current threshold, the amount of current given by the last term of (2). This type of threshold is especially effective for preventing false operation from electrostatically induced crosstalk. Also, it allows a faster rate of discharge of stray capacity on the input terminal at the end of the input pulse period.

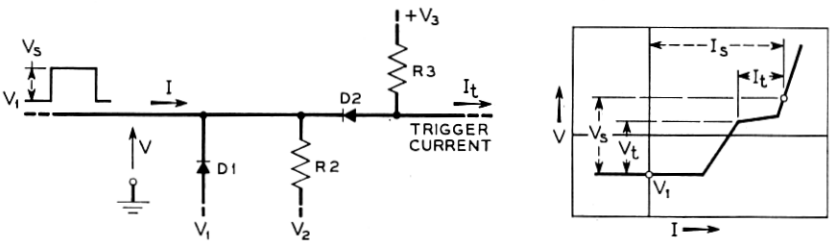
Although the circuit of Fig. 7 (b) is attractively simple, it is undesirably sensitive to variations in signal voltage. An increase in the input pulse voltage causes excessive triggering current and a decrease may easily result in failure to trigger. Since the circuit must be designed to operate reliably with the smallest expected input pulse, it is wasteful of input power with the average amplitude of input pulse.



(a) TRANSISTOR INPUT CHARACTERISTIC



(b) SIMPLE INPUT CIRCUIT



(C) ONE TERMINAL AND-TYPE INPUT CIRCUIT

Fig. 7 — Input trigger circuits.

The single terminal AND-type circuit[9, 10] Fig. 7 (c) has the desirable characteristics of the previous circuit, and is relatively insensitive to input signal variations. In this circuit the input pulse switches the current through R3 into the transistor input and then encounters the relatively high resistance R2, as compared to the parallel resistance of R2 and R1 in Fig. 7 (b). The blocking action of D2 thus reduces variations in the input signal current. However, R2, R3, V_3 and V_2 cannot be increased without limit to reduce the variations; the dc power dissipated in R2 and R3 would become excessive.

Another advantage of the AND-type circuit is that several inputs may be paralleled with a common R3 to provide an AND logic function as well as an input trigger function. This feature, when desired, saves components and does not reduce the gain of the amplifier.

When both the input circuit and the feedback circuit terminate at the same transistor input terminal, as is usually the case, some additional components are generally required to prevent one circuit from shunting the other circuit. To steer the trigger current into the transistor, a diode may be placed in the feedback path so that the diode is reverse biased except when there is feedback current. Similarly, a diode or a resistor may be placed in the input circuit so as to prevent the feedback current from flowing into the input circuit.*

Although the discussion has assumed positive polarity input pulses, the remarks apply equally well to negative pulses if the polarity of the diodes and the supply voltages are reversed.

It is recognized that the preceding remarks assume that the minimum triggering energy is known and that a step function of current or voltage is the optimum form of the triggering energy. Actually, until a study is made of the circuit and transistor parameters (including the non-linear aspects) that affect the initial triggering before the feedback is established, the design of an optimum input trigger circuit will remain an experimental art. Experience with the AND-type input circuit has indicated that appreciably more current is required to trigger junction units than point contact units.

5. OUTPUT COUPLING CIRCUITS

In addition to the obvious function of efficient power transfer from the amplifier to a load, the output coupling circuit is a convenient point at which to perform other functions, as for example, dc level restoration

* This precaution is not necessary if the transistor input exhibits appreciable negative resistance.

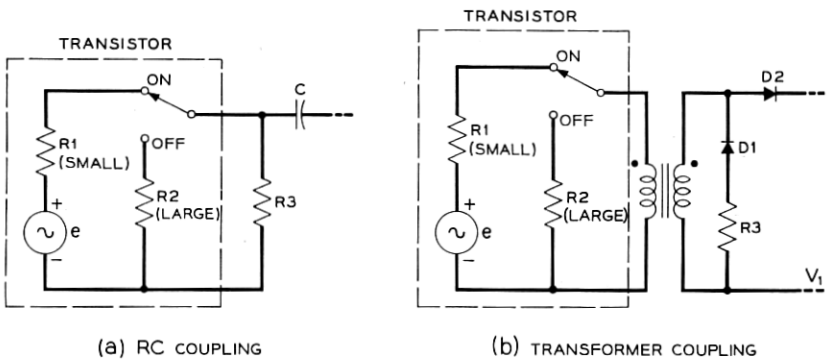
and pulse inversion. In a system of logic circuits interspersed with amplifiers at regular intervals, it is apparent that the dc level at similar points, such as the outputs of the amplifiers, must be identical if the amplifiers are to be interchangeable. Without some circuit or element to restore the dc level, the levels along the transmission path will monotonically decrease* due to the dc voltage loss through the logic circuits and across the transistor in the amplifier. The output circuit is one point where restoration of the dc level may be readily combined with other functions.†

In the following two sections three methods of output coupling are discussed and the interaction between the output and feedback circuits is considered.

5.1 *Output Coupling Elements*

Three types of coupling circuits are RC, transformer, and diode coupling. Each of these methods permits the dc level of the signal pulses to be corrected to a predetermined level. However, the restoration,‡ efficiency, and versatility characteristics of each circuit are quite different.

Although RC coupling is common in linear amplifiers, it is seldom used in transistor pulse amplifiers that operate at duty cycles near 50 per cent. The reason is that the time constants encountered do not permit both proper restoration of the capacitor and high efficiency of the output circuit. As indicated in Fig. 8 (a), the transistor is a low impedance in



(a) RC COUPLING (b) TRANSFORMER COUPLING

Fig. 8 — Reactive output coupling circuits.

* Decrease for positive pulses; increase for negative pulses.

† An exception, to be discussed, is diode output coupling where it is occasionally more convenient to correct the dc level in the input of the logic circuits or the amplifier.

‡ This refers to restoration of a reactive element (i.e., the return to a quiescent state) and is not to be confused with restoration of the dc level of a circuit.

the "on" state and a high impedance in the "off" state. Since C must be relatively large to make the voltage drop across it small during the pulse duration, R3 must be equal to or smaller than R1 for satisfactory restoration (50% duty cycle assumed). But then the current transmission efficiency of the coupling network is less than 50 per cent because generally R1 is smaller than the input resistance of the driven circuits during the pulse duration. Unless the pulse length is only a small fraction of the pulse repetition period, it is seldom possible to effect a suitable compromise. Also, it might be noted that variations of I_{co} current, which flows through R3, cause variations in the output pulse amplitude. Finally it is not possible to obtain pulse inversion.

A transformer coupled circuit, Fig. 8 (b), works efficiently with a transistor. Diode D2 isolates the transformer from the load and interlead stray capacitance during the interdigit period* so that the restoration time of the transformer is controlled by the value of R3. The restoration time is approximately proportional to the mutual inductance divided by the total shunting resistance. Diode D1 prevents R3 from shunting down the output during the pulse duration, thus permitting high output efficiency and proper restoration.†

As noted in Section 2, the maximum output power from the transistor is determined by the maximum collector voltage (as set by breakdown or punch-through) and the maximum collector current consistent with the permissible dissipation in the transistor. Usually this maximum voltage exceeds the desired amplifier output voltage and, occasionally, the maximum collector current is insufficient; in such instances a voltage step down is desirable. When the transistor is not required to operate at maximum power dissipation, it often is advantageous to balance the "off" and "on" power dissipation. An increase in the collector supply voltage increases the "off" power and decreases the "on" power (by decreasing the required collector current for the same output power). Thus the collector voltage may be adjusted to give the lowest total power dissipation consistent with the average duty cycle of the amplifier. The transformer turns ratio is specified to match the optimum collector voltage to the desired output voltage. Furthermore, I_{co} variations have negligible effect on the output voltage amplitude and pulse inversion (if desired, for example, for inhibition) is possible. For these reasons transformer coupling appears to give optimum output coupling performance.

* The minimum time interval between the end of one pulse and the beginning of a succeeding pulse; for a 50 per cent duty cycle the interdigit period is equal to the pulse duration.

† Occasionally it is possible to specify the collector impedance, the transformer losses, and the reverse impedance of D2 so that D1 and R3 are not necessary.

A third method of coupling, which is attractive for systems using only AND- and OR-type logic, utilizes the reverse characteristic of a breakdown diode, Fig. 9 (a). The interesting feature of this diode is the sharp transition between the high and low incremental resistance regions of the reverse characteristic. With this diode it is possible to shift dc levels by an amount equal to the reverse breakdown voltage of the diode, as indicated in Fig. 9 (b). In the quiescent state D2 operates in the breakdown region and D1 serves to clamp the collector voltage at $-V_3$; during the pulse duration D2 operates in the high resistance portion of its reverse characteristic. If the driven circuit has a voltage threshold, like the transistor threshold in Fig. 7 (a), less than $-V_3 + V_B + V_s$ and $V_s < |V_B|$, the circuit operates like a normal AND-type circuit except for the dc level change. For this reason it is convenient with AND-OR logic circuits to include only D1 and R2 in the output circuit of the amplifier and use D2 and R1 as the AND input elements in the logic circuits.

The principal advantages of diode coupling are simplicity and the lack of an energy storage element. The limitations are that there is no opportunity to match transistor and output conditions, variations in

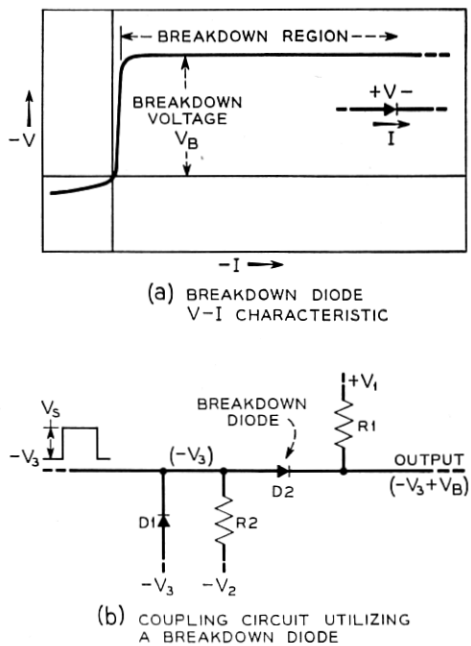
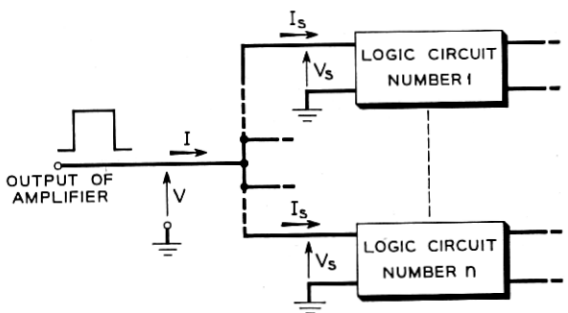


Fig. 9 — Direct output coupling circuit.

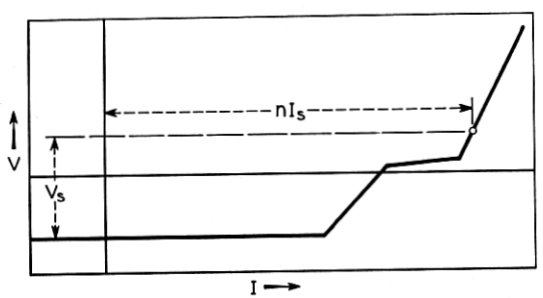
diode breakdown voltage reduce amplifier margins, and pulse inversion is not possible. For these reasons diode coupling has limited utility, but is attractive for some applications.

5.2 *Connection of Output and Feedback Circuits*

The performance of the amplifier is greatly affected by the method used to connect the output circuit and the feedback circuit together at the output of the transistor. Should these two circuits be connected in a shunt or a series fashion? Performance features, such as rise time, sufficient output voltage, degree of stability versus load current variations, and power dissipation directly depend upon this choice. With transformer output coupling, the choice always exists; with other types of output coupling the choice may or may not exist, depending upon the type of feedback coupling. The following discussion is in terms of transformer coupled output and feedback circuits and the general conclusions may be extended to other cases.



(a) CONNECTION OF AMPLIFIER LOAD



(b) V-I CHARACTERISTIC OF AMPLIFIER LOAD

Fig. 10 — Output load characteristic.

The principal factor that influences the choice of the output-feedback connection is the nature of the output load of the amplifier. In the majority of computer and switching systems the amplifier must drive a multiplicity of paralleled load circuits, as indicated in Fig. 10 (a). The input characteristic of each load circuit is assumed to be of the threshold type, like the AND-type input characteristic of Fig. 7 (c), which results in the amplifier load characteristic of Fig. 10 (b). During the initial portion of the rise time of the output pulse the incremental impedance is almost zero and during the remainder of the pulse duration it is relatively large. Due to the voltage threshold nature of the load, the amplifier load variations are current variations at a constant voltage. The minimum current is encountered in the system position where the amplifier drives the smallest number of logic circuits, often a single logic circuit; the maximum current is limited by the maximum output power of the amplifier. Although a desirable ratio of maximum to minimum current may be as high as 20:1, the amplifier is expected to exhibit optimum performance at any load current within this range.

The shunt connection of the output and feedback circuits is illustrated in Fig. 11.[12] Windings $1:n_1$ constitute the feedback coupling and $1:n_2$ the output coupling. The two circuits shunt each other in the sense that the ratio of the feedback to the output current is determined by the ratio of the impedance of these circuits as modified by the turns ratio of the transformer.

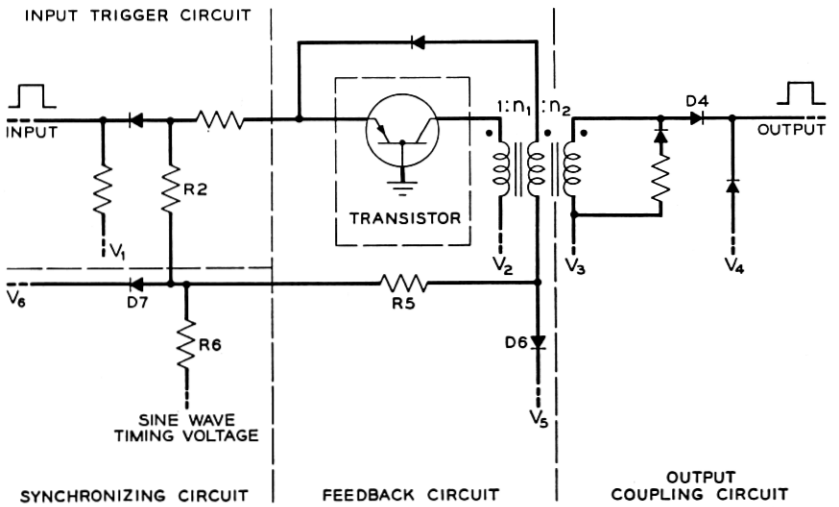


Fig. 11 — Shunt connection of output and feedback.

There are two limitations associated with this output-feedback connection. In the first place there is the possibility of insufficient output voltage, slow rise time, or complete failure of regeneration. This is caused by the shunt effect of the output load which places an almost zero initial incremental impedance across the feedback path. In order to overcome this limitation a current switch (R5 and D6 in Fig. 11) is used to obtain a low initial feedback impedance and the output diode (D4) is reverse biased so that the initial load impedance is large. The price paid is the undesirable power dissipation in the current switch. Moreover, stray capacity across the output terminal or a load current that exceeds the design value may still result in a long rise time, low output voltage, or regeneration failure.

The series connection of the output and feedback circuits is shown in Fig. 12. In this connection the output load is in series with the feedback loop. Thus, the transistor output current, feedback current, and output load current are all proportional to each other. This situation assures regeneration regardless of output load current variations.

The regeneration cycle of the series type amplifier is as follows. In the quiescent state diode D2 is reverse biased by V1 to prevent false triggering. After the arrival of an input signal, the timing signal voltage goes positive and steers the trigger current into the transistor. No

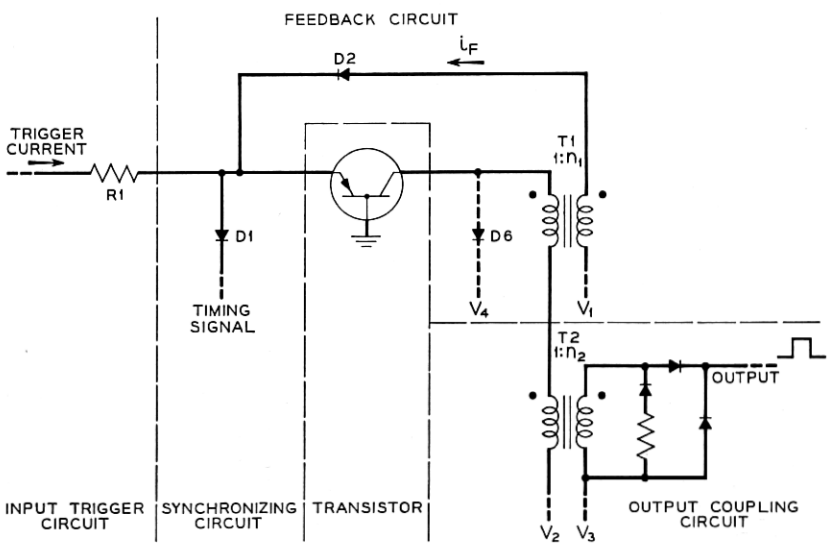


Fig. 12 — Series connection of output and feedback.

appreciable output current flows until the voltage across transformer T1 is sufficient to forward bias diode D2. Then both the feedback and output current build up simultaneously and rapidly since the turns ratio $1:n_1$ of T1 is selected to give a feedback loop gain greater than unity. When the sum of the voltages across the primaries of the feedback and output transformers almost equals the collector supply voltage, the transistor saturates and stabilizes the feedback loop. At the end of the pulse duration the timing signal voltage goes negative and robs current from the feedback loop, thus forcing the transistor out of saturation and causing the amplifier to turn off.

Because the feedback current is proportional to the output current during the rise time, the amplifier can deliver any value of load current up to the current corresponding to the maximum allowable collector current. Also, assuming that the leakage inductances of the transformers are small, a large stray capacitance across the output terminal does not appreciably degrade the rise time. Since a current switch is not necessary, the standby power dissipation in the feedback loop is negligible. These are the outstanding features of the series connection.

Two important performance considerations of the series type amplifier are the change in the degree of stability versus load current variations and the action of the amplifier when the timing signal fails. Both of these items may be controlled by the selection of suitable values for the turns ratio and the primary inductance of the feedback and output transformers.* In order to prevent burnout of the transistor in the event that the timing signal fails, the amount of excess feedback current must decrease during the pulse duration. Due to the low impedance of the feedback loop, this condition may be approximately† stated in terms of the primary inductances as:

$$\left|\frac{V_1}{n_1 L_1}\right| > \left|\frac{V_2 - \frac{V_1}{n_1} - V_{\text{sat}}}{L_2}\right| \left|1 - \frac{n_1}{\alpha}\right| \tag{3}$$

where V_{sat} is the collector saturation voltage and L_1 and L_2 are the primary inductances of T_1 and T_2 respectively.

The degree of stability in the series amplifier at the end of the pulse duration is proportional to the output load current. This situation may be seen more clearly if a "catching" diode (D6 in Fig. 12) is added to the

* If the transistor is not short circuit stable, it is also usually necessary to use a small resistance in series with the emitter.

† The principal approximation is that alpha is constant versus collector current. The value of alpha at the end of the pulse duration is a conservative value.

circuit to prevent saturation in the transistor.* Because the feedback loop gain, as determined by the alpha of the transistor and the turns ratio n_1, must be greater than unity for regeneration reasons, there will be current flow through D6 during the pulse duration. This current is proportional to the degree of stability. An increase Δi_{out} in the output current causes an increase of

$$\Delta i_c = \frac{\alpha n_2 \Delta_{i\text{out}}}{n_1} \tag{1}$$

in the collector current. Therefore, the current in D6 increases by an amount equal to

$$\Delta i_{\text{D6}} = \left[\frac{\alpha}{n_1} - 1\right] n_2 \Delta_{i\text{out}} \tag{5}$$

This variation in the degree of stability may be reduced by selecting α/n_1 close to unity and reducing n_2. However, since it is desirable to have α/n_1 much larger than unity for short rise time and since any reduction in n_2 increases the I_{co} standby power,† a compromise is necessary.

6. SYNCHRONIZING CIRCUITS

The majority of modern digital data processing systems employ coincidence gate circuits to perform the logical functions. In order to insure that digit pulses will coincide at the inputs to the logic circuits, it is convenient to synchronize the amplifiers. Usually a master oscillator, or "clock," produces the timing signals that are distributed to the amplifiers. The function of the synchronizing circuit in the amplifier is to turn on and to turn off the amplifier at predetermined time intervals in response to the clock signal.

In a regenerative amplifier there is always a small delay from the time triggering commences until the full output pulse is developed. Then there are variations in the transmission time to other amplifiers. For these reasons the clock signal must lag the input signal to the amplifier in order to maintain control of turn-on and to obtain a uniform pulse length from all amplifiers. Generally the time lag is one-fourth of the

* In an actual amplifier D6 is not required if the transistor saturation voltage is relatively constant versus collector current and the pulse fall time is not adversely affected by minority carrier storage in the transistor. Often the inductive "kick" of the transformers and the regenerative feedback are sufficient to make the minority carrier storage effect negligible. If D6 is used, its reverse recovery time may adversely affect the pulse fall time, thus nullifying its usefulness.

† The I_{co} standby power is proportional to V_2, which, for a given output voltage, is inversely proportional to n_2.

repetition period and, in such a case, the clock signal is made available in four phases.

Although the clock signal may have any one of a number of forms, a sine or a square wave are the most common forms. Usually a sine wave is preferred because it is simpler to distribute to a large number of amplifiers. Exceptions occur in cases where exceptionally precise timing is necessary, or the use of a square wave requires considerably less clock power. In the following discussion of where to synchronize, a square wave will do as well or better than the assumed sine wave. With either signal it is desirable to keep the clock power to a minimum.

If the synchronizing circuit is to be effective, the clock signal must be capable of accomplishing the following actions:

a. It must be able to hold the transistor in the "off" state in the presence of trigger current in order to control turn-on.

b. At the turn-on time it must rapidly inject the trigger current into the transistor.

c. At the turn-off time it must alter the conditions in the feedback loop in such a manner that the transistor turns off promptly.

In other words the synchronizing circuit must act like an inhibit logic circuit with the clock signal appearing as the inhibit signal during the interdigital period.

It is recognized that there are many amplifier configurations and several ways to synchronize each configuration. Generally it is preferable to synchronize at only one input terminal of the transistor or at only one point in the feedback circuit. A relatively complete discussion can be given with the aid of the following four examples.

A circuit that employs negative resistance feedback, such as in Fig. 4, requires a relatively large amount of clock power for synchronization. Because a capacitor (C2) is required on the emitter for regeneration,[2] the clock signal must be applied to the base of the transistor to control turn-on accurately. As far as turn-off is concerned, another clock signal might be applied to the emitter or to the current gate in the feedback circuit. However, this would result in additional components, a second clock signal 180° out of phase with the base clock signal, and approximately the same required clock power as if the base clock signal alone were used. Turn-off at the emitter is impractical due to the negative resistance characteristic. The power that the clock signal on the base must furnish is made up of two parts. One part is the average standby power that is absorbed every time the clock voltage is positive. It is composed of the I_{co} power supplied to the transistor plus the power dissipated in in R1 and R2. R2 and D2 serve to reduce the clock current in R1 and

R2, but the maximum value of R2 is limited by stray capacitance from the transistor base to ground.* The average clock standby power for this circuit (with a 10 volt peak clock voltage) is approximately 13 milliwatts. The second part of the clock power occurs at turn-off when the clock must supply approximately the full "on" state collector current. In this design the clock supplies about 20 milliamperes of current for 0.1 microsecond at voltages up to about 6 volts peak before the transistor turns off. Therefore, a negative resistance feedback circuit usually requires a relatively large amount of standby clock power continuously and a high peak clock power at turn-off. Also it should be noted that diode D1 must have a short reverse recovery time in order to prevent false triggering during the negative portion of the clock cycle.

A second example of synchronization is shown in Fig. 11. Here the clock signal is introduced in the feedback circuit to control turn-off. It is also applied to R2 in the input circuit so as to control turn-on. In this circuit most of the clock power is dissipated in R5 and R6 when the clock voltage is positive during the output pulse time slot (whether or not an output pulse is produced). Necessarily, this power is relatively large because the clock must supply the full amount of feedback current. Also, it is necessary to clip the positive peak of the clock voltage in order to prevent false triggering via R2 when there is no input pulse. A square wave clock signal would eliminate the need for R6 and D7, but would not change the power in R5. The average clock power in a typical circuit of this type is approximately 20 milliwatts, which is relatively large. The principal advantage of this method is that diode reverse recovery time is not a problem.

A third method of synchronization is to apply a square wave clock signal (a sine wave is not suitable in this case) between the base of the transistor and ground (for example, assume in Fig. 11 that R2 and R5 are returned directly to V6 and that the base of the transistor is the clock terminal instead of ground). Before turn-on the clock voltage must be more positive than the trigger voltage on the emitter. At turn-on the clock voltage drops rapidly to ground potential and triggering takes place. During the pulse duration the base current of the transistor is supplied by the clock source. At turn-off the clock voltage must rise rapidly several volts until D6 conducts and robs current from the feedback loop. The clock power required by this method is relatively large (order of 20 milliwatts) for point contact transistors because the base current of such units is large. In a junction transistor with alpha close

* The capacitance causes the base voltage to lag the clock voltage at turn-on if R2 is large, which degrades the timing.

to unity the base current is small and the required clock power may be as low as 3 milliwatts. However, it should be noted that this method of synchronization applies only to amplifiers with a gated feedback circuit (such as R5 and D6 in Fig. 11). In other circuits (Fig. 12, for example), a clock voltage applied to the base terminal of the transistor may never be able to turn off the transistor (the feedback current may actually increase instead of decrease). Thus, this method of synchronization is limited and is a low power method only when used with junction transistors.

A fourth synchronization method, which avoids the limitations cited in the previous examples, is illustrated in Fig. 12. The timing circuit is simply diode D1. The operation of the circuit, which is like an inhibit logic circuit, is as follows. When trigger current commences, the clock voltage is negative and D1 conducts the trigger current away from the emitter terminal. As the clock voltage rises positiveward, the emitter voltage follows until it reaches the threshold voltage of the transistor, usually ground potential. Then the trigger current flows into the transistor which turns on. As the clock voltage continues positiveward the emitter conduction clamps the emitter voltage so that D1 opens and the clock does not shunt the feedback path during the pulse duration. At the end of the pulse duration the clock voltage goes negativeward through ground potential and D1 becomes conducting. This action robs current from the feedback loop, thus causing the transistor to turn off. If no input pulse is present, D1 is always non-conducting and any small reverse leakage current is drained off through R1 (which is returned to voltage V1).

Because diode D1 is always non-conducting when no input pulse is present, the standby clock power is essentially zero. During a pulsing cycle the clock conducts only a small current before turn-on and only instantaneously at a low voltage at turn-off. Hence, the required clock power is usually less than two milliwatts.

It is important to note that the amplitude of the negative peak of the clock voltage usually should not be more negative than the quiescent bias voltage on the emitter. If it should be, D1 will conduct and, due to minority carrier storage, may cause false triggering when the clock voltage goes positive. The current through D1 at turn-off might have the same effect in the succeeding cycle except that the flyback voltage of the transformers during the interdigit period removes the minority carriers from both D1 and D2. Since D2 carries a larger current for a longer period than D1, the carriers are cleared from D1 first. It is then reverse-biased for almost one-half the repetition period before there is any chance

of false triggering. Hence, diode reverse recovery time is not a problem. However, D1 should have a short forward recovery time in order that turn-off will occur rapidly.

One possible limitation of this synchronization method is that a low impedance clock source is necessary. This is usually not difficult to obtain with a resonant circuit in the output of the clock signal source. Offsetting this point are the advantages of low clock power, esentially zero standby clock power, only one additional component, and no critical component tolerances.

7. ILLUSTRATIVE DESIGN

In the preceding sections the features of various configurations for the functional circuits of an amplifier have been described. The following discussion illustrates the application of these ideas to an amplifier design for use in a digital computer system. It is intended that the description of the design philosophy be sufficient to permit its application to other systems.

In the computer under consideration the amplifier is to be combined with a single level, diode logic circuit to form a logic network. The logic networks, together with delay lines, will be connected in appropriate arrays to perform the logic functions of the sytem, such as addition, multiplication, etc. Digital information is to be represented by one-half microsecond pulses and the amplifiers are to be synchronized at a one megacycle pulse repetition rate by a four phase sine wave master oscillator. Other system requirements are mentioned in connection with the selection of the corresponding functional circuit.

Since the amplifier is considered as a small system of functional circuits, it is necessary, as in most system designs, to re-examine, and possibly change, circuit choices as the design progresses. However, for the sake of clarity, the following discussion omits the re-examination and frequently refers to the final schematic shown in Fig. 13.

The first step in the design is to select the feedback configuration most suitable to the computer requirements. For this computer the dc and clock power are to be minimized and the amplifier should be able to drive from 1 to 12 logic networks. Miniaturization of the computer implies that there may be an appreciable amount of stray capacity across the amplifier output. These considerations suggest transformer coupled feedback connected in series with an output circuit. Since both positive and negative output pulses are to be required (one polarity for AND and OR logic and the other polarity for inhibition), transformer output coupling is indicated.

The next basic selection is the choice of an appropriate transistor. In this computer it is expected that pulses will occur in only about one third or less of the pulse time slots due to the nature of the digital information. In order to minimize the dc standby power an alloy junction transistor is a logical choice for this application because of the low I_{co} current. However, even with a junction unit possessing an alpha cut-off frequency of eight megacycles, it is difficult if not impossible to obtain acceptable gain and rise time with the desired output load current at a one megacycle repetition rate. If the rise time is improved by increasing the trigger current, the gain is decreased. The principal cause of the poor "gain-bandwidth" appears to be the depletion layer capacitance.[11] The difficulty can be overcome by selecting a point contact transistor. A particular germanium transistor coded GA-52996* appears to be suitable and has the following pertinent characteristics:

a. Collector capacitance less than 0.5 uuf.
b. Alpha cut-off frequency in excess of 80 mc.
c. Base resistance less than 100 ohms.

Since the alpha of this unit is greater than 2 at collector currents of the order of 10 ma, the common base connection will yield the greatest current gain. The disadvantage of a point contact unit, of course, is the I_{co} current. For this reason the amplifier will have to be designed to use the smallest possible collector supply voltage.

The point contact transistor, due to its high cut-off frequency relative to the amplifier pulse repetition rate and its high alpha at small emitter

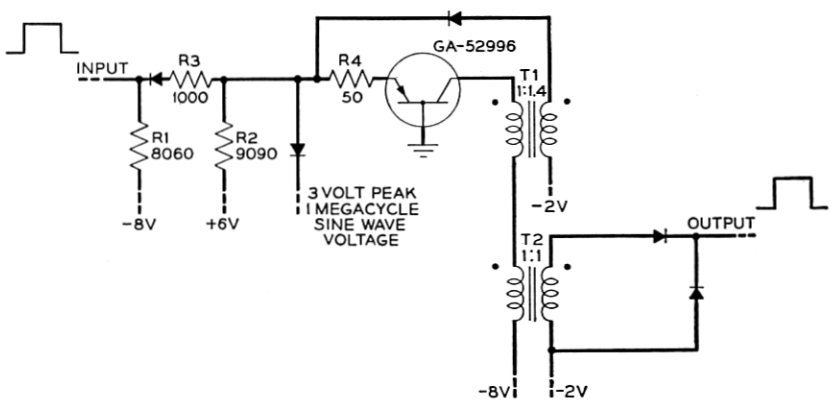


Fig. 13 — Illustrative design

* This is a relatively special unit especially suited for high speed switching applications.

currents,* permits the use of a simple input circuit. The AND type input circuit is suitable and desirable for another reason. When AND type logic is added to the amplifier, it may be paralleled with the basic input circuit and the input sensitivity of the complete network will be the same as for the amplifier alone. Other logic circuits will be added to an amplifier in a manner similar to that described by Felker[2] so that the input sensitivity will be reduced at most by the voltage drop across one series diode (approximately 0.3 volts).

The input pulse voltage and current requirements depend upon the voltage threshold necessary to prevent false operation and the minimum trigger current for reliable regeneration. A test of several sample transistors indicates that approximately 0.3-ma emitter current is required to trigger the transistor with an estimated collector supply voltage of 10 volts. The emitter breakpoint† voltage is found to vary between -0.25 and $+0.25$ volts. To allow for aging variations of the transistor and of R2, it seems reasonable to use a 6-volt source and R2 equal to 9090 ohms, which results in a trigger current a little more than twice the required minimum. Previous experience with computers of this type indicates that a 2-volt threshold will be sufficient to prevent false triggering. Thus, the secondary winding of the feedback transformer is returned to -2 volts and R1 is chosen to give a quiescent emitter voltage of -2 volts. With these considerations and an estimated voltage drop across R3, the input pulse amplitude is calculated to be 2.3 volts and 0.9 ma. Allowing 0.3 volts for a series logic diode, the minimum output voltage and current of the amplifier are 2.6 volts and 0.9 ma per driven network.

The selection of the collector supply voltage and the turns ratio of T2 depends upon the dc power dissipation due to I_{co} current and output voltage regulation versus collector current. For this transistor a unity turns ratio appears to represent a reasonable compromise. Then, by estimating the voltage drops across T1, T2, and the transistor, it is found that a collector supply voltage of -8 volts is sufficient to produce an output pulse voltage about 0.5 volt greater than the required miminum.

The next step is the selection of the turns ratio of T1 and the primary inductances of both T1 and T2. The two considerations involved are sufficient feedback with the minimum output current (the worst case with respect to feedback) and the maximum collector dissipation in the event that the clock fails. By means of the formulas and assumptions indicated in section 5, primary inductance values of 0.4 mh for T1 and

* Usually $\alpha > 4$ for $i_e = 0.5$ ma.
† The transition point of the emitter diode from cut-off to conduction.

0.2 mh for T2 together with a turns ratio of 1.4 for T1 are selected. Since the GA-52996 transistor is not quite short circuit staple, a 50-ohm resistor is added in series with the emitter. The excess emitter current at the end of the pulse duration is greater than 2 ma, thus assuring sufficient stability, and, if the clock fails, the amplifier will turn off by itself in approximately 7 μsec, at which time the instantaneous collector dissipation will be approximately 240 mw (considered to be a safe instantaneous dissipation for this transistor).

For low clock power and circuit simplicity the single diode synchronizing circuit is chosen. Although a peak clock voltage of 2 volts would normally be used (this value corresponds to the quiescent emitter bias voltage) it is found that the clock may be varied between 1 volt and 6 volts peak without a failure occurring. Therefore, the nominal clock voltage is set at a centered value of 3 volts peak. The dc level of the clock voltage is 0 volts, which approximately corresponds to the emitter break point voltage of the transistor. This concludes the basic selections in the design procedure.

The power dissipated in the amplifier is quite modest. In the quiescent state the amplifier absorbs only 0.2 mw average clock power and 30 mw dc power (this would be only 10 mw if the I_{co} power were negligible). When the amplifier is pulsing every microsecond the dc power is 50 mw and the averge clock power is 2 mw. Since the amplifier is so conservative of power, it is possible to use 4,000 networks in a computer and require less than 200 watts dc power.

One indication of the component sensitivity of a pulse amplifier is the magnitude of the supply voltage margins. In this amplifier the supply voltages may be varied, one at a time, over ± 12 per cent of the nominal values before a failure occurs. Generally margins of this magnitude under the worst conditions are considered sufficient to guarantee against failures caused by aging, or to insure that such failures will be indicated by routine checks before they occur. It is interesting to note that in a temperature test the amplifier continued to operate properly over a temperature range from -20 to $+80$°C. Even at $+75$°C the supply voltage margins were 10 per cent or better.

8. SUMMARY

A method of analysis and design procedure have been presented in which a transistor regenerative amplifier is considered as an interconnected system of functional circuits. Each functional circuit may be evaluated or chosen in terms of the requirements of the complete digital system in which the amplifier is to be used. In general no particular cir-

cuit or collection of circuits can result in an amplifier suitable for use in every type of digital system. The use of an AND type input circuit, transformer coupled output and feedback circuits, and an inhibit type synchronizing circuit appear to be an optimum set of functional circuits to make up an amplifier for use in a synchronous digital computer system employing passive logic circuits. An illustrative design is presented for such an amplifier which operates at a pulse repetition rate of 1 mc, uses 12 components (none of which are especially critical), requires an average of 40-mw dc power and 1-mw clock power, is capable of driving from 1 to 12 similar amplifiers, and has voltage margins in excess of 12 per cent. Although the design philosophy was developed for this type of amplifier, it is believed that much of the philosophy is applicable to regenerative amplifiers for use in other digital data processing systems.

9. ACKNOWLEDGEMENT

The final design and the performance data of the illustrative amplifier are due to L. C. Thomas and H. E. Coonce. The author also wishes to express his appreciation for the many helpful and stimulating discussions with other colleagues, especially A. J. Grossman, T. R. Finch, J. H. Felker, and J. R. Harris.

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