The Design of Tetrode Transistor Amplifiers

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The design of tetrode transistor amplifiers encounters problems of the type that occurs with other transistor uses. Desired frequency characteristics, limitations of parasitic elements, and other practical considerations impose constraints on the range of terminations that can be employed. With many transistors, one can terminate a transistor so that it will oscillate without external feedback; this oscillation or other exceedingly sensitive terminations must be avoided.

The two-port parameters of the transistor in any orientation in which it is to be used constitute the fixed or given information which is the starting point of the amplifier design. Using this starting point, methods are developed by which one can select, on simple bases, the kinds of terminations that will be suitable. To facilitate the design of amplifiers, a set of charts has been developed from which one can read power gain and input impedance as functions of the load termination.

Illustrative tetrode amplifiers are described. These include a common base 20-mc video amplifier, a common-emitter 10-mc video amplifier, an IF amplifier centered at 30 mc, and an IF amplifier centered at 70 mc. Predicted and measured gains are compared.

INTRODUCTION

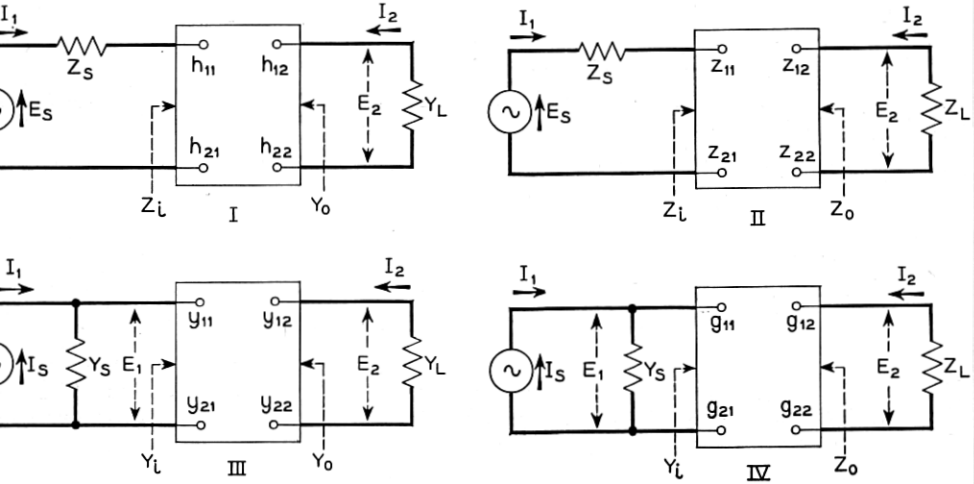
Junction tetrode transistors[1] of the type currently produced for research purposes at Bell Telephone Laboratories are suitable for high-frequency applications. They are being studied for use in video amplifiers, as IF amplifiers where the center frequency is below 100 mc, for oscillators up to 1,000 mc and for very fast pulse circuits.

Their application in amplifiers brings up design considerations similar to those encountered for other transistors but with differences resulting

[1] R. L. Wallace, L. G. Schimpf and E. Dickten, A Junction Transistor Tetrode for High-Frequency Use, Proc. I.R.E., **40**, pp. 1,395–1,400, Nov. 1952.

from different parameter values and variation. The analysis presented in this paper regarding amplifier design was motivated by the study of tetrodes, but the results are equally applicable for other types.

The design of an amplifier begins with a characterization of the transistor which is suitable for the study of its performance as an amplifier. From this characterization, or functional representation, one



CORRESPONDING QUANTITIES			
I	II	III	IV
h_{11}	z_{11}	y_{11}	g_{11}
h_{12}	z_{12}	y_{12}	g_{12}
h_{21}	z_{21}	y_{21}	g_{21}
h_{22}	z_{22}	y_{22}	g_{22}
I_1	I_1	E_1	E_1
E_1	E_1	I_1	I_1
E_2	I_2	E_2	I_2
I_2	E_2	I_2	E_2
E_S	E_S	I_S	I_S
Z_S	Z_S	Y_S	Y_S
Y_L	Z_L	Y_L	Z_L
Z_i	Z_i	Y_i	Y_i
Y_o	Z_o	Y_o	Z_o

RELATIONSHIPS BELOW ARE BETWEEN QUANTITIES IN COLUMN I. CORRESPONDING RELATIONSHIPS ARE WRITTEN DIRECTLY FOR CORRESPONDING QUANTITIE IN ANY OTHER COLUMN.

(1) $E_1 = I_1 h_{11} + E_2 h_{12}$

(2) $I_2 = I_1 h_{21} + E_2 h_{22}$

(3) $Z_i = h_{11} - \dfrac{h_{12} h_{21}}{Y_L + h_{22}}$

(4) $Y_o = h_{22} - \dfrac{h_{12} h_{21}}{Z_S + h_{11}}$

(5) $I_2 = \dfrac{h_{21} E_S Y_L}{(h_{11} + Z_S)(h_{22} + Y_L) - h_{12} h_{21}}$

Fig. 1 — Two-port parameters with summary of relationships.

determines the potentialities of amplifiers employing the transistor and designs a suitable amplifier circuit. This step involves answering two questions: What performance, maximum power gain for instance, is it possible to obtain? What source and load impedances should the transistor be associated with?

Two-Port Parameters of Transistors

For circuit applications, the two-port parameters are the most convenient for characterization of the transistor. These parameters implicitly but completely characterize the device from the performance standpoint.

Four sets of two-port parameters are illustrated in Fig. 1. Any set can be calculated from any other set, and the choice of the set to employ is determined only by convenience in the use of available measuring equipment and the preference of the designer. The relationships between parameters, input and output impedances, voltage and current ratios are summarized on Fig. 1. The same expressions given there for h's can be used for any parameter set so long as one uses the corresponding quantities applicable to the desired parameter set.

Though the transistor can be operated as an amplifier with the base, emitter or collector common between the input and output terminal pairs, the two-port parameters for any of the connections can be used to calculate the parameters for any other connection.

For determination of the two-port parameters of tetrode transistors, R. L. Wallace suggested the use of two-terminal impedance measurements with subsequent calculation of the two-port parameters of interest from these. The impedances indicated in Fig. 2 have proved simple to measure at typical operating points with conventional high-frequency bridges. These impedances have been measured at a set of frequencies extending to 30 mc. Because of the number of transistors measured it has been economical to program a digital computer to calculate two-port parameters and other quantities of interest from the measured two-terminal impedances.

THE RELATIONSHIPS OF TRANSISTOR PARAMETERS TO AMPLIFIER PERFORMANCE

Any of the sets of two-port parameters implicitly characterize all of the linear properties of the transistor for the range of frequencies for which the parameters have been measured. As mentioned before, it is necessary to translate the parameters into answers to the following questions. How much amplification can the transistor give at a particular

frequency? What impedance should it be supplied from? What impedance should it feed? What gain will be obtained using a pair of impedances different from the optimum ones? The answering of these and related questions amounts to establishing a convenient means of translating the parameter values into the quantities of interest applying to the amplifier. Such a convenient translating means for solving these problems is described in this section.

Earlier explicit solutions to special cases of the problem are well known. Wallace and Pietenpol[2] have given simple expressions in terms of the transistor parameters for matching input and output impedances and the maximum available gain when the transistor has purely real parameters. An implicit solution for optimum source and load impedances for maximum gain in the complex case has been known for a long time. It is simply that the transistor be terminated at the input and output by conjugate matching impedances. The implicit nature of this solution arises from the fact that the input impedance is a function of the load impedance, and the output impedance is a function of the source impedance for transistors with internal feedback. The solution for optimum source and load impedance from this approach amounts to the solution of simultaneous quadratic equations with complex unknowns and becomes involved.

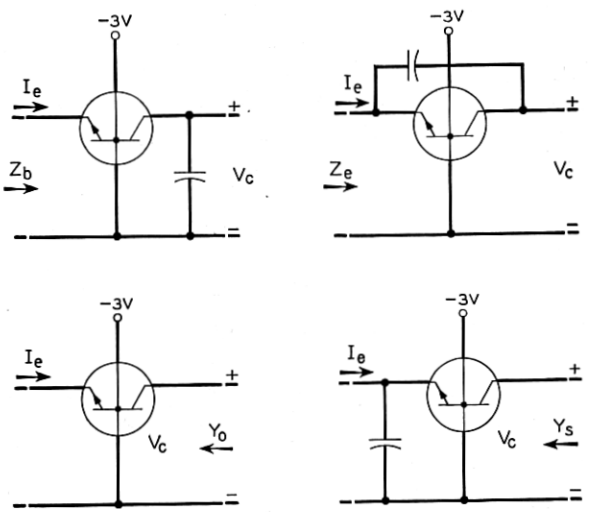


Fig. 2 — Two terminal impedance measurements for determination of two-port parameters.

[2] R. L. Wallace and W. J. Pietenpol, Some Circuit Properties of n-p-n Transistors, Proc. I.R.E., **39**, pp. 753–67, July, 1951.

From the approach to the problem taken in this paper, one solves first for the maximum power gain and subsequently determines the optimum terminations. It turns out that the solutions leads to explicit relationships for optimum performance and terminations and also leads to charts from which power gains and input impedance can be read for any terminations.

In all expressions to be developed, the h parameters are used. Precisely the same expressions can be obtained for z's, y's, or g's provided that one uses the corresponding quantities in the table of Fig. 1.

The maximum power gain is a quantity of primary interest in transistors since the transistor ordinarily has a resistive component in its driving-point impedance. Thus voltage or current amplification is constrained by the limited power gain attainable. In some cases, however, because of the inherent feedback internal to the device, instability can result simply from proper passive terminations without application of any additional feedback. Such cases are distinct because of this property. Transistors exhibiting this possibility are said to be potentially unstable at the frequency in question.

A quantity of interest presented here and derived later is a particular power gain defined for h-parameters as

$$\frac{\text{power out}}{\text{power in}} = \frac{P_{00}}{P_{i0}} = \frac{|h_{21}|^2}{4h_{11r}h_{22r} - 2Re(h_{12}h_{21})} \tag{1}$$

where h_{11r} and h_{22r} mean the real part of h_{11} and of h_{22}. $Re(h_{12}h_{21})$ means the real part of the product of h_{12} and h_{21}. Unless the amplifier is potentially unstable, the quantity P_{00}/P_{i0} is within 3 db of the maximum available gain for the transistor.

The matter of potential instability of the transistor is of great interest. Certainly the transistor is potentially unstable if P_{00}/P_{i0} is negative. Otherwise potential instability is indicated by greater than unity values of the criticalness factor

$$C = 2\frac{P_{00}}{P_{i0}}\left|\frac{h_{12}}{h_{21}}\right| \tag{2}$$

If the transistor is not potentially unstable the maximum available gain is $K_G(P_{00}/P_{i0})$ where

$$K_G = \frac{2(1 - \sqrt{1 - C^2})}{C^2} \tag{3}$$

For $0 \leqq C \leqq 1$, $1 \leqq K_G \leqq 2$. A plot of K_G as a function of C is shown in Fig. 3. The function is seen to be exceedingly flat near $K_G = 1$ for

C between zero and 0.6. Thus the value P_{00}/P_{i0} in the majority of cases where the transistor is not potentially unstable is a close approximation to the maximum available gain.

The optimum source and load impedances can be expressed in terms of the transistor parameters and other quantities given in terms of them by the following relationships where the transistor is not potentially unstable.

$$G = 1 \lfloor Arg\ (\overline{-h_{12}h_{21}}) = e^{j\theta} \tag{4}$$[3]

$$Z_s \text{ opt} = \overline{Z}_{in} = h_{11} - \frac{h_{12}h_{21}}{2h_{22r}}\left(1 - \frac{CK_GG}{2}\right) \tag{5}$$

$$Y_L \text{ opt} = -h_{22} + \frac{2h_{22r}}{1 - \frac{CK_GG}{2}} \tag{6}$$

Though explicit relationships for ideal terminations and for the maximum power gain which one can achieve with a transistor are of interest, such terminations limit the band width of the amplifiers. Therefore, it is important to have convenient means for evaluating power gain and input impedance for other than ideal terminations in order to realize a desired bandwidth. A chart which facilitates computation of these quantities is now developed from an analysis which leads to the other results quoted above.

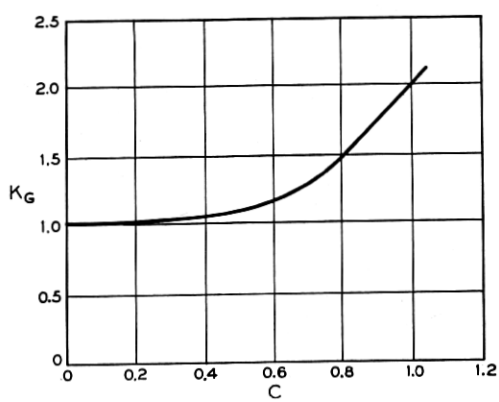


FIG. 3 — K_G plotted as a function of C.

[3] If $\overline{-h_{12}h_{21}}$ is $c + jd$, then $\theta = \tan^{-1}(d/c)$; $G = e^{j\theta}$ and $\overline{-h_{12}h_{21}}$ is the conjugate of $-h_{12}h_{21}$.

Power Flow in a Two-Port Device

A convenient point of departure in the analysis of power amplification in a transistor or other linear two-port device is the arrangement shown in Fig. 4. The two-port is supplied by a unit current at the frequency of interest and at reference phase at the input terminal pair. The output of the two-port is connected to a voltage source of the same frequency. The input-current and output-voltage time functions are

$$i_1 = Re\sqrt{2}\varepsilon^{j\omega t} = Re\sqrt{2}I_1\varepsilon^{j\omega t} \tag{7}$$

and

$$e_2 = Re\sqrt{2}(a + jb)\varepsilon^{j\omega t} = Re\sqrt{2}(L + jM)\left(\frac{-h_{21}}{2h_{22}r}\right)\varepsilon^{j\omega t} = Re\sqrt{2}E_2e^{j\omega t} \tag{8}$$

In (8), L and M are introduced for simplicity in some later relationships.

The whole analysis is essentially a study of power flow in the circuit shown in Fig. 4 as L and M of (8) are varied. All possible terminations and excitations can be simulated simply by varying L and M. Under some conditions the voltage source will absorb power; under others it will supply power to the two-port. Ordinarily the current source supplies power to the two-port, but for appropriate ranges of L and M if the two-port is potentially unstable, the transistor may supply power both to the current source and the voltage source. The problem of evaluating maximum power gain is simply finding the values of L and M corresponding to the greatest ratio of power out to power in. The load impedance to which this situation corresponds is $E_2/-I_2$. The input impedance for this condition is simply E_1/I_1, and the optimum source impedance is the complex conjugate of the latter quantity.

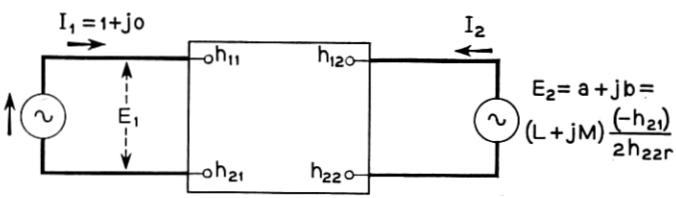


Fig. 4 — A two-port device supplied by a current source and feeding into a voltage source.

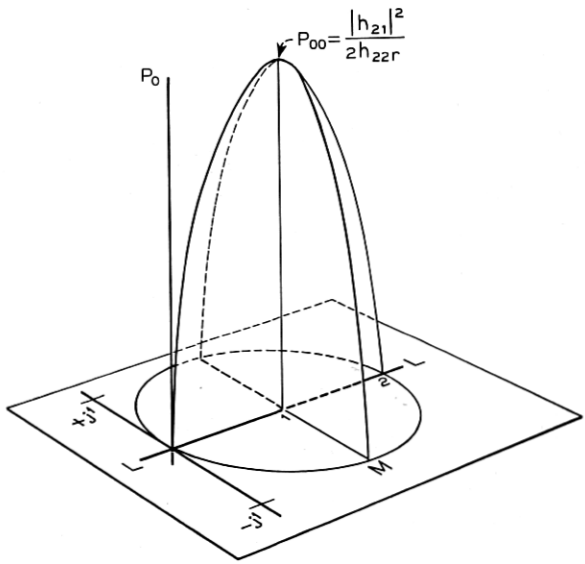


Fig. 5 — Sketch of power output as a function of L and M.

PROJECTION IN L-M PLANE OF GRADIENT
LINE IS G OR $\text{Arg}-h_{12}h_{21}$
SLOPE OF PLANE ALONG G IS $\left|\frac{h_{21}h_{12}}{2h_{22r}}\right|$

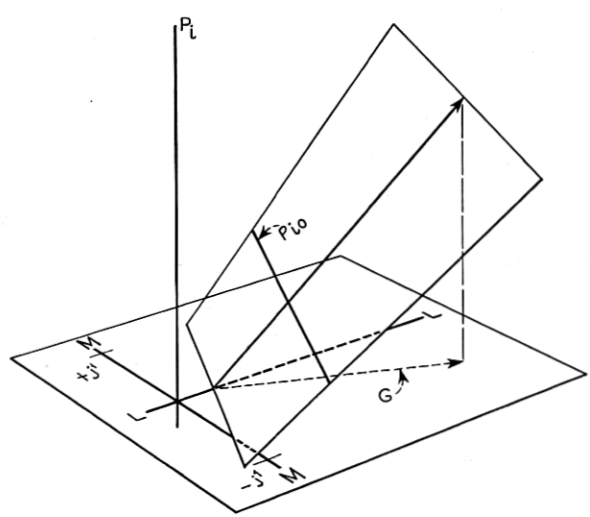


Fig. 6 — Sketch of power input as a function of L and M.

The output power can be readily evaluated in terms of L and M.

$$I_2 = I_1 h_{21} + E_2 h_{22} \tag{9}$$

$$I_2 = (1 + j0)h_{21} + (L + jM)h_{22} \frac{(-h_{21})}{2h_{22r}} \tag{10}$$

$$\text{Power out} = P_0 = Re(-\bar{E}_2 I_2) \tag{11}$$

$$P_0 = Re\left[\frac{(L - jM)\bar{h}_{21}}{2h_{22r}} h_{21} - (L^2 + M^2) \frac{h_{22} \mid h_{21} \mid^2}{4h_{22r}}\right] \tag{12}$$

$$= L \frac{\mid h_{21} \mid^2}{2h_{22r}} - (L^2 + M^2) \frac{\mid h_{21} \mid^2}{2h_{22r}} \tag{13}$$

On the basis of (13) the power output plotted as a function of L and M is a paraboloid as shown in Fig. 5, having the pertinent dimensions indicated there. Only within the circle centered at $L = 1$, $M = 0$ and passing through the origin does one obtain positive power output. The apex of the paraboloid corresponds to

$$P_0 = P_{00} = \frac{\mid h_{21} \mid^2}{4h_{22r}} \tag{14}$$

The input power can similarly be evaluated in terms of L and M.

$$E_1 = I_1 h_{11} + E_2 h_{12} \tag{15}$$

$$= (1 + j0)h_{11} + (L + jM) \frac{(-h_{21})}{2h_{22r}} h_{12} \tag{16}$$

$$\text{Power in} = P_i = Re[E_1 I_1] \tag{17}$$

$$P_i = Re\left[h_{11} + (L + jM) \frac{(-h_{21})h_{12}}{2h_{22r}}\right] \tag{18}$$

$$= h_{11r} - LRe \frac{(h_{12}h_{21})}{2h_{22r}} + MIm \frac{(h_{12}h_{21})}{2h_{22r}} \tag{19}$$

where $Im[(h_{12}h_{21})/2h_{22r}]$ means the imaginary part of the expression in parenthesis.

On the basis of Eq. 19 the input power plotted as a function of L and M is simply an inclined plane having the properties indicated on Figure 6.

Since Figures 5 and 6 turn out to be such simple geometrical figures the problem of finding the point of maximum ratio of P_0 to P_i is very simple and other interpretations are easy to make. First, a negative value of $P_{i0}(P_i$ at 1, 0) certainly indicates potential instability for both input and output terminations receive power from the two-port. Even if the plane of P_i intersects the L-M plane within the unit circle centered at

1, 0, then the two-port is potentially unstable since on one side of the intersection both input and output terminations receive power from the two-port. The change in P_i from the minimum value found on the unit circle centered at 1, 0 to P_{i0} divided by P_{i0} is the criticalness factor, C. Values of C greater than unity indicate potential instability.

The power input at 1, 0 is

$$P_{i0} = \frac{2h_{11r}h_{22r} - Re(h_{12}h_{21})}{2h_{22r}} \tag{20}$$

Using (14) and (20), one obtains

$$\frac{P_{00}}{P_{i0}} = \frac{|h_{21}|^2}{4h_{11r}h_{22r} - 2Re(h_{12}h_{21})} \tag{21}$$

$$C = \frac{\frac{|h_{12}h_{21}|}{2h_{22r}}}{\frac{2h_{11r}h_{22r} - Re(h_{12}h_{21})}{2h_{22r}}} = 2\frac{P_{00}}{P_{i0}}\left|\frac{h_{12}}{h_{21}}\right| \tag{22}$$

Now if the plane of power input, Fig. 6, is parallel to the L-M plane and above it, certainly the point of maximum power gain is the apex of the paraboloid, 1, 0 in Fig. 5. If the plane is inclined but always above the unit circle centered at 1, 0 certainly the point of maximum power gain is downward along the gradient line which lies above the point 1, 0. This must be so since for any contour of equal power out (a circle of fixed elevation around the paraboloid) the minimum power input (or greatest gain) lies along the line of steepest descent from 1, 0 in Fig. 6. Thus the problem of evaluation of the maximum available gain reduces to the simple problem of finding the abscissa of Fig. 7 where the ratio of ordinates of the parabola and straight line is a maximum. The parabola

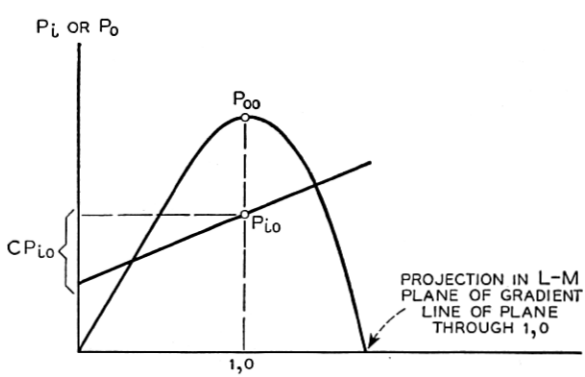


Fig. 7 — Section of paraboloid and inclined plane of Figs. 5 and 6.

and straight line are sections of the paraboloid and plane through the gradient line of the plane over 1, 0.

A straightforward analysis indicates that the point in the L-M plane where the maximum of P_0/P_i occurs is at

$$L + jM = 1 - \frac{CK_G G}{2} \tag{23}$$

where these quantities are defined as in (2), (3), and (4). The power gain at this optimum point is K_G times that obtained at 1, 0. One finds that the maximum gain is only two times P_{00}/P_{i0} even if C approaches unity which corresponds to the marginal case of potential instability.

The analysis just described leads to the maximum values of power gain and to the best terminating impedances. For many design problems these answers are a guide but one may prefer to use other than optimum values for other compelling reasons. For such a case charts from which one can get the pertinent quantities are very helpful.

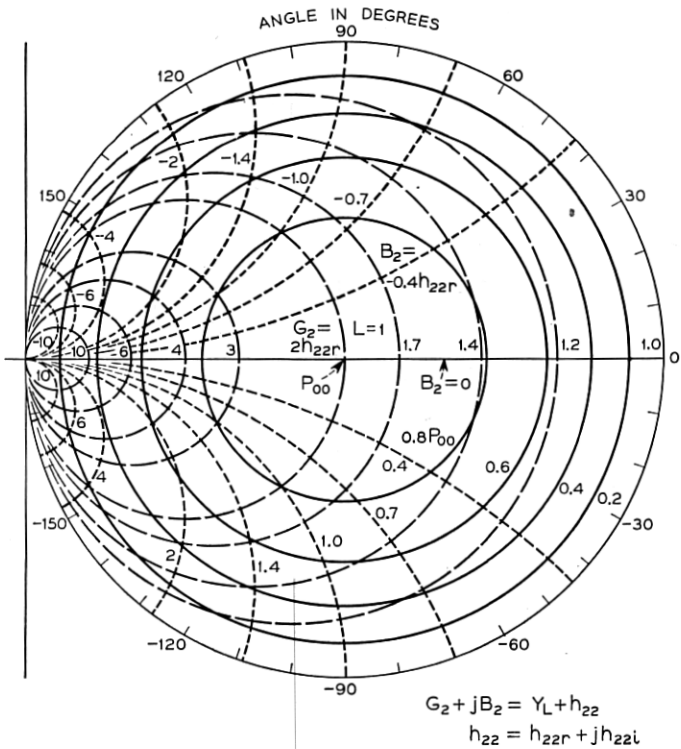


Fig. 8 — Gain and impedance chart.

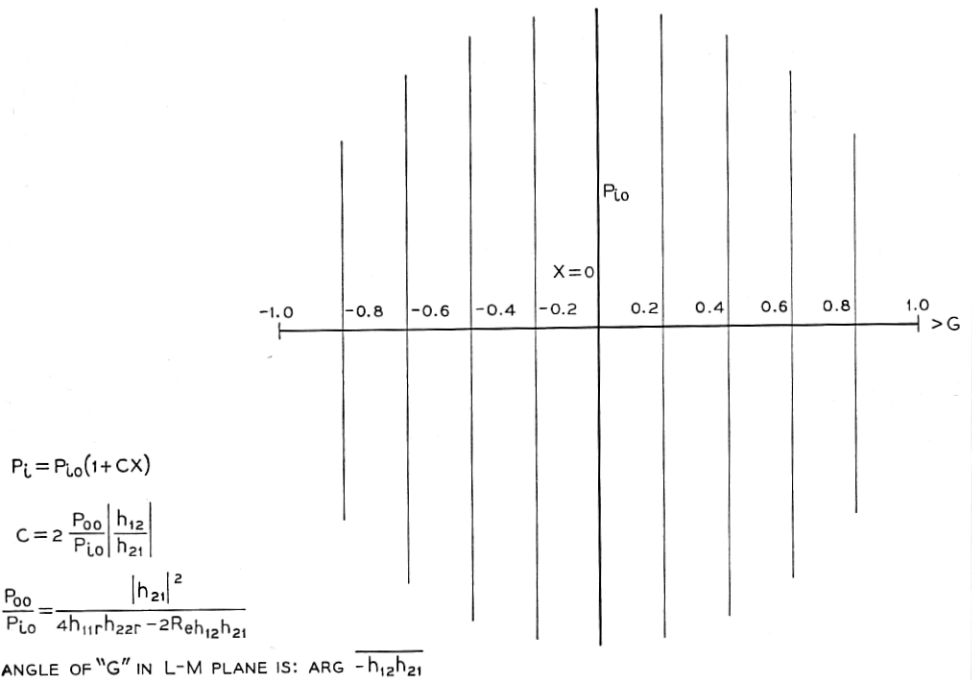


Fig. 9(a) — Input power as a function of X.

Development of Transmission and Impedance Charts

The same point of departure employed in the evaluation of optimum cases leads to a convenient set of charts. Equation 12 shows that a set of concentric circles centered at 1, 0 are loci in the L-M plane of constant power output for a unit current source at the input. It is convenient to plot these as is done on Figure 8, showing P_0 as a fraction of P_{00}.

$$\frac{P_0}{\frac{|h_{21}|^2}{4h_{22r}}} = \frac{P_0}{P_{00}} = 1 - (L-1)^2 - M^2 \tag{24}$$

Since Y_L, the load admittance, is $-I_2/E_2$, using (10) one obtains

$$\frac{-I_2}{E_2} = Y_L = -h_{22} + \frac{2h_{22r}}{L + jM} \tag{25}$$

Now it is clear that if one defines G_2 and B_2 by

$$Y_2 = G_2 + jB_2 = Y_L + h_{22} = \frac{2h_{22r}}{L + jM} \tag{26}$$

loci of constant real and imaginary parts of Y_2 become the mutually orthogonal circles shown in Fig. 8. Thus the value of $L + jM$ is determined by the load admittance and two-port parameters.

Contours representing constant input power, with equal increments of power between successive contours, are always parallel equally-spaced lines in the L-M plane. However, as may be seen from (19) and Fig. 6 different cases have different directions for the line normal to the contours, (the gradient line) and also different power increments for a given spacing of equal-power-input contours. It is convenient to define a new variable X which is the component along the gradient line of the vector starting at $L = 1$, $M = 0$ and going to L, M. Thus

$$P_i = P_{i0}(1 + CX) \tag{27}$$

Equation 27 suggests Fig. 9(a) which shows loci of constant power input plotted as a function of X. If Fig. 9(a) is shown on a transparent ma-

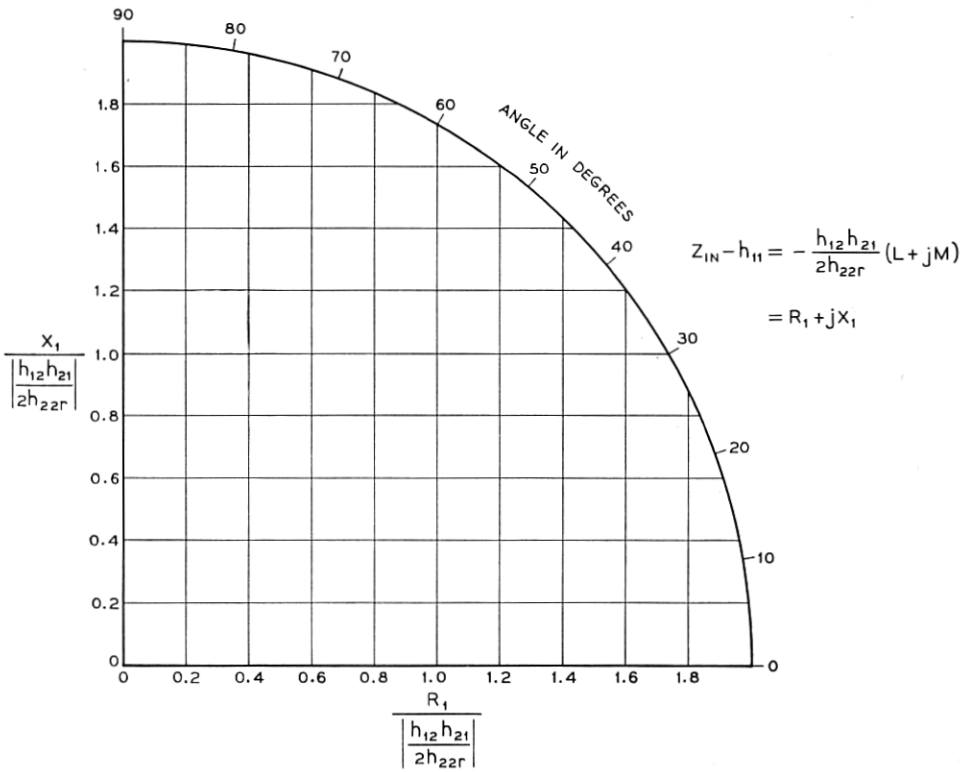


Fig. 9(b) — Input impedance as a function of L and M.

terial, its center (at $X = 0$ along the gradient line) can be superposed with the point $L = 1$, $M = 0$ of Fig. 8. With the gradient line of Fig. 9(a) oriented at the argument of $\overline{-h_{12}h_{21}}$, or θ in the L-M plane, one can easily determine graphically the power gain at any point in the L-M plane compared to the power gain at 1, 0. With Fig. 9(a) superposed on Fig. 8 as just described the viewer gets a bird's-eye-impression of the paraboloid of power output and the inclined plane of power input simultaneously. With such a bird's-eye view, it is easy to assess possibilities for power gain with all possible angles of load termination.

The evaluation in input impedance is done through use of (16) from which is obtained

$$\frac{E_1}{I_1} = Z_{in} = h_{11} + (L + jM)\frac{(-h_{12}h_{21})}{2h_{22r}}, \qquad \text{or} \tag{28}$$

$$Z_{in} = h_{11} + (L + jM)(e^{-j\theta})\left|\frac{h_{12}h_{21}}{2h_{22r}}\right| \tag{29}$$

For evaluating the second component of (29), it is convenient to have a second transparent overlay, Fig. 9(b), consisting of a rectangular grid to the same scale as the L-M plane, Fig. 8, with coordinates marked as

$$Re\frac{(Z_{in} - h_{11})}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|} = \frac{R_1}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

and

$$Im\frac{(Z_{in} - h_{11})}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|} = \frac{X_1}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

This overlay is placed over the L-M plane with the

$$\frac{R_1}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

axis making the angle θ with respect to the L axis. Thus on the rectangular overlay for any point in the L-M plane, one reads

$$\frac{Z_{in} - h_{11}}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

PARTICULAR DESIGNS OF TETRODE TRANSISTOR AMPLIFIERS

The charts and optimum relationships developed in the preceding section are convenient starting points in the design of amplifiers. They

do not ordinarily constitute a finished solution, however, since practical constraints frequently modify the design used. Moreover, all of the relationships are expressed on a single frequency basis, and many times the amplifier must operate over a range of frequencies broad enough that parameters change significantly over the range.

Four amplifier designs are described in this section: a single stage, common-base, 20-mc video amplifier; a common-emitter, 10-mc video amplifier; an IF amplifier at 30 mc and a 60 to 80-mc IF amplifier. Parameter measurements made with bridges support the first three designs.

Parameter values and associated constants of a typical tetrode transistor are given in Table I. The quantities shown there reveal some interesting facts about the typical tetrode transistor represented. First, in the common-base connection the tetrode is potentially unstable at 30 mc but not at the lower frequencies. The common-emitter amplifier is potentially unstable at 1 and 3 mc. Second, the power gains of common-emitter and common-base stages are about the same at 30 mc, the common-emitter connection giving more gain at low frequencies.

The matter of potential instability requires further consideration from a practical point of view. Potential instability at a frequency neither implies that a stable amplifier cannot be built at that particular frequency, nor does it imply that one can obtain an unlimited amount of stable amplification at that frequency. It does mean that by simultaneously tuning output and input one can adjust for oscillation. The region of potential instability corresponds to a region in which the input resistance may be negative for appropriate loads. Instability is avoided in the physical amplifier if one supplies the amplifier from a sufficiently high impedance that the input loop impedance always has a positive real part. To operate the amplifier with such a load that it presents a negative resistance to the source is attended by the difficulty that the amplification is more sensitive to changes in the source impedance than it is when the input resistance is positive. Hence the possible higher gain with internal positive feedback goes along with a greater sensitivity to changing termination impedance.

A Common-Base 20-Mc Video Amplifier

The data presented in Table 1 gives a quite comprehensive picture of possibilities for amplifier designs. To it must be added a practical fact. It is difficult to connect the load impedance without adding about 2 $\mu\mu$f of capacitance. This means that any termination considered must include about this amount of capacitance. By a theorem regarding

TABLE I — PARAMETERS AND ASSOCIATED CONSTANTS OF TETRODE No. 668

Freq. Mc	0.6	1.0	3.0	10.0	30.0
Common Base					
h_{11}	$49 + j0.0$	$49 + j2.0$	$49 + j2.0$	$50 + j2.0$	$51 + j4.0$
h_{12}	$(1.1 + j0.24)\cdot 10^{-3}$	$(1.1 + j0.40)\cdot 10^{-3}$	$(1.2 + j1.3)\cdot 10^{-3}$	$(1.3 + j4.6)\cdot 10^{-3}$	$(2.1 + j11)\cdot 10^{-3}$
h_{21}	$-0.93 + j0.015$	$-0.93 + j0.023$	$-0.92 + j0.055$	$-0.88 + j0.13$	$-0.82 + j0.24$
h_{22}	$(3.3 + j5.3)\cdot 10^{-6}$	$(3.7 + j8.9)\cdot 10^{-6}$	$(6.8 + j25)\cdot 10^{-6}$	$(28 + j57)\cdot 10^{-6}$	$(35 + j140)\cdot 10^{-6}$
P_{00}/P_{i0}	310	310	230	87	40
C	0.78	0.79	0.89	0.94	1.3
$-\theta$	11°	20°	45°	65°	64°
$\left\lvert\frac{h_{12}h_{21}}{2h_{22r}}\right\rvert$	160	150	120	77	150
Common Emitter					
h_{11}	$720 - j160$	$660 - j210$	$440 - j270$	$220 - j210$	$130 - j140$
h_{12}	$(2.0 + j2.8)\cdot 10^{-3}$	$(3.0 + j4.3)\cdot 10^{-3}$	$(8.0 + j6.9)\cdot 10^{-3}$	$(1.5 + j1.0)\cdot 10^{-3}$	$(18 - j2.2)\cdot 10^{-3}$
h_{21}	$13 - j3.3$	$12 - j4.3$	$7.2 + j5.6$	$2.8 - j4.1$	$0.98 - j2.7$
h_{22}	$(6.4 + j6.4)\cdot 10^{-5}$	$(8.6 + j9.8)\cdot 10^{-5}$	$(1.9 + j17)\cdot 10^{-5}$	$(34 + j18)\cdot 10^{-5}$	$(40 + j17)\cdot 10^{-5}$
P_{00}/P_{i0}	1570	1330	567	121	44.4
C	0.80	1.1	1.3	0.75	0.57
$-\theta$	−139°	−145°	−177°	128°	103°
$\left\lvert\frac{h_{12}h_{21}}{2h_{22r}}\right\rvert$	359	381	250	111	65

passive impedances[4] this puts an upper limit on the level of impedance presented by the load over a band of frequencies. The greatest possible constant level of load impedance over 20 mc is

$$|Z| = \frac{2}{C\omega} = \frac{2}{2.10^{-12} \cdot 2.10^{7} \cdot 2\pi} = 7{,}960\Omega \qquad (30)$$

Thus number, though not strictly applicable to this case, nonetheless gives a measure of the sort of value which one can expect. Hence one observes that for a broad-band video amplifier the load impedance is certainly going to be considerably less than $1/|h_{22}|$ which up to 10 mc is not less than 15,000 ohms. Moreover, the gain, if it is to be uniform, will certainly be limited by the gain obtainable at 20 mc.

Recognition that the load admittance will be a number of times h_{22r},

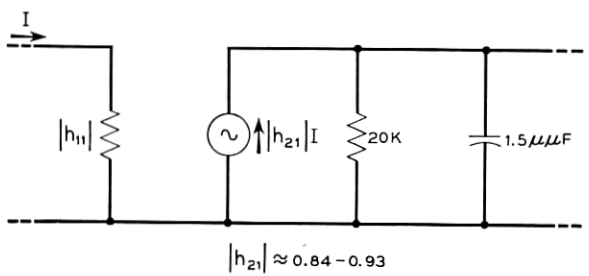


Fig. 10 — A rough approximant for the common base video amplifier. The variation of $|h_{21}|$ is a function of frequency and not variation between units.

five to ten, means that in Fig. 8 one will be operating near the origin where $(L + jM)$ is much less than one. Thus Z_{in} in (28) will be approximately h_{11}. Moreover, by superposing Fig. 9(a) on Fig. 8 at the correct angle for a frequency of 30 mc ($\theta = -64°$) one observes that negative power input occurs only in the small section of circle cut-off by a chord running from the 80° to the 155° points on the periphery. This region is quite a way from the likely point of operation. Thus, this points out that the low impedance termination precludes instability due to internal feedback.

If the amplifier is supplied by a 75-ohm source, its output admittance at 30 mc (Equation 4, Figure 1) is $(7.0 + j20) \cdot 10^{-5}$ mho. At 10 mc the output admittance is $(4.2 + j8.8) \cdot 10^{-5}$ mhos.

These computations reveal that the amplifier in the common-base connection appears quite like the model shown in Fig. 10. Clearly, the

[4] H. W. Bode, Network Analysis and Feedback Amplifier Design, D. Van Nostrand Co., New York, 1945.

about 1 db at frequencies up to 10 mc. Comparison of the measured and computed values is shown on Fig. 15 for a load of 500 ohms with no high-frequency compensation. The low-frequency gain is higher than for the common base connection but the response is down 3 db at 7 mc. By using the combination of R_1 in parallel with 800 $\mu\mu f$ in the emitter circuit, negative feedback is introduced at low frequencies which results in the reduction of low frequency gain tending to make the response more uniform. In addition the L-C network has been added in the output to compensate for the drop of $|h_{21}|$ with increasing frequency and the increasing effect of the output capacitance.

This results in the response shown as the dotted curve on Fig. 15. The low-frequency gain has been reduced to 17.5 db, but the response is now flat to within ± 0.3 db up to 13 mc and is 3 db down at 18 mc.

Although the data given on video amplifiers shows the results obtained using one transistor, similar response curves were obtained from some 6 or 8 units.

An I-F Amplifier Centered at 30 Mc.

The design of an IF amplifier at 30 mc is distinct from the preceding two cases in that one can use matching techniques over the narrow band.

Reference to Table 1 reveals that the common-base connection provides more potential gain at 30 mc than the common emitter connection; in fact, the common-base connection can be made to oscillate with certain terminations. The common-base connection is chosen for the 30-mc amplifier.

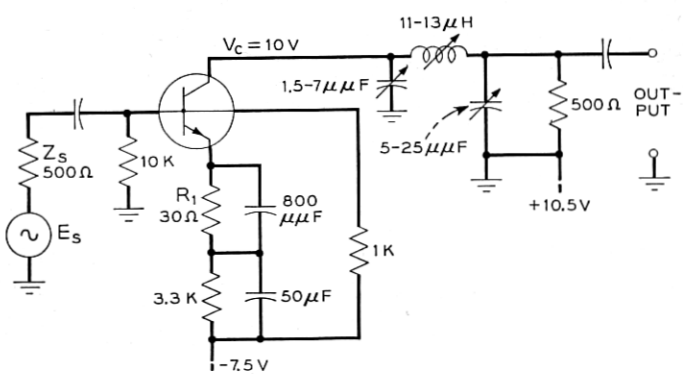


Fig. 14 — Circuit of a common emitter video amplifier. R_1 in parallel with 800 $\mu\mu f$ and the LC network in the output circuit peak the response at 10 to 12 mc.

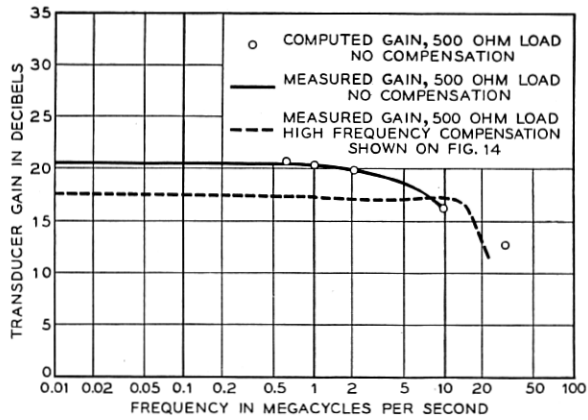


Fig. 15 — Computed and measured response of a common emitter amplifier.

In the design of the IF amplifier one is interested in a moderate range of frequencies. It will generally be true that the most frequency dependent parameters are the output and load admittances, since the load is to be tuned. One can take as a suitable load a parallel combination of a fixed conductance with a frequency dependent susceptance, the sort of termination typical of tuned circuits. Thus on Fig. 8, the locus of $G_2 + jB_2$ is one of the $G_2 =$ Const. circles.

Superposition of Fig. 9(b) on Fig. 8 with the

$$\frac{R_1}{\left|\dfrac{h_{12}h_{21}}{2h_{22r}}\right|}$$

axis making an angle of $-64°$ with the L axis reveals that $Z_{in} - h_{11}$ has a negative real part on the upper left edges of all of the contours of constant G_2. On the $G_2 = 2h_{22r}$ contour, $Re(Z_{in})$ reaches a minimum of 22.5 ohms. We select a load with $G_L = 2h_{22r}(G_2 = 3h_{22r})$ to avoid low values of input resistance resulting from the internal feedback.

Superposition of Fig. 9(a) on Fig. 8 with the gradient line making an angle of $-64°$ through the point L, $M = 1, 0$ reveals that the maximum value of P_0/P_i on the $G_2 = 3h_{22r}$ circle is 1.87 P_{00}/P_{i0} and it occurs for $B_2 = -2h_{22r}$. The input impedance at this point is $36 + j87$ ohms.

For an amplifier one is primarily interested in

$$\frac{P_0}{\text{Power Available from Source}}$$

(which is called transducer gain) rather than P_0/P_i, the quantities just

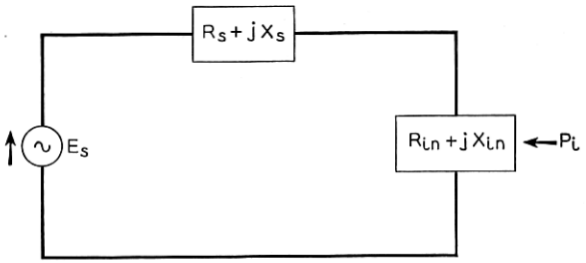


Fig. 16 — Typical input circuit.

read from the charts. From the source-load arrangement shown in Fig. 16, one readily computes

$$\frac{P_i}{\text{Power Available from Source}} = \frac{\dfrac{|E_s|^2 R_{in}}{(R_s + R_{in})^2 + (X_s + X_{in})^2}}{\dfrac{|E_s|^2}{4R_s}} = \frac{4R_s R_{in}}{(R_s + R_{in})^2 + (X_s + X_{in})^2} \tag{32}$$

The source impedance selected for the amplifier is $75 - j87$ ohms at 30 mc. The 75 ohms is selected to reduce the effect of variations in input impedance when it is reduced further by the internal feedback. The 87 ohms of capacitive reactance is selected to tune the input reactance at the peak of response. Using Fig. 8 with the overlay of Fig. 9(a) along with (32) under the assumption that X_s varies insignificantly over the frequencies involved one obtains Table II. This table shows the variation of transducer gain as the value of B_2 is changed as well as indicating the value of B_2 required for the maximum gain. Thus, if the total output capacitance is known, the load admittance required to give the maximum gain at the desired frequency can be computed. As will be shown

TABLE II — EVALUATION OF TRANSDUCER GAIN OF I-F AMPLIFIER

B_2	$-5h_{22r}$	$-4h_{22r}$	$-3h_{22r}$	$-2h_{22r}$	$-h_{22r}$	Oh_{22r}	h_{22r}
P_0/P_i	50	64	73	75	59	50	38
Z_{in}	$22 + j48$	$23 + j58$	$28 + j73$	$36 + j87$	$67 + j99$	$96 + j94$	$120 + j67$
P_i/Power available from source	0.61	0.66	0.78	0.87	0.98	0.98	0.94
Transducer gain	30	42	57	66	58	49	36
Gain, db	14.8	16.2	17.5	18.2	17.6	16.9	15.5

below, the bandwidth at which the response is down a given number of db can also be computed.

From Table II one observes that this design provides a gain of about 18 db with half power frequencies where the susceptance B_2 has changed by $\pm 3h_{22r}$ mhos from its value of $-2h_{22r}$ at the center of the pass band. The value of h_{22i} corresponds to approximately 1 $\mu\mu$f of capacitance and if the stray capacitance amounts to 3.5 $\mu\mu$f, then the bandwidth is $\Delta B2/2C$ since the slope of the susceptance of a tuned circuit is

$$2C \frac{\text{mhos}}{\text{rad/sec}}$$

Thus the bandwidth is approximately

$$\frac{6 \cdot 3.5 \cdot 10^{-5}}{2 \cdot 2.5 \cdot 10^{-12} \cdot 6.28}$$

or 3.7 mc. This is the actual value of load capacitance measured on an experimental amplifier with a vacuum tube voltmeter connected to the output. The measured response of this amplifier with a load of $Y_L = (68 - j215) \cdot 10^{-6}$ at 30 mc ($G_L \doteq 2h_{22r}$) shows a peak gain of 18.3 db and half power points separated by 3.8 mc. For a given value of G_L, the bandwidth of the amplifier will vary inversely with the total capacitance in the output circuit. The same gain as obtained in the sample given above, can be obtained over a narrower band by increasing the load capacitance. Since the minimum capacitance is fixed, if one wishes to increase the width of the pass band, a higher value of G_2 must be used. In the same manner as is used to arrive at the data shown on Table II, Table III is computed for a value of $G_2 = 6h_{22r}$ ($G_L = 5h_{22r}$).

In this case, the maximum value of P_0/P_i occurs when $B_2 = -3h_{22r}$. The source impedance is selected to be $75 - j45$ ohms at 30 mc and the remainder of the table is computed. The maximum computed gain is approximately 16 db with half power frequencies where the susceptance

TABLE III — EVALUATION OF TRANSDUCER GAIN OF I.F. AMPLIFIER

B_2	$-8h_{22r}$	$-5h_{22r}$	$-3h_{22r}$	$-2h_{22r}$	$-h_{22r}$	$+h_{22r}$	$+4h_{22r}$
P_0/P_i	25	33	43	40	39	31	21
Z_{in}	$35 + j22$	$35 + j35$	$50 + j45$	$56 + j46$	$65 + j48$	$77 + j39$	$83 + j20$
P_{in}/Power available from source	0.83	0.86	0.96	0.97	0.99	0.99	0.97
Transducer gain	21	28	41	39	39	31	20
Gain db	13.2	14.5	16.1	15.9	15.9	14.9	13.0

B_2 has changed by $\pm 6h_{22r}$ mhos from its value at the center of the band. Using the same value of circuit capacitance as above, the indicated bandwidth is about 7.4 mc. The measured response on an amplifier with this value of load impedance indicates a gain of 16.1 db at 30 mc, with the frequencies at the half power point separated by 7.6 mc.

Often it is desirable to build tuned amplifiers to work between like impedances in which case at least the output network must perform both the function of selectivity and impedance transformation. An example of a simple network to perform these functions is shown on Fig. 17. The impedance transforming properties of such a circuit are well known. With a given value of load resistance, the load admittance presented to the transistor can be made to have a given value at a certain frequency. However, since the circuit performs both the function of impedance transformation and selectivity the bandwidth is determined by the output impedance selected. This circuit does not present a fixed value of conductance as a function of frequency but for frequencies near the maximum gain it is a fair approximation to assume it constant. The output circuit of Fig. 17 was designed to present a load admittance such that $G_2 + jB_2 = 3h_{22r} - j2h_{22r}$ at 30 mc. This is the same condition as computed in Table II so one would expect the same value of maximum gain. However, in order to present the proper value of load impedance, a total load capacitance of about 4 $\mu\mu$f must be used. This indicates a bandwidth of 3.3 mc between the half power points. The measured response of this amplifier is shown on Fig. 18 as the solid line. The points indicate the computed maximum gain and the frequencies at which the gain is down 3 db.

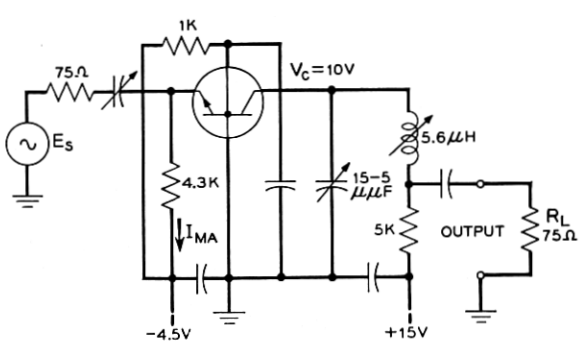


Fig. 17 — Simple tuned amplifier. The output circuit performs both the functions of impedance transformation and selectivity.

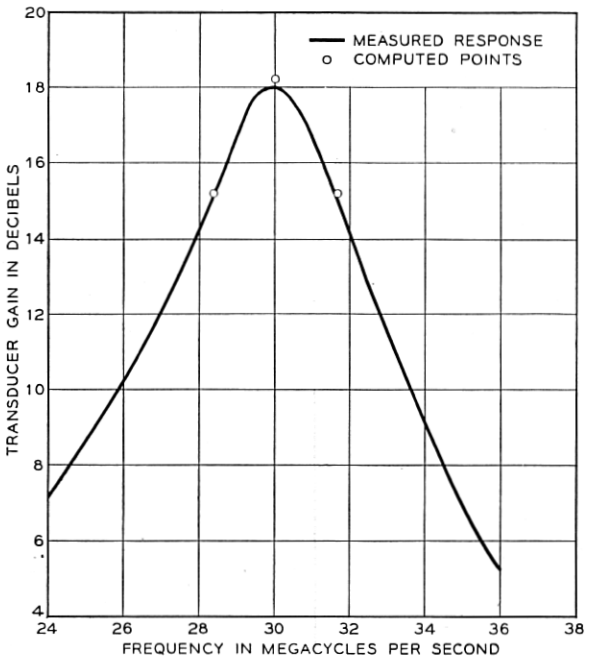


Fig. 18 — Measured and computed response of the stage shown on Fig. 17.

An IF Amplifier Centered at 70 Mc.

Although we do not have complete data on the parameter values of tetrode transistors in this frequency range, amplifiers with a center frequency of 70 mc have been built and their performance measured. The amplifier was designed to provide a flat gain characteristic over the frequency range from 60 to 80 mc. The stage was designed with the equivalent of a double tuned transformer, interstage circuit with the transformer being replaced by the equivalent tee section. The selective circuit is terminated at its output into the load resistance in the case of the last stage or by the input impedance of the following transistor when it is used as an interstage network. The impedance transformation of the network is approximately 75 ohms to 1,500 ohms so it is essentially unterminated at the collector. By using a sweeping oscillator, such a stage can be adjusted to result in a fairly flat frequency response. A typical stage is shown on Fig. 19. The output terminals are connected to either the load or the next emitter. The response obtained from a 3-stage amplifier is shown on Fig. 20. In order to determine the variation of gain

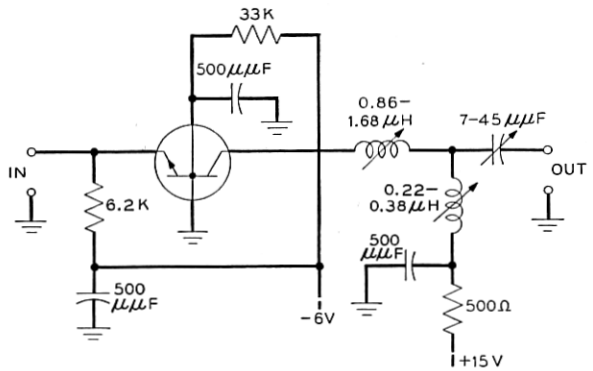


Fig. 19 — Circuit of a 60 to 80-mc band pass amplifier stage.

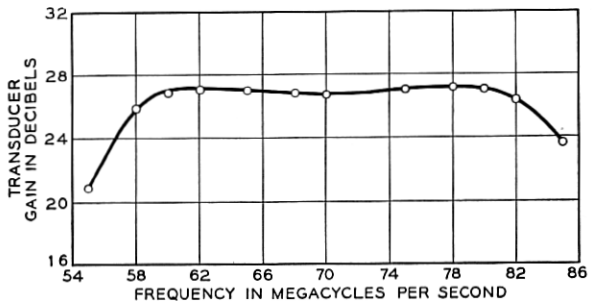


Fig. 20 — Gain of a 3-stage band pass amplifier working between 75-ohm impedances. Each stage uses the circuit shown on Fig. 19.

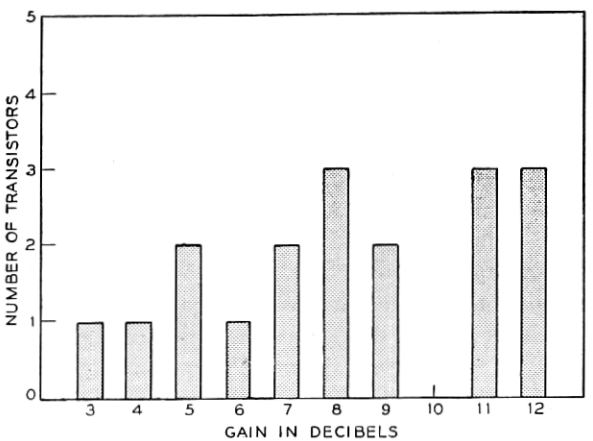


Fig. 21 — Variation of gain for a group of transistors used in the circuit of Fig. 19.

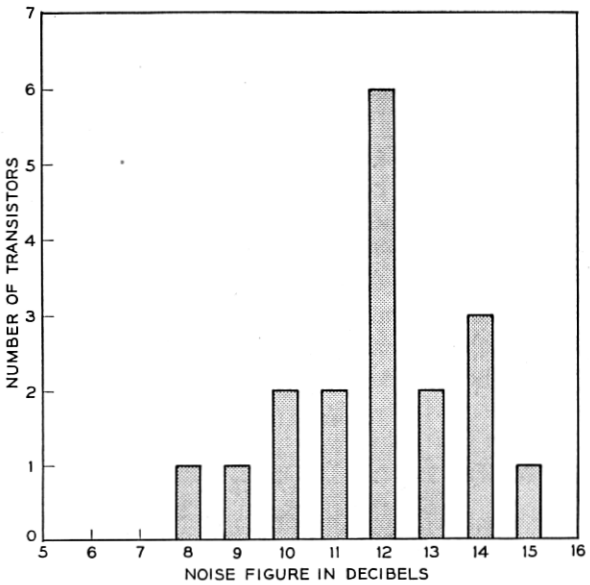


FIG. 22 — Noise figure for a group of transistors used in the circuit of Fig. 19.

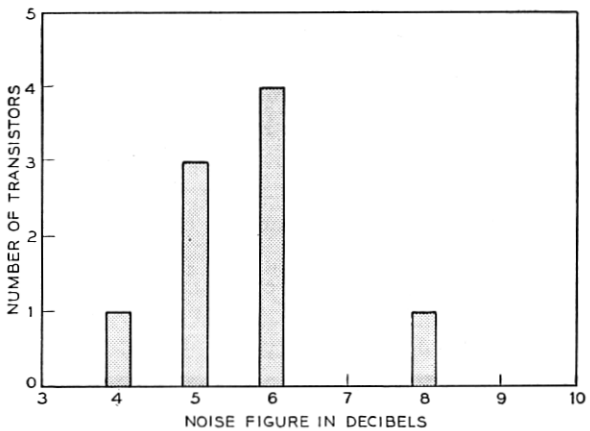


Fig. 23 — Noise figure for a group of transistors used in a 10-mc bandpass amplifier.

between various transistors, 18 tetrodes were measured in the first stage of the amplifier. If the measured gain of each transistor is rounded off to the nearest db and the number of transistors having this gain plotted as the abscissa, the results shown on Fig. 21 are obtained. Of the 18 transistors measured, 11 have a gain of 8 db or greater. Similar data has been obtained on the noise figure of the same 18 transistors, the results being shown on Fig. 22. In general, the transistors having the highest gain also have the lowest noise figure. The noise figure depends to some extent on the source impedance but a 75-ohm source results in a noise figure which is within a few tenths of a db of the minimum. The value of the noise figure does not vary a great deal as the collector voltage and emitter current are changed except that if the collector voltage is lowered below 6 or 8 volts the gain decreases and in general the noise figure increases.

Noise Figure at 10 Mc.

Although not described here, bandpass amplifiers centered at 10 mc with a 200-kc pass band have been constructed using tetrode transistors. A gain of slightly over 20 db per stage can be realized at this frequency. The noise figure of transistors tried in this circuit is shown on Fig. 23, the data being shown in the same manner as described above. At 10 mc the noise figures are lower than at 70 mc. The remarks made above concerning variation of noise figure with operating conditions also apply to this case.

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