Transistor Circuits for Analog and Digital Systems*

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This paper describes the application of junction transistors to precision circuits for use in analog computers and the input and output circuits of digital systems. The three basic circuits are a summing amplifier, an integrator, and a voltage comparator. The transistor circuits are combined into a voltage encoder for translating analog voltages into equivalent time intervals.

1.0. INTRODUCTION

Transistors, because of their reliability, small power consumption, and small size find a natural field of application in electronic computers and data transmission systems. These advantages have already been realized by using point contact transistors in high speed digital computers.[1] This paper describes the application of junction transistors to precision circuits which are used in dc analog computers and in the input and output circuits of digital systems. The three basic circuits which are used in these applications are a summing amplifier, an integrator, and a voltage comparator. A general procedure for designing these transistor circuits is given with particular emphasis placed on new design methods that are necessitated by the properties of junction transistors. The design principles are illustrated by specific circuits. The fundamental considerations in the design of transistor operational amplifiers are discussed in Section 2.0. In Section 3.0 an illustrative summing amplifier is described, which has a dc accuracy of better than one part in 5,000 throughout an operating temperature range of 0 to 50°C. The feedback in this amplifier is maintained over a broad enough frequency band so that full accuracy is attained in about 100 microseconds.

The design of a specific transistor integrator is presented in Section

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4.0. The integrator can be used to generate a voltage ramp which is linear to within one part in 8,000. By means of an automatic zero set (AZS) circuit which uses a magnetic detector, the slope of the voltage ramp is maintained constant to within one part in 8,000 throughout a temperature range of 20°C to 40°C.

The voltage comparator, described in Section 5.0, is an electrical device which indicates the instant of time an input voltage waveform passes through a predetermined reference level. By taking advantage of the properties of semiconductor devices, the comparator can be designed to have an accuracy of ± 5 millivolts throughout a temperature range of 20°C to 40°C.

In Section 6.0, the system application of the transistor circuits is demonstrated by assembling the summing amplifier, the integrator, and the voltage comparator into a voltage encoder. The encoder can be used to translate an analog input voltage into an equivalent time interval with an accuracy of one part in 4,000. This accuracy is realized throughout a temperature range of 20°C to 40°C for the particular circuits described.

2.0. FUNDAMENTAL CONSIDERATIONS IN THE DESIGN OF OPERATIONAL AMPLIFIERS

The basic active circuit used in dc analog computers is a direct coupled negative feedback amplifier. With appropriate input and feedback networks, the amplifier can be used for multiplication by a constant coefficient, addition, integration, or differentiation as shown in Figure 1.[2] The accuracy of an operational amplifier depends only on the passive components used in the input and feedback circuits provided that there is sufficient negative feedback (usually greater than 60 db). The time that is required for the amplifier to perform a calculation is an inverse function of the bandwidth over which the feedback is maintained. Thus a fundamental problem in the design of an operational amplifier is the development of sufficient negative feedback over a reasonably broad frequency range. The associated problem is the realization of satisfactory stability margins. Finally there is the problem of reducing the drift which is inherent in direct coupled amplifiers and particularly troublesome for transistors because of the variation in their characteristics with temperature.

The first step in the design is the blocking out of the configuration for the forward gain circuit (designated A in Fig. 1). Three primary requirements must be satisfied:

(1) Stages must be direct coupled.

(2) Amplifier must provide one net phase reversal.

(3) Amplifier must have enough current gain to meet accuracy requirements.

Three possible transistor connections are available:[3] (a) the common base connection which may be considered analogous to the common grid vacuum tube connection; (b) the common emitter connection which is analogous to the common cathode connection; and (c) the common collector connection which is analogous to the cathode follower connection. These three configurations together with their approximate equivalent circuits are shown in Fig. 2. It has been shown[4] that for most junction transistors the circuit element a is given by the expression

$$a = \operatorname{sech}\left[\frac{W}{L_m}(1 + p\tau_m)^{1/2}\right] \qquad (1)^*$$

where W is the thickness of the transistor base region, L_m is the diffusion length and τ_m the lifetime of minority charge carriers in the base region,

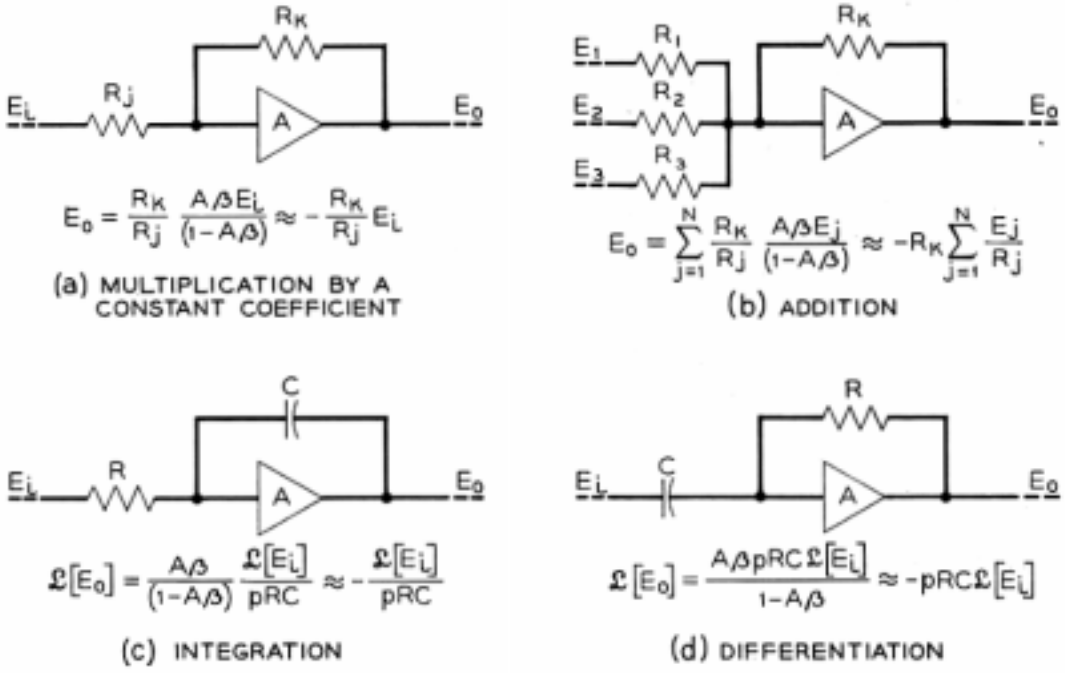


Fig. 1 — Summary of operational amplifiers.

* This expression assumes that the injection factor γ and the collector efficiency α_i are both unity. This is a good approximation for all alloy junction transistors and most grown junction transistors.

and $p = j\omega$. At frequencies less than $\omega_a/2\pi$, (1) can be approximated by

$$a = \frac{a_0}{1 + \frac{p}{\omega_a}} \qquad (2)^5$$

where a_0 is the low frequency value of

$$a \approx 1 - \frac{1}{2}\left(\frac{W}{L_m}\right)^2, \qquad \text{and} \qquad \omega_a = \frac{2.4 D_m}{W^2}$$

(D_m is the diffusion constant for the minority charge carriers in the base region). A readily measured parameter called alpha (α), the short circuit current gain of a junction transistor in the common base connec-

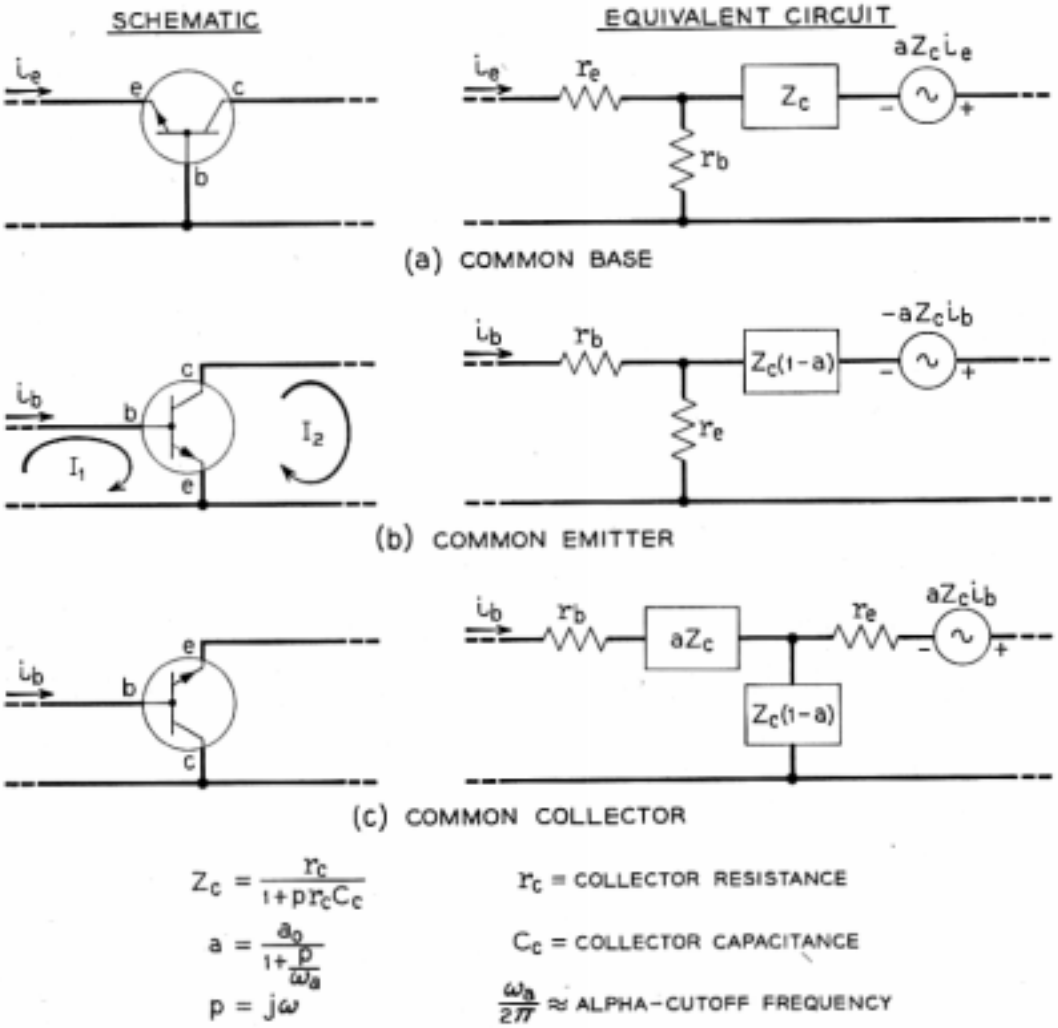


Fig. 2 — Basic transistor connections.

tion, is related to a by the equation

$$\alpha = \frac{aZ_c + r_b}{Z_c + r_b} \tag{3}$$

For most junction transistors the base resistance, r_b, is much smaller than the collector impedance $| Z_c |$, at frequencies less than $\omega_a/2\pi$. Therefore, $\alpha \approx a$ and $\omega_a/2\pi$ is very nearly equal to the alpha-cutoff frequency, the frequency at which $| \alpha |$ is down by 3 db.

The transistor parameters r_e and r_b are actually frequency sensitive and should be represented as impedances.[6] However, good agreement between theory and experiment is obtained at frequencies less than $\omega_a/2\pi$ with r_e and r_b assumed constant.

The choice of an appropriate transistor connection for a direct coupled, negative feedback amplifier, is based on the following reasoning. The common base connection may be ruled out immediately because this connection does not provide current gain unless a transformer interstage is used. The common emitter connection provides short circuit current gain and a phase reversal for each stage. Thus if the amplifier is composed of an odd number of common emitter stages, all three requirements previously listed, are satisfied. A common emitter cascade has the additional practical advantage, that by alternating n-p-n and p-n-p types of transistors, the stages can be direct coupled with practically zero interstage loss.[7]

The common collector connection provides short circuit current gain but no phase reversal. Consequently, the dc amplifier cannot consist entirely of common collector stages and operate as a negative feedback amplifier. This paper will consider only the common emitter connection since, in general, for the same number of transistor stages, the common emitter cascade provides more current gain than a cascade composed of both common collector and common emitter stages.

2.1 *Evaluation of External Voltage Gain*

Since the equivalent circuit of the junction transistor is current activated, it is convenient to treat feedback in a single loop transistor amplifier as a loop current transmission (refer to Appendix I) instead of as a loop voltage transmission which is commonly used for single loop vacuum tube amplifiers.[8] Fig. 3 shows a single loop feedback amplifier in which a fraction of the output current is fed back to the input. A is defined as the short circuit current gain of the amplifier without feedback, and β is defined as the fraction of the short circuit output current (or Norton

equivalent circuit current) fed back to the input summing node. With these definitions,

$$I_{SC} = AI_{IN}' \tag{4}$$

$$I_\beta = \beta I_{SC} \tag{5}$$

where I_{SC} is the Norton equivalent short circuit current.

From Kirchhoff's first law

$$I_{IN}' = I_{IN} + I_\beta \tag{6}$$

Combining relations (4) to (6) yields

$$\frac{I_{SC}}{I_{IN}} = \frac{A}{1 - A\beta} \tag{7}$$

Expression (7) provides a convenient method for evaluating the external

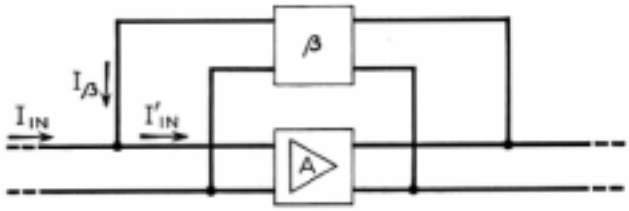


Fig. 3 — Single loop feedback amplifier.

voltage gain of an operational amplifier. Fig. 4 shows a generalized operational amplifier with N inputs. With this configuration,

$$I_{IN} = \sum_{j=1}^{N} \left[\frac{E_j - \frac{I_{SC}}{A} Z_{IN}'}{Z_j} \right] \tag{8}$$

where E_j, $j = 1, 2, \cdots, N$, are the N input voltages referred to the ground node.

Z_j, $j = 1, 2, \cdots, N$, are the N input impedances

Z_{IN}' is the input impedance of the amplifier measured at the summing node with the feedback loop opened.

$$I_\beta = \frac{E_{OUT} - Z_{IN}' \frac{I_{SC}}{A}}{Z_K} \tag{9}$$

$$E_{OUT} = \frac{I_{SC} - I_\beta}{\frac{1}{R_L} + \frac{1}{Z_{OUT}'}} \tag{10}$$

where Z_{OUT}' is the output impedance of the amplifier measured with the feedback loop opened. The expression for the output voltage is obtained by combining (7), (8), (9), and (10).

$$E_{OUT} = \sum_{j=1}^{N} E_j \frac{Z_K}{Z_j} \left[\frac{A\beta + \frac{Z_{IN}'}{Z_K}}{1 - A\beta + \sum_{j=1}^{N} \frac{Z_{IN}'}{Z_j}} \right] \tag{11}*$$

where

$$A\beta = A \left[\frac{1 - \frac{Z_{IN}'}{A} \left(\frac{1}{R_L} + \frac{1}{Z_{OUT}'} \right)}{1 + \frac{Z_K}{R_L} + \frac{Z_K}{Z_{OUT}'}} \right]$$

$A\beta$ is equal to the current returned to the summing node when a unit

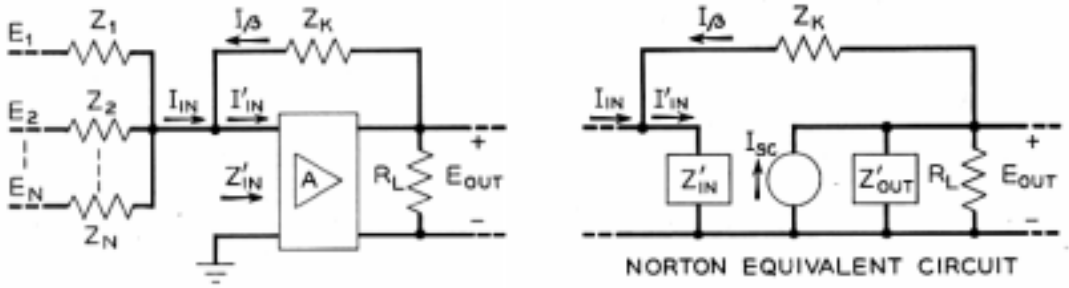


Fig. 4 — Generalized operational amplifier.

current is placed into the base of the first transistor stage ($I_{IN}' = 1$). If $|A\beta|$ is much greater than $|Z_{IN}'/Z_K|$ and

$$1 + \sum_{j=1}^{N} \left| \frac{Z_{IN}'}{Z_j} \right|,$$

then

$$E_{OUT} = -\sum_{j=1}^{N} E_j \frac{Z_K}{Z_j} \tag{12}$$

The accuracy of the operational amplifier depends on the magnitude of $A\beta$ and the precision of the components used in the input and feedback networks as can be seen from (11). There is negligible interaction between the input voltages because the input impedance at the summing node is equal to Z_{IN}' divided by $(1 - A\beta)$.[9] This impedance is usually negligibly small compared to the impedances used in the input circuit.

* In general, E_j and E_{OUT} are the Laplace transforms of the input and output voltages, respectively.

2.2. *Methods Used to Shape the Loop Current Transmission*

An essential consideration in the design of a feedback amplifier is the provision of adequate margins against instability. In order to accomplish this objective, it is necessary to choose a criterion of stability. In Appendix I it is shown that it is convenient and valid to base the stability of single loop transistor feedback amplifiers on the loop current transmission. In order to calculate the loop current transmission of the dc amplifier, the feedback loop is opened at a convenient point in the circuit, usually at the base of one of the transistors, and a unit current is injected into the base (refer to Fig. 24). The other side of the opened loop is connected to ground through a resistance $(r_e + r_b)$ and voltage $r_e I_4$. In many instances, the voltage $r_e I_4$ can be neglected. If $| Z_K |$ and

$$\frac{1}{\left| \sum_{j=1}^{N} \frac{1}{Z_j} \right|}$$

are much greater than $| Z_{IN}' |$, then $A\beta$ is very nearly equal to the loop current transmission. For absolute stability[10] the amplitude of the loop current transmission must be less than unity before the phase shift (from the low frequency value) exceeds 180°. Consequently, this characteristic must be controlled or properly shaped over a wide frequency

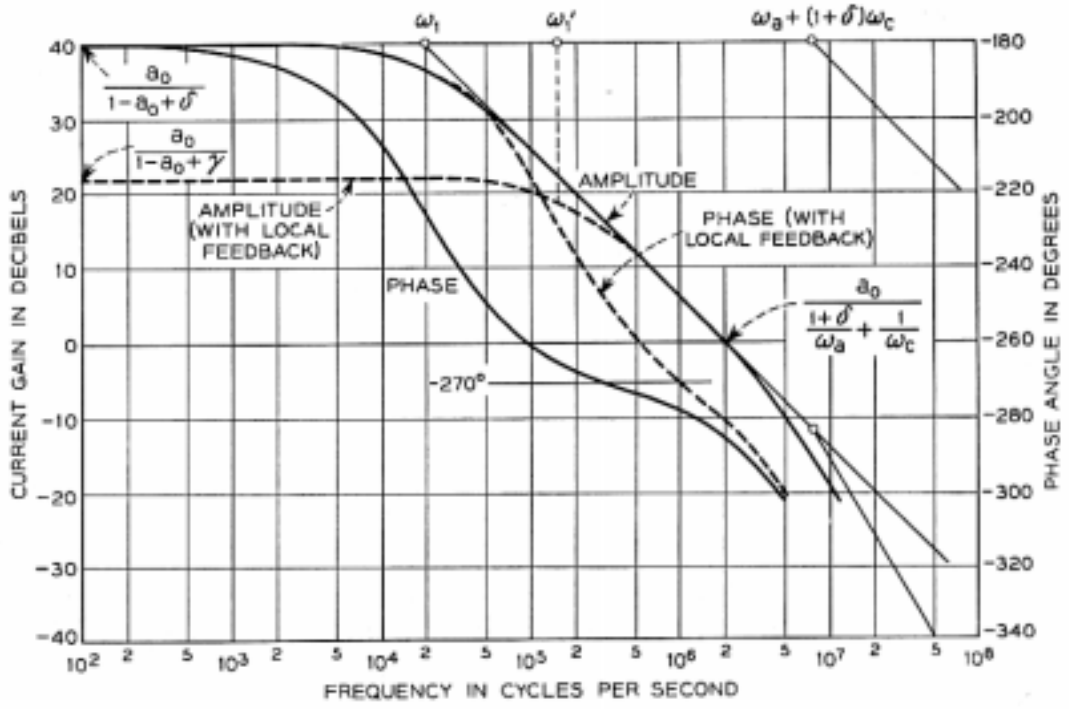


Fig. 5 — Current transmission of a common emitter stage.

band. In addition, it is desirable that the feedback fall off at a rate equal to or less than 9 db per octave in order to insure that the dc amplifier has a satisfactory transient response.

Three methods of shaping are described in this paper; local feedback shaping, interstage network shaping, and β circuit shaping. Local feedback shaping will be described first. The analysis starts by considering the current transmission of a common emitter stage, equivalent circuit shown in Fig. 2(b). If the stage operates into a load resistance R_L, then to a good approximation the current transmission is given by

$$G_I = \frac{I_2}{I_1} = \frac{-\dfrac{a_0}{1 - a_0 + \delta}}{1 + \dfrac{p}{\omega_1} + \dfrac{p^2}{\omega_a \omega_c (1 - a_0 + \delta)}} \qquad (13)^*$$

where

$$\delta = \frac{R_L + r_e}{r_c}$$

$$\omega_1 = \frac{(1 - a_0 + \delta)}{\dfrac{1 + \delta}{\omega_a} + \dfrac{1}{\omega_c}}$$

$$\frac{\omega_a}{2\pi} \approx \text{alpha-cutoff frequency}$$

$$\omega_c = \frac{1}{(R_L + r_e)C_c}$$

It is apparent from expression (13) that if $(1 - a_0 + \delta)$ is less than 0.1, then the current gain of the common emitter stage falls off at a rate of 6 db per octave with a corner frequency at ω_1 .† A second 6 db per octave cutoff with a corner frequency at $[\omega_a + (1 + \delta)\omega_c]$ is introduced by the p^2 term in the denominator of (13). A typical transmission characteristic is shown in Fig. 5. The current gain of the common emitter stage is unity at a frequency equal to

$$\frac{a_0}{\dfrac{1 + \delta}{\omega_a} + \dfrac{1}{\omega_c}}$$

* Expressions (13) and (14) are poor approximations at frequencies above $\omega_a/2\pi$.

† Strictly speaking the corner frequency is equal to $\omega_1/2\pi$. However, for simplicity, corner frequencies will be expressed as radian frequencies.

Since the phase crossover of $A\beta$* is usually placed below this frequency, the principal effect of the second cutoff is to introduce excess phase. This excess phase can be minimized by operating the stage into the smallest load resistance possible, thus maximizing ω_c .

An undesirable property of the common emitter transmission characteristic is that the corner frequency ω_1 occurs at a relatively low frequency. However, the corner frequency can be increased by using local feedback as shown in Fig. 6(a). Shunt feedback is used in order to provide a low input impedance for the preceding stage to operate into. The amplitude and phase of the current transmission is controlled principally by the impedances Z_1 and Z_2 . If $| A\beta |$ is much greater than one, and if $\beta \approx Z_1/Z_2$, then from (7) the current transmission of the stage is approximately equal to $-Z_2/Z_1$. Because of the relatively small size of $A\beta$ for a single stage, this approximation is only valid for a very limited range of values of Z_1 and Z_2 . If Z_1 and Z_2 are represented as resistances R_1 and R_2 , then the current transmission of the circuit is given to a good approximation by

$$G_I = \frac{I_2}{I_1} = -\frac{R_2}{(R_2 + r_b)} \cdot \frac{\dfrac{a_0}{1 - a_0 + \gamma}}{\left[1 + \dfrac{p}{\omega_1'} + \dfrac{p^2}{\omega_a \omega_c (1 - a_0 + \gamma)}\right]} \tag{14}$$

where

$$\gamma = \frac{R_1 + r_e}{\dfrac{(R_2 + r_b) r_c}{R_2 + r_b + r_c}} \approx \frac{R_1 + r_e}{R_2 + r_b}$$

$$\omega_1' = \frac{(1 + a_0 + \gamma)}{\dfrac{1 + \gamma}{\omega_a} + \dfrac{1}{\omega_c}}$$

$$\omega_c = \frac{1}{(R_1 + r_e) C_e}$$

By comparing (14) with (13), it is evident that the negative feedback has reduced the low-frequency current gain from $a_0/(1 - a_0)$ (δ may usually be neglected) to

$$\left(\frac{R_2}{R_2 + r_b}\right)\left(\frac{a_0}{1 - a_0 + \gamma}\right) \approx \frac{R_2}{R_1 + r_e} \qquad (\text{if } \gamma > 1 - a_0)$$

* The phase crossover of Aβ is equal to the frequency at which the phase shift of Aβ from its low-frequency value is 180°.

The half power frequency, however, has been increased from

$$\frac{1 - a_0}{\frac{1}{\omega_\alpha} + \frac{1}{\omega_c}} \quad \text{to} \quad \frac{1 - a_0 + \gamma}{\frac{1 + \gamma}{\omega_\alpha} + \frac{1}{\omega_c}}$$

as shown by the dashed curves in Fig. 5.*

The bandwidth of the common emitter stage can be increased without reducing the current gain at dc and low-frequencies by representing Z_1 by a resistance R_1, and Z_2 by a resistance R_2 in series with a condenser C_2. If $1/R_2C_2$ is much smaller than ω_1', then the current transmission of the stage is given by (14) multiplied by the factor

$$\frac{\left(1 + \frac{\omega_2}{p}\right)}{\left(1 + \frac{\omega_4}{p}\right)} \tag{15}$$

where

$$\omega_2 = \frac{1}{R_2C_2}$$

$$\omega_4 = \frac{1 - a_0 + \frac{R_1 + r_e}{r_c}}{C_2(R_2 + r_b)(1 - a_0 + \gamma)}$$

The current transmission for this case is plotted in Fig. 6(b). The condenser C_2 introduces a rising 6 db per octave asymptote with a corner frequency at ω_2. At dc the current gain is equal to

$$\frac{a_0}{1 - a_0 + \delta}$$

A second method of shaping the loop current transmission characteristic of a feedback amplifier is by means of interstage networks. These networks are usually used for reducing the loop current gain at relatively low frequencies while introducing negligible phase lag near the gain† and phase crossover frequencies. Interstage networks should be designed to take advantage of the variable transistor input impedance. The input impedance of a transistor in the common emitter connection

* In Figs. 5 and 6(b), the factor $R_2/(R_2 + r_b)$ is assumed equal to unity. This is a good approximation since in practice R_2 is equal to several thousand ohms while r_b is equal to about 100 ohms.

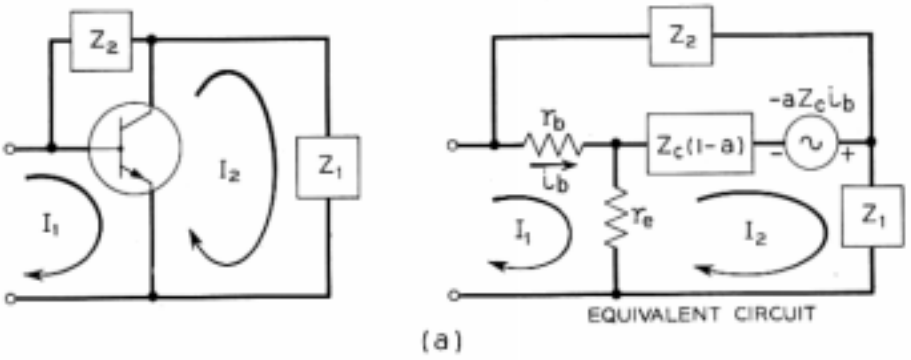
† The gain crossover frequency is equal to the frequency at which the magnitude of $A\beta$ is unity.

is given by the expression

$$Z_{\text{INPUT}} = r_b + r_e(1 - G_I) \tag{16}$$

where G_I is the current transmission given by (13). If G_I at dc is much greater than 1, then the input impedance and the current transmission of the common emitter stage fall off at about the same rate and with approximately the same corner frequency (ω_1). The input impedance finally reaches a limiting value equal to $r_e + r_b$.

A particularly useful interstage network is shown in Fig. 7(a). This network is analyzed in Appendix II and Fig. 7(b) shows a plot of the



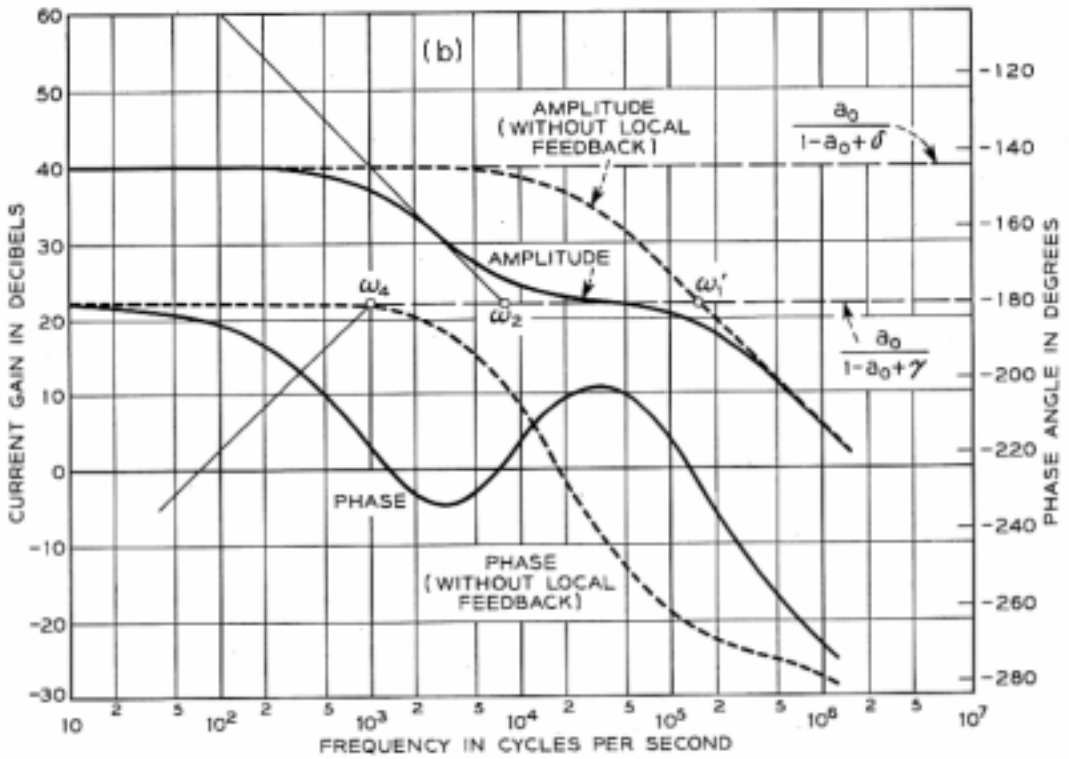
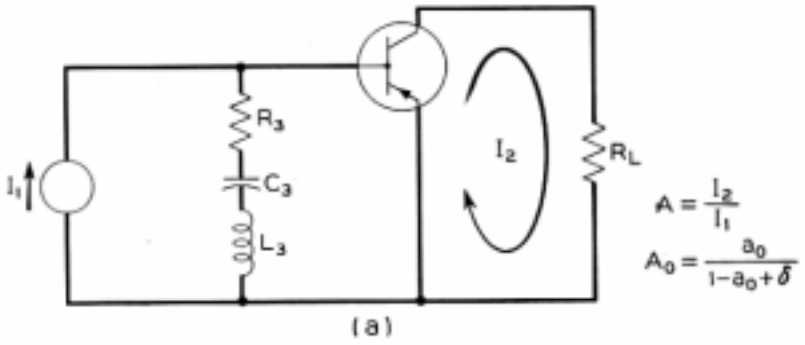


Fig. 6 — Negative feedback applied to a common emitter stage.

resulting current transmission. The amplitude of the transmission falls off at a rate of 6 db per octave with the corner frequency ω_5 determined by C_3 and the low frequency value of the transistor input impedance. The inductance L_3 introduces a 12 db per octave rising asymptote with a corner frequency at $\omega_3 = 1/\sqrt{L_3C_3}$. The corner frequencies ω_3 and ω_5 are selected in order to obtain a desirable loop current transmission characteristic (specific transmission characteristics are presented in Sections 3.0 and 4.0). The half power frequency of the current transmission of the transistor, ω_1, does not appear directly in the transmission characteristic of the circuit because of the variation in the transistor input impedance with frequency.

The overall β circuit of the feedback amplifier can also be used for



(a)

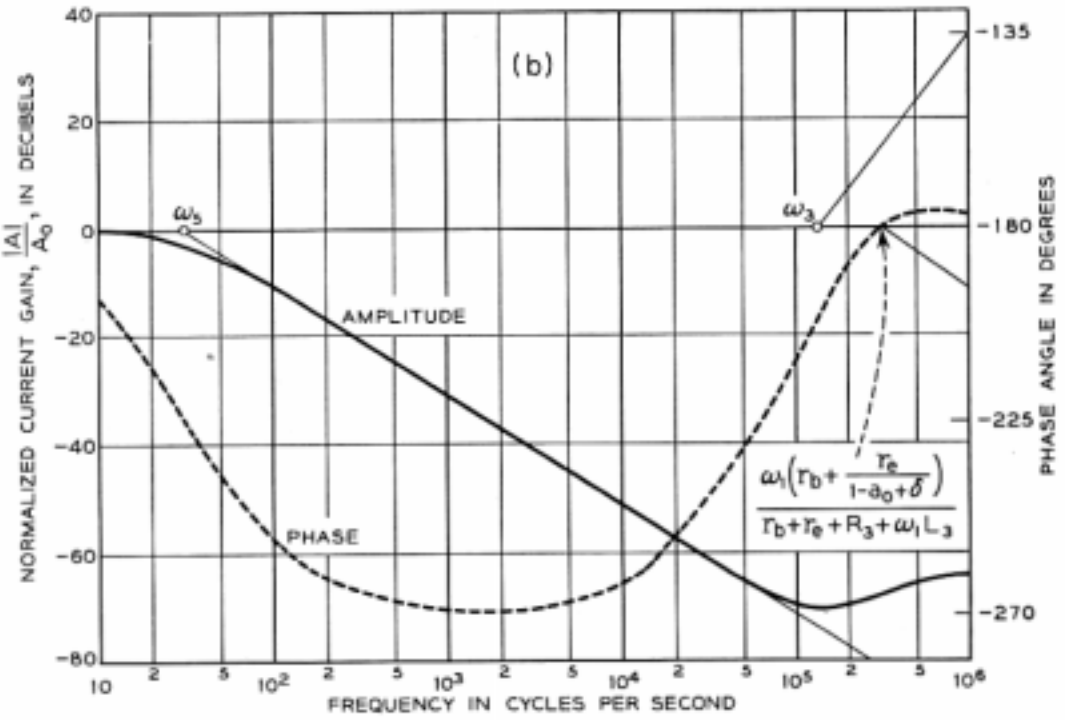


Fig. 7 — Interstage shaping network.

shaping the loop current transmission. If the feedback impedance Z_K (Fig. 4) consists of a resistance R_K and condenser C_K in parallel, then the loop current transmission is modified by the factor

$$\frac{\left(1 + \frac{p}{\omega_7}\right)}{\left(1 + \frac{p}{\omega_8}\right)} \tag{17}$$

where

$$\omega_7 = \frac{1}{R_K C_K}$$

$$\omega_8 = \frac{(R_L + R_K)}{R_L R_K C_K}$$

Since Z_K affects the external voltage gain of the operational amplifier, (11), the corner frequency ω_7 must be located outside of the useful frequency band. Usually it is placed near the gain crossover frequency in order to improve the phase margin and the transient response of the amplifier.

In Sections 3.0 and 4.0, the above shaping techniques are used in the design of specific operational amplifiers.

3.0. THE SUMMING AMPLIFIER

3.1. *Circuit Arrangement*

The schematic diagram of a dc summing amplifier is shown in Fig. 8. From the discussion in Section 2.0 it is apparent that each common emitter stage will contribute more than 90 degrees of high-frequency phase lag. Consequently, while the magnitude of the low-frequency feedback increases with the number of stages, this is at the expense of the bandwidth over which the negative feedback can be maintained. It is possible to develop 80 db of negative feedback at dc with three common emitter stages. This corresponds to a dc accuracy of one part in 10,000. In addition, the feedback can be maintained over a broad enough band in order to permit full accuracy to be attained in about 100 microseconds. Thus it is evident that the choice of three stages represents a satisfactory compromise between accuracy and bandwidth objectives.

The output stage of the amplifier is designed for a maximum power dissipation of 75 milliwats and maximum voltage swing of ±25 volts

when operating into an external load resistance equal to or greater than 50,000 ohms. A p-n-p transistor is used in the second stage and n-p-n transistors are used in the first and third stages. This circuit arrangement makes it possible to connect the collector of one transistor directly to the base of the following transistor without introducing appreciable interstage loss. "Shot" noise[11] and dc drift are minimized by operating the first stage at the relatively low collector current of 0.25 milliamperes. The 110,000-ohm resistor provides the collector current for the first stage, and the 4,700-ohm resistor provides 3.8 milliamperes of collector current for the second stage. The series 6,800-ohm resistor between the second and third stages, reduces the collector to emitter potential of the second stage to about 4.5 volts.

The loop current transmission is shaped by use of local feedback applied to the second stage, by an interstage network connected between the second and third stages, and by the overall β circuit. The 200-ohm resistor in the collector circuit of the second stage is, with reference to Fig. 6(a), Z_1 . The impedance of the interstage network can be neglected since it is small compared to 200 ohms at all frequencies for which the local feedback is effective. The interstage network is connected between the second and third stages in order to minimize the output noise voltage. With this circuit arrangement, practically all of the output noise voltage

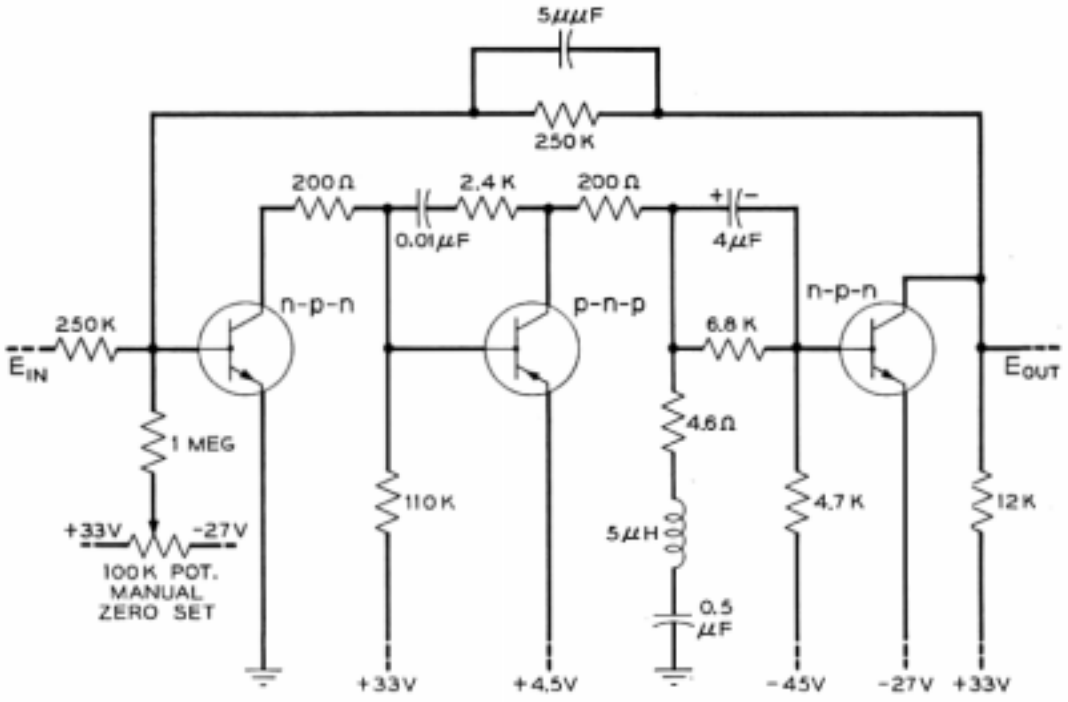


Fig. 8 — DC summing amplifier.

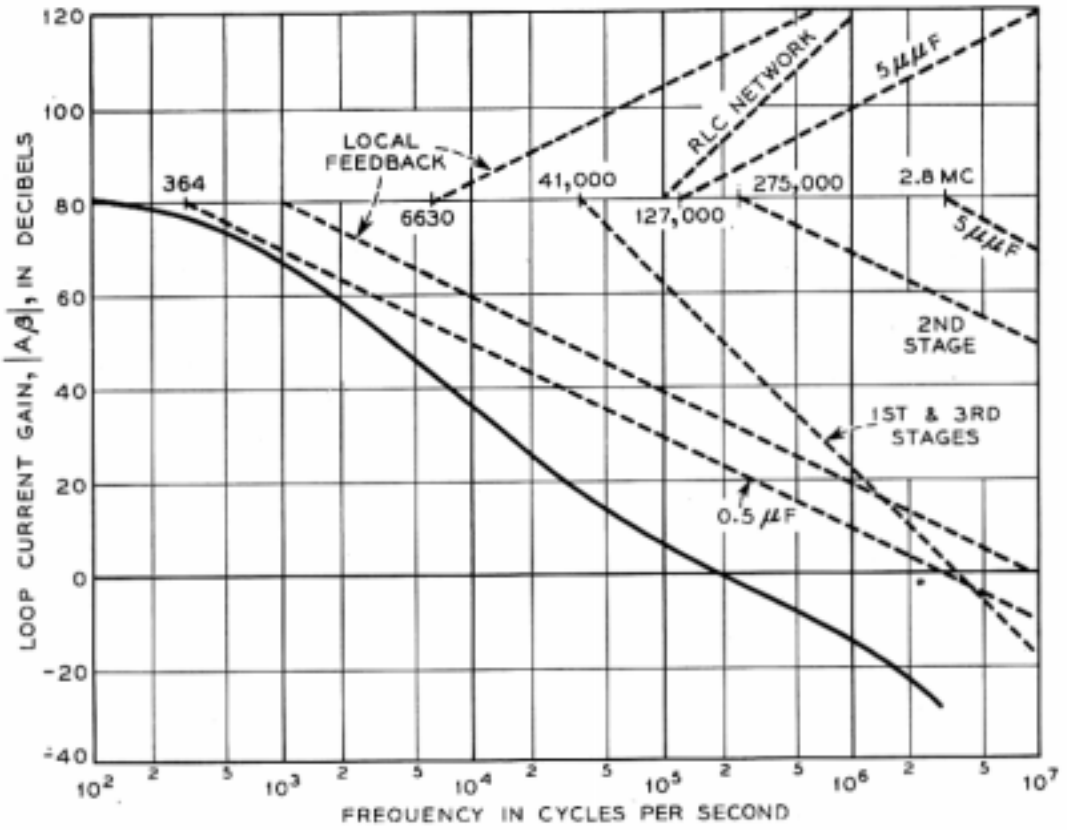


Fig. 9 — Gain-frequency asymptotes for summing amplifier.

is generated in the first transistor stage. If the transistor in the first stage has a noise figure less than 10 db at 1,000 cycles per second, then the RMS output noise voltage is less than 0.5 millivolts.

Fig. 9 shows a plot of the gain-frequency asymptotes for the summing amplifier determined from (13), (14), (15), (17), and (A6) under the assumption that the alphas and alpha-cutoff frequencies of the transistors are 0.985 and 3 mc, respectively. The corner frequencies introduced by the 0.5 microfarad condenser in the interstage network, the local feedback circuit, and the cutoff of the first and third stages are so located that the current transmission falls off at an initial rate of about 9 db per octave. This slope is joined to the final asymptote of the loop transmission by means of a step-type of transition.[12] The transition is provided by 3 rising asymptotes due to the interstage shaping network, and the overall β circuit. An especially large phase margin is used in order to insure a good transient performance.

Fig. 10 shows the amplitude and phase of the loop current transmission. When the amplitude of the transmission is 0 db, the phase angle is $-292°$, and when the phase angle is $-360°$, the amplitude is 27.5 db

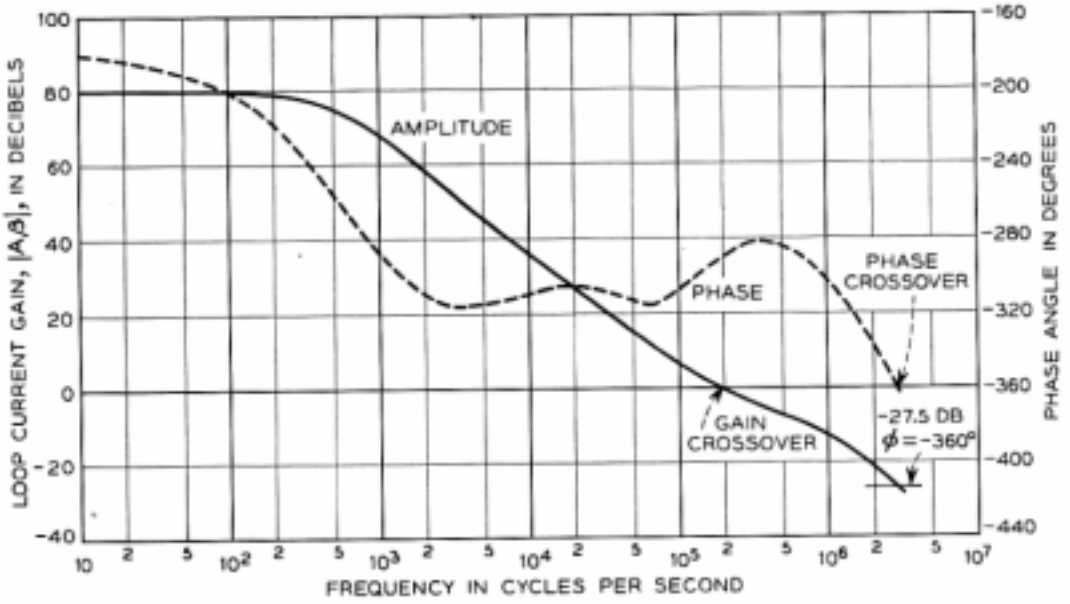


Fig. 10 — Loop current transmission of the summing amplifier.

below 0 db. The amplifier has a 68° phase margin and 27.5 db gain margin. In order to insure sufficient feedback at dc and adequate margins against instability, the transistors used in the amplifier should have alphas in the range 0.98 to 0.99 and alpha-cutoff frequencies equal to or greater than 2.5 mc.

3.2. *Automatic Zero Set of the dc Summing Amplifier*

The application of germanium junction transistors to dc amplifiers does not eliminate the problem of drift normally encountered in vacuum tube circuits. In fact, drift is more severe due principally to the variation of the transistor parameters alpha and saturation current with temperature variation. Even though the amplifier has 80 db of negative feedback at dc, this feedback does not eliminate the drift introduced by the first transistor stage. Because of the large amount of dc feedback, the collector current of the first stage is maintained relatively constant. The collector current of the transistor is related to the base current by the equation

$$I_c = \frac{I_{cr}}{1 - a} + \frac{a}{1 - a} I_b \tag{18}$$

The saturation current, I_{CO}, of a germanium junction transistor doubles approximately for every 11°C increase in temperature. The factor $a/(1 - a)$ increases by as much as 6 db for a 25°C increase in tempera-

ture. Consequently, the base current of the first stage, I_b, and the output voltage of the amplifier must change with temperature in order to maintain I_c constant. The drift due to the temperature variation in a can be reduced by operating the first stage at a low value of collector current. With a germanium junction transistor in the first stage operating at a collector current of 0.25 milliamperes, the output voltage of the amplifier drifts about ± 1.5 volts over a temperature range of 0°C to 50°C. It is possible to reduce the dc drift by using temperature sensitive elements in the amplifier.[13, 14] In general, temperature compensation of a transistor dc amplifier requires careful selection of transistors and critical adjustment of the dc biases. However, even with the best adjustments, temperature compensation cannot reduce the drift in the amplifier to within typical limits such as ± 5 millivolts throughout a temperature range of 0 to 50°C. In order to obtain the desired accuracy it is necessary to use an automatic zero set (AZS) circuit.

Fig. 11 shows a dc summing amplifier and a circuit arrangement for reducing any dc drift that may appear at the output of the amplifier. The output voltage is equal to the negative of the sum of the input voltages, where each input voltage is multiplied by the ratio of the feedback resistor to its input resistor. In addition, an undesirable dc drift voltage is also present in the output voltage. The total output voltage is

$$E_{\text{out}} = -\sum_{j=1}^{N} E_j \frac{R_K}{R_j} + E_{\text{drift}} \tag{19}$$

In order to isolate the drift voltage, the N input voltages and the output voltage are applied to a resistance summing network composed of resistors R_0, R_1', R_2', $\cdots$, R_N'. The voltage across R_s is equal to

$$E_s = \frac{R_s}{R_0} E_{\text{drift}} \tag{20}$$

if

$$R_s \ll R_0, R_j'; \qquad j = 1, 2, \cdots, N$$

and

$$R_0 R_j = R_K R_j'; \qquad j = 1, 2, \cdots, N$$

The voltage E_s is amplified in a relatively drift-free narrow band dc amplifier and is returned as a drift correcting voltage to the input of the dc summing amplifier. If the gain of the AZS circuit is large, the drift voltage at the output of the summing amplifier can be made very small.

Fig. 12 shows the circuit diagram of a summing amplifier which uses a mechanical chopper in the AZS circuit.[15] The AZS circuit consists of a

resistance summing network, a 400-cycle synchronous chopper, and a tuned 400-cycle amplifier. Any drift in the summing amplifier will produce a dc voltage E_s at the output of the summing network. The chopper converts the dc voltage into a 400 cycles per second waveform. The fundamental frequency in the waveform is amplified by a factor of about 400,000 by the tuned amplifier. The synchronous chopper rectifies the sinusoidal output voltage and preserves the original dc polarity of E_s. The rectified voltage is filtered and fed back to the summing amplifier as an additional input current. The loop voltage gain of the AZS circuit at dc is about 54 db. Any dc or low-frequency drift in the summing amplifier is reduced by a factor of about 500 by the AZS circuit. The drift throughout a temperature range of 0 to 50°C is reduced to ±3 millivolts.

Since the drift in the summing amplifier changes at a relatively slow rate, the loop voltage gain of the AZS circuit can be cutoff at a relatively low frequency. In this particular case the loop voltage gain is zero db at about 10 cycles per second.

4.0. THE INTEGRATOR

4.1. *Basic Design Considerations*

The design principles previously discussed are illustrated in this section by the design of a transistor integrator for application in a voltage

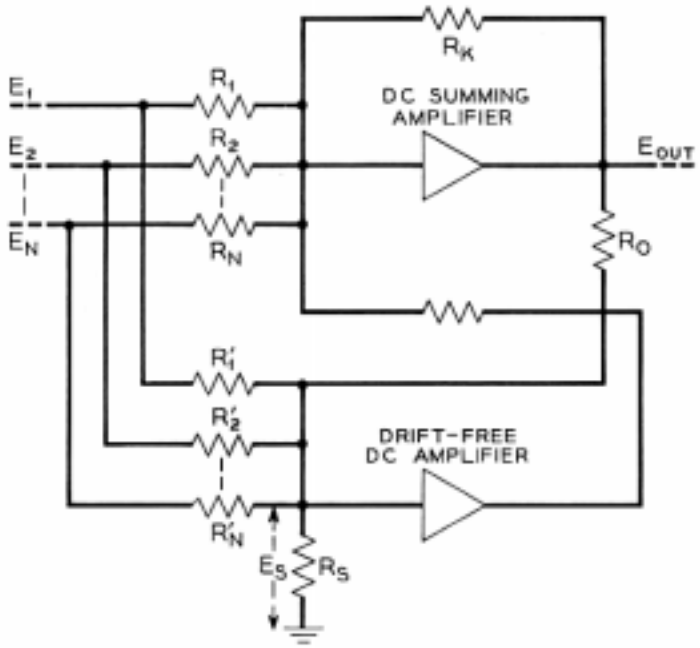


Fig. 11 — DC summing amplifier with automatic zero set.

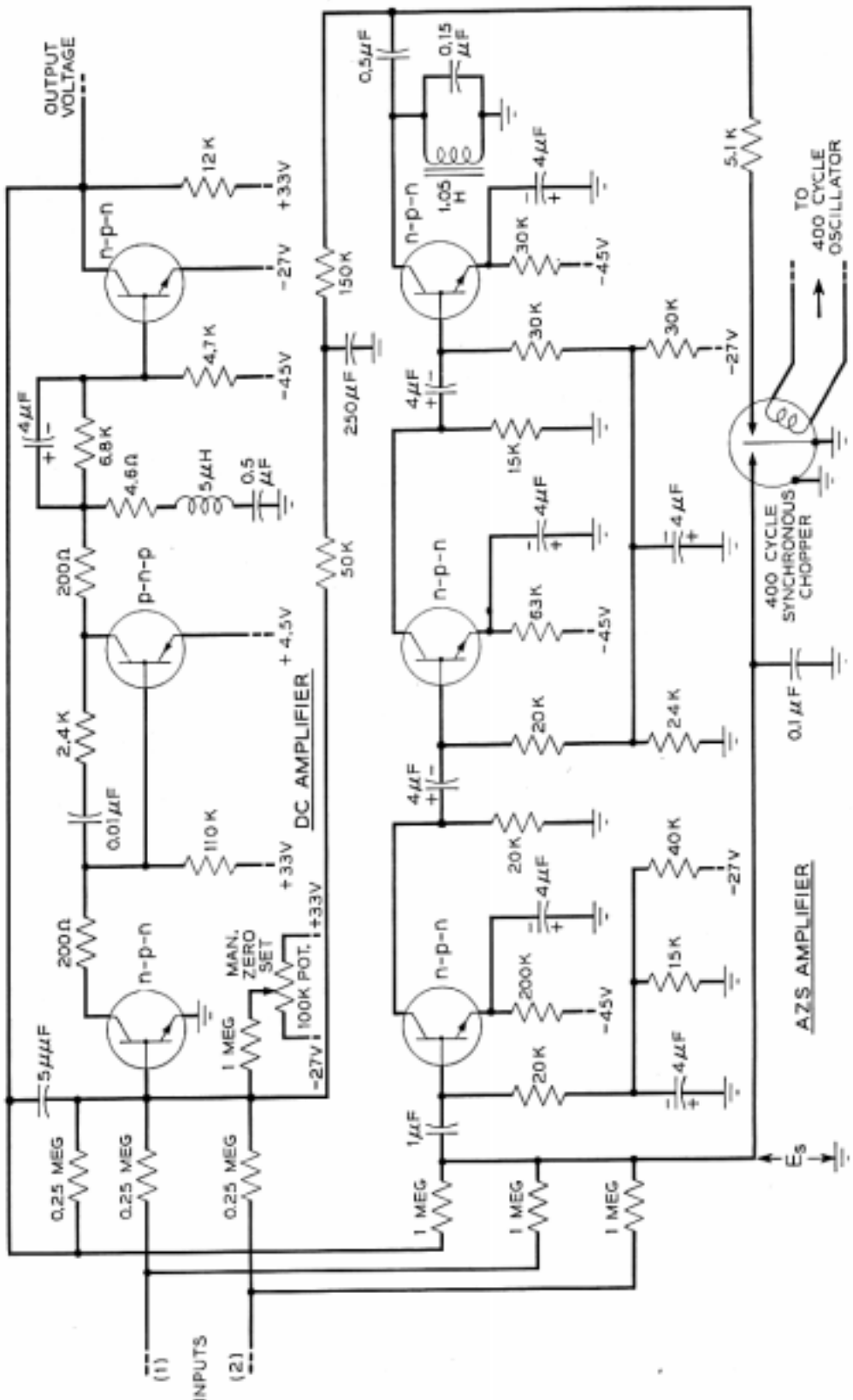


Fig. 12 — Summing amplifier.

encoder. The integrator is required to generate a 15-volt ramp which is linear and has a constant slope to within one part in 8,000. This ramp is to have a slope of 5 millivolts per microsecond for an interval of 3,000 microseconds.

The first step in the design is to determine the bandwidth over which the negative feedback must be maintained in order to realize the desired output voltage linearity. The relationship between the output and input voltage of the integrator can be obtained from expression (11) by substituting $(1/pc)$ for Z_K and R for Z_j (refer to Fig. 1).

$$\mathfrak{L}[E_{OUT}] = \frac{\mathfrak{L}[E_{IN}]}{pRC}\left[\frac{A\beta + Z_{IN}'pC}{1 - A\beta + \dfrac{Z_{IN}'}{R}}\right] \tag{21}$$

where $\mathfrak{L}[E_{OUT}]$ and $\mathfrak{L}[E_{IN}]$ are the Laplace transforms of the output and input voltages, respectively. In order to generate the voltage ramp, a step voltage of amplitude E is applied to the input of the integrator. The term Z_{IN}'/R is negligible compared to unity at all frequencies. Therefore,

$$\mathfrak{L}[E_{OUT}] = \frac{E}{p^2RC}\left[\frac{A\beta}{1 - A\beta}\right] + \frac{EZ_{IN}'}{pR}\left[\frac{1}{1 - A\beta}\right] \tag{22}$$

It will be assumed that $A\beta$ is given by the expression

$$A\beta = \frac{-K}{\left(1 + \dfrac{\omega_1}{p}\right)\left(1 + \dfrac{p}{\omega_2}\right)^2} \tag{23}$$

Expression (23) implies that $A\beta$ falls off at a rate of 6 db per octave at low frequencies and 12 db per octave at high frequencies. The output voltage of the integrator, as a function of time, is readily evaluated by substituting (23) into (22) and taking the inverse Laplace transform of the results. A good approximation for the output voltage is

$$E_{OUT} = -\frac{E}{RC}\left[t - \frac{\omega_1 t^2}{2K} - \frac{e^{-[(2\omega_2+\omega_1)\,t/2]}\sin\sqrt{K}\omega_2 t}{\sqrt{K}\omega_2}\right] + \frac{ER_{IN}'}{R}\left[1 - e^{-(\omega_1 t/K)} + e^{-[(2\omega_2+\omega_1)\,t/2]}\cos\sqrt{K}\omega_2 t\right] \tag{24}*$$

The linear voltage ramp is expressed by the term $-(Et/RC)$. The additional terms introduce nonlinearities. The voltage ramp has a slope of 5 millivolts per microsecond for $E = -21$ volts, $R = 42{,}000$ ohms,

* In evaluating E_{OUT} it was assumed that Z_{IN}' was equal to a fixed resistance R_{IN}', the low frequency input resistance to the first common emitter stage. A complete analysis indicates that this assumption makes the design conservative.

and $C = 0.1$ microfarads. For these circuit values, and $K = 10{,}000$ (corresponding to 80 db of feedback) the nonlinear terms are less than 1/8,000 of the linear term (evaluated when $t = 4 \times 10^{-3}$ seconds) if $f_1 \leqq 30$ cycles per second, $f_2 \geqq 800$ cycles per second, and if the first 1000 microseconds of the voltage ramp are not used. Consequently, 80 db of negative feedback must be maintained over a band extending from 30 to 800 cycles per second in order to realize the desired output voltage linearity.

4.2. *Detailed Circuit Arrangement*

Fig. 13 shows the circuit diagram of the integrator. The method of biasing is the same as is used in the summing amplifier. The 200,000-ohm resistor provides approximately 0.5 milliamperes of collector current for the first stage. The 40,000-ohm resistor provides approximately 0.9 milliamperes of collector current for the second stage. The output stage is designed for a maximum power dissipation of 120 milliwatts and for an output voltage swing between -5 and $+24$ volts when operating into a load resistance equal to or greater than 40,000 ohms.

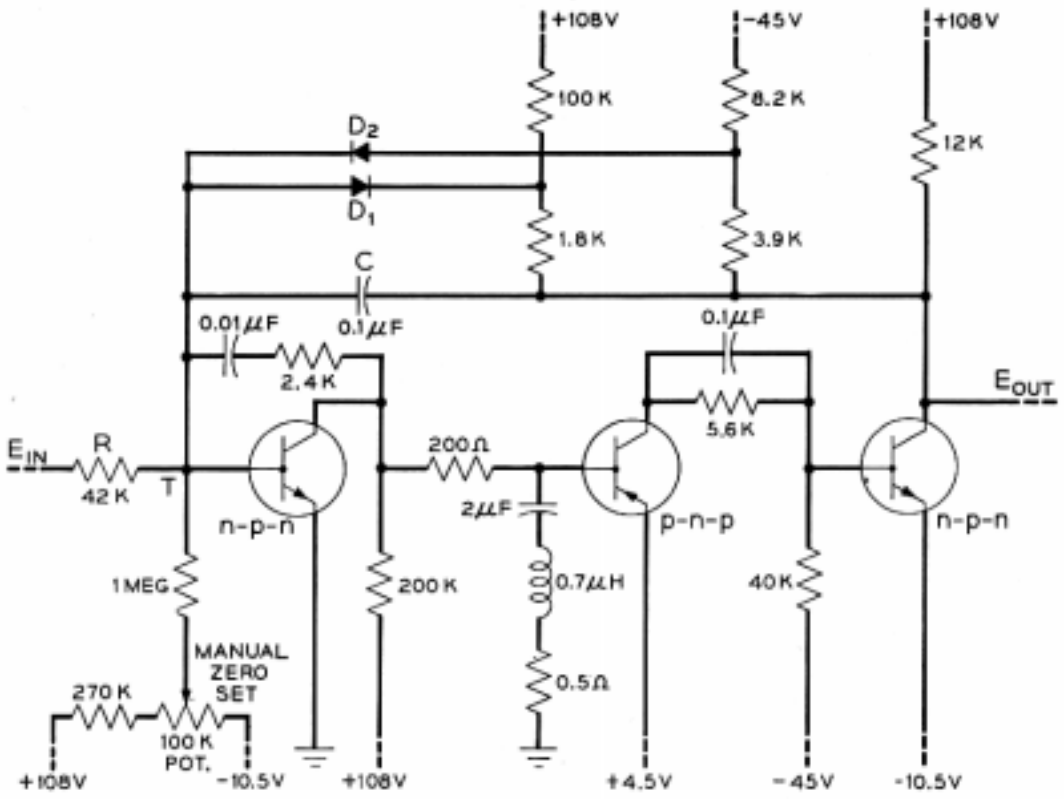


Fig. 13 — Integrator.

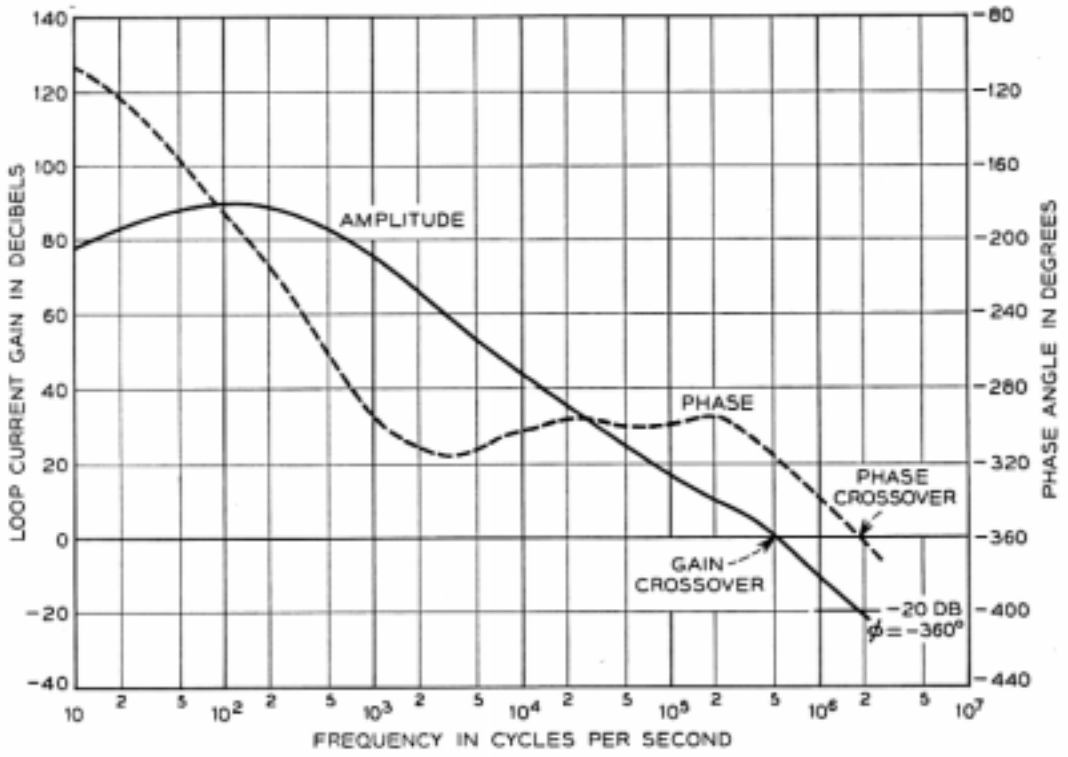


Fig. 14 — Loop current transmission of the integrator.

The negative feedback in the integrator has been shaped by means of local feedback and interstage networks as described in Section 2.2. The loop current transmission has been calculated from (13), (14), (15), and (A6) and is plotted in Fig. 14. The transmission is determined under the assumption that the alphas of the transistors are 0.985 and the alpha-cutoff frequencies are three megacycles. Since the feedback above 800 cycles per second falls off at a rate of 9 db per octave, the analysis in Section 4.1 using (23), is conservative. The integrator has a 44° phase margin and a 20 db gain margin. In order to insure sufficient feedback between 30 and 800 cycles per second and adequate margins against instability, the transistors used in the integrator should have alphas in the range 0.98 to 0.99 and alpha-cutoff frequencies equal to or greater than 2.5 megacycles.

The silicon diodes D_1 and D_2 are required in order to prevent the integrator from overloading. For output voltages between -4.0 and 21 volts the diodes are reverse biased and represent very high resistances, of the order of 10,000 megohms. If the output voltage does not lie in this range, then one of the diodes is forward biased and has a low resistance, of the order of 100 ohms. The integrator is then effectively a dc amplifier with a voltage gain of approximately 0.1. The silicon diodes affect the

linearity of the voltage ramp slightly due to their finite reverse resistances and variable shunt capacities. If the diodes have reverse resistances greater than 1000 megohms, and if the maximum shunt capacity of each diode is less than 10 micromicrofarads (capacity with minimum reverse voltage), then the diodes introduce negligible error.

As stated earlier, the integrator generates a voltage ramp in response to a voltage step. This step is applied through a transistor switch which is actuated by a square wave generator capable of driving the transistor well into current saturation. Such a switch is required because the equivalent generator impedance of the applied step voltage must be very small. A suitable circuit arrangement is shown in Fig. 15. For the particular application under discussion the switch S is closed for 5,000 microseconds. During this time, the voltage $E = -21V$ appears at the input of the integrator. At the end of this time interval, the transistor switch is opened and a reverse current is applied to the feedback condenser C, returning the output voltage to -4.0 volts in about 2500 microseconds. An alternate way of specifying a low impedance switch is to say that the voltage across it be close to zero. For the transistor switch, connected as shown in Fig. 15, this means that its collector voltage be within

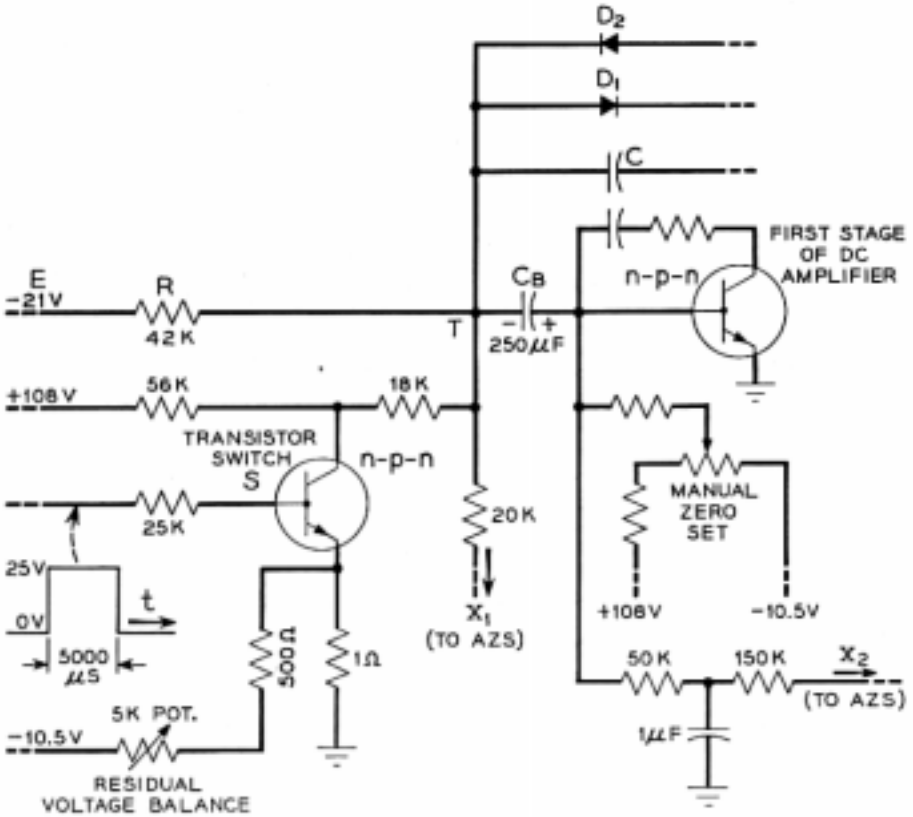


Fig. 15 — Input circuit arrangement of the integrator.

one millivolt of ground potential during the time the transistor is in saturation. Now, it has been shown[16] that when a junction transistor in the common emitter connection is driven into current saturation, the minimum voltage between collector and emitter is theoretically equal to

$$\frac{kT}{q} \ell n \frac{1}{\alpha_i} \tag{25}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the charge of an electron ($(kT/q) = 26$ millivolts at room temperature), and α_i is the inverse alpha of the transistor, i.e., the alpha with the emitter and collector interchanged. There is an additional voltage drop across the transistor due to the bulk resistance of the collector and emitter regions (including the ohmic contacts). A symmetrical alloy junction transistor with an alpha close to unity is an excellent switch because both the collector to emitter voltage and the collector and emitter resistances are very small.

At the present time, a reasonable value for the residual voltage* between the collector and emitter is 5 to 10 millivolts. This voltage can be eliminated by returning the emitter of the transistor switch to a small negative potential. This method of balancing is practical because the voltage between the collector and emitter of the transistor does not change by more than 1.0 millivolt over a temperature range of 0°C to 50°C.

4.3. *Automatic Zero Set of the Integrator*

A serious problem associated with the transistor integrator is drift. The drift is introduced by two sources; variations in the base current of the first transistor stage and variations in the base to emitter potential of the first stage with temperature. In order to reduce the drift, the input resistor R and the feedback condenser C must be dissociated from the base current and base to emitter potential of the first transistor stage. This is accomplished by placing a blocking condenser C_B between point T and the base of the first transistor as shown in Fig. 15. An automatic zero set circuit is required to maintain the voltage at point T equal to zero volts. This AZS circuit uses a magnetic modulator known as a "magnettor."[17]

A block diagram of the AZS circuit is shown in Fig. 16. The dc drift current at the input of the amplifier is applied to the magnettor. The carrier current required by the magnettor is supplied by a local transistor

* The inverse alphas of the transistors used in this application were greater than 0.95.

oscillator. The useful output of the magnettor is the second harmonic of the carrier frequency. The amplitude of the second harmonic signal is proportional to the magnitude of the dc input current and the phase of the second harmonic signal is determined by the polarity of the dc input current. The output voltage of the magnettor is applied to an active filter which is tuned to the second harmonic frequency. The signal is then amplified in a tuned amplifier and applied to a diode gating circuit. Depending on the polarity of the dc input current, the gating circuit passes either the positive or negative half cycle of the second harmonic signal. In order to accomplish this, a square wave at a repetition rate equal to that of the second harmonic signal is derived from the carrier oscillator and actuates the gating circuit.

A circuit diagram of the AZS circuit is shown in Figs. 17(a) and 17(b). The various sections of the circuit are identified with the blocks shown in Fig. 16. The active filter is adjusted for a Q of about 300, and the gain of the active filter and tuned amplifier is approximately 1000. The AZS circuit provides ± 1.0 volt of dc output voltage for ± 0.05 microamperes of dc input current. The maximum sensitivity of the circuit is limited to ± 0.005 microamperes because of residual second harmonic generation in the magnettor with zero input current.

When the transistor integrator is used together with the magnettor AZS circuit, the slope of the voltage ramp is maintained constant to within one part in 8,000 over a temperature range of 20°C to 40°C.

5.0. *The Voltage Comparator*

The voltage comparator is one of the most important circuits used in analog to digital converters. The comparator indicates the exact time that an input waveform passes through a predetermined reference level. It has been common practice to use a vacuum tube blocking oscillator as a voltage comparator.[18] Due to variations in the contact potential, heater voltage, and transconductance of the vacuum tube, the maximum

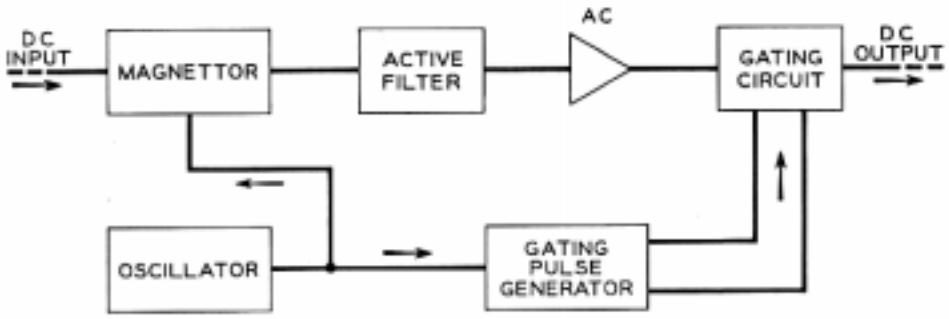


Fig. 16 — Block diagram of AZS circuit.

accuracy of the circuit is limited to about ±100 millivolts. By taking advantage of the properties of semiconductor devices, the transistor blocking oscillator comparator can be designed to have an accuracy of ±5 millivolts throughout a temperature range of 20°C to 40°C.

5.1. *General Description of the Voltage Comparator*

Fig. 18 shows a simplified circuit diagram of the voltage comparator. Except for the silicon junction diode D_1, this circuit is essentially a transistor blocking oscillator. For the purpose of analysis, assume that the reference voltage V_{cc} is set equal to zero. When the input voltage V_i is large and negative, the silicon diode D_1 is an open circuit and the junction transistor has a collector current determined by R_b and E_{bb} [Expression (18)]. The base of the transistor resides at approximately -0.2 volts. As the input voltage V_i approaches zero, the reverse bias across the diode D_1 decreases. At a critical value of V_i (a small positive potential), the dynamic resistance of the diode is small enough to permit the circuit to become unstable. The positive feedback provided by transformer T_1 forces the transistor to turn off rapidly, generating a sharp output pulse across the secondary of transformer T_2. When V_i is large and positive, the diode D_1 is a low impedance and the transistor is maintained cutoff. In order to prevent the comparator from generating more than one output pulse during the time that the circuit is unstable, the natural period of the circuit as a blocking oscillator must be properly chosen. Depending on this period, the input voltage waveform must have a certain minimum slope when passing through the reference level in order to prevent the circuit from misfiring.

The comparator has a high input impedance except during the switching interval.* When V_i is negative with respect to the reference level, the input impedance is equal to the impedance of the reverse biased silicon diode. When V_i is positive with respect to the reference level, the input impedance is equal to the impedance of the reverse biased emitter and collector junctions in parallel. This impedance is large if an alloy junction transistor is used. During the switching interval the input impedance is equal to the impedance of a forward biased silicon diode in series with the input impedance of a common emitter stage (approximately 1,000 ohms). This loading effect is not too serious since for the circuit described, the switching interval is less than 0.5 microseconds.

The voltage comparator shown in Fig. 18 operates accurately on voltage waveforms with positive slopes. The voltage comparator will operate accurately on waveforms with negative slopes if the diode and

* The switching interval is the time required for the transistor to turn off.

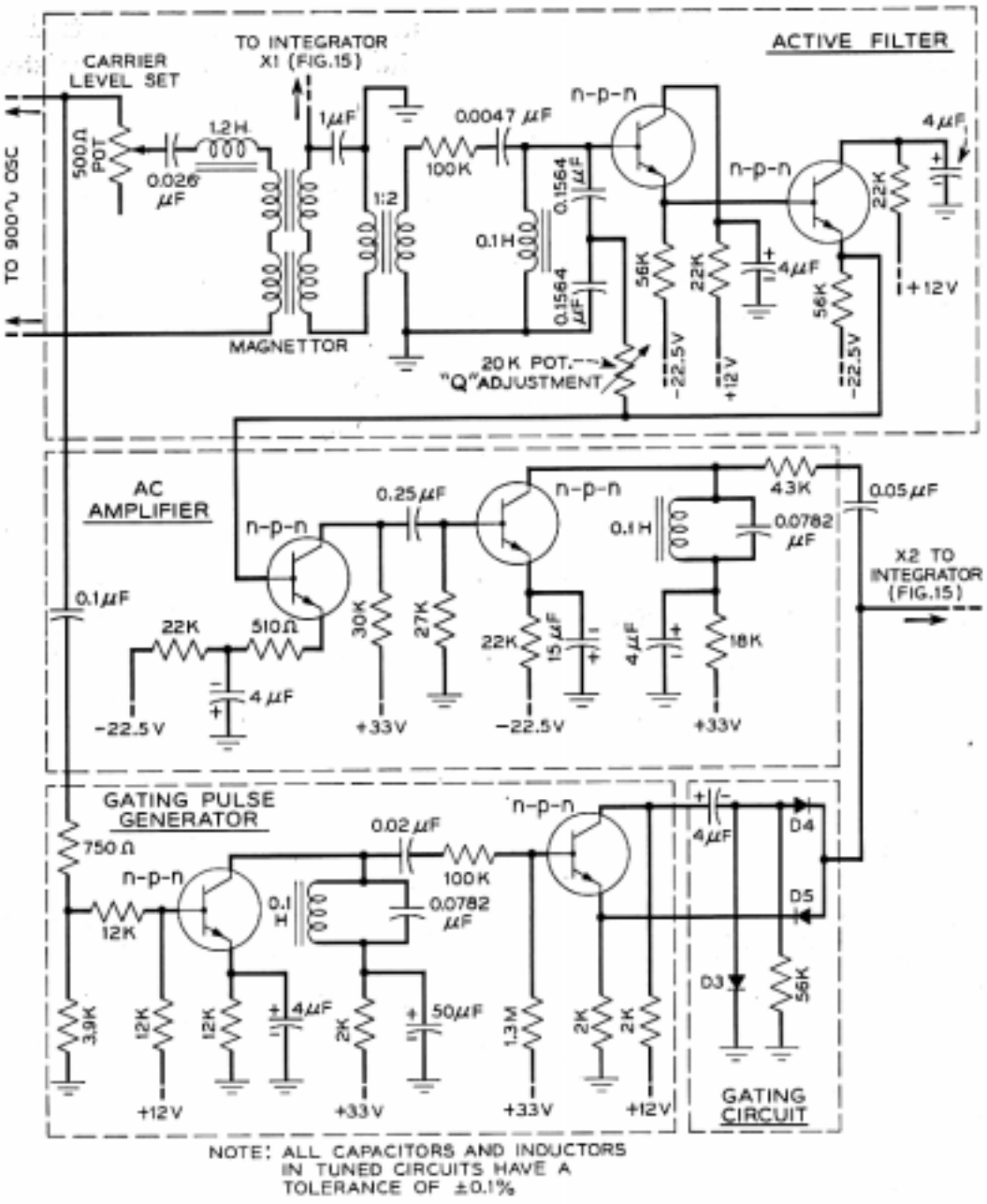


Fig. 17(a) — AZS circuit.

battery potentials are reversed and if an n-p-n junction transistor is used.

5.2. *Factors Determining the Accuracy of the Voltage Comparator*

Fig. 19 shows the ac equivalent circuit of the voltage comparator. In the equivalent circuit R_1 is the dynamic resistance of the diode D_1, Rg is the source resistance of the input voltage, and R_2 is the impedance of

the load R_L as it appears at the primary of the transformer T_2. R_1 is a function of the dc voltage across the diode D_1. At a prescribed value of R_1, the comparator circuit becomes unstable and switches. The relationship between this critical value of R_1 and the transistor and circuit parameters is obtained by evaluating the characteristic equation for the circuit and by determining the relationship which the coefficients of the equation must satisfy in order to have a root of the equation lie in the right hand half of the complex frequency plane. To a good approximation, the critical value of R_1 is given by the expression

$$R_1 + R_g + r_b = \frac{Ma_0}{R_2C_c + \frac{a_0}{\omega_a}} \tag{26}$$

where M is the mutual inductance of transformer T_1 and $R_2 = N'^2R_L$. Since the transistor parameters which appear in expression (26) have only a small variation with temperature, the critical value of R_1 is independent of temperature (to a first approximation).

It will now be shown that the comparator can be designed for an accuracy of ± 5 millivolts throughout a temperature range of 20°C to 40°C. In order to establish this accuracy it will be assumed that the critical value of R_1 is equal to 30,000 ohms. This assumption is based on the

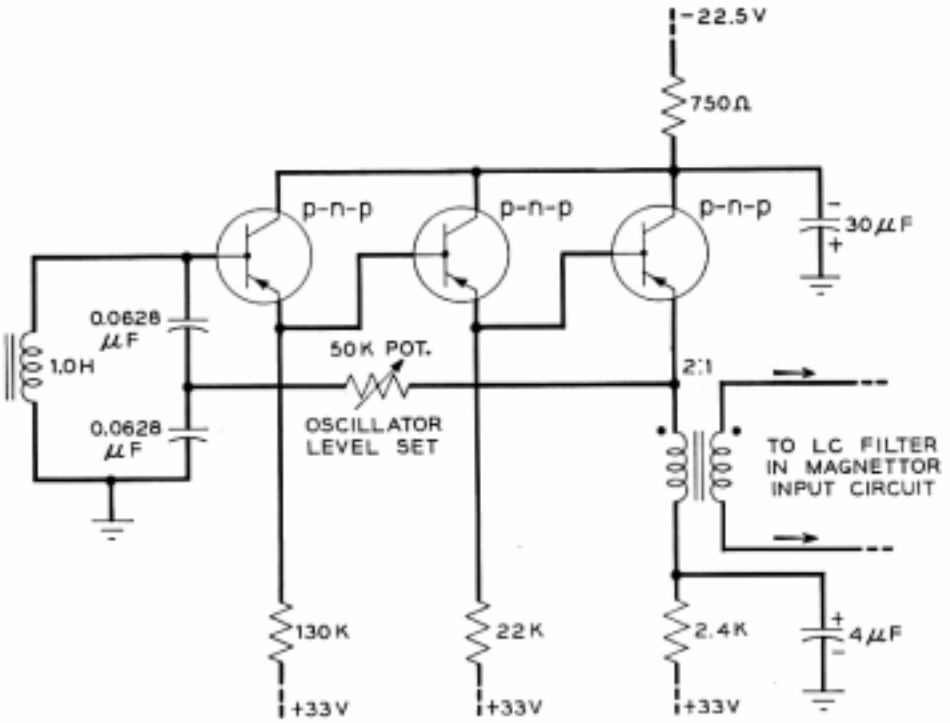


Fig. 17(b), 900-cycle carrier oscillator.

data displayed in Fig. 20 which gives the volt-ampere characteristics of a silicon diode measured at 20°C and 40°C. Throughout this temperature range, the diode voltage corresponding to the critical resistance of 30,000 ohms changes by about 30 millivolts. Fortunately, part of this voltage variation with temperature is compensated for by the variation in voltage V_{b-e} between the base and emitter of the junction transistor. From Fig. 18,

$$V_i = V_D - V_{b-e} + V_{ee} \tag{27}$$

For perfect compensation (V_i independent of temperature), V_{b-e} should have the same temperature variation as the diode voltage V_D . Experi-

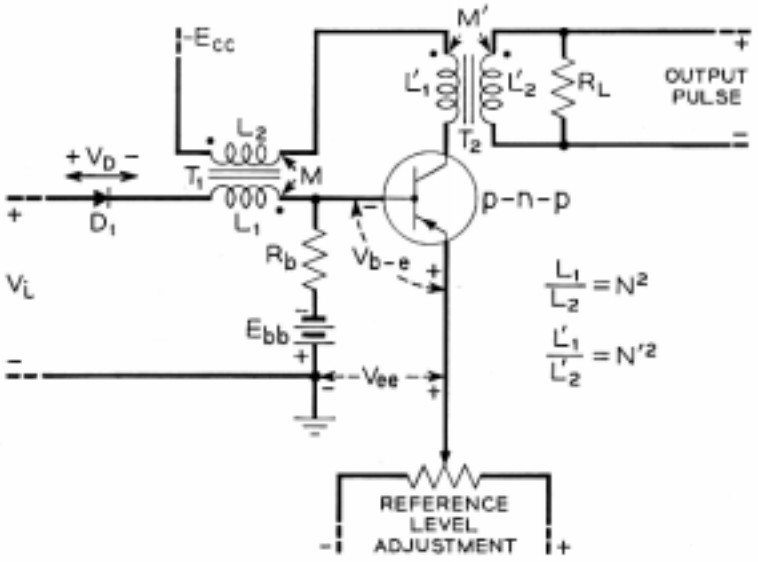


Fig. 18 — Simplified circuit diagram of voltage comparator.

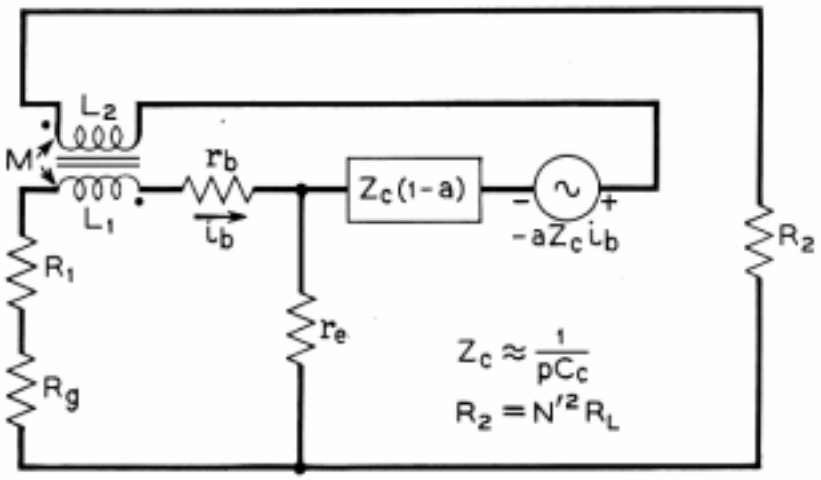


Fig. 19 — Equivalent circuit of voltage comparator.

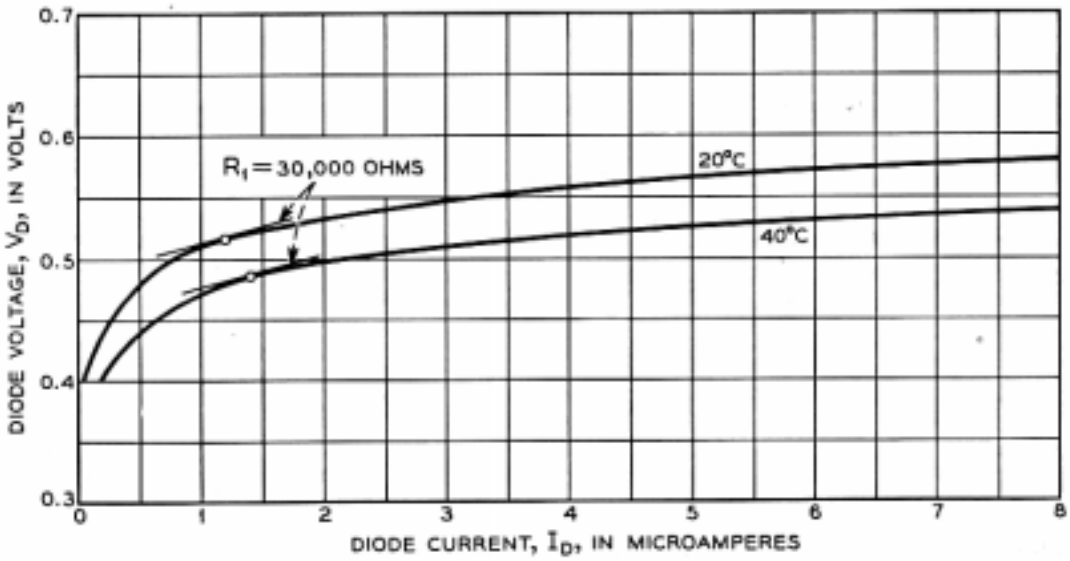


Fig. 20 — Volt-ampere characteristic of a silicon junction diode.

mentally it is found that V_{b-e} for germanium junction transistors varies by about 20 millivolts throughout the temperature range of 20°C to 40°C. Consequently, the variation in V_i at which the circuit switches is ± 5 millivolts.

It is apparent from Fig. 20 that the accuracy of the comparator increases slightly for critical values of R_1 greater than 30,000 ohms, but decreases for smaller values. For example, the accuracy of the comparator is ± 10 millivolts for a critical value of R_1 equal to 5,000 ohms. In general, the critical value of R_1 should be chosen between 5,000 and 100,000 ohms.

5.3. *A Practical Voltage Comparator*

Fig. 21 shows the complete circuit diagram of a voltage comparator. The circuit is designed to generate a sharp output pulse* when the input voltage waveform passes through the reference level (set by V_{ee}) with a positive slope. The pulse is generated by the transistor switching from the "on" state to the "off" state. To a first approximation the amplitude of the output pulse is proportional to the transistor collector current during the "on" state. When the input voltage waveform passes through the reference level with a negative slope an undesirable negative pulse is generated. This pulse is eliminated by the point contact diode D_2.

The voltage comparator is an unstable circuit and has the properties

* For the circuit values shown in Fig. 21, the output pulse has a peak amplitude of about 6 volts, a rise time of 0.5 microseconds, and a pulse width of about 2.0 microseconds.

of a free running blocking oscillator after the input voltage V_i passes through the reference level. After a period of time the transistor will return to the "on" state unless the voltage V_i is sufficiently large at this time to prevent switching. In order to minimize the required slope of the input waveform the time interval between the instant V_i passes through the reference level and the instant the transistor would naturally switch to the "on" state must be maximized. This time interval can be controlled by connecting a diode D_3 across the secondary winding of transformer T_1. When the transistor turns off, the current which was flowing through the secondary of transformer $T_1(I_c)$ continues to flow through the diode D_3 so that L_2 and D_3 form an inductive discharge circuit. The point contact diode D_3 has a forward dynamic resistance of less than 10 ohms and a forward voltage drop of 0.3 volt. If the small forward resistance of the diode is neglected, the time required for the current in the circuit to fall to zero is

$$T = \frac{I_c L_2}{0.3} \tag{28}$$

During the inductive transient, 0.3 volt is induced into the primary of transformer T_1 (since $N = 1$) maintaining the transistor cutoff. The duration of the inductive transient can be made as long as desired by increasing L_2. However, there is the practical limitation that increasing L_2 also increases the leakage inductance of transformer T_1, and in turn,

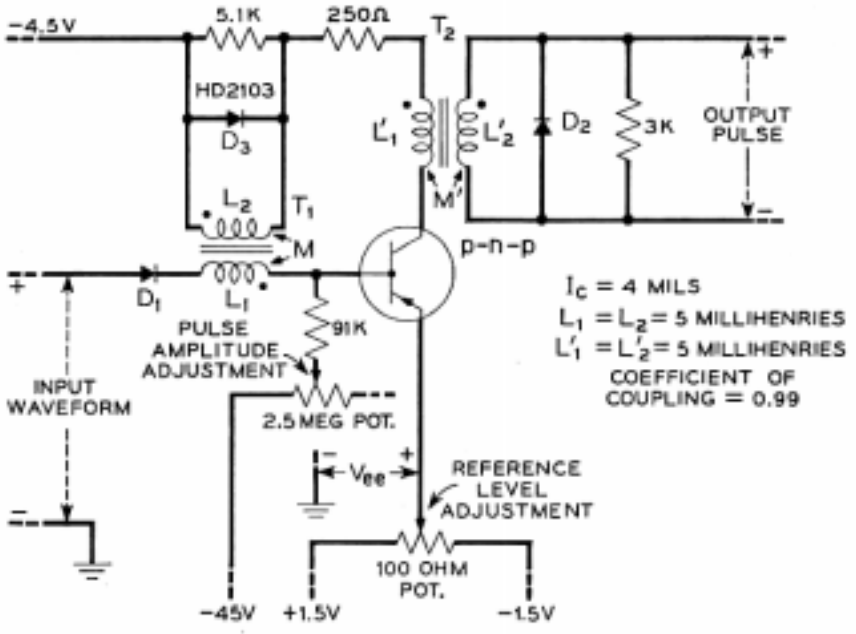


Fig. 21 — Voltage comparator.

increases the switching time. The circuit shown in Figure 21 does not misfire when used with voltage waveforms having slopes as small as 25 millivolts per microsecond, at the reference level.

6.0. A TRANSISTOR VOLTAGE ENCODER

6.1. *Circuit Arrangement*

The transistor circuits previously described can be assembled into a voltage encoder for translating analog voltages into equivalent time intervals. This encoder is especially useful for converting analog information (in the form of a dc potential) into the digital code for processing in a digital system. Fig. 22 shows a simplified block diagram of the encoder. The voltage ramp generated by the integrator is applied to amplitude selector number one and to one input of a summing amplifier. The amplitude selector is a dc amplifier which amplifies the voltage ramp in the vicinity of zero volts. Voltage comparator number one, which follows the amplitude selector, generates a sharp output pulse at the exact instant of time that the voltage ramp passes through zero volts.

The analog input voltage, which has a value between 0 and −15 volts,* is applied to the second input of the summing amplifier. The output voltage of the summing amplifier is zero whenever the ramp

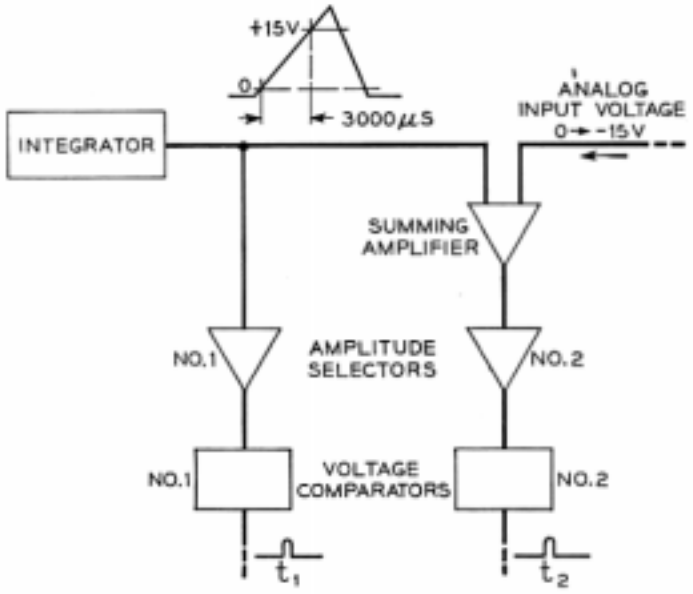


Fig. 22 — Simplified block diagram of voltage encoder.

* If the analog input voltage does not lie in this range, then the voltage gain of the summing amplifier must be set so that the analog voltage at the output of the summing amplifier lies in the voltage range between 0 and +15 volts.

voltage is equal to the negative of the input analog voltage. At this instant of time the second voltage comparator generates a sharp output pulse. The time interval between the two output pulses is proportional to the analog input voltage if the voltage ramp is linear and has a constant slope at all times.

6.2. *The Amplitude Selector*

The amplitude selector increases the slope of the input voltage waveform (in the vicinity of zero volts) sufficiently for proper operation of the voltage comparator. The amplitude selector consists of a limiter and a dc feedback amplifier as shown in Fig. 23. The two oppositely poled silicon diodes D_1 and D_2, limit the input voltage of the dc amplifier to about ± 0.65 volts. The dc amplifier has a voltage gain of thirty, and so the maximum output voltage of the amplitude selector is limited to about ± 19.5 volts. The net voltage gain between the input and output of the amplitude selector is ten.

The principal requirement placed on the dc amplifier is that the input current and the output voltage be zero when the input voltage is zero. This is accomplished by placing a blocking condenser C_B between point T and the base of the first transistor stage, and by using an AZS circuit to maintain point T at zero volts. The dc and AZS amplifiers are identical in configuration to the amplifiers shown in Fig. 12. The dc amplifier is

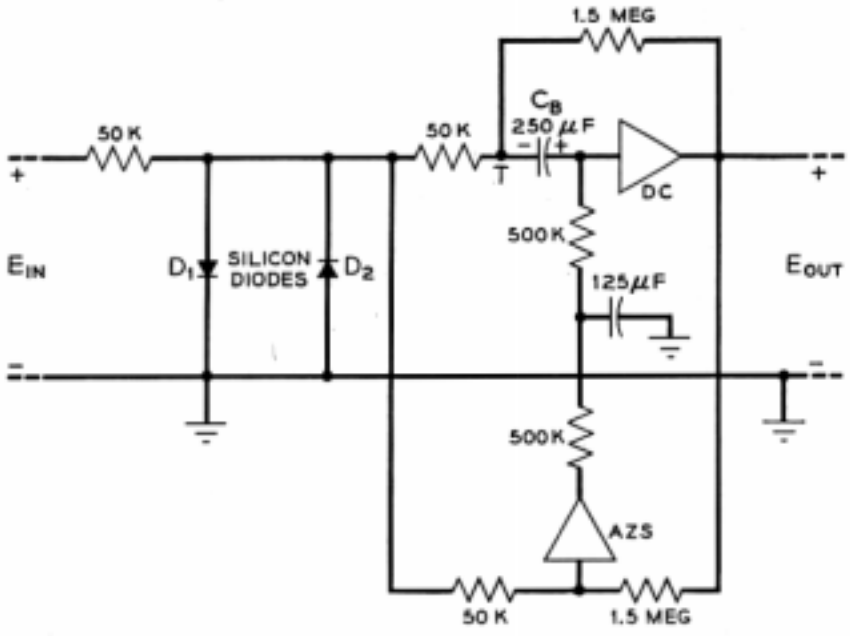


Fig. 23 — Block diagram of the amplitude selector.

designed to have about 15.6 db less feedback than that shown in Fig. 10 since this amount is adequate for the present purpose.

The bandwidth of the dc amplifier is only of secondary importance because the phase shifts introduced by the two amplitude selectors in the voltage encoder tend to compensate each other.

6.3. *Experimental Results*

The accuracy of the voltage encoder is determined by applying a precisely measured voltage to the input of the summing amplifier and by measuring the time interval between the two output pulses. The maximum error due to nonlinearities in the summing amplifier and the voltage ramp is less than ± 0.5 microseconds for a maximum encoding time of 3,000 microseconds. An additional error is introduced by the noise voltage generated in the first transistor stage of the summing amplifier. The RMS noise voltage at the output of the summing amplifier is less than 0.5 millivolts. This noise voltage produces an RMS jitter of 0.25 microseconds in the position of the second voltage comparator output pulse. The over-all accuracy of the voltage encoder is one part in 4,000 throughout a temperature range of 20°C to 40°C.

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Appendix I

RELATIONSHIP BETWEEN RETURN DIFFERENCE AND LOOP CURRENT TRANSMISSION

In order to place the stability analysis of the transistor feedback amplifier on a sound basis, it is desirable to use the concept of return difference.[8] It will be shown that a measurable quantity, called the loop current transmission, can be related to the return difference of aZ_e with reference r_e.*, † In Fig. 24, N represents the complete transistor network exclusive of the transistor under consideration. The feedback loop is broken at the input to the transistor by connecting all of the feedback paths to

* In this appendix it is assumed that the transistor under consideration is in the common emitter connection. The discussion can be readily extended to the other transistor connections.

† This fact was pointed out by F. H. Tendick, Jr.

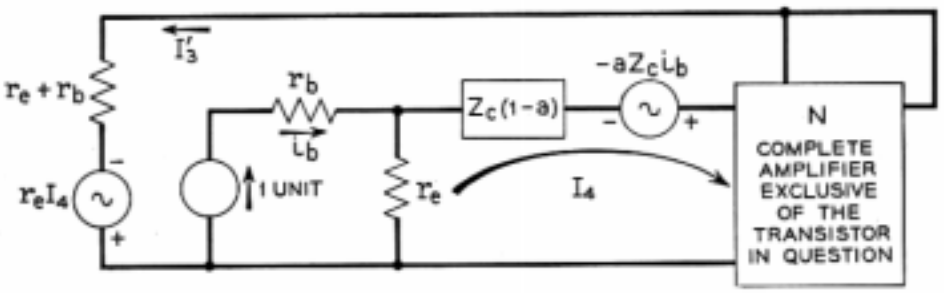

Fig. 24 — Measurement of loop current transmission.

ground through a resistance $(r_e + r_b)$ and a voltage $r_e I_4$. Using the nomenclature given in Reference 8, the input of the complete circuit is designated as the first mesh and the output of the complete circuit is designated as the second mesh. The input and output meshes of the transistor under consideration are designated 3 and 4, respectively. The loop current transmission is equal to I_3', the total returned current when a unit input current is applied to the base of the transistor.

The return difference for reference r_e is equal to the algebraic difference* between the unit input current and the returned current I_3'. I_3' is evaluated by multiplying the open circuit voltage in mesh 4 (produced by the unit base current) by the backward transmission from mesh 4 to mesh 3 with zero forward transmission through the transistor under consideration. The open circuit voltage in mesh 4 is equal to $(r_e - aZ_c)$. The backward transmission is determined with the element aZ_c, in the fourth row, third column of the circuit determinant, set equal to r_e. Hence, the return difference is expressed as

$$F_{r'_e} = 1 + (aZ_c - r_e)\frac{\Delta_{43}}{\Delta^{r'_e}} \qquad \text{(A1)}\dagger$$

$$F_{r'_e} = \frac{\Delta^{r'_e} + (aZ_c - r_e)\Delta_{43}}{\Delta^{r'_e}} \qquad \text{(A2)}$$

$$F_{r'_e} = \frac{\Delta}{\Delta^{r'_e}} = 1 + T_{r'_e} \qquad \text{(A3)}$$

The relative return ratio $T_{r'_e}$ is equal to the negative of the loop current transmission and can be measured as shown in Fig. 24. The voltage $r_e I_4$ takes into account the fact that the junction transistor is not perfectly

* The positive direction for the returned current is chosen so that if the original circuit is restored, the returned current flows in the same direction as the input current.

† $\Delta^{r'_e}$ is the network determinant with the element aZ_c in the fourth row, third column of the circuit determinant set equal to r_e.

unilateral. Fortunately, in many applications, this voltage can be neglected even at the gain and phase crossover frequencies.

In the case of single loop feedback amplifiers, $\Delta^{r'_e}$ will not have any zeros in the right hand half of the complex frequency plane. A study of the stability of the amplifier can then be based on $F_{r'_e}$ or $T_{r'_e}$.

Appendix II

Interstage Network Shaping

This appendix presents the analysis of the circuit shown in Fig. 7(a). The input impedance of the common emitter connected junction transistor is given by the expression

$$Z_{\text{INPUT}} = r_b + r_e(1 - G_I) \tag{A4}$$

where G_I is the current transmission of the common emitter stage, expression (13). The current transmission A of the complete circuit is equal to

$$A = \frac{I_2}{I_1} = \frac{Z_3}{Z_3 + Z_{\text{INPUT}}} \cdot G_I \tag{A5}$$

where $Z_3 = R_3 + pL_3 + (1/pC_3)$. Combining (13), (A4), and (A5) yields

$$A = \frac{-\dfrac{a_0}{1 - a_0 + \delta}\left[\left(1 + \dfrac{p}{\omega_3}\right)^2 + p\left(R_3C_3 - \dfrac{2}{\omega_3}\right)\right]}{\left(1 + \dfrac{p}{\omega_5}\right)\left\{1 + p\,\dfrac{C_3\omega_5}{\omega_1}(r_b + r_e + R_3 + \omega_1 L_3) + p^2\left[\dfrac{\omega_5}{\omega_1\omega_3^2} + \dfrac{C_3\omega_5(r_b + r_e + R_3)}{\omega_a\omega_c(1 - a_0 + \delta)}\right] + \dfrac{p^3\omega_5}{\omega_3^2\omega_a\omega_c(1 - a_0 + \delta)}\right\}} \tag{A6}$$

where

$$\delta = \frac{R_L + r_e}{r_c}$$

$$\omega_1 = \frac{(1 - a_0 + \delta)}{\dfrac{1 + \delta}{\omega_a} + \dfrac{1}{\omega_c}}$$

$$\omega_c = \frac{1}{(R_L + r_e)C_c}$$

$$\omega_3 = \frac{1}{\sqrt{L_3C_3}}$$

$$\omega_5 = \frac{1}{\left[r_b + \dfrac{r_e}{(1 - a_0 + \delta)}\right]C_3}$$

Expression (A6) is valid if $1/\omega_3 \gg 1/\omega_1 + R_3C_3$. The denominator of the expression indicates a falling 6 db per octave asymptote with a corner frequency at ω_3 . The second factor in the denominator can be approximated by a falling 6 db per octave asymptote with a corner frequency at

$$\frac{\omega_1\left[r_b + \dfrac{r_e}{(1 - a_0 + \delta)}\right]}{r_b + r_c + R_3 + \omega_1 L_3}$$

plus additional phase and amplitude contributions at higher frequencies due to the p^2 and p^3 terms. If

$$\frac{1}{\omega_3 C_3 R_3} = \tfrac{1}{2}$$

then the circuit has a rising 12 db per octave asymptote with a corner frequency at ω_3 . Fig. 7(b) shows the amplitude and phase of the current transmission.

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