Sun 501-1206 CPU Board

Configuration Procedures

Credits and Trademarks

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WARNING

There is a Lithium Battery (BBCV2), Matsushita Electric Type No. BR2325, located on the Sun 501-1163 or 501-1164 CPU Board. This battery is NOT a field replaceable part. The battery is marked as follows: "Warning— Replace battery with MATSUSHITA ELECTRIC or PANASONIC Part No. BR2325 only.

The battery may explode if mistreated. Do not dispose of the battery in fire. Do not disassemble it or recharge it.

General Description	The Sun 501-1206 CPU board is the heart of the Sun-3/260 workstation and the Sun-3/280 file server.

NOTE   *Early versions of the board carry Sun P/N 501-1100. This document supports both versions of the board.*

The board features:

- An MC68020 CPU, operating at 25 Mhz
- An MC68881 Floating Point Coprocessor, operating at 20 Mhz
- On-board, 64 Kbyte Sun-3 Virtual Address Cache for instructions and data
- Zero wait state reads and writes from the cache
- DVMA access through the cache for data consistency and speed
- Cache operation that is transparent to application programs
- 256 Kbytes dual-ported video RAM and logic to support a monochrome monitor with 1600 x 1280 resolution
- A 64-bit, multiplexed address/data bus that supports the ECC Memory and the Floating Point Accelerator Board
- Interface circuitry that supports the VMEbus, Ethernet, two serial ports, as well as the keyboard and mouse

The 501-1206 board must be paired with at least one 501-1102 Memory Board to provide 8 Megabytes of Error Checking and Correction (ECC) main memory.

The Sun-3 Cache Memory stores the most recently accessed data in a high speed buffer so that it will be very quickly available if accessed again in a short period of time.

Configuration Jumpers

The tables on the following pages show the factory configuration of jumper-blocks on two versions of the board, and list coordinates that aid in locating them. Table 1 supports the 501-1100 version of the board and Table 2 supports the 501-1206 version of the board. The "bare-board" equivalent of these part numbers is marked on the boards: The 501- prefix becomes 270-, so that a 501-1206 board is marked 270-1206.

Figures 1 and 2 depict the sections of the board where jumper-blocks are located. The 501-1206 layout supports both versions of the board due to the fact that all jumper-blocks are at the same locations on both boards with the exception of J300, which is present only on the 501-1100 board. Tables 1 and 2 show differences in jumper installation and function.

The board has grid markings that form an X-Y coordinate system. Letters of the alphabet define the X coordinate and numbers define the Y coordinate of the grid. For example, the location "A-16" on the following table indicates that jumper-block J2401 is located at the intersection of coordinates "A" and "16".

The *Configuration* column on the table indicates whether or not the board is shipped with the referenced jumper installed on the indicated pins. "1-2" in that column means that the jumper is installed across pins 1 and 2. "IN" means that the board is shipped with the jumper installed. "OUT" means that the jumper is not installed at the factory. The illustrations that follow show the orientation of the jumpers.

Pin 1 of each jumper-block is to the left of the v-shaped mark on the board, as it is on IC packages. If the reference designator or the "v" mark is not readily visible on the component side of the board, look on the other side of the board for the same information.

The *Description* heading describes the function of a jumper when installed in the indicated position.

Table 1   *Factory Configuration of Jumpers on the 501-1100 CPU Board*

Jumper	Location	Configuration	Description
J2401	A-16	1-2, IN	Enable Ethernet Clock
J2401	A-16	3-4, OUT	+5V to Ethernet Tap
J2401	A-16	5-6, OUT †	For Level 2 Ethernet
J2401	A-16	7-8, OUT	Null
J2000	H-1	1-2, IN	Select 27512 Boot PROM
J2000	H-1	3-4, OUT	Select 27256 Boot PROM
J300	H-2	1-2, IN	"P2" Bus Enable
J500	H-3/4	1-2, IN	VME Interrupt Level 1
J500	H-3/4	3-4, IN	VME Interrupt Level 2
J500	H-3/4	5-6, IN	VME Interrupt Level 3
J500	H-3/4	7-8, IN	VME Interrupt Level 4
J500	H-3/4	9-10, IN	VME Interrupt Level 5
J500	H-3/4	11-12, IN	VME Interrupt Level 6
J500	H-3/4	13-14, IN	VME Interrupt Level 7
J500	H-3/4	15-16, OUT	Null
J100	H-5	1-2, OUT	68020 Cache Disable
J200	H-6	1-2, OUT	Null
J200	H-6	3-4, IN	25 Mhz CPU Enable
J200	H-6	5-6, OUT‡	Select 25 Mhz 68881 Clock
J200	H-6	7-8, IN	Select 20 Mhz 68881 Clock
J2500	L-11	1-2, IN	CPU is VME Arbiter & Requester
J2500	L-11	3-4, OUT	CPU is VME Requester Only
J2500	L-11	5-6, OUT	CPU is VME Reset Slave
J2500	L-11	7-8, IN	CPU is VME Reset Master
J2600	L-9	1-2, IN	Enable VME Clock

† This jumper is IN for Level 1 Ethernet
‡ The FPC is not designed to operate at 25 Mhz

Table 2   *Factory Configuration of Jumpers on the 501-1206 CPU Board*

Jumper	*Location*	*Configuration*	*Description*
J2401	A-16	1-2, IN	Enable Ethernet Clock
J2401	A-16	3-4, OUT	+5V to Ethernet Tap
J2401	A-16	5-6, OUT †	For Level 2 Ethernet
J2401	A-16	7-8, IN	UART Clock Enable
J2000	H-1	1-2, IN	Select 27512 Boot PROM
J2000	H-1	3-4, OUT	Select 27256 Boot PROM
J500	H-3/4	1-2, IN	VME Interrupt Level 1
J500	H-3/4	3-4, IN	VME Interrupt Level 2
J500	H-3/4	5-6, IN	VME Interrupt Level 3
J500	H-3/4	7-8, IN	VME Interrupt Level 4
J500	H-3/4	9-10, IN	VME Interrupt Level 5
J500	H-3/4	11-12, IN	VME Interrupt Level 6
J500	H-3/4	13-14, IN	VME Interrupt Level 7
J500	H-3/4	15-16, OUT	Null
J100	H-5	1-2, OUT	68020 Cache Disable
J200	H-6	1-2, OUT	Null
J200	H-6	3-4, IN	25 Mhz CPU Enable
J200	H-6	5-6, OUT‡	Select 25 Mhz 68881 Clock
J200	H-6	7-8, IN	Select 20 Mhz 68881 Clock
J2500	L-11	1-2, IN	CPU is VME Arbiter & Requester
J2500	L-11	3-4, OUT	CPU is VME Requester Only
J2500	L-11	5-6, OUT	CPU is VME Reset Slave
J2500	L-11	7-8, IN	CPU is VME Reset Master
J2600	L-9	1-2, IN	Enable VME Clock

† This jumper is IN for Level 1 Ethernet
‡ The FPC is not designed to operate at 25 Mhz

Figure 1   *A-E Section of the Board*

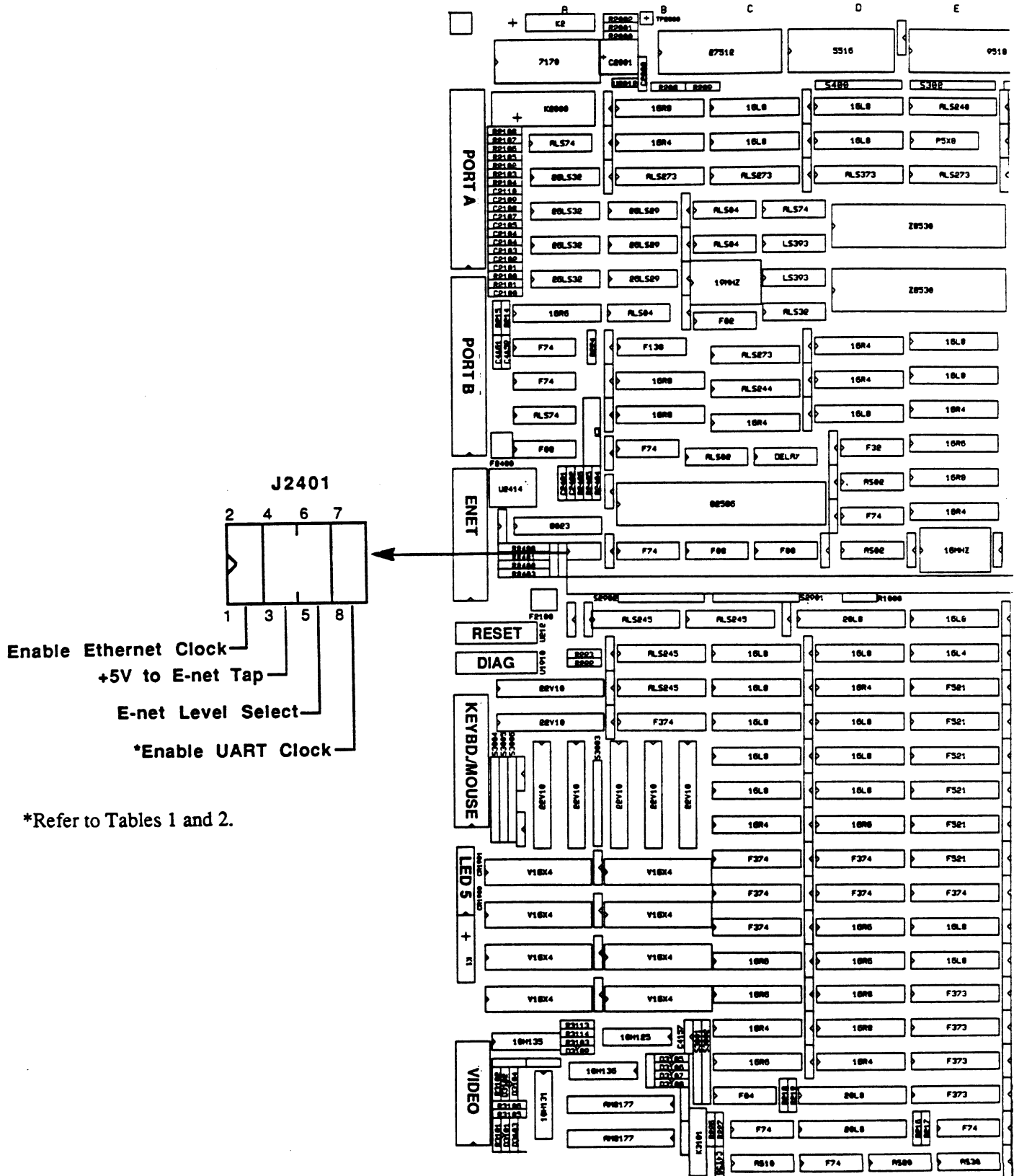This illustration applies to both the 501-1100 and the 501-1206 CPU board.

J2401

Enable Ethernet Clock
+5V to E-net Tap
E-net Level Select
*Enable UART Clock

*Refer to Tables 1 and 2.

Figure 2 _G-L Section of the Board_

This illustration applies to both the 501-1100 and the 501-1206 CPU board.

Select 27256 Boot PROM
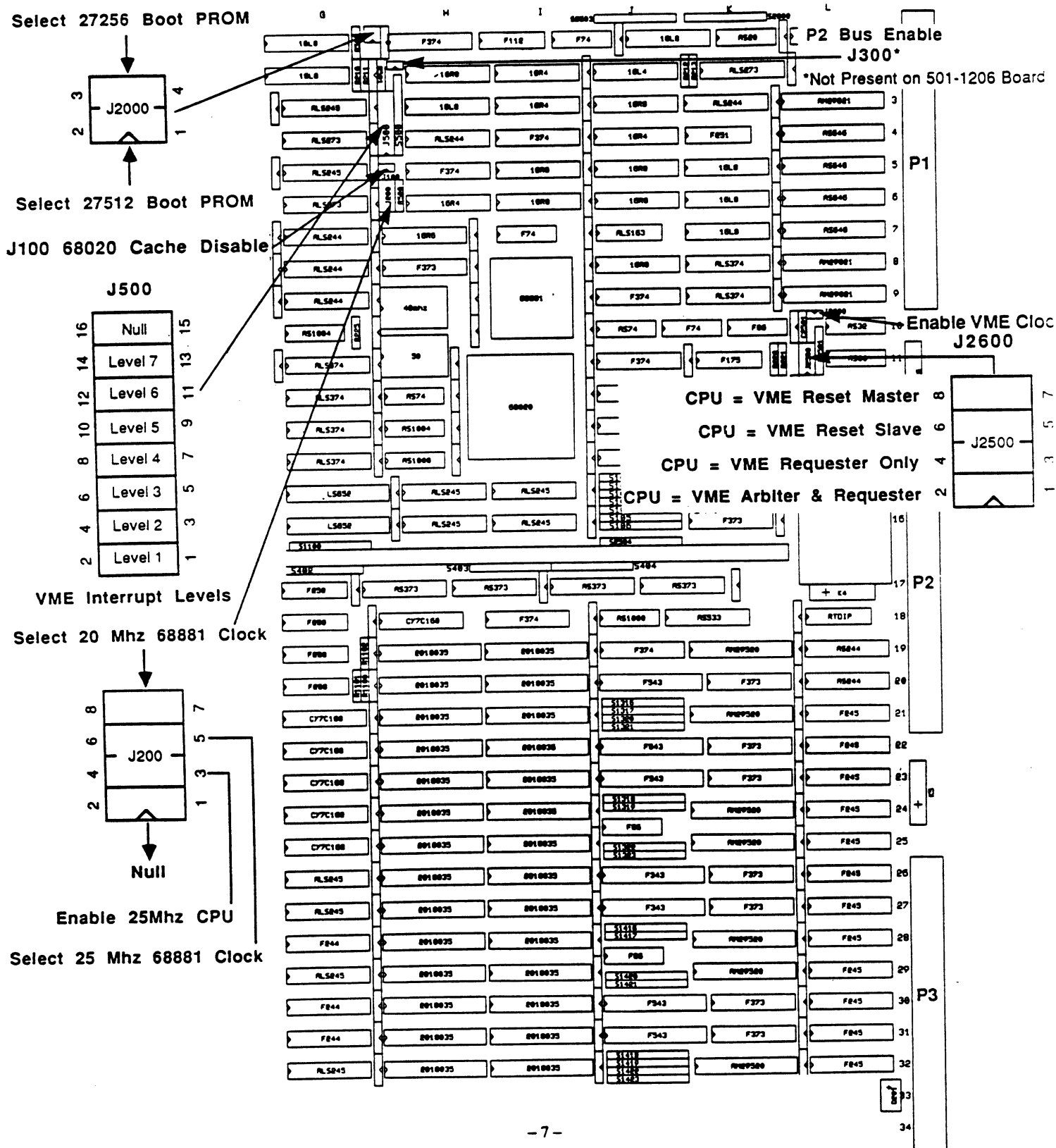
J2000

Select 27512 Boot PROM

J100 68020 Cache Disable

J500

16	Null	15
14	Level 7	13
12	Level 6	11
10	Level 5	9
8	Level 4	7
6	Level 3	5
4	Level 2	3
2	Level 1	1

VME Interrupt Levels

Select 20 Mhz 68881 Clock

J200

Null

Enable 25Mhz CPU

Select 25 Mhz 68881 Clock

P2 Bus Enable
J300*
*Not Present on 501-1206 Board

P1

Enable VME Cloc
J2600

CPU = VME Reset Master 8
CPU = VME Reset Slave 6
CPU = VME Requester Only 4
CPU = VME Arbiter & Requester 2

J2500

P2

P3

Table 3   *Revision History*

Revision	Date	Comments
Review Draft	30 June 1986	First Draft of this Configuration Procedure.
50	21 July 1986	Engineering Release of this Configuration Procedure.
05-A	10 October 1986	Production Release of this Configuration Procedure; reflects conversion of 501-1100-05 board to 501-1206.