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Xylogics 450/451 SMD Controller Board
Configuration Procedures

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Xylogics 450/451 SMD Controller
General Description

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The Xylogics 450/451 SMD Controller manages the operation of a maximum of two disk drives with a DMA transfer rate of 3.0 megabytes per second. Disk transfer rates of up to 1.8 megabytes per second (for the 450 controller board) and 2.4 megabytes per second (for the 451 controller board), overlapped seeks and multiple drive types are supported by this controller. Four drives may be operated with the addition of a second controller. The first controller is configured as xy0 and the second as xy1.

The illustrations below show board layouts and shunt pin locations for three fabrication levels of the 450 board and one fabrication of the 451 board.
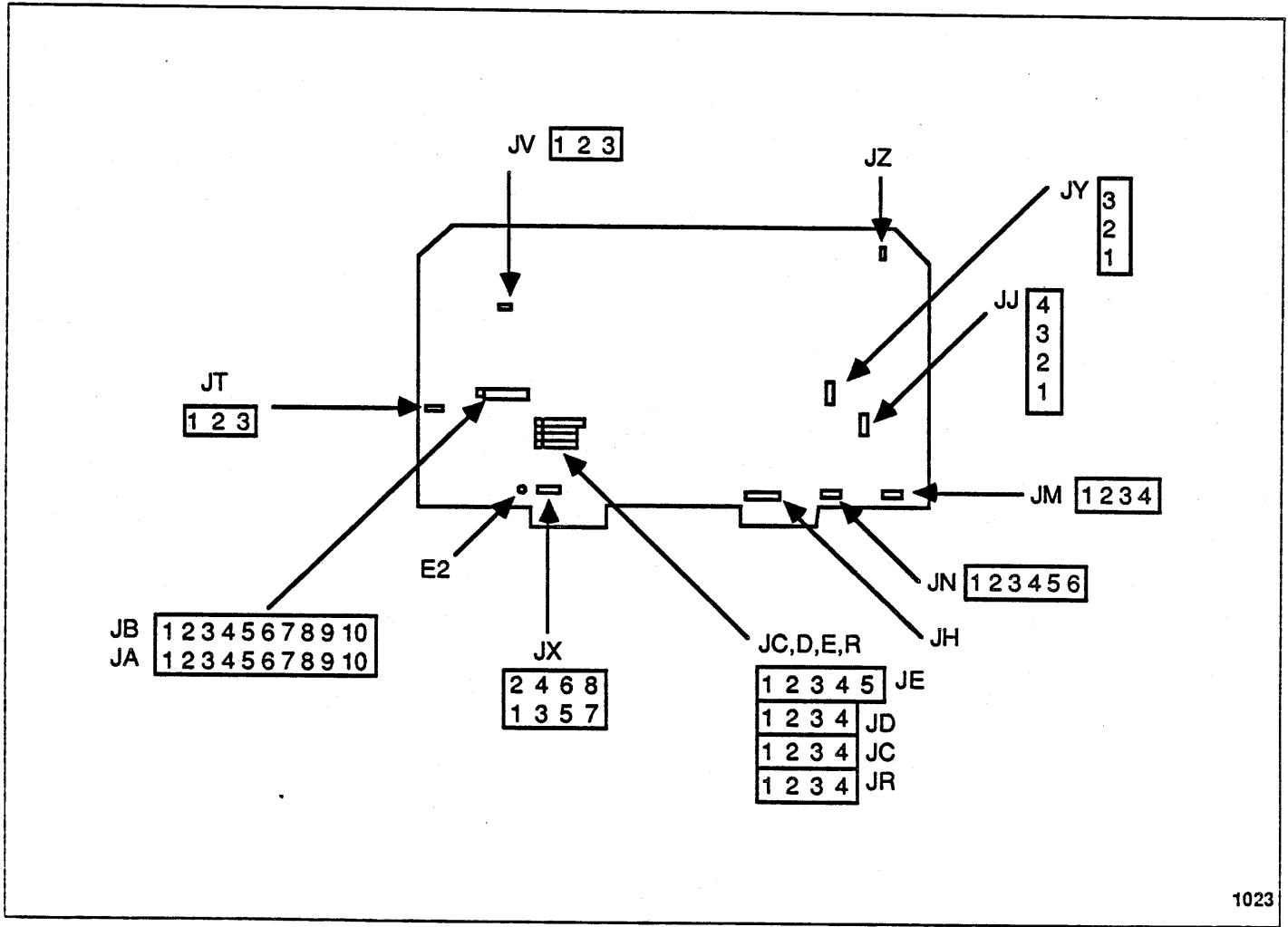
Figure 1-1   *Xylogics 450 — Fabrication C, Assembly Revisions J,K*
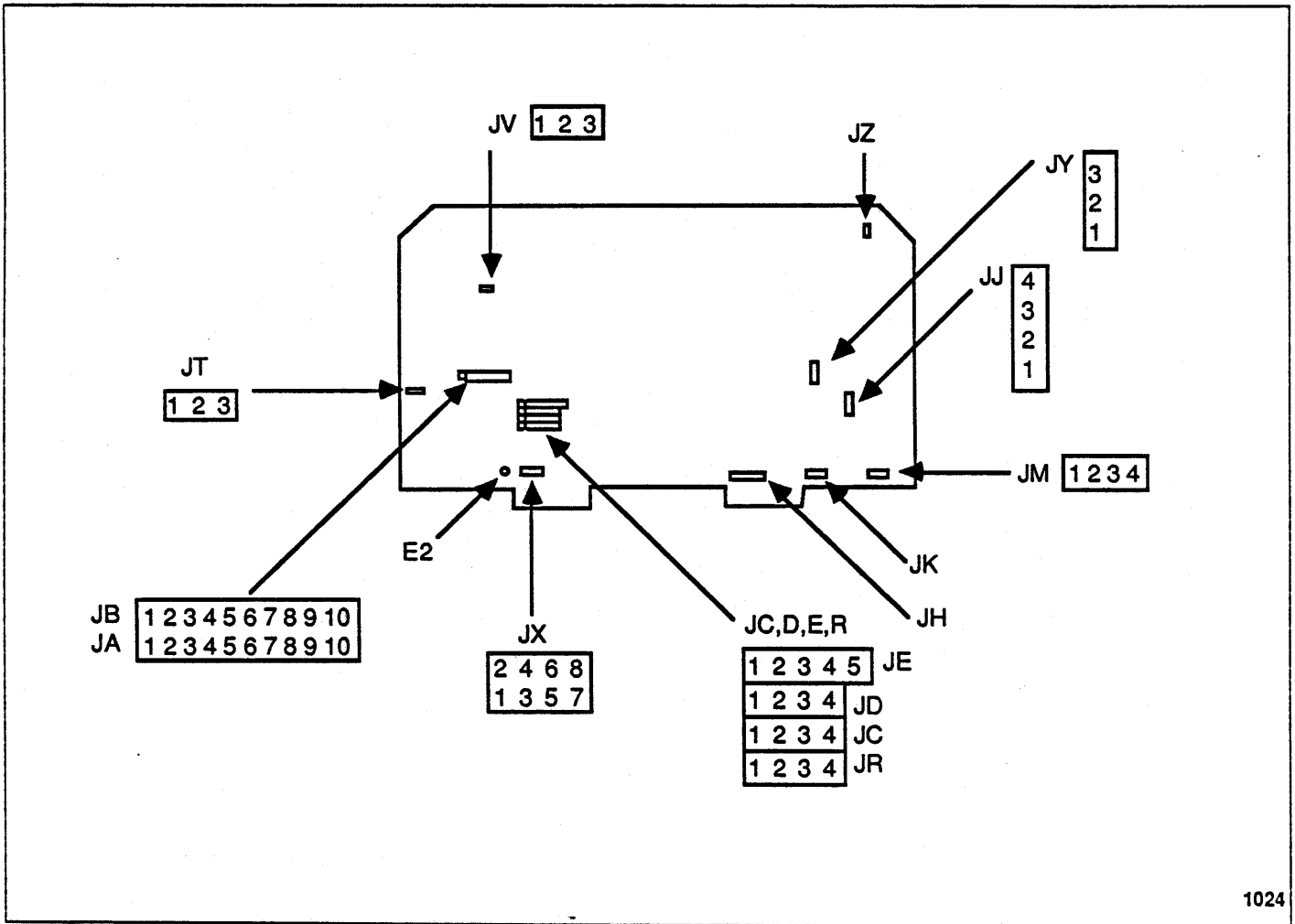
Figure 1-2   *Xylogics 450 — Fabrication D, Assembly Revisions K,L,M*
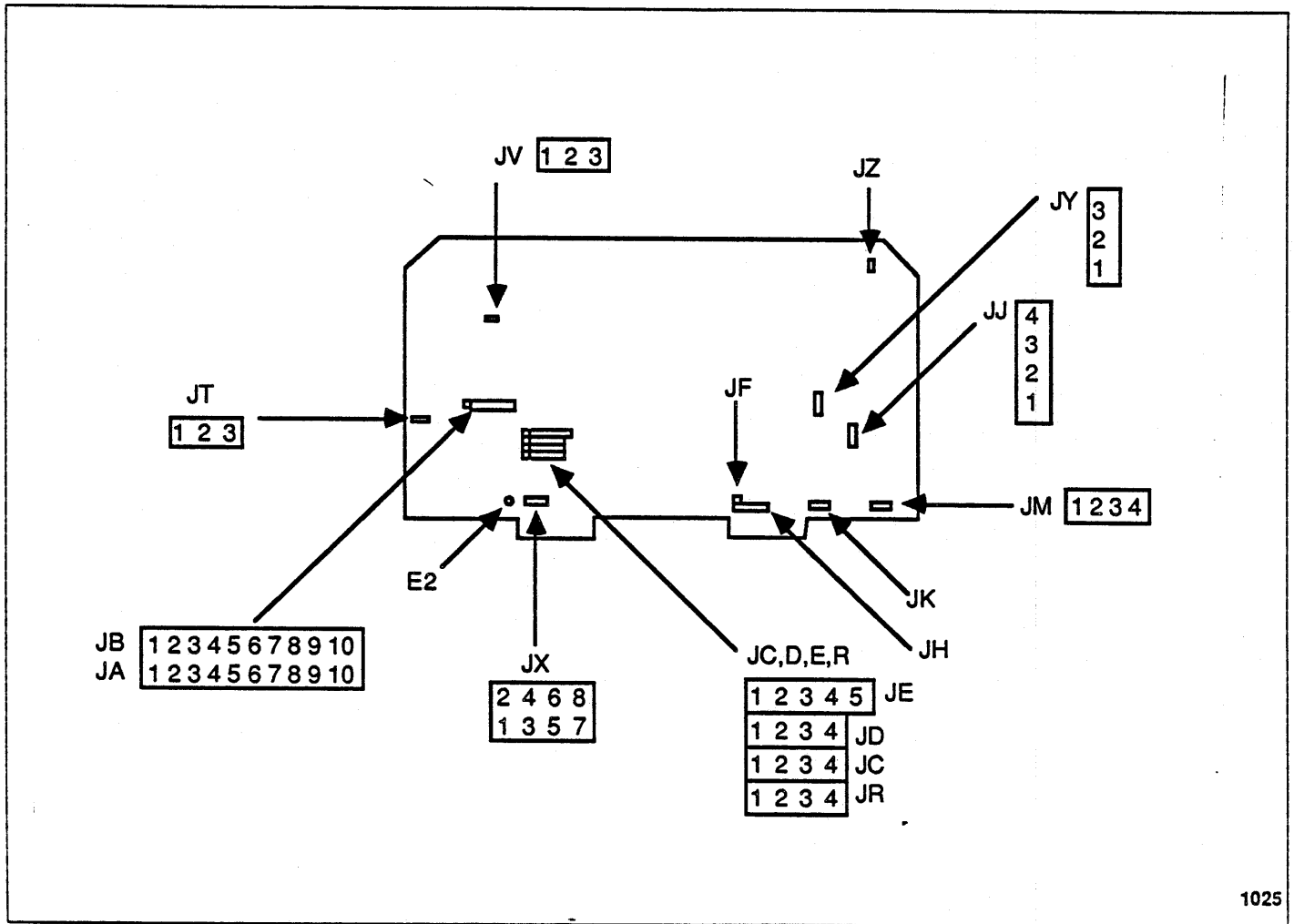
Figure 1-3   *Xylogics 450 — Fabrication E, Assembly Revision N*
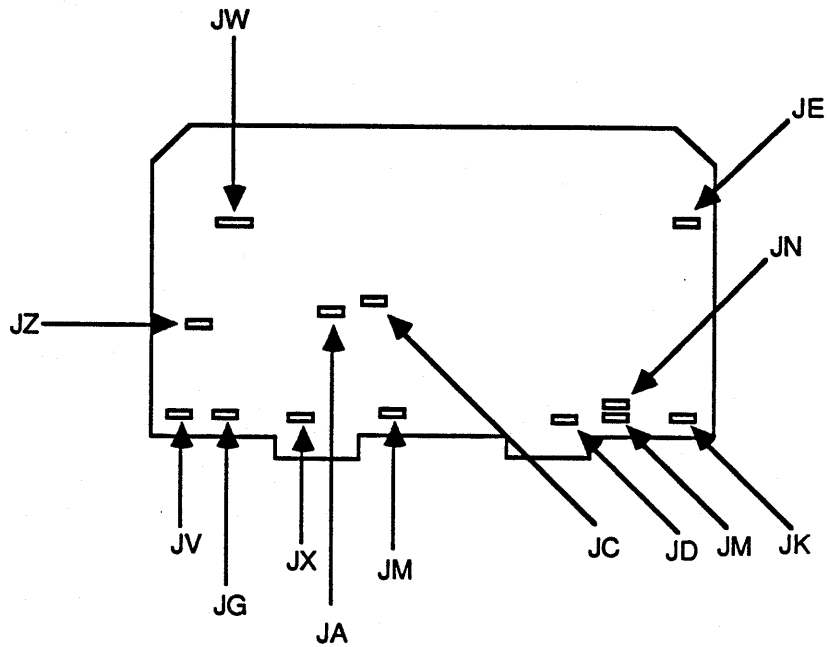
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Figure 1-4   *Xylogics 451 SMD Controller Board*

If the Xylogics 450/451 is being installed in a VMEbus system, refer to the VME-to-Multibus Adapter Board General Description which follows.

NOTE   *Xylogics 450 Controller boards earlier than Fabrication level C, Assembly Revision J are not guarenteed to be compatible with Sun products. These boards should be exchanged for units having the correct Fab and Revision levels.*

Table 1-1   *Configuration for the Xylogics 450 SMD Controller*

Label	Pins	Description	In or Out
JV	1-2	Optional 8KB	IN
	3		OUT
JT	1-2	Optional 8KB	IN
	3		OUT
JF-JH*	1-1	see note	
JH*	1-2	see note	
JH	3-4	Inhibits DMA Sequencer CLK	OUT
	5-6	Selects DMA Sequencer CLK	IN
JM*		see note	
JJ	1-2	Select Disk Squencer CLK	OUT
	3-4		IN
JY	1	Close ECC Feedback	OUT
	2-3		IN
JX		Interupt Request Level (connect wire from E2 to 1 of 8 pins)	
	E2-2	INT0-no connection	
	E2-7	INT1-no connection	
	E2-4	INT2-connection	
	E2-5	INT3-no connection	
	E2-8	INT4-no connection	
	E2-3	INT5-no connection	
	E2-6	INT6-no connection	
	E2-1	INT7-no connection	
JA-JB (pin 1 at left)	1-1	16 or 8 Bit Address Cntrl	OUT
	2-2	Address Bit F	OUT
	3-3	Address Bit 8	IN
	4-4	Address Bit E	OUT
	5-5	Address Bit 9	OUT
	6-6	Address Bit D	OUT
	7-7	Address Bit A	OUT
	8-8	Address Bit C	IN
	9-9	Address Bit B	OUT
	10-10	Ground	OUT
JE	1-2	DMA Arbitration	**
	4-5	Address bit 7 hex	IN
JC-JR#		Address bits	
JD-JC#		Address bits	

Table 1-1   *Configuration for the Xylogics 450 SMD Controller — Continued*

Label	Pins	Description	In or Out
		see note	
JZ	1-2	Crystal Shunt	IN
JK*		see note	
JN		Refer to Fab Level Tables	

NOTES

*   The configuration of JF, JH, JK and JM varies with the fabrication level of the board. Refer to the table with the fabrication level of your board for the neccessary configuration information.

**   For Sun 100's: 1-2 should be IN and 3 should be OUT (selects serial DMA). For Sun-2/120's, /150's, /170's and all VMEbus machines: 1-2 and 3 should be OUT (selects parallel DMA).

These configuration jumpers are set dependent upon the address of the board. Refer to the table labelled *Controller Board Addresses* for the required information.

Table 1-2   *Configuration for Fabrication Level C Boards*

Label	20-bit Oper Multibus	24-bit Oper VMEbus*	Description
JM	1-2, OUT 3-4, IN	1-2, IN 3-4, OUT	Select 24-bit Select 20-bit
JK	N-A N-A	N-A N-A	
JN	1-2, OUT	N-A	Disable Remote Act Ind

*   Boards at this fabrication level support 20-bit operation for Multibus and 24-bit operation for VMEbus systems. Note however, that the upper four address bits can not be disconnected from the Multibus' P2 connector. For this reason, Fabrication level C boards must not be installed in slots 1-6 of Multibus systems, where the P2 connector signals are bussed to other slots.

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Table 1-3   *Configuration for Fabrication Level D and E Boards*

Label	20-bit Oper Multibus	24-bit Oper VMEbus	Description
JM	1-2, OUT 3-4, IN 5-6, OUT	1-2, IN 3-4, OUT 5-6, IN	Select 24-bit Select 20-bit Connect ADR0x14
JK JK JK JK	1-2, OUT 3-4, OUT 5-6, OUT 7-8, OUT	1-2, IN 3-4, IN 5-6, IN 7-8, OUT	Connect ADR0x16 Connect ADR0x17 Connect ADR0x15 Disable Act Ind
JN	N-A	N-A	Disable Remote Act Ind

Table 1-4   *Configuration for Fabrication Level C and D Boards*

Label	Pins	Description	In or Out
JH	1-2	AC Power-down Protection	OUT*

*   AC Power-down protection is automatically selected if the pin 1-2 shunt is out.

Table 1-5   *Configuration for Fabrication Level E Boards*

Label	Pins	Description	In or Out
JF-JH JH	1-1 1-2	DC Power-down Protection AC Power-down Protection	IN OUT

Table 1-6   *Controller Board Addresses*

Label	Pins	Description	In or Out
JC-JR JD-JC	1-1 2-2 3-3 4-4	xy0 Addr:EE40 Address bit 6 hex Address bit 5 hex Address bit 4 hex Address bit 3 hex	IN IN IN IN
JC-JR	1-1 4-4	xy1 Addr: EE48 Address bit 6 hex Address bit 3 hex	IN IN

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Table 1-6   *Controller Board Addresses— Continued*

Label	Pins	Description	In or Out
JD-JC	2-2 3-3	Address bit 5 hex Address bit 4 hex	IN IN

Table 1-7   *Address Shunt Assignment Table xy0 = ee40*

Label	Pin 1	Pin 2	Pin 3	Pin 4
JD		x	x	x
JC	x	x	x	x
JR	x			

Table 1-8   *Address Shunt Assignment Table xy1 = ee48*

Label	Pin 1	Pin 2	Pin 3	Pin 4
JD		x	x	
JC	x	x	x	x
JR	x			x

Table 1-9   *Configuration for the Xylogics 451 SMD Controller*

| Label	Configuration	Description
JC	OUT	Enables 16-bit addressing mode (for all products)
JA	 1-2, IN 3-4, IN 5-6, IN 7-8, OUT 9-10, IN 11-12, IN 13-14, IN 15-16, OUT 17-18, OUT 19-20, IN 21-22, OUT 23-24, OUT	Base address setting (ee40) ADR0xF ADR0xE ADR0xD ADR0xC ADR0xB ADR0xA ADR0x9 ADR0x8 ADR0x7 ADR0x6 ADR0x5 ADR0x4

Table 1-9   *Configuration for the Xylogics 451 SMD Controller— Continued*

Label	Configuration	Description
	25-26, OUT	ADR0x3*
JM	see description	1-2, IN 16-24 Mode (for VMEbus) 2-3, IN 16-20 Mode (for Multibus)
JK	ALL IN (for VMEbus) ALL OUT (for Multibus)	24-bit address jumpers ADR0x17 - ADR0x14
JX		Interrupt Request level
	1-2, OUT	INT0
	3-4, OUT	INT1
	5-6, IN	INT2
	7-8, OUT	INT3
	9-10, OUT	INT4
	11-12, OUT	INT5
	13-14, OUT	INT6
	15-16, OUT	INT7
JY		Bus arbitration (BPRO)
	1-2,OUT	
JH	1-2, IN	AC Power-down protection
JZ	2-3, IN	Common bus request disabled
JN	OUT	Activity indicator
JD	1-2,3-4, OUT	Local −5 VDC regulator disabled
JE	1-2,3-4, OUT	−5 VDC from backplane
JG	1-2,3-4, IN	
JW	1-2, IN	BUSY not synchronized to bus clock

* IN for address ee48 (xy1), OUT for address ee40 (xy0).

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VME to Multibus Adapter Board General Description
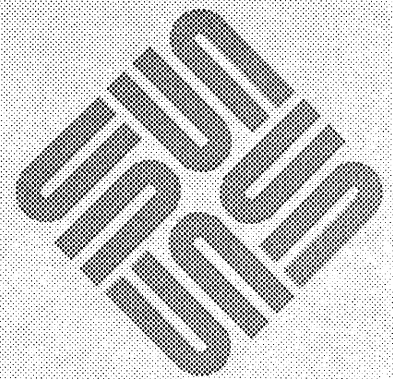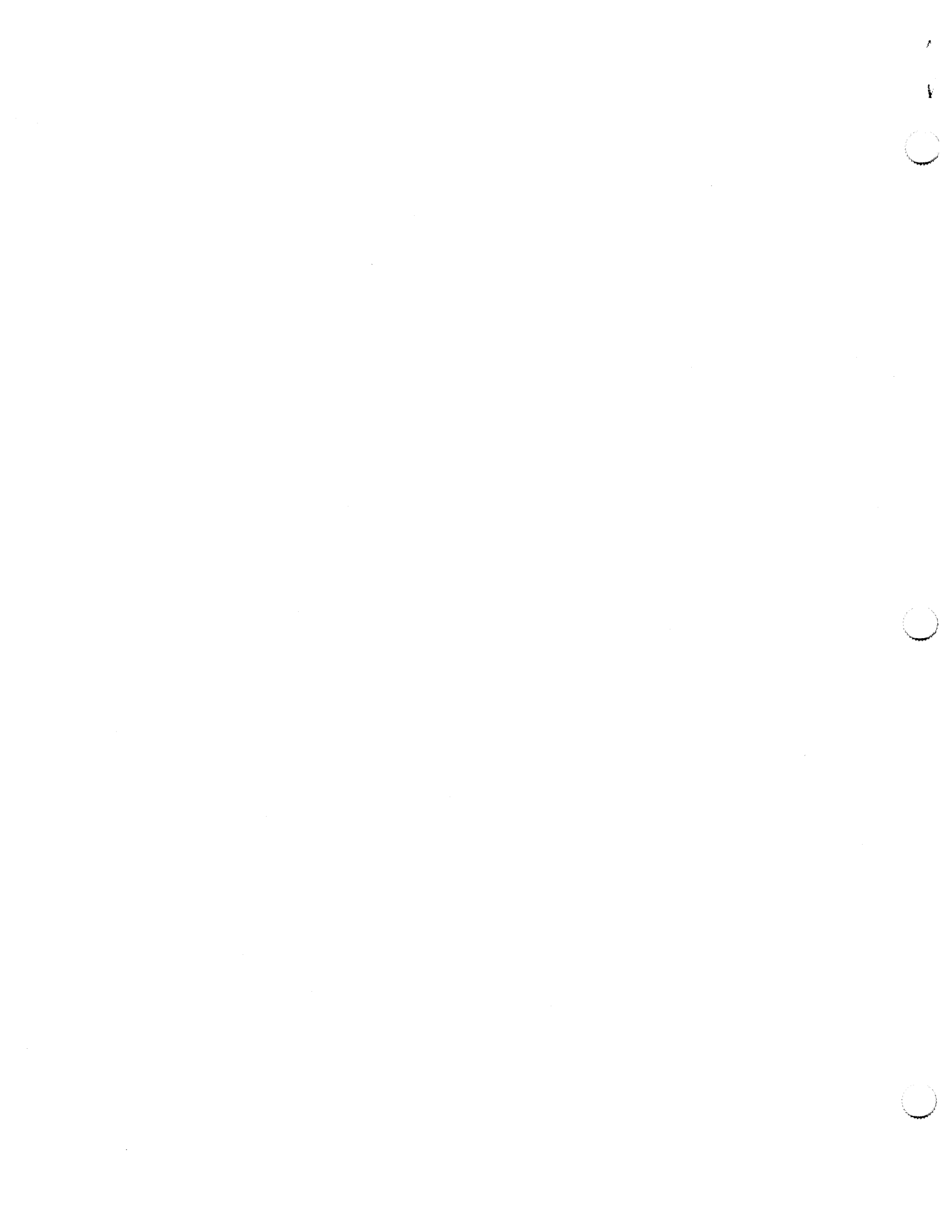
VME to Multibus Adapter Board
General Description

The VME-to-Multibus Adapter board allows Multibus and non-standard
VMEbus boards to reside mechanically and electrically in VMEbus systems.
The Adapter board is comprised of twelve sets of eight DIP switches, used to
define the base address of the Multibus memory, I/O space, and the block size of
the memory and I/O space. The illustration below shows the board layout and
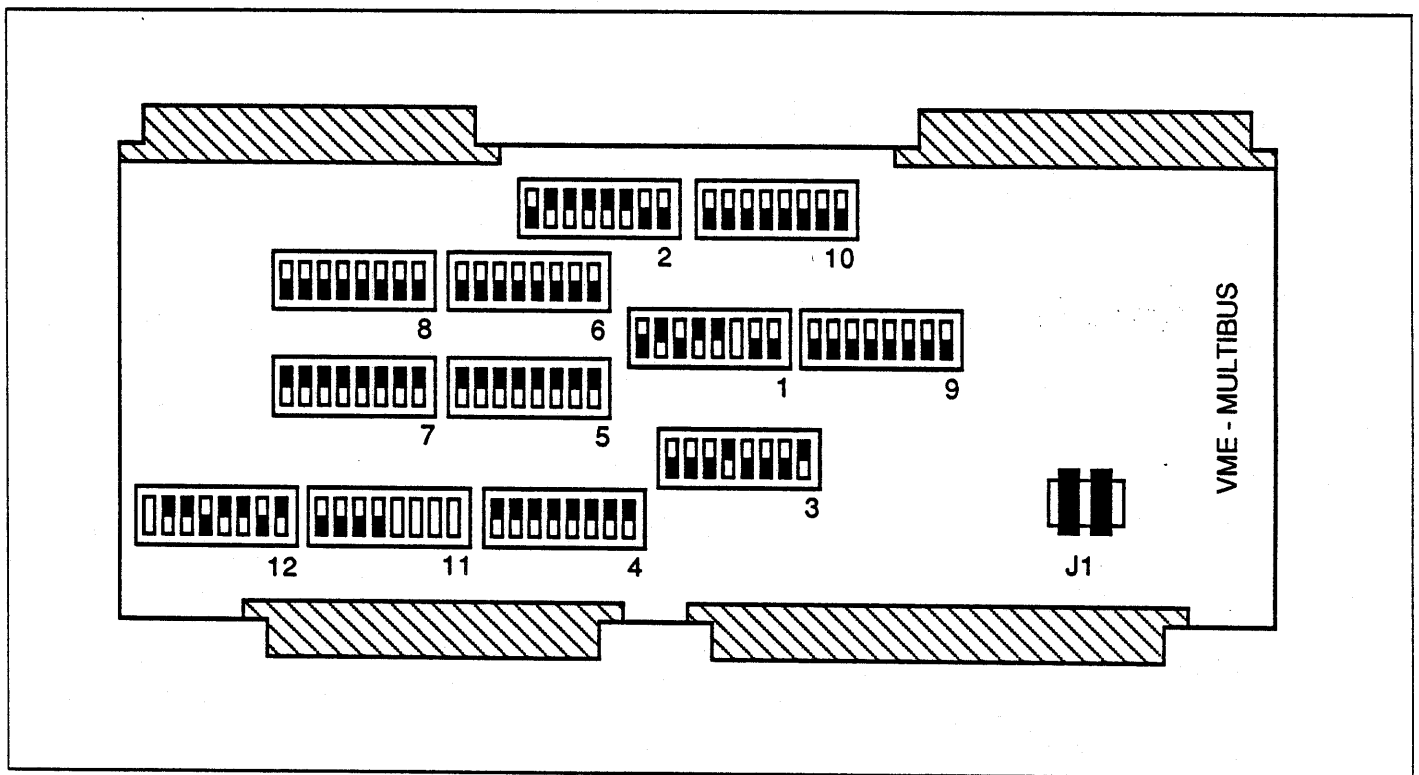the locations of the dip switches:

Figure 2-1   *VME-to-Multibus Adapter Board Switch Locations*

The following table details how to configure the VME-to-Multibus Adapter
Board for use with the Xylogics 450/451 SMD Controller.

Table 2-1   *Adapter Configuration for the Xylogics 450-451 SMD Controller*

Switch #	1	2	3	4	5	6	7	8	Description
Dip 1	OFF	ON	OFF	ON	ON	*	OFF	OFF	I-O Address*
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I-O Space = 8
Dip 3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Address 0xEE
Dip 4	ON	ON	ON	ON	ON	ON	ON	ON	VME Address Space
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	24-Bit Address Space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-Bit Block Size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	24-Bit Address Space
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-Bit Block Size
Dip 9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Connection
Dip 10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Connection
Dip 11	OFF	OFF	OFF	OFF	#	#	#	#	Sets A23-A20
Dip 12	*	ON	ON	OFF	ON	ON	OFF	ON	Interupt Vector*
J-1	Pins 1-2				Pins 3-4				
	BCLK-Installed				CCLK-Installed				

*   xy0 = ON (I-O Address = 0xee40, Interrupt Vector = 0x48)

xy1 = OFF (I-O Address = 0xee48 Interrupt Vector = 0x49)

\#   For 20-bit addressing, these switches should all be OFF.

For 24-bit addressing, these switches should all be ON.

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Revision History

Revision	Date	Comments
1	10 Feb 1986	First (alpha) release of this configuration procedure.
07-A	31 June 1986	Production release of this configuration procedure.
08-A	2 Dec 1986	First revision of this configuration procedure.
09-A	1 April 1987	Second revision of this configuration procedure.