## Systems

# IBM 4341 Processor Channel Characteristics 

## Preface

This manual describes how to check the effects of loads imposed on the IBM 4341 Processor channels. It is intended for programmers and systems analysts who wish to verify that a proposed configuration of input/output ( $\mathrm{I} / \mathrm{O}$ ) devices can work satisfactorily with the 4341 Processor.

The sections present general 4341 channel organization and implementation, a description of subchannels and unit control words, the procedure for channel interference determination, concurrent I/O capabilities, block-multiplexer and byte-multiplexer channel loading, specific device considerations, and channel evaluation tables.

Before using this manual, you should have a thorough understanding of input/output operations for the 4341 as described in:

- IBM 4341 Processor Functional Characteristics and Processor Complex Configurator. Order No. GA24-3672
- IBM System/370 Principles of Operation, GA22-7000
- IBM 4300 Processors Principles of Operation for ECPS:VSE Mode, GA22-7070
When testing for data overrun on the bytemultiplexer channel, two special worksheets are required:
- IBM 4341 Byte-Multiplexer Channel Preliminary Worksheet, GX24-3746
- IBM 4341 Processor Channel Load Sum Worksheet, GX24-3670


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## IBM 4341 Processor Channel Characteristics

This publication describes the calculations required to optimize channel operation on the IBM 4341 Processor. Detailed formulas, along with timing charts for input/output devices, enable users to determine maximum channel throughput with data overrun avoidance for actual 4341 configurations.

## General Channel Information

The channels of the 4341 Processor transfer data between main storage and I/O devices under control of a channel program that is executed independently of the processor program. The 4341 is free to resume the processor program after initiating an I/O operation.
The 4341 channels can run concurrently within the data-rate and channelprogramming conventions specified in this manual.

A major feature of the channels is the common I/O interface connection between a variety of I/O devices and System/360, System/370, and 4300 Processor input/output control units.
At the end of an I/O operation, the channel signals an I/O interruption request to the processor. If not disallowed, an $I / O$ interruption occurs that places the I/O new program status word (PSW) in control of the processor. When I/O interruptions are disallowed, interruption requests are queued (stacked). Until honored, an I/O interruption condition is called a pending I/O interruption.

At the end of an I/O interruption, a channel has information about the success or lack of success of the operation. The information (status) is available to the processor program.
Each 4341 channel can perform these functions:
Accept an I/O instruction from the processor.
Address the device specified by an I/O instruction.
Fetch the channel program from main storage.
Decode the channel command words that make up the channel program.
Test each channel command word (CCW) for validity.
Execute CCW functions.
Place control signals on the I/O interface.
Accept control-response signals from the I/O interface.
Transfer data between an I/O device and main storage.
Check parity of bytes transferred.
Count the number of bytes transferred.
Accept status information from I/O devices.
Maintain channel-status information.
Signal interruption requests to the processor.
Sequence interruption requests from I/O devices.
Send status information to location 40 hexadecimal when an interruption occurs.
Send status information to location 40 hexadecimal upon processor request.

## Channel Control

The 4341 channels provide a common input/output interface that permits the attachment of control units. The control units are governed by six channel commands and seven processor instructions. The instructions are:

[^0]All I/O instructions set the PSW condition code. Under certain conditions, all except Test Channel cause a channel status word to be stored. A Test Channel instruction calls for information about the addressed channel; a Test I/O instruction calls for information about a channel and a particular device. Halt I/O terminates any operation on the addressed channel, subchannel, or device. Halt Device terminates an I/O operation on a particular device on a channel without interfering with other I/O operations in progress on the channel. Only Start I/O and Start I/O Fast Release make use of channel command words.
A Start I/O instruction initiates execution of one or more I/O operations, and specifies a channel, subchannel, control unit, and I/O device. The channel fetches the channel address word (CAW) from location 48 hexadecimal. The CAW contains the protection key and the address of the first channel command word for the operation. Beginning with the first CCW specified by the CAW, the channel fetches and executes one or more CCWs.

Note: In the 4341., Start I/O Fast Release is decoded and executed as a Start I/O instruction. Throughout this manual, references to Start I/O also apply to Start I/O Fast Release.
The Clear I/O instruction causes the current operation being executed by the addressed device to be terminated with both byte-multiplexer and blockmultiplexer channels. In selector channel mode, the instruction is executed as a Test I/O.
Six channel commands are used:
Read
Write
Read Backward
Control
Sense
Transfer-in-Channel (TIC)
The first three are self-explanatory.
Control commands specify such operations as advance paper in a printer, set tape density, and rewind tape.
A Sense command brings information from a control unit into main storage. This information can concern unusual conditions detected during the latest I/O operation and detailed status about the device.
A Transfer-in-Channel (TIC) command specifies the location in main storage from which the next CCW in the channel program is to be fetched. A TIC cannot specify another TIC. Also, the CAW cannot address a TIC.
Each CCW specifies the channel operations to be performed and, for datatransfer operations, specifies contiguous locations in main storage to be used. One or more CCWs make up a channel program that directs a channel operation.
Command retry is a channel and control-unit procedure that causes a command to be retried without requiring an I/O interruption.
Retry is initiated by the control unit. When the command being executed encounters a retriable error, the control unit presents unit check and status modifier (retry status) along with channel end, or channel end and device end, to the channel. If conditions permit, a normal device reselection occurs to reissue the previous command. If retry is not possible, any chaining is terminated, and an I/O interruption follows.

For each I/O device selected, the 4341 channels maintain the following channel-control information:
Protection key
Data address
Identity of operation specified by command code
CCW flags
Byte count
Channel status
Address of next CCW
On byte- and block-multiplexer channels, the listed information must be maintained for each subchannel in operation. Storage for this information is provided by special channel storage that is not directly addressable. Each subchannel has provision in a special area of storage for channel-register information. When a particular subchannel is selected by a Start I/O instruction and a channel program is initiated, the channel storage locations for the subchannel are loaded with the information necessary for each operation of the subchannel.
At the completion of each activity in a subchannel, its particular area in storage contains updated information, and the multiplexer channel is available for operation of another subchannel.
Figure 1 shows the sharing of facilities by the channels and the processor.


A trap is an interruption of the current activity to allow another activity of a higher priority to take precedence.

Figure 1. Sharing of Processor and Channel Facilities

## Chaining

A single CCW may specify contiguous locations in main storage for a datatransfer operation, or successive CCWs may be chained together to specify a set of noncontiguous storage areas. The presence of a flag bit in a CCW causes chaining to the next CCW.
In data chaining, the address and count information in a new CCW is used; the command code field is ignored.
Entire CCWs, including their command code fields, can also be chained together for a sequence of channel operations. Such coupling, called command chaining, is specified by a different flag bit in a CCW.
Data chaining has no effect on a device, as long as the channel has sufficient time to perform both data chaining and data transfer for the device.
In this manual, when a device is said to data-chain, the channel program for the device specifies data chaining.

## Fetching Channel Command Words

The channel must fetch a new CCW whenever a CCW specifies data chaining, command chaining, or transfer in channel (TIC). The extra control activity caused by these operations takes time and diminishes a channel's ability to do other work.
A data-chaining fetch usually occurs while a channel also has a datatransfer load from the same device. The time required to fetch the new CCW necessarily limits the time available for successive data transfers through the channel. An absence of data chaining ordinarily permits a channel to operate with a faster I/O device. Similarly, when a channel is not transferring data, a data-chaining operation has a lesser impact on channel facilities.

## Data Chaining in Gaps

For direct-access storage devices, such as an IBM 3330 Direct Access Storage or an IBM 2314 Direct Access Storage Facility, formatting Write commands causes the control unit to create gaps between count, key, and data fields on the recording track. Read, Write, and Search commands that address more than one of the fields can specify data chaining to define separate areas in main storage for the fields.
The gaps on a track have significance to channel-programming considerations for direct-access storage devices. The channel does not transfer data during the time a gap is created or passes under the read-write head. This time is sufficient for a 4341 Processor to perform a command-chaining or data-chaining operation.
Command chaining ordinarily occurs only during gap time, but data chaining can occur during gap time or while data is being transferred. A datachaining operation occurring during gap time has less impact on channel facilities than when data transfers also occur. If a channel program for a direct-access storage device calls for data chaining only during gap time, the device's overall load on channel facilities is significantly less.
When a direct-access device is said to data-chain in a gap, the reference is to a gap other than a gap following a data field. The latter causes a deviceend indication. Command chaining is used in such a gap if the transfer or more information is desired. Device end occurring in the absence of a CCW specifying command terminates the operation. When command chaining continues the operation, the status information available at the end of the operation relates to the last operation in the chain.
During a read operation, an attempt to data-chain in a gap following a data field causes an incorrect length indication in the channel status byte.

## Late Command Ckaining

Operation of direct-access devices, such as disk storage, requires command chaining. Between certain operations, such as the search for a record identification key and the reading of a data field on a direct access-storage device, the control unit has a fixed time interval during which it must receive and execute a new command. If activity on other channel(s) causes too much delay in initiation of the operation specified by the new command, the channel program is terminated and an I/O interruption occurs. If, however, the device has command retry capabilities, the command is retried.

## Storage Addressing

During data chaining, the beginning and ending byte addresses and the minimum number of bytes transferred are factors in the maximum data rates that different System/360 and System/370 models and 4300 Processors. channels can sustain. When writing channel programs for larger systems, consider the storage width and the possibility of adding faster I/O devices.

## Channel Implementation

The 4341 Processor has two basic types of channels. A byte-multiplexer channel and two block-multiplexer channels are standard. Three additional block-multiplexer channels are available as an option. Within this option, a second byte channel may be selected on channel 4 .
The 4341 channels are integrated. They share with the processor the use of control storage, the processor storage data flow, and the arithmetic logic unit. Each channel can attach as many as eight control units and can address up to $256 \mathrm{I} / \mathrm{O}$ devices, except for the byte-multiplexer channels (channel 0 and 4) which can attach up to seven control units and has addresses 0 F0-0FF reserved. Control units are connected to all channels through the standard $\mathrm{I} / \mathrm{O}$ interface.

## Byte-Multiplexer Channel

The byte-multiplexer channels have a single data path that can be fully utilized by one I/O device (burst mode) or shared by many I/O devices (multiplex mode). Burst mode is defined as operation in which the device and the channel remain connected for a relatively long period of time in terms of system operation. Multiplex mode is defined as byte-interleaved operation in which the channel and any one device remain connected for a relatively short period of time, typically long enough to transfer one byte or a small number of bytes. Multiplexing, however, refers to the channel and device capability of disconnecting and reconnecting during an operation. The byte-multiplexer channel operates either in burst mode or in multiplex mode with multiplexing capability between bytes or groups of bytes.
Some control units are designed to operate on the byte-multiplexer channel in burst mode or in multiplex mode. Other control units allow the mode to be set at the installation.
When multiple I/O devices concurrently share byte-multiplexer channel facilities, the operations are in multiplex mode. Each device is selected, one at a time, for transfer of a byte or a few bytes to or from main storage. Bytes from multiple devices are interleaved and routed to or from desired locations in main storage. Thus, the byte-multiplexer channel data path is used by one device for transfer of one or a few bytes of data, and then another device uses the same data path. The sharing of the data path makes each device appear to the programmer as if it has a data path of its own. A device's share of the data path is called a subchannel.

## Block-Multiplexer Channels

Two block-multiplexer channels are standard on the 4341 Processor. Blockmultiplexer channel operation is described in the IBM 4300 Processors Principles of Operation for ECPS:VSE Mode, Order No. GA22-7070, and IBM System /370 Principles of Operation, GA22-7000.
The block-multiplexer channels can operate in either block-multiplex mode or selector mode. The mode of operation is determined by the blockmultiplex mode bit of the control registers, as well as how the the I/O device is described to the system.
The block-multiplexer channel in block-multiplex mode allows concurrent operation of many I/O devices. This mode is intended for relatively highspeed burst operations. A single block-multiplexer channel can support interleaved, concurrent execution of multiple high-speed channel programs. The block-multiplexer channel in this mode can be shared by multiple highspeed $1 / O$ devices operating concurrently just as the byte-multiplexer channel can be shared by multiple low-speed devices. Like the byte-multiplexer channel, the block-multiplexer channel has multiple subchannels, each has an associated UCW in control storage and can support one I/O operation.
A block-multiplexer channel functions differently in selector mode in the way that it handles command-chained channel programs. A blockmultiplexer channel operating in selector mode and executing a commandchained channel program is busy during the entire time the channel program is in operation, whether or not data transfer is occurring. A blockmultiplexer channel in block-multiplex mode executing a command-chained channel program can disconnect from the operational program during certain nondata transfer operations. That is, a block-multiplexer channel in blockmultiplex mode can be freed during nonproductive activity (for example, during disk seeking and most record positioning) to allow more data to be transferred per unit of channel busy time.
The selector and block-multiplex modes monitor the interface for an expected tag sequence. If an erroneous tag is activated (by a control unit) in addition to the normal interface sequence, the channel may not indicate a check. The channel may ignore the erroneous tag and proceed as if it did not exist.

## Channel-Available Interruption

The 4341 Processor implements the channel-available interruption on channels 1 through 5 when they are operating as block-multiplexer channels.

The channel-available-interruption condition is meaningful only for the block-multiplexer. In selector mode, the channel always terminates a channelbusy condition with an interruption or an interruption-pending condition.

## Channel Priority

All channels share one trap level for all functions, such as data transfer, chaining, status handling, and UCW fetching and storing.

The priority for handling channel trap requests is channel $1,2,3,4,5$, and
0 . To prevent high priority channels with constant trap requests from locking out low priority channels, each channel, except channel 0 , has a trap request inhibit latch. When a channel's inhibit latch is on or when a channel is in a trap, the trap priority controls do not consider a pending trap request for that channel. When a channel trap is taken, the inhibit latch for that channel is set on, or all inhibit latches are reset off. That is: the inhibit latch for the trapping channels is set if any trap requests are pending for lower priority channels; otherwise, all inhibit latches are reset.

[^1]Traps are requested by the channel hardware to indicate to the microcode that certain events have occurred or that certain conditions exist. Examples: the last command issued to the channel hardware has been completed, a device has connected to the I/O interface because of a polling sequence, or there is data in the data buffer to be transferred to storage.
The channel-trap microcode: fetches and stores the UCWs; transfers data between storage and the channel data buffers; fetches CCWs for SIO, command chaining, and data chaining; handles status and interface check conditions detected by the hardware; etc.

## Channel Data Buffer

When the channel operation is set up, hardware controls the data transfer.
Each channel has 256 bytes of channel data buffer. Depending on the data length and address boundary, hardware controls the transfer of data to processor storage:

- in 64-byte blocks
- in a partial block to line up to a 64-byte address boundary
- in a partial block to complete a data transfer
- in a partial block for very short records
- in a partial block for byte-multiplex operation.


## Subchannels and Unit Control Words

## Subchannels

The channel facilities required to sustain a single $I / O$ operation are called a subchannel. Subchannels can be either unshared or shared. An unshared subchannel has the facilities to operate only one I/O device. A shared subchannel provides facilities to operate one of an attached set of $1 / O$ devices.
The initiation of multiple I/O operations requires that the subchannels have channel storage to record the addresses, count, status, and control information associated with the I/O operation. In the 4341., the storage for a single set of such information is called a unit control word (UCW). The UCW storage is provided by moving the high address boundary of user storage. The number of required UCWs is determined by the number of I/O devices described to the system. A maximum of $1,024 \mathrm{UCWs}$ are available.
When an I/O operation is initiated, the UCW specified by the I/O unit address is modified (if the subchannel is not already busy) according to the operation to be performed. Each channel has one local-storage area for use in processing a single UCW. Therefore, when a UCW is set up in that area during execution of an $I / O$ operation, requests from other units on that channel are prevented.

## Unit Control Words (UCWs)

A UCW is either shared or unshared according to the type of subchannel it contains. The subchannel type is determined by the control and device(s) that use the subchannel and the UCW. An unshared UCW is reserved for a specified device. Examples are:

1. A single control unit that controls one $I / O$ unit and requires one unshared UCW. For example, the 1443 Printer or the 3211 Printer each requires an unshared UCW.
2. A single unit that contains several control units and requires an unshared UCW for each unit. For example, the 2821 Control Unit that handles functions for a 1403 Printer and the reader and punch sections of a 2540 Read/Punch requires three unshared UCWs.
3. A single control unit that services the requirements of several devices at once and requires an unshared UCW for each device. For example, the 3830 Storage Control requires an unshared UCW for each device.

A shared UCW is reserved for a specified control unit and is shared by the devices attached to that control unit. For example, each 3272 Control Unit requires an exclusive UCW, but all 3277 Displays serviced by that control unit share the UCW assigned to the 3272 .

## UCW Pool

From 128 to 1,024 subchannels (UCWs) can be configured. If more than 128 UCWs are required, additional groups of 32 UCWs are allocated, up to the maximum of 1,024 .
Each of the minimum allocation of 128 UCWs occupies 64 bytes of processor storage (for a total of 8,192 bytes). Additional UCWs (in groups of 32 , up to a maximum of 1,024 ) may be assigned (by trained service personnel), with the user-storage reduction described in the following section.

A portion of processor storage is required for systems functions and reduces the amount of processor storage available for user programming. The size of the reduction depends upon the processor configuration.
Each group of 32 additional UCWs reduces the usable processor storage by 2,048 bytes. For example, 128 UCWs require 8 K of storage, and 1,024 UCWs require 64 K of storage. For each increase in the number of UCWs, the additional UCW storage requirement limits the high address boundary.
Sixteen UCWs ( 000 through 00F) are reserved for natively attached I/O and for internal functions. Each channel has a shared UCW through which all unassigned I/O devices can present asynchronous interruptions. Each device attached to a channel must have a UCW associated with its address.

## Channel UCW Directory

Each channel has a channel directory. Each directory has 256 entries, one for each possible device address ( $00-\mathrm{FF}$ ) on the channel.
Each directory entry contains the reference number of its associated UCW.
Each entry also contains the following status and attribute bits:
ASSIGNED indicates that this entry was assigned to an I/O device by the user.
SHARED indicates a shared UCW.
SEL indicates a device that must operate in selector mode.
DATA STREAM indicates a control unit or device attached to a control unit that can operate in data streaming mode.

## UCW Assignment

## Device Considerations

UCWs for natively attached I/O devices (such as the 3278-2A) are preassigned. The logical addresses for these devices are assigned by the user. All other I/O devices must be described to the processor by the service representative at the user's request.
The device addresses for a channel that are not used by a described device are assigned to a channel shared $U C W$. A device that has not been described to the system can submit status via the channel shared UCW, but I/O instructions issued to that device result in a not operational condition (condition code 3). This information is kept in the UCW directory tables for automatic assignment of UCWs by the processor.
All UCW assignments are written onto the system diskette and become effective after subsequent initial microcode load (IML) operations. Note, however, that UCW reassignments for natively attached equipment become effective immediately (without a re-IML).
Figure 2 shows the special control-unit and devices requirements to be entered to describe them to the systems for UCW assignments.
system is generally able to provide better throughput if devices are assigned an unshared UCW and allowed to multiplex; however, this is not always the case. Some shared control units are capable of sustaining only one operation as a time. A shared UCW is quite satisfactory for this type of control unit. Assigning a UCW for each device is wasteful of UCWs. Some


Figure 2. UCW Assignment Chart
control units rely on the characteristics of the selector mode. These control units must have the multiplexing ability of the block-multiplex mode inhibited.
Devices that share a control unit and operate in selector mode can share a common UCW on the channel. The SEL mode bit must be on in the directory entry.
Devices capable of running in block-multiplexer mode can use an unshared UCW for each actual device attached, or one shared UCW for all devices attached to the control unit. Normally, UCWs for the block-multiplexer channel are unshared, with SEL mode off.
Some devices, such as the IBM 3272 Control Unit, require one exclusive UCW for each control unit on the channel. Each 3277 attached to that control unit shares that control unit's UCW. The SHARED bit must be on in the directory entry for that UCW.
Magnetic tape devices use a shared UCW and operate in selector mode.
Channel-to-channel adapters are treated as control units and require one UCW for each interface attached to the processor.
The use of data streaming mode is independent of whether a UCW is shared or unshared, or whether operation is in selector or block-multiplexer mode. The use of data streaming mode is still determined by device type.

## Channel Interference with Processor

Because the processor and the channels share main storage and control storage, execution of processor instructions is slowed by activities on the channels. This is referred to as channel interference with processor or channel/processor interference. For simplicity, channel interference with processor is referred to as interference in this section.
This section defines how to calculate this amount of interference for $1 / \mathrm{O}$ operations. To calculate interference time requires a knowledge of the particular systems I/O configurations and of the I/O programming involved. To calculate this time involves:

1. Calculation of the total interference time caused by the individual activities on the channel.
2. Calculation of the total interference percentage with the processor by relating the total interference time to a particular time span that is pertinent to the operation; for example, the time taken to execute all or part of an I/O operation, or even an entire program. The choice of a particular span of time is up to you.

## Calculation of Total Channel/Processor Interference Time

The channel activities that can cause channel/processor interference and the duration of those activities are listed in Figures 3 and 4. To calculate total duration of interference:

1. From the figures, list the channel activities and their associated interference times that can occur in the time span chosen.
2. Record the number of times each channel activity (step 1) occurs in this time span.
3. For each channel activity (step 1), multiply the interference time (step 1) by the number of times that the activity occurs (step 2 ). This product is the duration of interference caused by that activity.
4. Add together the individual duration of interference times (step 3) to obtain the total interference duration.

| Channel Activity | Channel Mode |  |  |
| :---: | :---: | :---: | :---: |
|  | Byte <br> Multiplex | $\begin{gathered} \text { Block } \\ \text { Multiplex } \end{gathered}$ | Selector Channel |
| Data Transfer Byte Mode/Byte Multi-Byte Mode/Connection Burst Mode/64 Bytes | $\begin{array}{r} 20.8 \\ 20.8 \\ 3.7 \end{array}$ | 3.7 | 3.7 |
| CCW Execution <br> Command Chaining with: <br> CE and DE Together* <br> CE and DE Separated* <br> Data Chaining* <br> TIC | 26.0 40.6 8.8 2.1 | 5.2 19.8 4.3 2.1 | 5.2 7.3 4.3 2.1 |
| 1/0 Operations Concluding with: <br> $C E$ and DE Together** <br> CE and DE Separated** | $\begin{aligned} & 37.3 \\ & 73.5 \end{aligned}$ | $\begin{aligned} & 35.3 \\ & 76.9 \end{aligned}$ | $\begin{aligned} & 30.7 \\ & 71.8 \end{aligned}$ |
| PCI Processing | 28.7 | 39.9 | 39.9 |
| IDAW Fetch | 2.3 | 2.3 | 2.3 |

* Add time for one IDAW fetch if IDA bit is $O N$ in the new CCW.
** Includes creation time and $1 / 0$ inter $u p t i o n ~ t i m e . ~$

Figure 3. Processor Interference Times in Microseconds (System/370 Mode)

| Channel Activity | Channel Mode |  |  |
| :---: | :---: | :---: | :---: |
|  | Byte Multiplex | B lock Multiplex | Selector Channel |
| Data Transfer Byte Mode/Byte Multi-Byte Mode/Connection Burst Mode/64 Bytes | 22.8 22.8 3.7 | 3.7 | 3.7 |
| CCW Execution <br> Command Chaining with: <br> CE and DE Together* <br> CE and DE Separated* <br> Data Chaining* TIC | 29.9 44.5 12.7 4.1 | 7.2 23.7 6.3 4.1 | 7.2 9.3 6.3 4.1 |
| 1/0 Operations Concluding with: <br> CE and DE Together** <br> CE and DE Separated** | 37.3 73.5 | $\begin{aligned} & 35.3 \\ & 76.9 \end{aligned}$ | $\begin{aligned} & 30.7 \\ & 71.8 \end{aligned}$ |
| PCI Processing | 28.7 | 39.9 | 39.9 |

* Add time for one IDAW fetch if IDA bit is ON in the new CCW.
** Includes creation time and $1 / 0$ interruption time.

Figure 4. Processor interference Times in Microseconds (ECPS:VSE Mode)

Figure 5 gives an example calculation of total interference time that is caused by a tape-to-printer operation during which:

| Channel Activity | Processor InterFerence Factors | Number of Bytes or Occurrences | Duration of Interference with Processor |
| :---: | :---: | :---: | :---: |
| Reading tape in selector mode: Data transfer in burst mode | 3.7 usec/byte | $\begin{aligned} & 1000 \text { bytes } / 64 \\ & =16 \end{aligned}$ | 59.2 usec |
| CCW execution by data chaining | 4.3 usec | 9 | 38.7 usec |
| Concluding of $1 / 0$ operation with CE and DE together | 30.7 usec | 1 | 30.7 usec |
| Writing to printer on byte multiplexer channel: <br> Data transfers (in byte mode) | 20.8 usec/byte | 1000 bytes | 20,800 usec |
| Execution of a CCW by command chaining with CE and DE separated | 40.6 usec | 9 | 365.4 usec |
| Concluding of $1 / 0$ operation with CE and DE separated | 73.5 usec | 1 | 73.5 usec |
| Total duration of interference |  |  | $\begin{aligned} & 21,367.5 \mathrm{usec}= \\ & 21.4 \mathrm{~ms} \end{aligned}$ |

Figure 5. Duration of Channel Interference with Processor - (Example Calculation for a Tape-to-Printer Operation in System/370 Mode

1. A 1,000-byte record is read from tape (selector mode on a blockmultiplexer channel) by ten data-chained CCWs.
2. The 1,000 bytes are then sent to the printer (byte mode on a bytemultiplexer channel) by ten command-chained CCWs.
3. The example time span is assumed to be the duration of the complete operation.

The duration of interference time does not depend on the data rate of the device but on the characteristics of the 4341 channels and on the amount of data being transferred.

## Calculation of Total Channel/Processor Interference Percentage

The previous calculations describe how to obtain the actual duration of interference in microseconds over a particular time span. This time figure, divided by the time span used for calculations, yields a percentage of interference.
The significance of the derived percentage of interference depends on the choice of time span. For example, the percentage of interference due to the tape-to-print operation in Figure 5 over a period of one minute is as follows:
[21.4 ms $\div(1 \times 60$ seconds $\times 1000$ bytes $)] \times 100=0.036 \%$
Conversely, the processor available time is

$$
100 \%-0.036=99.964 \%
$$

The percentage interference figure is the percentage by which the processing of processor instructions is slowed. If the interference is too great for the device being operated (see "Program Overrun"), queues develop for those
buffered devices that need service on the byte-multiplexer channel. This results in loss of performance on those devices.

## Program Overrun

Program overrun is a particular effect of channel interference with the processor (see previous section). Program overrun results from a program being slowed to such an extent that the program is late in providing realtime service to a device and, hence, causes incorrect operation of that device.
Program overrun must always be considered for those I/O operations that involve high-speed document handling devices, such as the IBM 1419 Magnetic Character Reader. In program-sort mode, the 1419 reads data into the processor while the document is passing the read station. Then, before the document reaches the stacker-select station, the processor must calculate the stacker required and issue the correct stacker-select command. If the stacker select command arrives too late (because of program overrun), the document is not stacked correctly and the channel program stops.

## Assessing Program Overrun

To investigate the possibility of program overrun:

1. Establish the available program time, that is, the time during which the program must perform calculations and issue the command. Call this time A (available time).
2. Establish the time that the program takes between reading data and issuing the command. This time can be established by totaling the execution times of the instructions (see "Instruction Timings" in IBM 4341 Processor Functional Characteristics, GA24-3672). When establishing this time, take all program activity into account, including the handling of the $\mathrm{I} / \mathrm{O}$ interruption after the data is read, and any possible supervisor program activity. Call this time $P$ (processing time).
3. Establish the maximum possible processor interference time that can be caused by simultaneous activities on all channels during time A. The calculation of total channel/processor interference time is described previously in this section. Call this time I (interference time).
4. Calculate P (processing time) +I (interference time) and compare the result to A (available time). If $\mathrm{P}+\mathrm{I}$ is greater than A , program overrun may occur.

Example: Consider the possibility of program overrun with a single-address 1419 and assume that additional channel activities are: (1) a 3330 Disk Storage Device transferring data on one of the channels in burst mode at the rate of 806 kilobytes per second, and (2) a 1442 Card Read Punch using one-byte transfers and punching EBCDIC characters.
For this example, assume that the interference with the processor caused by these two operations during the available time A is the worst that can occur in this application or that it has the highest interference time I.
Check for program overrun as follows:

1. Establish the available program time A. From IBM 1219 Reader Sorter, IBM 1419 Magnetic Character Reader, GA24-1499, the minimum time available for giving the stacker-select command is 9.50 milliseconds.
2. Establish the processing time $P$ of the program instruction sequence that calculates the stacker required and issues the stacker-select command. For the purpose of this example, assume that the processing time $P$ including possible supervisor activity, is 8.00 milliseconds.
3. Establish the total interference time I.
a. Calculate the duration of interference that is caused by the 3330 data transfer within the time span A. At 806 kilobytes per second, the number of bytes transferred in time $\mathbf{A}$ ( 9.50 milliseconds) is:

Number of bytes $=(806,000 \times 9.50) \div 1000=7,657$ bytes
By using the duration of interference on a channel in burst mode to be $3.7 \mu \mathrm{~s} /$ byte (from Figure 3), the total interference in time A caused by transferring 7,657 bytes is:

```
7,657 bytes }\div64=120 64-byte transfer
120 x 3.7 }\mu\mathrm{ s per 64 bytes = 444.0 }\mu\textrm{s}\mathrm{ of interference time
```

b. Calculate the duration of interference caused by the 1442 within the time span A. This is assumed to be the execution of one commandchained CCW, and two one-byte data transfers (see Figure 4).

> Execution of a CCW with command chaining: $$
\begin{array}{l}26.0 \mu \mathrm{~s} \times 1=26.0 \mu \mathrm{~s} \text { Data transfer in byte mode: } \\ 20.8 \mu \mathrm{~s} \times 2=41.6 \mu \mathrm{~s}\end{array}
$$ Total: $\quad 67.6 \mu \mathrm{~s}$

c. Calculate the total interference time I from steps $a$ and $b$

$$
444.0 \mu \mathrm{~s}(\text { Step } \mathrm{a})+67.6 \mu \mathrm{~s}(\text { Step } b)=511.6 \mu \mathrm{~s}
$$

or 0.512 ms total interference time
4. Calculate $\mathbf{P}+I$ and compare the result with $\mathbf{A}$.

$$
\mathrm{P}(8.00 \mathrm{~ms})+\mathrm{I}(0.512 \mathrm{~ms})=8.512 \mathrm{~ms}
$$

or $\mathrm{P}+\mathrm{I}=8.512 \mathrm{~ms}$
Because A ( 9.50 ms ) is larger than $\mathrm{P}+\mathrm{I}(8.512 \mathrm{~ms})$, no program overrun can occur.

## Concurrent Input/Output Capabilities

Each I/O device in operation places a load on its channel facilities. The magnitude of a load depends on a device's channel programming and its data-transfer rate. In this manual, numeric factors are used to relate the loads caused by operation of I/O devices to the channel's abilities to sustain concurrent operation of the devices.
One or more numeric factors are specified for each I/O device and channel available with a 4341 Processor. The numeric factors are given in tables in the Appendix and are used in arithmetic procedures for determining whether the operations of specific 4341 input/output configurations are satisfactory.
Several procedures are provided for evaluating a configuration of I/O devices for concurrent operation on 4341 channels. For most configurations, using the basic procedures suffices in determining whether operation is satisfactory. Use detailed procedures only for configurations that appear to exceed 4341 input/output capabilities.

## Worst-Case Loads

## Overrun

The evaluation factors and procedures allow for a worst-case situation, when the most demanding devices in the configuration make their heaviest demands on 4341 I/O capabilities at the same time. Such a situation may not occur frequently, but this is the situation that the evaluation procedures test. If a particular configuration fails this test, one or more devices can be expected to incur overrun or loss of performance.

Overrun occurs when a channel does not accept or transfer data within the required time limit. This data loss may occur when the total channel activity initiated by the program exceeds channel capabilities. Depending on the device, the operation may be halted, or data transfer may continue until the end of the block is reached.
An overrun may cause a unit-check indication to be presented to the channel and stored in the CSW. Chaining, if any, is suppressed, and an I/O interruption condition is generated at the end of the operation. Certain control units, however, can initiate a command-retry sequence without storing a CSW or requiring an I/O interruption.

## Loss of Performance

Overrun occurs only on unbuffered I/O devices. When buffer service is not provided within required time limits, the device merely waits for channel service. This means a loss of performance.

## Conventions for Satisfactory Channel Programs

Execution of a channel program causes a load on channel and system I/O facilities. Some I/O devices require execution of a chain of commands before transfer of a data block. However, the impact of the load caused by a channel program is not a simple function of the number of commands used. The sequence in which particular types of commands appear in a channel program is also a factor.

Control commands are particularly significant to sequencing considerations because they are executed at electronic speed and cause no motion. The command is executed as an immediate operation and provides device end in the initial status byte. When command chaining is specified in such an
immediate operation, channel facilities are not disengaged from the channel program until the chain ends or a command causing mechanical motion or data transfer is executed. Therefore, when immediate operations with device end in the initial status byte are chained together, fetching and execution of the CCWs can cause a heavy load on channel facilities. This load can cause excessive delay in channel service to one or more devices in the I/O configuration and result in overrun or loss of performance. For example, a chain of No-Op commands can contribute heavily to channel loading. Thus, a programming convenience may cause a severe overrun situation for concurrently operating devices.

## Data-Chaining Considerations

A 4341 user can specify data chaining in channel programs, although a channel is able to transfer data at a faster rate, without overrun, when data chaining is not specified. The channel-evaluation procedures and tables in this manual provide guidance in gauging the effects of data-chaining operations.

## Relationship of Conventions and Evaluation Procedures

The evaluation procedures depend on channel programs having command sequences that provide efficient operation of I/O devices and that avoid placing unnecessary loads on channel facilities. Channel-programming conventions help I/O programmers avoid overrun situations.
Observing channel-programming conventions is fundamental to the selection of an $I / O$ configuration that permits satisfactory concurrent operation of I/O devices. The channel-programming conventions described are integral to the channel-evaluation procedures. An evaluation indicating satisfactory channel performance is not dependable for channel programs written in violation of the conventions.

## Scope of Conventions

1. The conventions relate to the sequence in which certain types of commands can be executed, not to their sequence in main storage.
2. The conventions define four classes of commands and the sequence in which they can be used.
3. The command sequences provided by the conventions differ for different types of devices. Sequences are provided for:

DASD: $2305,2311,2314 \mathrm{~A}, 3330,3340,3350$
Tape unit: series $2400,2420,3410,3420$
Card units: $1442,2501,2520,2540,3505,3525$
Printers: 1403, 1442, 3211, 3203
Communication adapters: $2701,3704,3705$
4. The conventions relate to all the commands in a chain including the CCW addressed by the CAW and the terminating CCW that does not specify any chaining. This is of particular interest to I/O programmers working on segments of a single channel program. The conventions still apply when one segment is chained to another segment.
5. The conventions relate only to commands addressed by the CAW that specify chaining.
6. The conventions relate only to the avoidance of overrun; they do not define invalid command sequences that are that are rejected by a channel (such as TIC to TIC), or that are rejected by a control unit. CCW sequences causing command reject are specified in the I/O device manuals.

The channel-programming conventions in this manual are recommended to 4341 users, particularly in a multiprogramming environment where a programmer is not aware of the overall load on channel facilities. Where a programmer controls or has knowledge of all I/O activity, he can establish somewhat less restrictive channel programming conventions that are particularly suited to his application and configuration.

## Classes of Commands

The conventions establish four classes of commands. Commands that always cause mechanical motion are in one class. The other three classes encompass commands that are executed at electronic speeds, plus commands that are sometimes executed at electronic speeds. An example of the latter is rewind, which is executed at electronic speeds when tape is already at load point. The three classes of commands having electronic-speed properties differ in the length of time required for their execution.
The conventions for the different devices specify classifications for the specific commands pertinent to each device.
The conventions define the four classifications by the sequence in which they can precede or follow other commands:

Class A Commands: These commands can be chained in any order, without restriction. In general, Class A commands always cause mechanical motion.

Class B Commands: Only one Class B command can be chained between two Class A commands:
$-->\mathrm{A}-->\mathrm{B}-->\mathrm{A}=\quad$ permissible command-chaining sequence
$-->\mathrm{A}-->\mathrm{B}-->\mathrm{B}-->\mathrm{A}=\quad$ command-chaining sequence excluded by conventions
A Class B command can be substituted for a Class C or Class D command.

Class C Commands: A Class C command generally appears only once in a channel program, and then only as the first command in a channel program; therefore, a Class C command usually appears only in the location specified by CAW:
$\begin{array}{ll}\text { CAW }->\mathrm{C}-->\mathrm{A}-->\mathrm{B}= & \text { permissible program } \\ \mathrm{CAW}->\mathrm{A}->\mathrm{C}-->\mathrm{A}= & \text { program excluded by conventions }\end{array}$
A Class B command can be substituted for a Class $C$ command:
CAW $-->B-->A-->B-->A-->B=$ permissible program
Class D Commands: A Class D command can appear only as the last command in a channel program; it cannot specify any chaining.

| CAW $->X-->X-->D=$ | permissible program |
| :--- | :--- |
| CAW $-->X->D-->A=$ | program excluded by conventions |

A Class B command can be substituted for a Class D command. Some devices have conventions that exclude specific sequences of commands not excluded by the classifications previously described. Some devices have conventions that allow a specific command sequence to be substituted for a single command of a specified class. For detailed information, refer to the publications that describe the individual devices.

## Command Classifications for I/O Devices

The following rules define classifications for specific commands used with a particular device. The bit pattern for each command code byte is specified to provide positive identification of commands.
Commands not classified in the following text cannot specify any chaining and can be placed only in the location specified by the CAW. Each such command thus constitutes an entire channel program in which it is the only command. The Sense command is used in this manner for all devices.

Note: For diagnostic or device feature-dependent commands, refer to the device-associated manuals.

Direct-Access Storage Devices: These command classifications are valid for all DASD devices.

Class A commands (any order):

| Read 1 Write ${ }^{\text {dxx }}$ x 10 |  |  |
| :---: | :---: | :---: |
|  |  |  |
| Search | xxxx xx 01 |  |
| Erase |  |  |
| Space Count | 00001111 |  |
| Recalibrate | 00010011 | (Class A, 2311 only) |
| Orient | 00101011 |  |
| No-Op | 00000011 | (No-Op can be used |
|  |  | only when preceded <br> by a 0001 xx01 or |
|  |  | 00000001 formatting |
|  |  | Write.) |

Class B commands (not more than one between Class A commands):
TIC

$$
\text { xxxx } 1000
$$

$$
\left\{\begin{array}{l}
00000111 \\
000 \times 1011
\end{array}\right.
$$

Set Sector 00100011
Read Sector 00100010
These command chains have the properties of a single Class B command:

| TIC-->Seek | $\text { xxxx 1000--> }\{$ | $\left\{\begin{array}{l}00000111 \\ 000 \times 1011\end{array}\right.$ |
| :---: | :---: | :---: |
| Seek--> TIC | $\left\{\begin{array}{l}00000111 \\ 000 \times 1011\end{array}\right\}$ | --->xxxx 1000 |
| TIC-->Seek--> Set Sector |  |  |
| xxxx 1000--> | $\left\{\begin{array}{l} 0000 \text { 0111--> } \\ 000 \times 1011 \end{array}\right\}$ | $00100011$ |
| Seek-->Set Sector--> TIC |  |  |
| $00000111\}$ |  |  |
| 000x 1011 \} | -->0010 0011--> | >xxxx 1000 |

Note that a Read Sector must be preceded by a Read, Write, or Search command and that a Seek must precede a Set Sector.

Class C commands (first CCW in program): These command chains have the properties of a single Class C command:


Excluded chains:
Search $-->$ TIC -->Write
x011 0001$\}$
$x 010$ 1001 $\quad-->x x x x 1000-->0000 \times 101$
Data chaining can propagate through a TIC command for gap-only data chaining (see "Data Chaining in Gaps").

## Tape Units:

Class A commands (any order):

| Read | xxxx $x \times 10$ |
| :--- | :--- |
| Write | xxxx $\times x 01$ |
| Read Backward | xxxx 1100 |
| Forward Space | $0011 \times 111$ |
| Backspace | $0010 \times 111$ |
| Write Tape Mark | 00011111 |
| Erase Gap | 00010111 |

Class B commands (not more than one between Class A commands): TIC xxxx 1000

Class C commands (first CCW in program):
Set Mode $\quad$ xxxx x011
This command chain has the properties of a single Class C command:
Set Mode-->TIC xxxx x011--> xxxx 1000
Class D commands (last CCW in program):

| Rewind | 00000111 |
| :--- | :--- |
| Rewind and Unload | 00001111 |
| No-Op | 00000011 |
| Data Security Erase | 10010111 |

Mixed-Mode, Seven-Track Tape Operations: A routine can be used to select a tape unit, set its density mode, and then TIC to a desired channel program:

$$
\begin{array}{cl}
\text { SIO--> Set Mode } & \text { Class } C \\
\text { TIC } & \text { sequence }
\end{array}
$$

The conventions require the CCW addressed by the TIC to be Class A.

If the tape applications involve mixed-mode, seven-track operations, the programmer can make provision for placing the proper Set Mode command in the location addressed by the CAW before SIO is issued, or the programmer can begin each channel program addressed by the TIC with an appropriate Set Mode command. This additional Set Mode command violates the convention for Class $C$ commands and causes an additional load on channel facilities.

## Card Units:

Class A commands (any order):
Read $\quad x x x x \times x 10$
Write $\quad \operatorname{xxxx} x \mathrm{x} 01$

Class B commands (not more than one between Class A commands):
TIC
xxxx 1000
Class Commands (first CCW in program):
Control $\quad$ xxxx xx 11

Class D commands (last CCW in program):
Control $\quad$ xxxx xx 11

## Printers:

Class A commands (any order):
Write $\quad$ xxxx xx01
Class B command (not more than one between Class A commands):
TIC $\quad$ xxxx 1000
Class Commands (first CCW in program):
Control $\quad x x x x$ xx 11

Class D commands (last CCW in program):
Control 00000011
Communication Adapters: Data chaining with or without TIC can be used for these adapters.
Class A commands (any order):

| Write |
| :--- |
| Dial |
| Break |
| Diagnostic write |
| Read |
| Prepare |
| Inhibit |
| Search |
| Diagnostic read |$\quad$ xxxx xx01

Class B commands:
Not applicable
Class C commands (first CCW in program):
Control* $\quad$ xxxx xx11
Class D commands (last CCW in program):
Control* $\quad$ xxxx xx 11

* For a communications network of switch-type terminals, these two control commands are Class A:

| Disable | 00101111 |
| :--- | :--- |
| Enable | 00100111 |

## Evaluating Heavily Loaded Channels

When evaluating the performance of a system susceptible to channel overload conditions, consider the relative ease of restarting an interrupted I/O operation. For example, an overrun on a communication line coupling two processors is handled more readily than a read overrun on a card read-punch. Preferential priority can be given to devices that require manual intervention in response to an overrun condition.
Some circumstances may warrant placing devices with heavy load factors on the same block-multiplexer channel, rather than on separate block-multiplexer channels, to reduce the channel load on the system.
Evaluations should not ignore the characteristics of IBM Programming
Systems packages:
Operating System/360
Disk Operating System
These programs attempt to execute any start I/O instruction for which the channel and device are available.

## Block-Multiplexer Channel Loading

## Overrun Evaluation Consideration

When more than one channel is running concurrently, the channels compete for the processor's resources. If any channel is delayed in its bid for the shared resources because the resources are being used by other channels, the channel being delayed may overrun. Block-multiplexer channel operations resulting in overrun cause degradation of the total system because of the time required for error-recovery procedures. Using data chaining with TIC increases the time that a channel needs the shared resources; this can, in turn, reduce the maximum data rate that can be sustained on the channel and can diminish the capabilities of lower-priority channels.
If the program causes data chaining to occur only during gap time, the data chaining does not reduce the maximum data rate that can be sustained on that channel.

## Late Command Chaining

In systems that have disk-storage and/or fixed-head storage facilities operating on the lower-priority channels, simultaneous chaining can cause late command chaining on the lower priority channel.
When late command chaining occurs on the facilities with retry capabilities, the channel and control unit cooperate to reissue the late command to repeat the operation after one revolution of the disk. In this case, because it occurs infrequently, system performance is not likely to be affected significantly. Without retry facilities, the channel program ends and an I/O interruption condition occurs. This can cause significant performance degradation.

## Testing for Overrun

To determine the maximum individual block-multiplexer channel capabilities with various configurations and operating conditions, refer to Appendix C and D. Check to ensure that no device operating under the conditions specified exceeds the maximum data rate specified.

## Byte-Multiplexer Channel Loading

The byte-multiplexer channel should not be required to handle a burst-mode I/O device that is subject to data overrun. Burst-mode devices (tapes or disk drives) should be attached on a block-multiplexer channel. However, the operation of non-overrunnable buffered I/O devices, such as printers, and card readers and punches, is supported in burst mode. Other devices attached to the byte-multiplexer channel are locked out during this period. This can cause overrun when the ability to wait for channel service is exceeded.

## Byte-Mode Considerations

Concurrent operation of I/O devices on a byte-multiplexer channel is governed by several variables:

1. Devices vary in data-transfer rates.
2. Devices have buffers varying in capacity.
3. Devices vary in the number and type of CCWs needed for their operation.
4. Combinations of devices on the block-multiplexer channels vary in the interference they cause.
5. The large number of I/O devices available for use on a byte-multiplexer channel can be combined in many different ways.
6. Devices in a particular configuration can be physically connected in many different priority sequences.

Worksheet and factor tables can be used to determine whether a byte-multiplexer channel configuration can run concurrently in a satisfactory manner.

## Device Load

A numeric factor, called a device load, for each byte-mode device represents its load on channel facilities. The factors are listed in Appendix A for channel 0, and in Appendix B when channel 4 is selected as a second byte-multiplexer channel.
The values given in Appendix A and B need to be modified if any block-multiplexer channel is active. The D1 factor is used in the following formula to modify the device load:

Device Load (modified) $=$ Device Load $+($ D1 x n $)$
where $\mathrm{n}=$ number of active block-multiplexer channels.
Appendix A and B lists other factors for use in considering the impact of higher-priority devices on lower-priority devices.

## Device Wait Time

After requesting channel service, a byte-mode device has a fixed time that it can wait for service. If service is provided within this time, the device operates satisfactorily. If, however, the channel does not service the device within the device's wait time, either of two things occurs: if the device is not susceptible to overrun, it continues waiting; if it is, it loses data and causes an I/O interrupt condition. For example, if a 1403 Printer on a overloaded byte-multiplexer channel fails to receive data, it waits until service is provided by the channel. The delay does not cause an interrupt condition, nor is a new start I/O instruction required for selecting the 1403 . The only effect is a slight reduction in performance. If, however, a 1442 Card Read Punch read operation does not receive data service within its wait time, an overrun occurs.

Wait time factors for byte-mode devices are listed in Appendix A and B.

## Device Priority on Byte-Multiplexer Channel

The priority of devices on a byte-multiplexer channel is established at the time of installation by the sequence in which they are connected to the channel. The cabling facilities provide considerable flexibility in the physical location and logical position of I/O devices.
Devices may have the priority sequence in which they are attached to the cable (select-out line priority), or the device most remote from the channel may be connected to have highest priority and the device nearest the channel connected to have lowest priority (select-in line priority).
Each device on the byte-multiplexer channel cable may be connected (for selection) either to the select-out line or to the select-in line. Thus, one or the other of the lines is specified in establishing priority for a desired physical layout of devices.
Priority assignments and machine-room layout should be established during the physical planning phase of an installation so that cables for the I/O devices can be properly specified.
A major consideration is assigning priority to multiplex-mode devices is their susceptibility to overrun. Devices are identified in this manual as being in one of three classes:

Class 1: Devices subject to overrun; for example, the IBM 2501 Card Reader.
Class 2: Devices that require channel service to be in synchronization with their mechanical operations. For example, the IBM 2540 Card Read Punch has a fixed mechanical cycle. Delay in channel service for such devices usually occasions additional delay because of synchronization lag.

Class 3: Devices that do not require synchronized channel service; for example, the IBM 2660 Display Station with a 2848 Display Control. An IBM 1443 Printer is another device that does not require synchronized channel service; it can begin printing as soon as its buffer is full and line spacing is completed. Any loss of performance by devices in this class is limited to that caused by channel delay in providing service.

Devices in the first class need the highest priority. The devices in the last two classes may operate with reduced performance on an overloaded channel but are not subject to overrun. Their control units have data buffers or an ability to wait for channel service. Devices in the second class, however, should have higher priority than those in the third class.
Within each class, devices are assigned decreasing priority in the order of their increasing wait-time factors; smaller wait-time factors should have higher priority. Wait-time factors are listed in Appendix A and B.
When devices that operate only in burst mode, such as magnetic-tape or disk-storage devices, are attached to the byte-multiplexer channel, they should have lower priority than byte-mode devices. Low-priority devices take longer to respond to selection than do higher-priority devices; a burst-mode device need be selected only once for an operation, but a byte-mode device must be selected for the transfer of each byte, or a short burst, of data.
The control unit determines whether a device operates on the byte-multiplexer channel in burst mode or in byte mode.
Some devices, such as the IBM 2821 Control Unit, can operate on a byte-multiplexer channel in either burst mode or in byte mode, as determined by the setting of a manual switch on the control unit's customer engineer panel.
Such devices are assigned priority on the byte-multiplexer channel according to the mode of operation selected.

A byte-multiplexer channel can transfer data most rapidly in burst mode. Where an application uses only class 2 or 3 devices that have the mode choice, improved byte-multiplexer-channel efficiency can be obtained by operating the devices in burst mode.
The support processor and the integrated consoles are connected through the byte-multiplexer channel and have the lowest priority. Other byte-multiplexer channel activity may cause interference with these devices.

## Interference from Priority Devices

The byte-multiplexer channel sustains concurrent operations in byte mode by servicing one device at a time.
The operating devices compete for service, and the byte-multiplexer channel services then in the order of their priority.
Devices on the block-multiplexer channels or higher-priority devices on the byte-multiplexer channel can force lower-priority, byte-mode devices to wait for channel service. The former are called priority devices, and the latter waiting devices.
When a priority device forces a waiting device to wait for channel service, the priority device is said to interfere with the lower-priority device.
When there is more than one priority device, each of the priority devices may generate interference. All such interference must be considered in determining whether the waiting device is to receive channel service before its wait time is exceeded.
The test procedures for concurrent operation of byte-mode devices assume that a waiting device has made its request for channel service at the worst possible time; that is, when the priority devices cause maximum interference during the waiting device's wait time.
The channel ordinarily works its way through the interference, and the waiting device is unaffected by the wait. If, however, heavy interference forces the waiting device to wait past its particular wait time, it is subject to overrun.

## Priority Loads

To evaluate the effect of priority-device interference on a waiting device, a numeric priority load is computed.
Three factors determine a priority load:

1. The control load caused by execution of CCWs including chaining and transfer-in-channel operations.
2. The priority device's data-transfer load.
3. The wait time of the device being evaluated.

Note that because a priority load is a function of wait time, a fixed priority load cannot be established for a priority device; the priority load caused by a priority device must be computed as a function of a particular waiting device's wait time.

## Ranges of Wait Times

The relationship between the interference generated by a priority device (expressed as priority load) and various wait times is shown in Figure 6. The abscissa relates to device wait times. The short wait time shown results in a heavy priority load; the longer wait time falls in a part of the curve showing much less priority load. This curve shows that the impact of a priority device on a waiting device is more intense for a waiting device with a short wait time than it is for a device with a long wait time.

Two factors, called $A$ and $B$, relate each device's priority load curve to different wait times. The priority load curve was considered in segments related to different time intervals, and an $\mathbf{A}$ and a $\mathbf{B}$ factor were computed for


Figure 6. Priority Load Curve
each curve segment. These factors are used to compute the priority load for a waiting device having a wait time that falls within the range of the interval established for the curve segment.
The values of the A and B factors in Appendix A and B need to be modified if any block-multiplexer channel is active. The A1, A2, and B1 factors are used to modify the given time ( T ), A, and B factors by the formula:

$$
\begin{aligned}
& \mathrm{A}(\text { modified })= \mathrm{A}+(\mathrm{A} 1 \times \mathrm{n})-\left(\mathrm{A} 2 \times \mathrm{n}^{2}\right) \\
& \mathrm{B}(\text { modified })= \mathrm{B}+(\mathrm{B} 1 \times \mathrm{n}) \\
& \mathrm{T}(\text { modified })= \text { (difference of modified } \mathrm{A} \text { values for previous and present } \\
& \text { lines) divided by (difference of modified } \mathrm{B} \text { values for } \\
& \text { previous and present lines) } \\
& \mathrm{n}=\text { number of active block-multiplexer channels. }
\end{aligned}
$$

Multiple A and B Factors: The appendixes list the A and B factors for each 4341 Class 1 input/output device.
Some devices have only one set of A and B factors. Other devices have more than one set. Each set has an associated priority time factor that represents the beginning of the time interval over which the $A$ and $B$ factors are effective.

Priority Time Factors: The priority time factors in Appendix A or B are used in the evaluation procedure to identify the A and B factors to be used.
Each waiting device is evaluated on a byte-multiplexer channel worksheet; its wait time is used to select a set of A and B factors for each priority device.
Each set of A and B factors in Appendix A or B has a priority time factor next to it that specifies the beginning of a time interval significant to that set of A and B factors. The range extends from the priority time factor specified for that set to the priority time factor specified for the next set, if any. The end of the last interval is assumed to be unbounded. For example, a device may have three sets of A and B values that describe the priority load function over three contiguous intervals. Figure 7 shows the priority time factors and $\mathbf{A}$ and B factors as they appear in Appendix A or B for an IBM 1442 Card Read Punch Model N1 reading EBCDIC.


Figure 7. Use of Priority Time Factors

## Priority Load Formula

The A and B factors and wait-time factors in Appendix A and B are used in a formula that yields the priority load that occurs when a priority device interferes with a waiting device.
The sum of the B factor and the quotient obtained by dividing the A factor by the wait-time factor of the waiting device is the priority load. The arithmetic looks like this:

$$
(\mathrm{A} \div \text { wait time })+\mathrm{B}=\text { priority load }
$$

A-Factor Interference: A-factor interference is caused by channel microprogram activity, such as command chaining, for the priority device. The duration of this type of interference is significant compared with typical wait times. Therefore, the priority load, being expressed as a percentage of wait time, depends on the wait time of the waiting device. For example, if a waiting device's wait time is 0.20 millisecond and the microprogram activity associated with the priority device lasts for 0.10 millisecond, then the priority load is 50 percent. (In the channel evaluation factor tables, the $\mathbf{A}$ factors are expressed in milliseconds multiplied by 100 . In the foregoing example, the A factor associated with a microprogram activity lasting 0.10 millisecond is therefore: $0.10 \times 100=10.00$.)
Figure 8 shows how A-factor interference varies with the wait time of the waiting device.

B-Factor Interference: B-factor interference is typically caused by data transfers to and from the priority device. As shown by the example in Figure 9 , the duration of each data transfer is short compared with typical wait times. The data transfers occur frequently enough, however, to have a total effect that can be expressed as a percentage interference, namely, the B factor, that is constant for all wait times.


* The A-factor given in the channel evaluation factor tables (in the appendixes) is the duration of interference in milliseconds multiplied by 100. If the duration of interference is 0.10 millisecond (as shown in the illustration), the A-factor is $0.10 \times 100=10.00$. Thus, for a waiting device having a wait time of 0.2 millisecond, the interference is obtained directly as a percentage:

$$
\frac{\text { A-Factor }}{\text { Wait Time }}=\frac{10.00}{0.2}=50 \%
$$

Figure 8. Example of Priority Device Causing Interference by Command Chaining (A-factor Interference)


Figure 9. Example of Priority Load Curve of a Priority Device Causing Interference by Transferring Data (B-Factor Interference)

A and B Factors Combined: In actual I/O operations, the pattern of interference tends to be more complex than has been suggested by the example priority load curves in Figures 8 and 9. Usually, the A and B factors are both nonzero, and the total priority load of a priority device is given by:

Priority Load $=\left[\frac{A}{\text { Wait time }}+B\right] \%$
where the wait time is that of the waiting device.

Multiple A and B Factors: Some devices have only one set of A and B factors but others have more than one set; see the tables in the appendixes. In these tables (as shown in Figure 10), the A and B factors have priority time factors associated with them that show the ranges of wait times (of waiting devices) for which the A and B factors are valid. Figure 10 also shows how to choose the appropriate $A$ and $B$ factors according to the wait time of a waiting device. (The A and B factors for integrated adapters vary, depending upon the channel command. The figures given in the appendixes are representative of worst case interference for a typical channel command sequence.)


## Example 1

When considering the priority load of a 2520 Card Read Punch Model B1, (that is reading or punching EBCDIC) upon a waiting device that has a wait time of 1.00 ms , use the following priority load factors:

$$
A=0.00 \text { and } B=100.00 \text { (because } 1.00 \mathrm{~ms} \text { is the range } 0.10 \mathrm{~ms} \text { to } 2.15 \mathrm{~ms} \text { ) }
$$

## Example 2

Similarly, for a waiting device that has a wait time of 10.00 ms , use the foliowing priority load factors:
$A=214.77$ and $B=0.00$ (because 10.00 ms is in the range 2.15 ms to 24.78 ms )
Figure 10. Examples Showing How to Choose Priority Load Factors

## Previous Load

A waiting byte-mode device may be forced to wait for channel facilities, not only by devices with higher priority, but also by a device with lower priority that is in operation when the waiting device requests channel facilities. This interference is called a previous load and must be added to the priority load caused by priority devices. Previous load factors are calculated for each device by using the formula:

Previous Load $=[13.0+(2.5 \times n)] \div W T$
$\mathrm{n}=$ number of active block-multiplexer channels.
$\mathrm{WT}=$ wait time of the device.

Several load factors relating to byte-mode operations have been described:
Device load (contributed by waiting device)
Priority load (contributed by each priority device)
Previous load (contributed by a lower-priority device)
These loads added together form a load sum for each waiting device. The load sum represents the total load on system channel facilities under a worst-case condition when:

1. All priority devices are causing maximum priority loads.
2. Any lower-priority device, already in operation, is making maximum demands on channel facilities (previous load)
3. The waiting device places its maximum device load on channel facilities.

A step-by-step procedure for computing load sums is given in "Byte-Mode Evaluation Procedure."

## Byte-Mode Channel Load Limit

A numeric factor of 100 is considered the byte-mode channel load limit. If a load sum exceeds 100 , overrun is indicated during worst-case situations.

## Byte-Mode Evaluation Procedure

The following step-by-step procedure is used with a IBM 434 I Processor Byte-Multiplexer Channel Preliminary Worksheet (GX24-3746), shown in Figure 11, and a IBM 4341 Processor Channel Load Sum Worksheet (GX24-3670), shown in Figure 12.
Most of the steps call for an entry to be made on a worksheet. Each circled number shown on the worksheets in Figures 13 and 14 refer to the numbered step in the following procedures. For example, a circled number 1 is shown at the top of the worksheet in each of the two spaces that receive the entries called for by step 1. As an additional aid for where entries are made on a worksheet, see Figures 15 and 16 which show worksheets that have been completed for a configuration specified in "Worksheet Example."
1




Figure 12. Sample 4341 Processor Channel Load Sum Worksheet
)
Figure 13. Example of Preliminary Worksheet Entries


Figure 14. Example of Final Worksheet Entries

## Preliminary Worksheet Example

This procedure uses the IBM 4341 Processor Byte-Multiplexer Channel Preliminary Worksheet (GX24-3746).

1. Enter the system identification and the date.
2. This item contains instructions for the calculation of the values $\mathrm{N}_{\mathrm{d}}, \mathrm{N}_{\mathrm{p}}$ and $\mathrm{M}_{\mathrm{p}}$ for the byte-multiplexer channel preliminary and Load Sum worksheets.
In these calculations, $\mathrm{N}_{\mathrm{d}}$ is the value used to calculate device load, $\mathrm{N}_{\mathrm{p}}$ is the value used to calculate previous load and the A and B factors, and $\mathbf{M}_{p}$ is the value used to calculate previous and prior load on the Load Sum worksheet.
These values are shown on the following charts:
$\mathrm{N}_{\mathrm{d}}=$ The number of active block-multiplexer channels, plus 1.0 if the other byte-multiplexer channel is active, plus .4 for each channel that is data chaining out of a file gap.
$\mathrm{N}_{\mathrm{p}}=$ The number of active block-multiplexer channels with high data rate, plus .4 for each block-multiplexer channel with high data rate that is data chained when not in a file gap, plus 1.4 if the other byte-multiplexer channel is also active, plus .6 if the other byte-multiplexer channel is active and data chaining.

## $\mathrm{M}_{\mathrm{p}}=$

```
        18
        18-\Sigma EDR
```

Where $\Sigma$ EDR (Effective Data Rate) is the sum of the maximum EDR in megabytes per second of each block-multiplexer channel that is not included in $\mathrm{N}_{\mathrm{p}}$.
The EDR for each device on a block-multiplexer channel is equal to the Device Data Rate (DDR) if it is not being data chained, or:

```
(1 + 256) x DDR - if the device is being data-
    ---
    chained when not in a file gap
    CNT
```

Where CNT is equal to the smallest CCW count being used when data chaining.
The starting values for the preliminary and Load Sum worksheets are obtained from results derived from the following chart. To calculate $\mathrm{N}_{\mathrm{d}}$,
$N_{p}$, and $M_{p}$, refer to the following chart and steps a through i:
Sample chart completed for one byte-multiplexer channel on channel 0 , and a block-multiplexer channel on channel 4:

|  | $(1)$ | $(2)$ | $(3)$ | $(4)$ | $(5)$ | $(6)$ | (7) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Channel | Active | Chain Data | Byte Mpx | Max EDR | nd | $n p$ | Used EDR |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | $H$ | 1.0 | 1.0 | 0 |
| 2 | 1 | 1 | 0 | $H$ | 1.4 | 1.4 | 0 |
| 3 | 1 | 0 | 0 | $H$ | 1.0 | 1.0 | 0 |
| 4 | 1 | 0 | 0 | .333 | 1.0 | 0 | .333 |
| 5 | 1 | 1 | 0 | 1.800 | 1.4 | 0 | 1.800 |
| $M p=18-2.133$ |  |  |  |  |  |  |  |

Blank form for calculations:

|  | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Channel | Active | Chain Data | Byte Mpx | Max EDR | nd | np | Used EDR |
| 0 |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |  |

Only channel zero, and optionally channel four, can be configured as byte-multiplexer channels. First enter ' 0 ' in all seven columns of the chart for the byte-multiplexer channel being evaluated.
To arrive at columns 1 through 4 for the remainder of the channels:
a. Column 1 - Enter a ' 1 ' in the 'Active' column for each active channel, and a ' 0 ' in the 'Active' column for each inactive channel. If a zero appears in the 'Active' column, enter ' 0 ' in all remaining columns for that channel. .
b. Column 2 - Enter a ' 1 ' in the 'Chain Data' column for each active channel that is data chaining when it is not in a file gap; otherwise enter '0'.
c. Column 3-Enter a ' 1 ' in the 'Byte-MPX' column for the other byte-multiplexer channel (channel 0 or 4 ) if it is being being configured as a byte-multiplexer channel; otherwise enter ' 0 '.
d. Column 4 - Enter a ' 0 ' in the 'Max EDR' column for the other byte-multiplexer channel if it is configured as a byte-multiplexer channel.
The maximum EDR for a channel is determined by calculating an EDR for each device and selecting the maximum value.
Enter an 'H' if the effective data rate (EDR) is high, and will not be used to calculate load; otherwise enter the maximum EDR for each channel.
The EDR for a particular device is determined by the following:

```
If not data chaining or if EDR = Device Data Rate
data chaining in a file gap. (DDR)
If data chaining, when not EDR =(1+256) x DDR
in z file gap.
CNT
```

e. Columns 5 and 6 - To calculate a final value for $N_{d}$ and $N_{p}$, fill in the nd and np columns for each channel using the following chart:
Col 1 Col $2 \operatorname{Col} 3 \quad \operatorname{Col} 4=\operatorname{Col} 5 \operatorname{Col} 6$

| Act ive | Chain Date | Byte Mpx | Max EDR | nd | np |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | $H$ | 1.0 | 1.0 |
| 1 | 1 | 0 | $H$ | 1.4 | 1.4 |
| 1 | 0 | 0 | $L$ | 1.0 | 0.0 |
| 1 | 1 | 0 | $L$ | 1.4 | 0.0 |
| 1 | 0 | 1 | 0 | 1.0 | 1.4 |
| 1 | 1 | 1 | 0 | 1.4 | 2.0 |

f. Column 7 - If the np value in column 6 is ' 0 ', enter the maximum EDR from column 4 in the 'Used EDR' column 7; otherwise enter ' 0 '.
g. Sum the 'nd', 'np', and 'Used EDR' columns to obtain the $\mathbb{N}_{\mathrm{d}}, \mathbb{N}_{\mathrm{p}}$, and $\mathrm{\Sigma}$ EDR values.
h. Calculate:


The following table may be used as a guide to help determine whether to enter ' H ' in the maximum EDR column.
Find the column for the byte-multiplexer channel being evaluated. If the accumulative EDR for any number of active block-multiplexer channels exceeds the value given in the table, enter 'H' for those channels; otherwise enter the maximum EDR value.

Note: For accumulative $E D R$ close to the value in the table. it might be necessary to use both methods and then choose the one resulting in the lower Load Sum. $M_{\mathrm{p}}$ represents the interference of the block-mulitiplexer channels on the byte-multiplexer channel resulting from the EDR. However, this interference can never exceed the amount associated with mp, which represents the maximum possible interference.

For instance, assume there are a total of three active block-multiplexer channets with respective EDRs of $2.5,0.4$, and $2.0 \mathrm{Mb} /$ second, and the optional byte-multiplexer channel is configured. When channel 0 is evaluated, the accumulative EDR for the first and third block-multiplexer channel exceeds $3.9 \mathrm{Mb} /$ second, ' $H$ ' is entered for those channels. However, the accumulative EDR for all three block-multiplexer channels does not exceed $5.3 \mathrm{Mb} /$ second, so 0.4 is entered for the second block-multiplexer channel.

| ACCUMULATIVE EDR FOR PREVIOUS/PRIORITY LOAD CONSIDERATIONS (all values in $\mathrm{Mb} / \mathrm{sec}$ ) |  |  |  |
| :---: | :---: | :---: | :---: |
| Active Block Multiplexer Channels | Standard <br> Byte MPX Channel | Optional <br> Byte MPX Channels |  |
|  | Channel 0 | Channel 0 | Channe 14 |
| 1 | 2.7 | 2.2 | 2.8 |
| 2 | 4.7 | 3.9 | 4.8 |
| 3 | 6.2 | 5.3 | 6.4 |
| 4 | 7.4 | 6.5 | 7.6 |
| 5 | 8.4 | --- | --- |

If the device being calculated is a 3704 or 3705 operating in the Emulation programming mode, go to "IBM 3704/3705 Calculations" to calculate the values for the Load Sum worksheet for those devices.
i. Enter $N_{d}$ and $N_{p}$ on the preliminary worksheet, and $M_{p}$ on the Load Sum worksheet.
3. Arrange the byte-mode devices proposed for simultaneous operation in sequence by priority class ( 1,2 , and 3 ).
Class 1 devices that have an inseparable class 2 component should be included with the class 1 devices. Examples of such devices: 1442 and 2520-B1.
Enter the class 1 devices on the worksheet in any order.
Although class 2 and 3 devices can be delayed in some worst-case situations, they are not subject to overrun and need not be include in the overrun evaluation.
4. For each device entered in step 2 that is not a 3705, enter the Wait Time, Device Load, and D1 values, and the sets of Time, A, A1, A2, B, and B1 values. These values are obtained from Appendix A or B, depending on the multiplexer channel selected, 0 or 4 .
If the device is one of the following Class 2 or Class 3 devices, no information is given in Appendix A or B because these devices do not overrun.

| 1017 | 1018 | 1403 | $1442-\mathrm{N} 2$ | 1443 |
| :--- | :--- | :--- | :--- | :--- |
| 2250 | $2520-\mathrm{B} 2, \mathrm{~B} 3$ | 2540 | 2671 | 2715 |
| 3203 | 3211 | 3250 | 3277 | 3278 |
| 3284 | 3286 | 3287 | 3288 | 3289 |
| 3505 | 3525 | 3540 | 3791 | 3800 |
| 3881 | 3886 | 3890 | 3895 |  |

The following steps can be performed without referring to the tables. All the needed information is now recorded on the preliminary worksheet.
5. Compute the modified factors for each device by using the following formulas:

Device Load (modified) $=$ Device Load (original) $+\left(\right.$ D1 $\times \mathrm{N}_{\mathrm{d}}$
Previous Load (modified), except $3705=$
IF there is a slow device on byte-multiplexer channel 0
THEN use $\left[13.0+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div$ Wait time
ELSE use $\left[10.0+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div$ Wait time
Previous Load (modified), except $3705=$
IF there is a slow device on byte-multiplexer channel 4,
AND it is not the slowest, or last, device,
THEN use $\left[10.0+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div$ Wait time
ELSE use $\left[7.0+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div$ Wait time

## Notes:

1. The slowest, or last, device on channel 4 has a fixed previous value of 0 .
2. Slow devices are shown in Table C-2.

Previous Load (modified), $3705=$ Device Load (modified)
$A_{L}($ modified $)=A_{L}($ original $)+\left(A 1_{L} \times N_{p}\right)-\left(A 2_{L} \times N_{p}{ }^{2}\right)$
$B_{L}($ modified $)=B_{L}($ original $)+\left(B 1_{L} \times N_{p}\right)$
Time $_{1}($ modified $)=$ Time $_{1}($ original $)$
Time $_{2}$ (modified) $=\left[\mathbf{A}_{1}\right.$ (modified) $-\mathbf{A}_{2}$ (modified) $] \div\left[\mathrm{B}_{2}\right.$ (modified) $-\mathbf{B}_{1}$ (modified)]
Time $_{3}$ (modified) $=\left[\mathbf{A}_{2}\right.$ (modified) $-\mathbf{A}_{3}$ (modified) $] \div\left[\mathbf{B}_{3}\right.$ (modified) $-\mathbf{B}_{2}$ (modified)]
where:
$\mathrm{N}_{\mathrm{d}}, \mathrm{N}_{\mathrm{p}}=$ effective number of other active channels.
WT = wait time of selected device.
$\mathrm{L}=$ line number 1,2 , or 3 (preliminary worksheet).
6. Proceed to the "Channel Load Sum Worksheet Procedure."

## Channel Load Sum Worksheet Procedure

This procedure uses the IBM 4341 Processor Channel Load Sum Worksheet (GX24-3670).

1. Enter the system identification and date; enter the $\mathbf{M}_{\mathfrak{p}}$ value if not previously entered.
2. Arrange the devices entered on the preliminary worksheet according to increasing wait time. Devices with the smallest wait times are listed first (receive highest priority).
3. Copy the modified factors from the preliminary worksheet to the appropriate areas of this worksheet for each device.
4. For the second and each other waiting device on the byte-multiplexer channel, compare its wait time to the time factors given for each of the byte-multiplexer channel devices with higher priority. Enter the appropriate set of A and B factors (that is, the set that is on the same line with the largest time factor that is less than the wait time).
5. For each byte-multiplexer channel waiting device. add the selected A factors, and enter the A sum and B sum.
6. Divide the A sum by the wait-time factor for the device, and enter the quotient.
7. For each byte-multiplexer channel waiting device, add the B sum, the quotient found in step 6, the previous load, and enter this sum as the subtotal.
8. Calculate $\mathrm{M}_{\mathrm{p}}$ times the subtotal for each byte-multiplexer channel waiting device, and add this value and the device load and enter this sum as the Load Sum. The load sum must be less than, or equal to, 100 for satisfactory operation of the waiting device.

Worksheet Example

Channel 1
Channel 2
Channel 3
Channel 4
Byte-MPX
Channe

3330 Disk Storage, no data chaining

2420 Magnetic Tape Unit Model 7
$320 \mathrm{~Kb} / \mathrm{sec}$, no data chaining
2501 Card Reader Model B2
EBCDIC; 1288 Optical Page Reader, reading formatted alphameric

The completed worksheets (Figures 15 and 16) for the given configuration show satisfactory operation for all byte-mode devices. No load sum exceeds 100.

Figure 15. Example of Preliminary Worksheet with a 2501-B2 and a 1288



Figure 16. Example of Final Worksheet with a 2501 -B2 and a 1288

## IBM 3704/3705 Calculations

This step calculates the values for $3704 / 3705$ devices only. This series of steps provide the information to derive the necessary factors for the Load Sum Worksheet for 3704 and 3705 devices.

The set of numbers in parentheses in the Example Column are provided as examples of values that would be derived if the user has a 3705 II on byte-multiplexer channel 0 , with a type 2 scanner, and the device has two lines at 9.6 kilobits per second, and one line at 19.2 kilobits per second.

1. Enter the required data to calculate Wait Time values: Example Column
a. Check the appropriate device. 3704_3705I_3705I__(3705II)
b. Check the appropriate scanner No. 1 $\qquad$ 2 $\qquad$ 3 $\qquad$ ( 2 )
(If you have checked scanners 2 and 3, use scanner 2 only. For multiple scanners of the same type, use the most heavily loaded scanner for these calculations.)
c. Check cycle time in microseconds . $1.2 \ldots 1.0 \ldots$ ( 1.0 )
(If you have checked 3704 or 3705 I, check the value of 1.2).
2. If scanner 3 is checked, enter the buffer length if known, otherwise enter the value 4.

BFL $\qquad$ ( 4 )
3. If scauner 3 is checked, enter the channel transfer length if known, otherwise enter the value 4. CTL $\qquad$ ( 4 )
4. Enter the number of low speed lines (those less than 19,200 bits per second.) $\qquad$
5. Enter the speed of the fastest low speed line in kilobits per second.

LM $\qquad$ ( 9.6 )
6. Calculate the total low speed kilobits per second:
$1 T=E \cdot 1$
(where ${ }_{n!}$ is the number of lines at speed I, and I is line speed in kilobits per second, and $I$ is less than 19,200 bits per second.)
$1 T$ _ 19.2 )
7. Enter the number of high speed lines (those equal to of getuer than 19,200 bits per second).

NH $\qquad$ ( 1 )
8. Enter the speed of the fastest high-speed line in kilobis per second.

HM $\qquad$ ( 19.2 )
9. Calculate the total high speed kilobits per second

$$
H T=E a 1
$$

(where ${ }_{n}$ is the number of lines at speed I, and I is line speed in kilobits per second, and I is equal to or greater than 19.200 bits per second.)

HT $\qquad$ (19.2)

If the above $\mathrm{NH}=0$, continue to step A 1 , otherwise go to step A2

Step A1. This step calculates the Wait Time factor when no high speed lines are involved. Refer to Table D-2 for the required values.
From Table D-2, and using the scanner selection, cycle time specification, and buffer load values values from step 1 (previous page), determine the TA, TB, TC and TD values for the following lines:

TA $\qquad$
TB $\qquad$
TC $\qquad$
TD $\qquad$
Calculate $\mathrm{TE}=$
Low maximum $(\mathrm{LM})+[\mathrm{TC}$ value $\times$ Low total $(\mathrm{LT})]=\mathrm{TE}=$ $\qquad$
Calculate $\mathrm{TF}=$
$10-[$ TD value $\times$ Low total $(\mathrm{LT})]=\quad \mathrm{TF}=$
Calculate Wait Time $=$
$(\mathrm{TA} \div \mathrm{TE})-(\mathrm{TB} \div \mathrm{TF})=\quad$ Wait Time $=$
Note: If the device is a 3704, multiply the Wait Time by 0.9.
Proceed to Step B1.

Step A2. This step calculates the High Wait Time value where high speed lines are involved. Refer to Table D-2 for the required TB and TD values.

| Example |
| :---: |
| Column |
| TB $-(.830)$ |

$\mathrm{TD} \longrightarrow \quad$ (.0406 $)$

From Steps 2 through 9:

$$
\begin{equation*}
\text { Calculate total } \mathrm{KB}=\mathrm{LT}+\mathrm{HT}=\mathrm{TKB} \quad \mathrm{TKB}= \tag{38.4}
\end{equation*}
$$

To calculate NHM:

$$
\begin{align*}
& \text { If } \mathrm{NL}=0, \mathrm{NHM}=\mathrm{HM} \times \mathrm{NH} \\
& \text { or } \\
& \text { If } \mathrm{NL} \neq 0, \mathrm{NHM}=\mathrm{HM} \times(\mathrm{NH}+1) \tag{38.4}
\end{align*}
$$

$\mathrm{NHM}=$ $\qquad$
To calculate the Critical Time (CH) for high speed lines:
If $\mathrm{NL}=0, \mathrm{CH}=8 \times \mathrm{BFL} \div \mathrm{NHM}$
or
If $\mathrm{NL} \neq 0, \mathrm{CH}=8 \times(\mathrm{BFL}+1) \div \mathrm{NHM}$
$\mathrm{CH}=$ $\qquad$ ( 1.04 )

To calculate TF:
If $\mathrm{NH}=1, \mathrm{TF}=10$
or
If $\mathrm{NH} \neq 1, \mathrm{TF}=10-(\mathrm{TD} \times \mathrm{TKB})$
$\mathrm{TF}=$ $\qquad$ ( 10 )

Then calculate:
High Wait Time $=\mathrm{CH}-(\mathrm{TB} \div \mathrm{TF})=$ High Wait time $=$ $\qquad$ (.957)

If $\mathrm{NL}=0$, enter the value for High Wait Time (times 0.9 if 3704 was checked) as the Wait Time at the end of Step A3, and proceed directly to Step B1.

If $N L \neq 0$, do step A3 to derive the Low Wait Time value.

Step A3. This step calculates a value of Low Wait Time for a combination of both High Speed and Low Speed lines.

Example
Column
Calculate IA:

$$
\mathrm{A}=.575 \times \mathrm{LM} \div(\mathrm{BFL}+1)
$$

$\mathrm{IA}=$ $\qquad$ ( 1.10 )

Calculate IB:

$$
\mathrm{IB}=\mathrm{TKB} \div(16 \times \mathrm{BFL})
$$

$$
\mathrm{IB}=
$$

$\qquad$ (. 600 )

Calculate IC:

$$
\mathrm{IC}=\mathrm{HT} \div(16 \times \mathrm{BFL})
$$

$\mathrm{IC}=$ $\qquad$ (. 300 )

Calculate ID:

$$
I D=I B+I C+I A
$$

$$
\mathrm{ID}=
$$

$\qquad$ ( 2.00 )

Calculate IE:

$$
\begin{equation*}
I E=\quad \sqrt{I D^{2}-(4 \times I B \times I C)} \tag{1.81}
\end{equation*}
$$

$$
\mathrm{IE}=
$$

$\qquad$
To calculate the Critical Time (CL) for Low Speed Lines:

$$
C L=(I D-I E) \div(2 \times I B \times I C)
$$

$\mathrm{CL}=$ $\qquad$ (. 528 )

To calculate Low WT:

$$
\text { Low } \mathrm{W} T=\mathrm{CL}-(\mathrm{TB} \div \mathrm{TF})
$$

Low WT = $\qquad$ (. 445 )

For this step final result Wait time, enter the value of High
Wait Time calculated in step A2, or this step's calculated
Low Wait Time, whichever is the lower value.
If the 3704 device had been checked in step A1, multiply this page final value by 0.9 .

Wait Time $=$ (.445)

Step B1. From steps 1 through 6 of the "Preliminary Worksheet Example," enter the values for $\mathrm{Nd}, \mathrm{Np}$ and Mp .


Use the CTL value and the table below to derive the device factor (DF).

|  | CTL $=4$ | CTL $=8$ | CTL=16 | CTL=32 |
| :--- | :---: | :---: | :---: | :---: |
| Channel 0 | 8.1 | 8.7 | 9.9 | 12.3 |
| Channel 4 | 5.2 | 5.8 | 7.0 | $9.4 \quad$ DF $=\square$ |
|  |  |  |  |  |

Calculate bursts per transfer $=$
$\mathrm{BFL} \div \mathrm{CTL}$
$M B=-\quad\left(\begin{array}{l}1\end{array}\right)$
To calculate service time (TS).

$$
\begin{equation*}
\mathrm{TS}=\mathrm{DF}+\left(1.4 \times \mathrm{N}_{\mathrm{p}}\right) \tag{13.7}
\end{equation*}
$$

$T S=$ $\qquad$
To calculate Device Load:

$$
\begin{array}{r}
\mathrm{DL}=\left[\left[\mathrm{DF}+\left(2.4 \times \mathrm{N}_{\mathrm{f}}\right)\right]+\left[\mathrm{M}_{\mathrm{p}} \times(\mathrm{NB}-1) \times \mathrm{TS}\right]\right] \div \mathrm{WT} \\
\mathrm{DL}= \tag{39.8}
\end{array}
$$

For channel 0 , if there are no slow devices, then:

$$
P L=\left[10+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div \mathrm{WT}
$$

otherwise

$$
P L=\left[13+\left(1.75 \mathrm{x} \mathrm{~N}_{\mathrm{p}}\right)\right] \div \mathrm{WT}
$$

For channel 4, if there are no slow devices, then:

$$
P L=\left[7+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div \mathrm{WT}
$$

otherwise

$$
\begin{equation*}
P L=\left[10+\left(1.75 \times \mathrm{N}_{\mathrm{p}}\right)\right] \div \mathrm{WT} \tag{44.9}
\end{equation*}
$$

PL $=$
Proceed to Step B2.

Step B2. If no lower priority over-runnable devices than the 3704/3705 exist on the channel, priority Load factors need not be calculated; proceed directly to the Load Sum Worksheet. Otherwise, calculate the Load Factor values below.

## Example

Column
To calculate TSN:

$$
\mathrm{TSN}=\mathrm{TS} \times \mathrm{NB} \quad \mathrm{TSM}=\ldots
$$

Calculate and enter the priority Load Factor on the Load Sum Worksheet as follows:

$$
\begin{align*}
& \text { Time }_{1}=0.100 \\
& B_{1}=100.000 \\
& A_{1}=0.000 \\
& \mathrm{Time}_{2}=0.2 \times \mathrm{TSN} \\
& \mathrm{~B}_{2}=(10 \times \mathrm{TSN}) \div[(.1 \times \mathrm{TSN})+\mathrm{TB}] \\
& \mathrm{A}_{2}=\mathrm{Time}_{2} \times\left(100-\mathrm{B}_{2}\right) \\
& \text { Time }_{2}= \\
& \text { (. } 274 \text { ) } \\
& B_{2}= \\
& \text { ( 62.27) } \\
& A_{2}= \\
& \text { ( } 10.34 \text { ) } \\
& \text { Time }_{3}=(\mathrm{NH}+\mathrm{NL}) \times[(.01 \times \mathrm{TSN})+(.1 \times \mathrm{TB})] \text { Time }_{3}=\ldots \quad(.660) \\
& B_{3}=[(L T+H T) \times T S N] \div(8 \times B F L) \\
& B_{3}= \\
& \text { —— } \\
& \text { ( } 16.44 \text { ) } \\
& A_{3}=A_{2}+\left[\text { Time }_{3} \times\left(B_{2}-B_{3}\right]\right. \\
& A_{3}= \tag{40.59}
\end{align*}
$$

Proceed to the "Channel Load Sum Worksheet Procedure;" enter the Device Load, Previous Load and Priority Load factor values.

Appendix A. Evaluation Factors for Channel 0

| ¢ |  |  | $\begin{aligned} & \text { Oinn } \\ & \text { Oin } \\ & \underset{\sim}{n} \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| ※ |  | 8\%Non | 응№ |
| - |  |  | O-N min min |
| $\begin{array}{l\|l} \frac{\lambda}{2} & \infty \\ \frac{\partial}{0} & \end{array}$ |  |  |  |
| 2 $<$ |  |  |  |
| $\stackrel{\otimes}{\stackrel{\rightharpoonup}{E}} \stackrel{\square}{\square}$ |  |  |  |
| $\bar{\square}$ |  | ñ | $\begin{aligned} & \text { Na } \\ & \text { n } \end{aligned}$ |
|  |  | $\stackrel{\infty}{\sim}$ | $\stackrel{\sim}{\sim}$ |
|  |  | - | - |
|  |  | 은 | $\infty$ |
|  |  | $\stackrel{m}{m}$ | 운 |
| $\stackrel{\text { ® }}{\stackrel{\otimes}{\otimes}}$ |  | $\Sigma$ | $\Sigma$ |
|  |  | $\begin{aligned} & \bar{\sim} \\ & \bar{\sim} \\ & \bar{\sim} \\ & \stackrel{0}{0} \\ & \frac{0}{2} \end{aligned}$ |  |



[^2]Table A-1. Channel Evaluation Factors-1255 and 1287

| $\bar{\infty}$ |  <br>  <br>  |
| :---: | :---: |
| $\underset{\sim}{\sim}$ |  NゥJルMNNーーーーーOOO 000000000000000 |
| － |  mmommmonunn ono－N <br>  コココココココココココココココ |
| $\begin{array}{l\|l} \lambda & \\ \hdashline \stackrel{\pi}{\circ} & \infty \\ \hline 1 \end{array}$ |  <br>  NNJいMNNーーーーー |
| $\ll$ |  NヘコNNOーNMmmJコココ <br>  NNNNNNNNNNNNNNN |
| $\stackrel{\otimes}{\stackrel{ \pm}{E}}$ | 응ㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇ |
| $\overline{0}$ | ○○○ーの○mNJのコー <br>  NNー－ |
| $\begin{aligned} & 0 \\ & \cup \\ & \hdashline> \\ & \hline \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ |  <br>  <br>  |
|  | 000000000000000 <br>  <br>  |
|  | $\frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi} \frac{1}{\pi}$ $\ggg \ggg \ggg \ggg \ggg$ |
|  |  |
| $\underset{\text { ¢ }}{\substack{\text { ¢ }}}$ | $\Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma \Sigma$ |
|  |  |



[^3]Table A－2．Channel Evaluation Factors－1288 and 1419

| $\infty$ | 000000 OOOJOO 000000NOONOO onoomonoonoo $m \dot{m}$ |
| :---: | :---: |
| $\underset{\sim}{\sim}$ | $0 \rightarrow \infty 0 \infty \infty 000000$ ○小N0小NーOO－OO 000000000000 |
| $\underbrace{0}_{10} 8$ | OMLOMO－OOMOO <br>  Nonnivaoosoo - Jー J J |
| $\begin{array}{l\|l} \underset{\sim}{2} & \\ \hdashline- & \infty \\ \vdots & \end{array}$ | ONMONJNOOMOO <br>  ownonunoonoo oi＝$\dot{N} \dot{\sim}-$ |
| 童 | すのびールー○○の○。 の－omanmoonoo $\infty M \sim \infty \sim \omega \infty$ OOJOO ヘiNNNNN N |
| $\stackrel{@}{E}$ | OJのOMLIOOOOOO omnomaooogoo <br>  |
| $\overline{0}$ | $\begin{array}{llll} 0 & 0 & 0 & 0 \\ 0 & 0 & m & M \\ 0 & 0 & J & J \\ 0 & 0 & 1 & \end{array}$ |
| 0 $U$ $\cdots$ $>$ 0 0 0 0 | $\begin{array}{cccc} 0 & J & m & N \\ \sim & \infty & \infty & N \\ N & \dot{N} & - & \cdots \\ \sim & N & & \end{array}$ |
|  | $\begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & 0 & 8 & 0 \\ 0 & 0 & 0 & 0 \\ & & - & - \end{array}$ |
| $\begin{aligned} & \frac{\otimes}{U} \stackrel{\otimes}{E} \underset{E}{~} \\ & \underset{\sim}{E} \end{aligned}$ | $\begin{array}{llll} 0 & 0 & 0 & 0 \\ n & n & n & i n \\ - & - & 0 & 0 \end{array}$ |
|  | $\cdots \begin{array}{cc}\text { in } & \cdots \\ \cdots & \sim \\ \cdots\end{array}$ |
| $\xrightarrow{3}$ | $\Sigma \Sigma \Sigma$ |
|  |  |


| $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $0-0$ 0 0 <br> 0 0 $-\infty$ <br> 0 0 0 <br> 0 0 0 <br> $i$ 0 $\infty$ <br> $n$ $n$ $n$ |
| :---: | :---: |
|  |  |
|  | ○～○ 0 o in o <br>  <br>  |
|  | OnON OnON ONON ONON． $\because$ の - の |
|  |  |
|  |  |
| $\overline{0}$ |  |
| $\begin{array}{ll} 0 \\ U & \\ \hdashline & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \end{array}$ | $\begin{array}{cccc} N & J & N & J \\ N & N & N & \underset{N}{N} \\ \underset{N}{N} & \dot{J} & \underset{N}{N} & \dot{J} \end{array}$ |
|  | $\frac{n}{\sigma} \frac{n}{\sigma} \quad \frac{n}{\sigma} \quad \frac{n}{\sigma}$ |
|  | $\begin{array}{llll} \circ & 0 & 0 & 0 \\ 0 & 0 & 6 & 1 \end{array}$ |
|  |  |
| $\underset{\underset{\sim}{\otimes}}{\substack{2}}$ | $\Sigma \Sigma \Sigma$ |
|  |  |

[^4]Table A－3．Channel Evaluation Factors－1442 and 2501 B1 and B2


Table A-4. Channel Evaluation Factors-2520

| $\bar{\infty}$ | $\begin{aligned} & -2 \\ & 00 \\ & 00 \end{aligned}$ | $\begin{aligned} & \vec{\infty} \\ & 0 \\ & \hline \end{aligned}$ | $$ | $\frac{N}{0}$ | 응웡 | $\frac{J}{0}$ | $\begin{aligned} & \circ \\ & 8 \\ & \hline 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 응ㅇㅇㅇ } \\ & \text { NMJ } \end{aligned}$ | inooooroo <br>  | －060006 <br> $\checkmark \infty \infty 0 \infty$ No <br> －NJルJル joi= |  | $\begin{aligned} & 000 \\ & \text { a } \\ & \sim N \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| N | $\cdots m$ | $\begin{aligned} & \text { m } \\ & \hline 0 \end{aligned}$ | $8=$ | $\begin{aligned} & 0 \\ & 8 \\ & \hline \end{aligned}$ | $\begin{aligned} & 880 \\ & 888 \\ & \hline 80 \end{aligned}$ | $8$ | $88$ | 응ㅇN N |  |  | mín | $\begin{aligned} & \text { ta } \\ & 0 . \frac{1 r}{6} \frac{\infty}{0} \end{aligned}$ |
| 1  <br> 10  <br> 0  <br> 0  | $\begin{aligned} & \mathbb{J} \\ & \underset{\sim}{n} \end{aligned}$ | $\begin{aligned} & \underset{\sim}{\mathrm{N}} \\ & \mathrm{~m} \end{aligned}$ | $\begin{array}{ll} \sigma & \infty \\ 5 & \\ 0 & 0 \\ \mathrm{n} \\ \mathrm{~min} \end{array}$ | $\begin{aligned} & 0 \\ & \underset{\sim}{\mathbf{n}} \end{aligned}$ | 今ペo $\mathrm{mmm}$ | $\begin{aligned} & 0 \\ & \text { } \\ & \mathrm{m} \end{aligned}$ | $$ | ○MNN6 かざNさN mmmn | $\infty \times m \sim M m N J$ <br>  <br> $m m m m \sim N$ |  | $\infty 6 \mathrm{mNm}$ <br> $=\infty$ <br> mimmin |  |
| 立 | 의 | $0$ | $\begin{gathered} \infty \\ \Gamma \\ \end{gathered}$ | $\begin{aligned} & n \\ & 0 \end{aligned}$ | Jin | $\hat{O}$ | す̂ | on $n \infty m$ in の $60 \infty$ $--n m$ |  テのぃののがN ーーmiñ | மNO <br> 6mN๒－$\infty$ on <br> ーNNーコ寺 |  |  |
| $4$ | 的志 <br> 以 | $\begin{aligned} & \text { in } \\ & N \\ & \hline 1 \end{aligned}$ |  | $\begin{aligned} & 0 \\ & 10 \\ & n \\ & n \end{aligned}$ | 응 0 $n$ in in | $\begin{aligned} & 0 \\ & 0 \\ & n \\ & n \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & n \\ & n \\ & n \end{aligned}$ |  niningo |  ninininimoó |  ninnin $n \rightarrow$ | ○かべニ जinwin | mmon 6 Ls mm以 |
| $\stackrel{\text { E }}{\stackrel{1}{\square}}$ | $88$ | $8$ | $8 \text { 응 }$ | ㅇ | 응ㅇㅇ | 응 | ㅇㅇ | ㅇㅇㅇㅇㅇㅇㅇ | 응ㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇ | 응ㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇ은 | $\begin{aligned} & \circ 8898 \\ & \text { 으으은 } \end{aligned}$ | $8898$ |
| $\overline{0}$ | す！ | $\pm$ | $\underset{\sim}{\infty} \mathrm{N}$ | O | Nõo | m | Nom |  | ののーが№Nさ OーMMNのMN |  |  | ¢ |
| $\begin{aligned} & 0 \\ & \vdots \\ & \hdashline 0 \\ & >0 \\ & 0 \\ & 0 \end{aligned}$ | さ． | No | $\begin{aligned} & \sigma \operatorname{m} \\ & 0- \\ & -N \end{aligned}$ | $\infty_{0}^{\infty}$ | 용․ | ־ | ¢． | $\infty \infty \times 0$ <br> －Ninin in |  |  －injoi | ทin oño －civis |  |
|  | $\begin{aligned} & 88 \\ & \text { iO } \\ & \text { m } \\ & \text { w } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0 \\ & 2 \\ & 1 \end{aligned}\right.$ | $\begin{aligned} & 8 \text { 8 } \\ & \text { m } \\ & \infty \text { j } \end{aligned}$ | $\begin{aligned} & \text { O} \\ & \text { n. } \\ & \text { m } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 옹ㅇ } \\ & \text { M응 } \\ & \text { 士nio } \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & \infty \\ & \text { in } \\ & \infty \end{aligned}$ | $\begin{aligned} & \text { 응 } \\ & \underset{\sim}{\infty} \\ & \infty \\ & \underset{\sim}{\infty} \\ & \hline \infty \end{aligned}$ |  | ㅇㅇㅇㅇㅇㅇㅇㅇ으응 かoNㅓ№mm ninim N－ | 응ㅇㅇㅇㅇㅇ Nぃト 0 NN ginis | $\begin{aligned} & \text { 응ㅇㅇ } \\ & \text { No응․ } \\ & \text { jr jmi... } \end{aligned}$ | $\begin{aligned} & 8888 \\ & 808 \\ & \text { gnm } \end{aligned}$ |
| $\begin{array}{ccc} 10 & 0 & 0 \\ 10 & 0 & 0 \\ 10 & 0 & 0 \end{array}$ | $\begin{aligned} & 00 \\ & \infty \\ & \pm 0 \\ & \hdashline i n \end{aligned}$ | $\begin{aligned} & 8 \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \circ 8 \\ & 00 \\ & 00 \\ & \end{aligned}$ | $\underset{m}{n} \underset{\infty}{m} .$ | 응응 ono | ㅇ | $\begin{aligned} & 08 \\ & 60 \\ & \text { oo } \end{aligned}$ |  | ㅇㅇㅇㅇㅇㅇㅇㅇ － noㅇoㅇoㅇㅇ nininoo으눈 Nin |  | $\begin{aligned} & 08888 \\ & 0888 \\ & \text { wig88 } \\ & n M m 0 \end{aligned}$ | $\begin{aligned} & 8888 \\ & 88 m 8 \\ & 88 \mathrm{~m} \end{aligned}$ |
| $\frac{0}{\infty} \frac{\tilde{m}}{\infty} \underset{\infty}{\infty}$ | $\begin{aligned} & 78 \\ & m 8 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 . \\ & 0 . \end{aligned}$ | $\begin{aligned} & 00 \\ & 00 \\ & 00 \\ & 0 . \end{aligned}$ | $\begin{aligned} & 0 \\ & i n \end{aligned}$ | $\begin{aligned} & n 9 N \\ & \text { in } \end{aligned}$ | $\begin{aligned} & 0 \\ & \underline{0} \end{aligned}$ | $\begin{aligned} & 00 \\ & \text { in } \end{aligned}$ |  | 000000000 －000000000 응엉Nㅇㅇㅇㅕ －Nへのか○。 －寸in | 00000000 ㅇㅇㅇㅇㅇㅇㅇ OOOOOOOO <br>  －NNOTin | $\begin{aligned} & 00000 \\ & 08880 \\ & 0.888 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 0000 \\ & 8880 \\ & 6880 \\ & 0.0 \end{aligned}$ |
| ? |  |  | － <br> $\overline{0}$ 1 $\vdots$ 0 0 <br>  <br> $\sum_{\infty}$ | 1 <br> $\pm$ <br> 0 <br> 0 <br> 0 <br> 0 | $\begin{aligned} & \text { Telegraph Adapter } \\ & \text { Type । } \end{aligned}$ | $\begin{aligned} & = \\ & \stackrel{\sim}{\alpha} \\ & \stackrel{\lambda}{\lambda} \end{aligned}$ |  |  |  |  |  |  |

Tabie A－5．Channel Evaluation Factors－2701


Table A-6. Channel Evaluation Factors--7770

Appendix B. Evaluation Factors for Byte Multiplexer Channel 4

| $\bar{\infty}$ |  |  |  |
| :---: | :---: | :---: | :---: |
| $\underset{\sim}{2}$ |  |  | 8\%®̃ |
| - |  | 앙으N m-m $\dot{m}$ |  |
| $\begin{array}{l\|l} \frac{\pi}{2} & \infty \\ \frac{1}{0} & \infty \end{array}$ |  | $8 \underset{\sim}{0 . n}$ | $\underset{\sim}{8-\mathrm{m}}$ |
| $\stackrel{\circ}{\circ} \mathrm{C}$ |  |  |  |
| $\stackrel{ \pm}{E}$ |  |  |  |
| $\overline{0}$ |  | $\begin{aligned} & \underset{\sim}{n} \\ & \dot{n} \end{aligned}$ | $\begin{aligned} & \stackrel{\sigma}{n} \\ & \underset{\sim}{n} \\ & m \end{aligned}$ |
|  |  | ㅇ. $=$ $=$ | 으﹎ $=$ |
|  |  | - | - |
|  |  | $\stackrel{\text { 글 }}{ }$ | - |
|  |  | m | in |
| $\stackrel{\otimes}{\otimes}$ |  | $\Sigma$ | $\Sigma$ |
|  |  | $\begin{aligned} & \bar{\sim} \\ & \stackrel{1}{2} \\ & \stackrel{\rightharpoonup}{\circ} \\ & \frac{\square}{\Sigma} \end{aligned}$ |  |


| - |  |
| :---: | :---: |
| $\underset{4}{\text { ® }}$ |  |
| $\overline{0} \overline{0}$ |  <br>  |
| $\begin{array}{\|l\|l} \stackrel{\lambda}{\lambda} & \infty \\ \hdashline & \infty \\ \hline \vdots & \end{array}$ |  |
| - $<$ |  <br>  |
| $\stackrel{\otimes}{E}$ |  |
| ־ |  |
| $\begin{aligned} & 0 \\ & \stackrel{0}{\lambda} \\ & \stackrel{0}{0} \\ & 0.0 \end{aligned}$ |  |
|  |  |
|  |  |
|  |  |
| $\stackrel{\text { ® }}{\stackrel{\text { ® }}{\sim}}$ |  |
|  |  |

[^5][^6]| $\bar{\infty}$ |  <br>  |
| :---: | :---: |
| ※ |  <br>  |
| $\begin{array}{\|l\|l} \hline \bar{\pi} & \bar{\alpha} \\ \hline 0 \end{array}$ |  mmin in <br>  |
| $\begin{array}{l\|l} \stackrel{\lambda}{\grave{2}} & \infty \\ \hdashline \dot{\partial} & \infty \end{array}$ |  いinminー・• |
| ¢ |  <br>  |
| $\stackrel{\stackrel{\rightharpoonup}{E}}{\stackrel{\text { E }}{-}}$ | 응ㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅡ․ |
| $\overline{0}$ |  Nルー・• |
|  |  <br>  |
|  |  <br>  |
|  |  |
|  |  |
| $\stackrel{\text { ® }}{\stackrel{\text { u }}{\sim}}$ |  |
|  |  |



Table B－2．Channel Evaluation Factors－1288 and 1419

| $\bar{\infty}$ |  |
| :---: | :---: |
| ※ |  |
| ¢ $\overline{0}$ |  |
| $\stackrel{2}{2}$  <br> $\vdots$  <br> $\vdots$ $\infty$ |  |
| c |  |
| $\stackrel{\stackrel{\rightharpoonup}{E}}{\stackrel{-}{*}}$ |  |
| $\bar{\square}$ | $\begin{array}{llll} 8 & 0 & \stackrel{\infty}{8} & \stackrel{\infty}{7} \\ 0 & 0 & \underset{\sim}{7} & \end{array}$ |
| ¢ | $\begin{array}{llll}\infty & \sim \\ \sim & \sim & \sim \\ 0 & \sim \\ \sim & \sim & \infty \\ \sim & \sim & \sim\end{array}$ |
|  |  |
|  | in |
|  | $\cdots \xrightarrow{\sim} \stackrel{\sim}{\square}$ |
| $\stackrel{\rightharpoonup}{\otimes}$ | $\Sigma \leq$ |
|  |  |


| ¢ |  |
| :---: | :---: |
| ~ |  |
| - ¢ | 으애NN M inginn $\cdots-\infty \quad-\infty$ |
|  |  |
| $\varangle$ | MNMO MNMO ○ing oino |
| $\stackrel{\stackrel{\rightharpoonup}{E}}{\stackrel{\sim}{\square}}$ |  |
| $\bar{\square}$ |  |
| $\xrightarrow{\sim}$ | $\begin{array}{llll}n & \sim & \sim & \sim \\ \infty & \sim & \sim \\ \dot{0} & \dot{\sim} & \dot{\sim} & 0 \\ \sim & \sim\end{array}$ |
|  | $\frac{n}{\sigma} \frac{n}{\sigma} \quad \frac{n}{\sigma} \frac{n}{\sigma}$ |
|  | $\bigcirc \bigcirc \bigcirc \bigcirc$ |
|  | $\cdots \stackrel{O}{0} \quad \stackrel{m}{m}$ |
|  | $\Sigma \leq \leq$ |
|  |  |

[^7]Table B.3. Channel Evaluation Factors-1442 and 2501 B1 and B2

|  | Key | Nominal Data Rate (kb/sec) | Cycle Time (ms) | Wait Time (ms) | Device Load | D1 | Priority Load |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | Time | A | B | A 1 | A2 | B 1 |
| 2520 Card Read/Punch: Reading EBCDIC | IM | . 67 | 120 | 1.020 | 16.06 | 4.71 | . 100 | 21.26 | . 00 | 3.500 | . 000 | . 000 |
|  |  |  |  |  |  |  | 1.513 | 5.14 | 10.65 | 3. 1.102 | . 036 | 2.593 |
|  |  | 1.33 | 120 | 1.020 |  | 4.71 | 42.718 | 286.57 | 4.06 | 70.839 | . 013 | . 962 |
| Reading Card Image | 1M |  |  |  | 19.37 |  | . 100 | 21.26 | . 00 | 3.500 | . 000 | . 000 |
|  |  |  |  |  |  |  | 1.078 | 6.41 373.30 | 13.77 | 1.014 | . 036 | 2.593 |
|  | 2M | . 67 | 120 | 9.000 | 34.92 |  | 42.734 | 373.30 | 5.19 | 70.807 | . 013 | . 962 |
| Punching EBCDIC |  |  |  |  |  | 6.53 | . 100 | 206.00 | 100.00 | . 0000 | . 000 | . 000 |
|  |  |  |  |  |  |  | 3.143 | 306.06 | 2.62 | 55.720 | . 288 | . 490 |
| Punching Column Binary | 2M | 1.33 | 120 | 9.000 | 67.97 | 12.76 | . 100 | . ${ }^{\text {. } 00}$ | 100.00 | . 000 | . 000 | . 000 |
| Reading And Punching | 1,2M | 1.33 | 120 | . 000 | . 00 | . 67 | 6.117 | 580.55 | 5.10 | 103.095 | 1.098 | . 957 |
| Reading And Punching EBCDIC |  |  |  |  |  |  | .100 3.187 | 318.71 | 100.00 .00 | .000 59.500 | .000 .000 | .000 .000 |
|  |  |  |  |  |  |  | 29.442 | 5.14 | 10.65 | 1.102 | . 036 | 2.593 |
|  | 1,2M | 2.67 |  | . 000 | . 00 | 1.33 | 42.718 | 180.69 | 6.54 | 50.484 | . 016 | 1.438 |
| Reading and Punching |  |  | 120 |  |  |  | . 100 | . .00 | 100.00 | 115.000 | . 000 | . 000 |
| Card Image |  |  |  |  |  |  | 6.162 42.734 | 616.16 182.70 | 10.00 | 115.500 | . 000 | . .000 |
|  |  |  |  |  |  |  | 42.734 | 182.70 | 10.14 | 33.967 | . 027 | 1.905 |

[^8]Table B-4. Channel Evaluation Factors-2520
1

| $\bar{\infty}$ | －̇． | $\begin{aligned} & \ddagger \\ & \infty \\ & 0 \end{aligned}$ | $\begin{aligned} & \infty \infty \\ & \underset{-\infty}{\infty} \end{aligned}$ | $\cong$ | 응응 | $\frac{\mathrm{J}}{0}$ | $\stackrel{5}{8}$ | 으우N웅 <br> NM．$\underset{m i n}{m-1}$ |  |  | in응윽웅 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\underset{\sim}{2}$ | 등응 | $\stackrel{n}{\circ}$ | $8$ | 응 | $\begin{aligned} & 8 \circ \\ & \hline 80 \end{aligned}$ | $8$ | $8:$ | 응ํo응 |  88⿹̃으N | すoincoon | mn=mio |  |
| 可 $\overline{4}$ | $\frac{0}{\mathrm{f}} \frac{\mathrm{~m}}{\mathrm{mim}}$ | $\frac{m}{m}$ | $\begin{aligned} & \underline{0} \\ & =0 \\ & \text { min } \end{aligned}$ | $\frac{\stackrel{\infty}{ \pm}}{\stackrel{\sim}{\mathrm{m}}}$ | が ming | $\frac{\mathrm{I}}{\mathrm{I}}$ | $\begin{aligned} & \stackrel{\infty}{ \pm} \underset{\mathrm{min}}{2} \end{aligned}$ |  응ํํํ minin－ |  | －Minnionon ํํㄴNNNN mmmmin－ | ふへのざの ヘOスう゚ minimis | －minno <br> ํํñ <br> minimi |
| $\frac{2}{\frac{2}{\circ}}{ }^{\infty}$ | ôo | $\stackrel{\text { N }}{ }$ | Mn | O． | nọos | O | ¢ิ． |  |  <br> －NONN |  |  |  |
| $\cdots$ | $\begin{aligned} & \underset{\sim}{N} \\ & \underset{\sim}{0} \\ & 0 \end{aligned}$ | $\begin{aligned} & \hat{N} \\ & \vdots \end{aligned}$ | $$ | $\begin{aligned} & \underset{\sim}{n} \\ & \dot{0} \end{aligned}$ | $\begin{aligned} & \text { NON } \\ & \underset{N}{N} \\ & \dot{O} 0 \end{aligned}$ | $\begin{gathered} \underset{\sim}{n} \\ \stackrel{0}{0} \end{gathered}$ | $\begin{aligned} & \text { ָัN } \\ & \stackrel{0}{0} \\ & \end{aligned}$ | ペーセ゚～へ <br> óooni |  <br> 으으응N | かMNさNがN <br> 응ㅇ웅 | miñonn 응ㅇㅇ | miñ 으으으으 |
| $\stackrel{\underset{E}{E}}{F}$ | $\therefore 0$ | $\therefore$ | 으응 | 응 | 으으응 | 응 | 으응 | 으응ㅇㅇㅇㅇ | 응ㅇㅇㅇㅇㅇ응 | 응ㅇㅇㅇㅇㅇㅇㅇㅇㅇ | 으으으응 | 응ㅇㅇㅇㅇㅡ․ |
| $\overline{0}$ | す！ | $=$ | Nへ． | O． | Nõon | ¢ | No． |  |  |  | =mingm | NJへの |
|  | －${ }_{\sim}^{\infty}$ | $\stackrel{\infty}{\sim}$ |  | $\bigcirc$ | $\stackrel{\sim}{\circ} \mathrm{O} 0_{0}^{\circ} \mathrm{O}$ | － | $\stackrel{n}{0} \mathrm{O}$ |  |  $-\operatorname{Nin}^{-\infty}$ |  |  | in orga $-i N$ |
|  | $\begin{aligned} & \text { BO } \\ & \text { Ni } \\ & \text { ñ } \\ & \text { niz } \end{aligned}$ | $\begin{aligned} & 8 \\ & \underset{y}{2} \\ & \vdots \end{aligned}$ | $\begin{aligned} & 0.0 \\ & \text { ORO } \\ & \infty \\ & \infty \end{aligned}$ | $\begin{aligned} & 0 \\ & \underset{m}{m} \\ & \underline{m} \end{aligned}$ |  | $\begin{aligned} & 0 \\ & \infty \\ & \infty \\ & \dot{\infty} \\ & \hline \end{aligned}$ |  | 용ㅇㅇㅁ oingon ท่ゥ～ | ㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇㅇ은 ñinm |  |  | ㅇㅇㅇㅇㅇ ○inin |
| $\begin{array}{lc} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 \end{array}$ |  | $\begin{aligned} & \circ \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & m \\ & m \\ & \infty \end{aligned}$ | 80 요 <br> －능 | $\begin{aligned} & \circ \\ & \hline \end{aligned}$ | $\begin{aligned} & 08 \\ & 0.8 \\ & \dot{0} 0 \end{aligned}$ | $\begin{aligned} & \text { 옹ㅇㅇ } \\ & \text { ing } \\ & \text { ingo } \\ & \text { nin } \end{aligned}$ | 88888888 nin $0^{\circ \circ} 0^{\circ} 0^{\circ}$ <br> －in inco | 8888880 8.9088 m －NmJ～～～iom | $\begin{aligned} & 80880 \\ & \text { noigo } \\ & \text { ningo } \end{aligned}$ |  |
|  | $\begin{aligned} & \text { no } \\ & \text { mio } \\ & \text { miob } \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 00 \\ & 0.0 \\ & 0.0 \\ & \mathrm{O} \end{aligned}$ | $\begin{aligned} & 0 \\ & i n \end{aligned}$ | $\begin{aligned} & \text { ing } \\ & \text { noñ } \\ & \text { non } \end{aligned}$ | $\stackrel{0}{0}$ | $\begin{aligned} & 00 \\ & \text { in } \\ & \hline \end{aligned}$ |  | 000000000 8ㅇㅇㅇㅇㅇㅇㅇ －NOJmNoOJ －N～テのO우우N | 00000000 8ㅇㅇㅇㅇㅇㅇ －NO No N －NNOTHM |  | $\begin{aligned} & 0000 \\ & 0.00 \\ & 0.00 \\ & 0.0_{N}^{0} \end{aligned}$ |
|  |  | 11 loatuoj leu！ulat Wal |  |  |  | $=$ $\pm$ $\stackrel{\sim}{2}$ $\stackrel{\rightharpoonup}{2}$ |  |  |  |  |  |  |

Table B－5．Channel Evaluation Factors－2701


Table B-6. Channel Evaluation Factors-7770

## Appendix C. Device Data Rates



Table C-1. Data Rates by Device

| CONTROL UNIT(S) | DEVICE | $\begin{aligned} & \text { TAG } \\ & \text { SPEED } \end{aligned}$ | INSTANTANEOUS DATA RATE (Mb/sec) |
| :---: | :---: | :---: | :---: |
| Direct Access Storage Devices: | 3540 | slow | Note 1 |
| Punched Card $1 / 0$ and Printers: $\begin{aligned} & 2821 \\ & 2821 \end{aligned}$ $3811$ | 1442 1443 2501 2520 1403 2540 3203 3211 3505 3525 3800 | slow slow s low s low slow slow fast slow fast fast fast | Note 1 <br> Note 1 <br> Note 1 <br> Note 1 <br> 0.200 <br> 0.166 <br> 0.598 <br> 0.288 <br> EBCDIC: 0.167 / card image 0.350 <br> EBCDIC: 0.167 / card image 0.350 <br> 0.235 |
| $\begin{aligned} & \text { Display and Console Printers: } \\ & \begin{array}{l} 3272 \\ \\ \\ 3274-1 \mathrm{~A} \\ \\ 3274-1 \mathrm{~B}, 1 \mathrm{D} \\ \\ 3791 \end{array} \end{aligned}$ | 3793 | fast fast fast fast | $\begin{aligned} & 0.650 \\ & \text { Note } 1 \\ & 0.650 \\ & \text { Note } 1 \end{aligned}$ |
| Magnetic Character and Optical Reader: | $\begin{aligned} & 1255 \\ & 1287 \\ & 1288 \\ & 1419 \\ & 3881 \\ & 3886 \\ & 3890 \\ & 3895 \end{aligned}$ | slow <br> slow <br> fast <br> slow <br> slow <br> fast <br> slow <br> fast | Note 1 <br> Note 1 <br> Note 1 <br> Note 1 <br> 0.115 <br> 0.126 <br> 0.200 <br> Note 2 |
| ```Communication/Data Acquisition/ Process Control: 2715 2715``` | $\begin{aligned} & 2701 \\ & 2791 \\ & 2793 \\ & 3704 \\ & 3705 \end{aligned}$ | fast slow slow fast fast | Note 1 <br> Note 2 <br> Note 2 <br> Note 2 <br> Note 1 |
| $\begin{array}{r} \hline \text { Paper Tape } 1 / 0: \\ 2822 \\ \\ 2826 \\ \\ 2826 \end{array}$ | $\begin{aligned} & 2671 \\ & 1017 \\ & 1018 \end{aligned}$ | $\begin{aligned} & \text { slow } \\ & \text { slow } \\ & \text { slow } \end{aligned}$ | Note 1 <br> Note 2 <br> Note 2 |
|  | 3850/51 | fast | Channel Speed ( $1 \mathrm{Mb} / \mathrm{sec}$ or $1 \mathrm{Mb} / \mathrm{sec}$ ) |
| Audio Response Unit: | 7770 | slow | Note 2 |
|  | CHAN-to CHAN ADAPTER | fast | Channel Speed ( $1 \mathrm{Mb} / \mathrm{sec}$ or $1 \mathrm{Mb} / \mathrm{sec}$ ) |

Table C-2. Data Rates by Device

## Notes:

1. Negligible for EDR consideration.
2. Not applicable for $E D R$ consideration.

## Appendix D. Miscellaneous Tables

| SECTION 1 | Channel 1 | Channel 2 | Channel 3 | Channel 4 | Channel 5 |
| :--- | :---: | :---: | :---: | :---: | :---: |
| No Data Chaining | 3.0 Mb | 3.0 Mb | 2.0 Mb | 2.0 Mb | 1.0 Mb |
| If Data Chaining | Section <br> 2 or $3^{*}$ | Section <br> 2 or $3^{*}$ | Section <br> 3 | Section <br> 3 | Section <br> 3 |

* Use Section 2 if Extra Channel feature is not installed. Use Section 3 if Extra Channel feature is installed.



Table D-1. Data Chaining Rates for Block Multiplexer Channels


Table D-2. IBM 3704/3705 Timing Chart

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[^0]:    Start I/O
    Start I/O Fast Release
    Test Channel
    Test I/O
    Halt I/O
    Halt Device
    Clear I/O

[^1]:    :0 ? 3n: 4341 Processor Channel Characteristics

[^2]:    1 Device subject to overrun; highest priority required. Device does not require synchronized channel service; not subject to overrun; lowest priority

    Byte mode on byte multiplexer channel. Var Variable.

[^3]:    Device subject to overrun；highest priority required．$\quad$ iece requires synchronized channel service；not subject to overrun；second highest priority required Key Device does not require synchronized channel service；not subject to overrun；lowest priority Byte mode on byte multiplexer channel loads for the independent operations．
    Variable．

[^4]:    Device subject to overrun；highest priority required． Device does not require synchronized channel service；not subject to overrun；lowest priority

    Evaluate punching and reading separately by using the wait rimes，device loads，and previous
    loads for the independent operations．

[^5]:    1 Device subject to overrun; highest priority required. 2 Device requires synchronized channel service; not subject to overrun; second hich lowest priority
    $M$
    $E$ Evte mode on byte multiplexer channel. punching and reading separately by using the wait times, device ioads, and previous loads for the independent operations.
    Var Variable.

[^6]:    Table B-1. Channe Evaluation Factors-1255 and 1287

[^7]:    1 Device subject to overrun, highest priority required. . .
    Device subject to overrun, highest priority required.
    Device requires synchronized channel service; not sub Device does not require synchronized channel service; not subject to overrun; lowest priority

    Byte mode on byte multiplexer channel.
    Var loads for the independent operations.

[^8]:    Device subject to overrun; highest priority required.
    Key:
    Key
    1
    2 Device does not require synchronized channel service; not subject to overrun; lowest priority.

    Evaluate punching and reading separately by using the wait times, device loads, and previous
    Var loads for the independent operations

