



ALIOS COMPUTER SYSTEMS
8500 CENTRAL PROCESSING UNIT PCB
HARD DISK CONTROLLER PCB
TAPE CONTROLLER PCB
I/O PORT ASSIGNMENTS
SCHEMATICS

TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
<u>PART TWO</u>		
1.	8500 CENTRAL PROCESSING UNIT PRINTED CIRCUIT BOARD AND THE 8" HARD DISK CONTROLLER BOARD	1-1
2.	THE 8500 CPU PRINTED CIRCUIT BOARD (PCB)	2-1
2.1	Memory	2-1
2.2	The Hard Disk Controller (HDC)	2-1
2.3	Floppy Disk Controller (FDC)	2-1
2.4	Magnetic Tape Unit Controller	2-3
2.5	I/O Port Assignments for the 8500 PCB	2-3
2.6	Z80 Interrupt Daisy Chain	2-10
2.7	ALTOS Interface Connector Wiring	2-11
3.	ALTOS 8" HARD DISK CONTROLLER, MTU CONTROLLER, AND THE SHUGART 8" SOFT-SECTORED DRIVE	3-1
3.1	8" Hard Disk Controller	3-1
3.1.1	Commands/Command Ports	3-6
3.1.2	Status/Status Port	3-7
3.1.3	Ports 022H and 021H	3-10
3.2	Formatting	3-11
3.3	Reading or Writing a Sector	3-13
3.3.1	Reading a Sector	3-13
3.3.2	Writing a Sector	3-14
3.4	Controller Responses	3-15
3.5	Shugart 8" Soft-Sector Drive	3-15
3.6	Magnetic Tape Controller	3-17

SCHEMATICS

8500 CPU PCB SCHEMATICS

8" HARD DISK CONTROLLER SCHEMATICS

XENTEK 6055 POWER SUPPLY SCHEMATICS

REAR PANEL I/O PCB SCHEMATIC

QUANTUM SCHEMATICS

LIST OF FIGURES

<u>FIGURE</u>	<u>TITLE</u>	<u>PAGE</u>
<u>PART TWO</u>		
2-1	8500 CPU PCB Matrix Map	2-2
3-1	8" HDC Controller Board Matrix Map	3-2
3-2a	50-Pin Daisy Chain Connector for the 8" HDC	3-3
3-2b	20-Pin Radial Connector to Drive 1	3-4
3-2c	20-Pin Radial Connector to Drive 2	3-4
3-2d	34-Pin CPU to Controller Interconnect Cable	3-5
3-2e	Power Connector Pl	3-6
3-3	MTU Controller Board Matrix Map	3-18

LIST OF TABLES

<u>TABLE</u>	<u>TITLE</u>	<u>PAGE</u>
<u>PART TWO</u>		
2-1	I/O Port Assignments for the 8500 PCB	2-4
2-2	Bit Assignments, Input/Output Signals for I/O Ports	2-7
2-3	Interrupt Daisy Chain	2-10
2-4	Serial I/O Connector	2-11
2-5	Parallel I/O Connector	2-12
3-1	Addresses	3-1
3-2	Commands (Port 023H)	3-7
3-3	Status Byte (Port 023H)	3-10
3-4	Drive/head Byte (Port 020H)	3-11
3-5	Head Select	3-11
3-6	Header Image	3-12
3-7	Disk Drive Specifications	3-16
3-8	Format for Soft-sectored 8" Hard Disk	3-17
3-9	MTU Controller to DEI Drive Signal Pin Assignments	3-19

1. 8500 CENTRAL PROCESSING UNIT PRINTED CIRCUIT BOARD
AND THE EIGHT-INCH HARD DISK CONTROLLER BOARD.

The following two sections are dedicated to a detailed discussion of the 8500 CPU PCB and the eight-inch hard disk controller PCB. Most of the information contained in these sections are for user reference only.

2. THE 8500 CPU PRINTED CIRCUIT BOARD (PCB).

Most of the data contained in this Section is for information purposes only as the operating system handles the operations discussed herein. The 8500 CPU PCB has the capability of supporting up to four floppy disk drives and up to two eight-inch hard disks. Figure 2-1 is a matrix map of the 8500 PCB.

2.1 Memory.

The 8500 PCB Memory bank switching allows selection of the bank the DMA will access independently of the bank selected for access by the CPU. Thus, the CPU may be operating in one memory bank when the DMA interrupts to read from or write to another memory bank. This requires two more bits (UN3 and UN4) at port 25.

The ability to swap the fixed 16K address space from high-order memory to low-order memory has been facilitated by a pair of jumpers (S21 and S22), on the PCB at matrix positions 12A/B. This jumper allows the user to configure the system for OASIS, CP/M or MP/M operating systems. The write protect function operates on the common memory only, independently of whether common memory is pinned to be in high-order or low-order space.

2.2 The Hard Disk Controller (HDC).

The hard disk controller is a separate PCB that attaches, piggyback, onto the right side mother board. This allows different types of disk drives to be used. Currently, the hard disk controller that will mount on the 8500 board is the for the soft-sectored drives such as the SA1000.

2.3 Floppy Disk Controller (FDC).

When double-sided floppy disk drives are installed, they are pinned for accessibility as one logical drive with two heads via the side-select control line.

2.3 --Continued.

When switching from one floppy drive to another, it is necessary to force unloading of the head-load signal. This insures that, when the newly selected drive is READ from or WRITTEN to, the head load delay one-shot in the controller circuit will be triggered and delay sufficiently for the head of the newly selected drive to settle. This is done by doing a SEEK with the head load flag bit set to unload the head at the beginning.

The FDC IC chip has been changed from the FD1791 to the FD1797. The 1797 IC chip is able to read to some single-density diskettes that the 1791 cannot.

Bit 1 on the 1797 establishes which side is being compared; bit 3 dynamically alters the code for the sector length field (This is done in conjunction with the sector length byte in the header). Thus, the side select bit changes from bit 3 to bit 1, and the option not to compare is not available. To maintain compatibility with the present sector length field code, bit 3 should be set to bit 1.

The 1797 has an output that can be used to control the side-select line to the disk drive. This happens automatically as determined by bit 1 in the READ and WRITE commands. However, the CPU board is wired to use bit 5 out of the PIO at B7 to do this selection. If necessary, the signal from the 1797 can be used to control side select by cutting a trace and installing a jumper at S25.

2.4 Magnetic Tape Unit Controller.

The magnetic tape controller is a separate PCB that attaches, piggyback, onto the left side of the 8500 board. It currently controls a Data Electronics Inc., (DEI) funnel drive.

2.5 I/O Port Assignments for the 8500 PCB.

Table 2-1 lists the I/O port assignments with their corresponding schematic reference and functions. Table 2-2 lists the bit assignments for the I/O port.

Table 2-1. I/O Port Assignments for the 8500 PCB

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
00-03	Y0 (DMA)	Initialize DMA.
04 05 06 07	Y1 (FD1797) (Floppy disk)	Input drive/controller status. Output command. Input/output track number. Input/output sector number. Input data. Output data when WRITING to the disk and the desired track number prior to doing a SEEK.
08 09 0A 0B	Y2 (PIO-CH A) Y2 (PIO-CH B) Y2 (PIO-CH A) Y2 (PIO-CH B)	Input interrupts from FDC and from HDC. Output floppy disk drive select, and recording density. Input END from 9511A, DISK CHANGE, CPU board type and two-sided (TS) signal from floppy disk drive. Out put MR to FDC chip. Initialize channel A. Initialize channel B.
0C 0D 0E 0F	Y3 (CTC-CH 0) Y3 (CTC-CH 1) Y3 (CTC-CH 2) Y3 (CTC-CH 3)	Baud rate generator for console number 1 at JX. not used. Baud rate generator for printer number 1 at JT. Used to count index pulses of the floppy disk drive.
10 11 12 13	Y4 (PIO-CH A) Y4 (PIO-CH B) Y4 (PIO-CH A) Y4 (PIO-CH B)	Parallel port I/O at J2 (normally used in I/O mode). Parallel port I/O at J2 (normally used for data in an I/O mode). Initialize channel A. Initialize channel B.
14-17	Y5 (IPL)	An output to any of these ports turns off the PROM after initial program load (IPL).
18 19 1A 1B	Y6 (9511) " " "	Input/output data from the 9511's stack. Input status, output commands to/from the 9511. Same as 18. Same as 19.

Table 2-1. Continued

PORT NUMBER	SCHEMATIC REFERENCE	FUNCTION
1C	Y7 (DART-CH A)	Input/output data to I/O port at JX (normally Console #1). Input status of channel A. Output commands to CH A.
1E	Y7 (DART-CH B)	Input/output data to I/O port at JT (normally printer number 1).
1F	"	Input status of channel B. Output commands to CH B.
20	Y8 (Hard Disk)	Output drive and head number to HDC.
21	"	Output sector number and old cylinder number to the HDC; also input and output data to or from the hard disk via the DMA.
22	"	Output new cylinder number to the controller.
23	"	Output commands to the controller. Input status of the controller.
24	Y9 (PIO-CH A)	Input configuration of CPU and controllers.
25	Y9 (PIO-CH B)	Input nothing. Output memory write protect bit and memory bank select bits.
26	Y9 (PIO-CH A)	Initialize channel A.
27	Y9 (PIO-CH B)	Initialize channel B.
28	Y10 (SIO-CH A)	Input/output data to I/O port at JV (normally printer number 2 but on the 8500 is reconfigurable as a bisync modem port).
29	"	Input status of channel A. Output commands to CH A.
2A	Y10 (SIO-CH B)	Input/output data to I/O port at JZ (normally console number 4).
2B	"	Input status of channel B. Output commands to CH B.
2C	Y11 (SIO-CH A)	Input/output data to I/O port at JY (normally console number 2). Input/Output data to network port JW
2D	"	Input status of channel A. Output commands to CH A.

Table 2-1. Continued.

2E	Y11 (SIO-CH B)	Input/output data to I/O port at JU (normally console number 3).
2F	"	Input status of channel B. Output commands to CH B.
30	Y12 (CTC-CH 0)	Baud rate clock for console # 2 at JY.
31	Y12 (CTC-CH 1)	Baud rate clock for consoles # 3 and #4 at JU and JZ.
32	Y12 (CTC-CH 2)	Baud rate clock for printer number 2 at JV.
33	Y12 (CTC-CH 3)	Real time clock generator for time slicing the usage of the processor.

Table 2-2. Bit Assignments, Input/Output Signals for I/O Ports

PORT # SCH. REF.	BIT #	DESCRIPTION
<p>00-03 (DMA)</p> <p>04-07 (FD1797)</p> <p>08 Y2 (PIO-CH A)</p>	<p>7</p> <p>6</p> <p>5</p> <p>4</p> <p>3</p> <p>2</p> <p>1</p> <p>0</p>	<p>(See Zilog DMA Manual)</p> <p>(See the applicable Western Digital data sheet).</p> <p>INTERRUPT input from the HDC.</p> <p>INTERRUPT input from the FDC chip.</p> <p>DRIVE SELECT 4 to select drive D. 0=unselected, 1=selected. Select only one drive at a time.</p> <p>DRIVE SELECT 3 to select drive C.</p> <p>DRIVE SELECT 2 to select drive B.</p> <p>DRIVE SELECT 1 to select drive A.</p> <p>HLD input from the floppy disk controller chip to indicate when the head is loaded. 0=not loaded; 1=loaded.</p> <p>DDEN output to set the recording mode. 0=single density, 1=double density.</p>
<p>09 Y2 (PIO-CH B)</p>	<p>7</p> <p>6</p> <p>5</p> <p>4</p> <p>3</p> <p>2</p> <p>1</p> <p>0</p>	<p>TWO-SIDED (TS) input from the floppy disk drive. 0=single-sided diskette, 1=two-sided diskette.</p> <p>Input (hardwired) to indicate the type of PCB. 0=8500..</p> <p>Side select output to the floppy disk drives (unless SSO on the controller chip is used). 0=side 0 selected, 1=side 1 selected.</p> <p>Not connected.</p> <p>Not connected.</p> <p>DISK CHANGE input from the floppy disk drive. (See the disk drive spec sheet for details).</p> <p>(master reset) (/MR) output to the floppy disk controller chip. Normally a 1, take 50 seconds to reset.</p> <p>END, input from the 9511A to indicate the completion of a calculation.</p>
<p>OA</p>		<p>(See Zilog PIO Manual)</p>
<p>OB</p>		<p>(See Zilog PIO Manual)</p>

Table 2-2. Continued.

0C Y3 (CTC-CH 0)	In Out	2 Mhz. Baud rate for channel A of the DART that outputs to JX (normally console number 1).
0D Y3 (CTC-CH 1)	In Out	2 Mhz. Not attached.
0E Y3 (CTC-CH 2)	In Out	2Mhz. Baud rate for channel B of the DART that outputs to JT (normally printer number 1).
0F Y3 (CTC-CH 3)	In Out	Index pulses from the selected floppy disk drives. (None).
10 Y4 (PIO-CH A)	7 6 5 4 3 2 1 0	(Unnamed) normally an input from printer to PIO SELECT " BUSY " PAPER EMPTY " FAULT " CNTL normally an output to the printer. INPUT PRIME " DATA STROBE "
11 Y4 (PIO-CH B)	7 6 5 4 3 2 1 0	DATA 7 normally an output to the printer. DATA 6 " DATA 5 " DATA 4 " DATA 3 " DATA 2 " DATA 1 " DATA 0 "
12-13 Y4 (PIO-CH A)		(See Zilog PIO Manua).
14-17 Y5 (IPL)		An output to any of these ports turns off the PROM after initial program load (IPL)
18,19 Y6 (9511A)		(See the AMD9511A specification sheet).
1A Y6 (9511A)		Same as 18
1B Y6 (9511A)		Same as 19

Table 2-2. Continued.

1C Y7 (DART-CH A)		(Refer to the Zilog Manual)
1D Y7 (DART CH A)		(Refer to the Zilog Manual)
1E Y7 (DART-CH B)		(Refer To Zilog Manual)
1F YA (DART-CH B)		(Refer to Zilog Manual)
20-23 Y8 (Hard disk)		(See the HARD DISK interface specifi-
24 Y9 (PIO-CH A)		All bits have yet to be assigned. They will be pinned to indicate the type(s) of controllers attached to the CPU board.
25 Y9 (PIO-CH B)	7	UN4, MSB of a two bit nibble that sets the bank of memory that DMA accesses.
	6	UN3, LSB of the above nibble.
	5	WRITE PROTECT, output to the hardware to prevent writing into the upper 16K of memory space. 0=not protected, 1=write protected.
	4	UN2, MSB of a two bit nibble that sets the bank of memory that the CPU accesses.
	3	UN1, LSB of the above nibble.
	2	Unassigned.
	1	Unassigned.
	0	Unassigned.
26, 27		(Refer to the Zilog Manual)
28 (SIO-CH A) 28 to 2B		Console # 4
2A Y10 (SIO-CH B)		Printer #2
2B		(Refer to the Zilog Manual)
2C (SIO-CH A) 2C to 2F		Console # 2
2D		(Refer to the Zilog Manual)
2E Y11 (SIO-CH B)		Network 1

Table 2-2. Continued.

30 Y12 (CTC-CH 0)	In Out	2Mhz. Baud rate for channel A of the SIO that outputs to JY (normally console number 2).
31 Y12 (CTC-CH 1)	In Out	2Mhz. Baud rate for channel B of the SIO that outputs to JU and channel B of the SIO that outputs to JZ (normally consoles 3 and 4).
32 Y12 (CTC-CH 2)	In Out	2Mhz. Baud rate for channel A of the SIO that outputs to JV (normally printer number 2).
33 Y12 (CTC-CH 3)	In Out	2Mhz. (none).

2.6 Z80 Interrupt Daisy Chain.

On the Z80 interrupt chain the SIOs are at the bottom of the chain so they can return from interrupt by a command rather than by RETI instruction which ripples down the daisy chain. See Table 2-3 for the interrupt daisy chain sequence.

Table 2-3. Interrupt Daisy Chain

Top of chain	Y0	DMA
	Y2	PIO (Hard disk, Floppy disk and 9511 interrupts)
	Y4	PIO (user's port)
	Y3	CTC (Baud rates and timer)
	Y12	CTC (baud rates and real time clock)
	Y7	SIO (console 1 and Printer 1)
	Y10	SIO (printer 2 and Console 4)
Bottom of Chain	Y11	SIO (Consoles 2 and 3)

2.7 ALTOS Interface Connector Wiring.

Table 2-4 lists the pin connections of the device connectors on the rear of the ACS8000 computer. All of the console connectors are Serial I/O devices as is the serial printer jack. The auxiliary printer connector is a Parallel I/O device available to the user.

Table 2-5 lists the Parallel I/O Pin connectors.

Table 2-4. Serial I/O Connector

Pin	Use
1	Chassis Ground
2	Transmitted Data
3	Received Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Signal Ground
20	Data Terminal Ready*

*All ALTOS CP/M, MP/M and ADX system diskettes require pin 20 (Data Terminal Ready) handshaking.

Other pins are not used. Request to Send (pin 4) and Clear to Send (pin 5) are not normally implemented. Jumpers on the Printed Circuit board allow their connection. Pin 8 is tied high through a resistor. Contact ALTOS for instructions for activating Request to Send or Clear to Send.

Table 2-5. Parallel I/O Connector

Pin	Use
1	Data Source
2	Data 0
3	Data 3
4	Data 1
5	Data 6
6	Data 7
7	Acknowledge
8	Busy
9	Data 2
10	Data 4
11	Data 5
12	Control
13	Select
14	+5 Volts
15	Paper Empty
16	-12 Volts
17	Input Prime
18	Floating
19	Floating
26	Unassigned
34	Fault
35	Unassigned
36	+12 Volts

All of the remaining pins are ground

3. ALTOS EIGHT INCH HARD DISK CONTROLLER, MTU CONTROLLER,
AND THE SHUGART EIGHT-INCH SOFT-SECTORED DRIVE.

Most of the data contained in this Section is for information purposes only, as the operating system handles the operations discussed herein. This section discusses the ALTOS eight-inch hard disk controller, the MTU controller, and the specifications for the Shugart eight-inch soft sectored drive. For further information on the Shugart eight-inch soft-sectored drive, refer to the SA1000 Fixed Disk Drive Service Manual.

3.1 Eight-inch Hard Disk Controller.

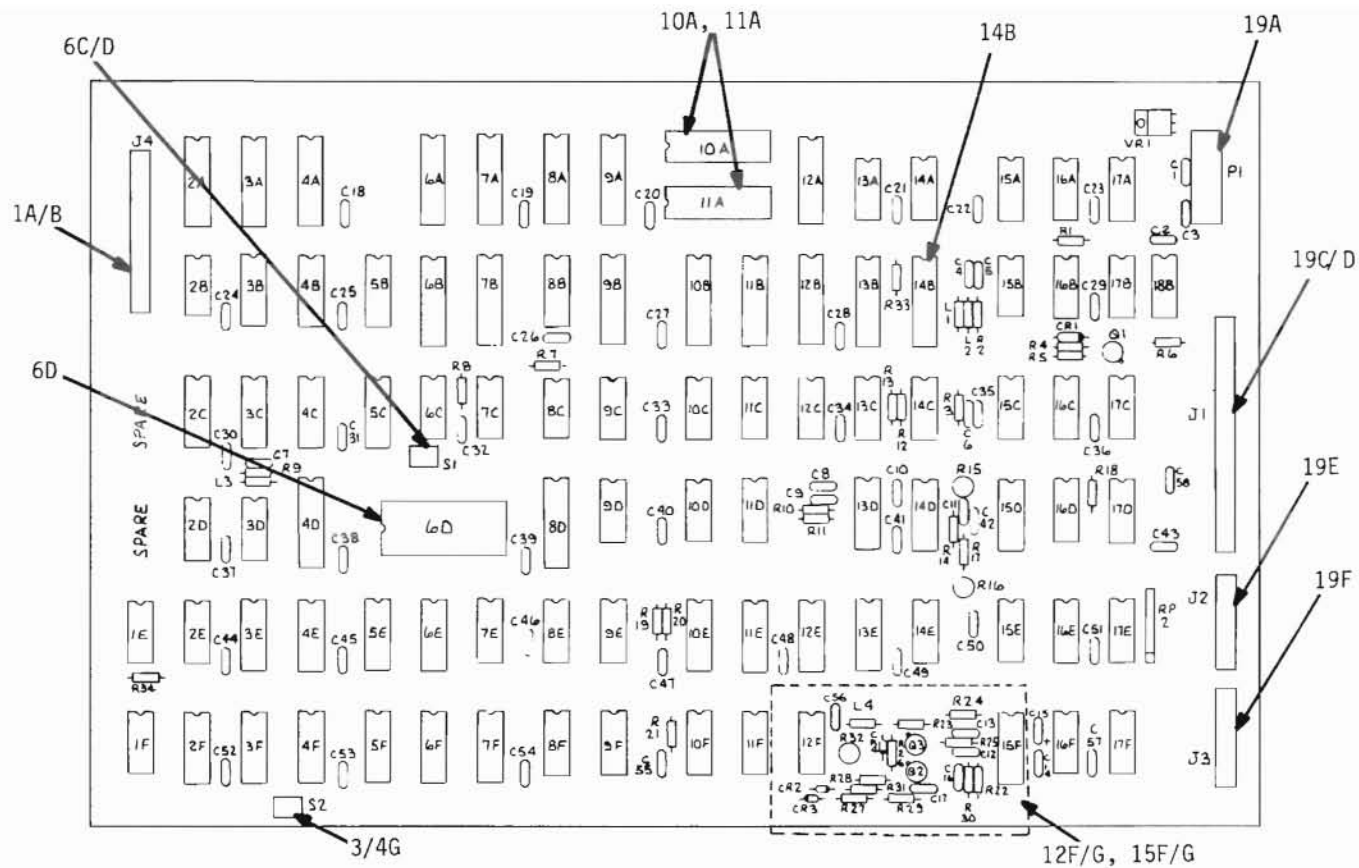
See Figure 3-1 for a diagram of the eight-inch hard disk controller matrix map. Jumper S1 on the controller must be set to coincide with the type of hard disk in the system. This must be set to S for the Shugart drive. This jumper determines the cylinder number, 128, at which write precompensation takes place. See Figures 3-2a, b, c, d and e for connector and pin assignments for the eight-inch hard disk controller.

Data is stored on the disks in blocks or sectors of 256 bytes (not programmable), identified by cylinder, head and sector numbers. The addresss for each sector is previously written (by a FORMAT command) ahead of the data field. When reading from or writing to the disk, this address is read and verified. A correct match must be found for the address and its check bytes before the sector can be written to or read from.

The general procedure to read or write data is to first position the heads over the desired cylinder via a SEEK command, load the head and sector numbers into the appropriate ports, and finally, issue a READ or WRITE command. When the correct sector is found, the data is transferred between disk and system memory under control of the DMA by way of a FIFO buffer. The controller is addressed by way of four I/O ports (020H-023H). Table 3-1 lists the four ports and their corresponding read and write addresses.

Table 3-1. Addresses

Port	Read	Write
020H	X	Drive and head numbers
021H	Data	Old cylinder number (in two bytes), sector number and data
022H	X	New cylinder number in two bytes
023H	Status	Commands



- | | | | |
|------|--------------------------------|-------|------------------------------------|
| 6C | FPLA | 19A | P1 Power |
| 1A/B | J4 CPU Interface | 19C/D | J1 50-Pin Daisy Chain Cable |
| 6C/D | S1 Precomp Block | 19E | J2 20-Pin Radial Cable Drive 1 |
| 10A | } FIFO Buffers | 19F | J3 20-Pin Radial Cable Drive 2 |
| 11A | | 12F/G | } PLO Circuitry |
| 14B | Programmable Array Logic (PAL) | 15F/G | |
| | | 3/4G | S2 Sector Size Configuration Block |

Figure 3-1. Eight-Inch HDC Controller Board Matrix Map.

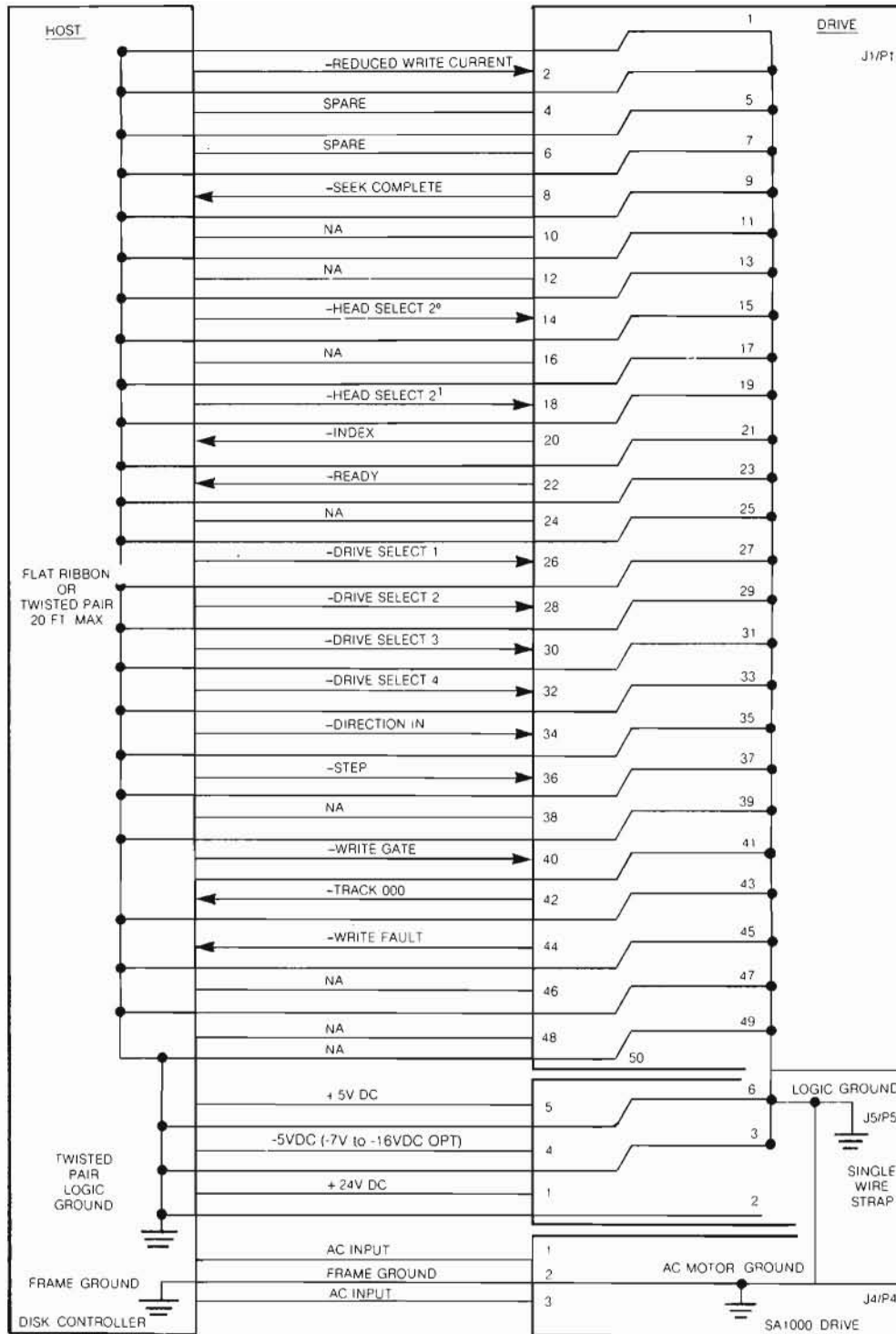


Figure 3-2a. 50-Pin Daisy Chain Connector for the 8-inch Hard Disk Controller

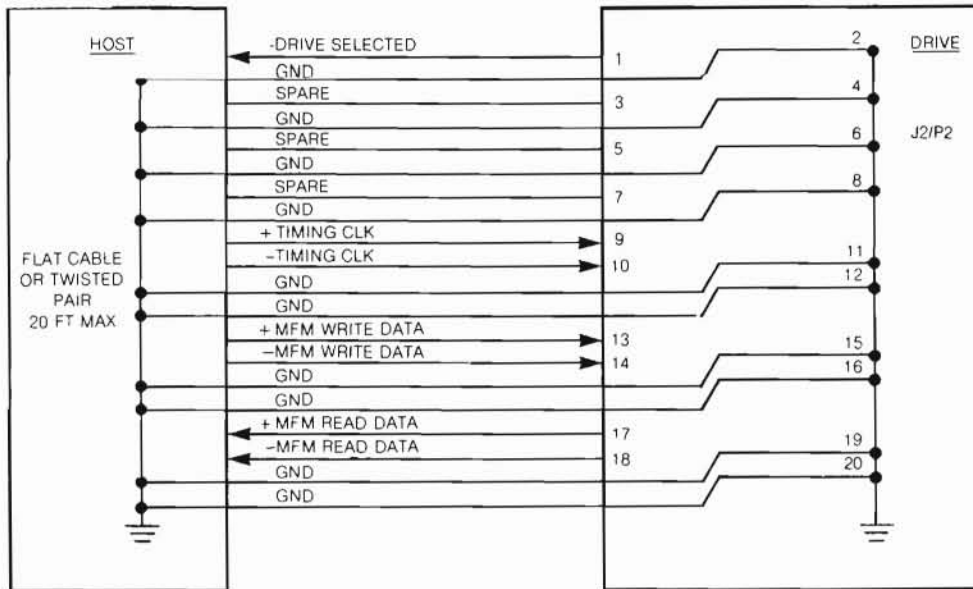


Figure 3-2b. 20-Pin Radial Connector to Drive 1

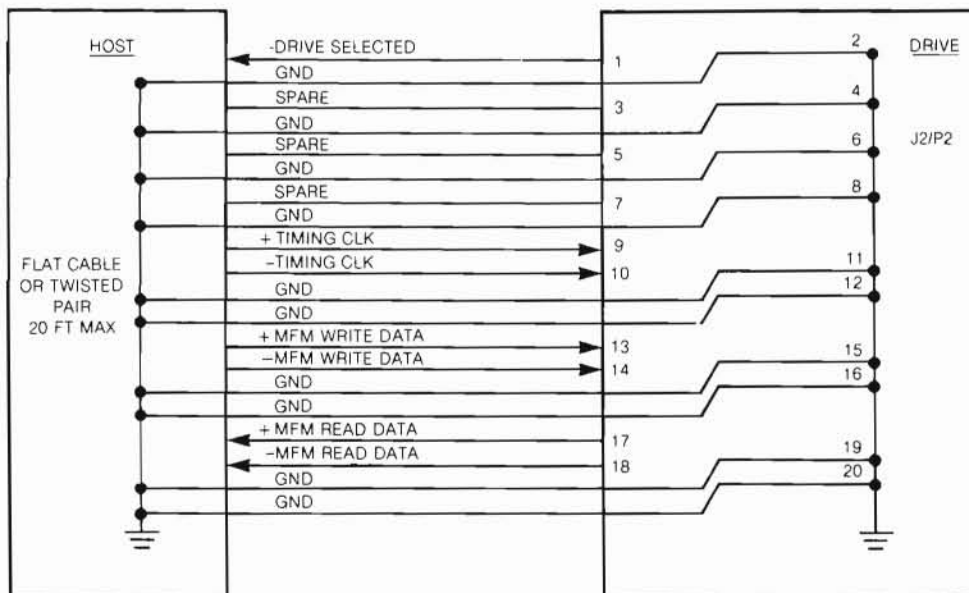


Figure 3-2c. 20-Pin radial connector to Drive 2

- 1 Ground
- 2 INT (interrupt), output to CPU, goes true at completion of a command
- 3 (not used)
- 4 /HDWR, output from controller, negative AND of controllers' address (Y8) and /IOWR, used to control transceivers on the CPU PCB
- 5 /Y15 (not used by this controller)
- 6 Ground
- 7 /HDRD, output from controller, negative AND of controllers' address (Y8) and /IORD, used to control transceivers on the CPU PCB
- 8 /MR RESET from CPU
- 9 Ground
- 10 /IORD, input to controller, negative AND of /RD and /IORQ
- 11 DIOB3
- 12 DIOB7 (MSB of bidirectional data bus)
- 13 DIOB2
- 14 Ground
- 15 DIOB1
- 16 DIOB6
- 17 Ground
- 18 /IOWR, input to controller, negative AND of /WR and /IORQ
- 19 /HDWAIT, output (not used by this controller)
- 20 DIOB5
- 21 DIOB4
- 22 Ground
- 23 DIOB0, (LSB of bidirectional data bus)
- 24 AB0, input, (LSB of CPU's address bus)
- 25 Ground
- 26 AB1, input
- 27 /RDMA, (ready DMA), output from controller to start and pace transfer of data
- 28 /BUSAKB, (bus acknowledge output bit), input from CPU, true-to-false transition is used by controller to recognize completion of a data transfer
- 29 System clock
- 30 Ground
- 31 /Y8, input to controller, used with AB0 and AB1 to address the controller
- 32 /RDB (CPU/DMA read signal), output from controller to properly position the RDMA signal (i.e., early in a transfer cycle)
- 33 Ground
- 34 1Mhz input from CPU

Figure 3-2d. 34-Pin CPU-to-Controller Interconnect Cable

1	0	Volts
2	0	Volts
3	-12	Volts
4	+5	Volts
5	+5	Volts
6	+12	Volts (not used by this controller)

Figure 3-2e. Power Connector P1

3.1.1 Commands/Command Ports.

Port 023H is the command port when writing and the status port when reading. There are seven commands that may properly be issued. These commands, when issued, cause associated circuitry functions. Table 3-2 contains the Commands and associated bit number.

COMMAND	FUNCTION
NULL	Quiescent state
RESET	Initializes the controller circuit. A reset is done automatically at power on and is not normally required thereafter.
RECAL	Positions the heads over track zero. This must be done for each drive following power on before any disk access is attempted and thereafter as part of the error recovery routine. A recal requires about 18 msec/cylinder for a maximum time of approximately 4 seconds.
SEEK	Moves the heads from the programmed "old cylinder" to the programmed "new cylinder".
READ	Reads the addressed sector from the disk.
WRITE	Writes to the addressed sector to the disk.

3.1.1 --Continued.

FORMAT Formats an entire track. (This consists of writing out the address or header for each sector on the specified track by cylinder and head.)

Table 3-2. Commands (Port 023H)

Command	bit number								Hex
	7	6	5	4	3	2	1	0	
NULL	0	0	0	0	0	0	0	0	00
READ	0	0	0	0	X	0	0	1	01
WRITE	0	0	0	0	X	0	1	0	02
FORMAT	0	0	0	0	X	1	0	0	04
SEEK	0	0	0	1	X	0	0	0	10
RECAL	0	0	1	0	X	0	0	0	20
RESET	1	0	0	0	X	0	0	0	80

3.1.1 --Continued.

No more than one command may be issued at one time. For all the commands except NULL and RESET, when the command has been completed, the controller will issue an interrupt (via the PIO at port 008H bit 7). Following the interrupt, the status port is read to clear the status register via the clearing all status latches and to permit subsequent interrupts. If more than one command is outstanding (i.e., a second command issued before the status register is cleared), both commands will be aborted.

3.1.2 Status/Status Port.

The status byte, also on port 023H, reports on the status of the drive or controller. The status byte should be read at the completion of every operation. Table 3-3 lists the bits of the Status Byte and their meaning.

3.1.2 --Continued.

<u>STATUS BYTE</u>	<u>DESCRIPTION</u>
READY	Indicates that the selected drive has power and is up to speed. No operation will take place until a drive is selected and ready is true. Normally being READY indicates that the drive is ready to be read from or written to but a special case exists with this Shugart drive: upon being powered on these drives require a two minute stabilization time before they should be read from or written to. Unfortunately, READY will go true before these two minutes are up (in about five seconds) and does not allow for this warm-up time.
WRITE FAULT	Indicates a disk error during writing. To clear a write fault, the selected drive must be de-selected then re-selected.
CRC ERROR	Indicates that either the header or data field read off the disk was in error. If the operation was a write, the error occurred while reading the header and the sector was not written to. If the operation was a read, then the error could have occurred in either the header or data field. If it occurred in the header, the operation was aborted and the data field was not read. If it occurred in the data field, the data was transferred before the error was detected.
RECORD NOT FOUND (RNF)	During a READ or WRITE operation the specified header was not found in four revolutions of the disk. This may be caused by a seek error or incorrectly specified head or sector. RNF During a read may also indicate that the data sync field (00, A1 or F8) was not found even after the header was located. This is most likely caused by trying to read a sector that had been formatted, but before it was written to.

3.1.2 --Continued.

BAD SECTOR	The sector to be read or written was previously specified as a bad sector. A sector is flagged as bad during disk initialization with a 1 at bit 3 of the header byte. Good sectors have a 0 at bit 3.
TASK COMPLETE	The requested command was carried out or aborted. Analysis of the status byte will show whether or not the operation was aborted.
BUSY	The controller is in the process of carrying out an operation. BUSY is a 0 at the completion of an operation.

Table 3-3. Status byte (Port 023H)

Bit	Mnemonic	Meaning
7	RDY	Selected drive is ready
6	WR FLT	Write fault (from drive)
5	(none)	
4	CRC ERR	CRC error encountered
3	RNF	Record not found
2	BD SECT	Bad sector encountered
1	TC	Task complete
0	BUSY	Busy

3.1.3 PORTS 022H, 020H and 021H

Port 022H is used for writing the new cylinder number. This is entered in two consecutive bytes, the low order eight bits first, then the high order three bits.

Cylinder Bytes	Bits							
Least significant	7	6	5	4	3	2	1	0
Most significant	X	X	X	X	X	A	9	8

Port 021H has the following three functions:

- a. Before doing a SEEK the old cylinder is entered (in two bytes as for new cylinder).
- b. Before doing a READ or WRITE, the sector number is entered into this port,
- c. When data is being transferred between disk and memory, it is done through port 021H.

Port 020H is used for selecting the drive and head to be used. The heads are selectable in a binary sequence (limited by the number of heads on the drive). One or the other but not both drives can be selected. Table 3-4 contains the drive-head byte bit numbers, names and their functions.

Table 3-4. Drive/head byte (Port 020H)

Bit	Name	Function
7	HS3	Head select bit 3
6	HS2	Head select bit 2
5	HS1*	Head select bit 1
4	HS0*	Head select bit 0
3		(none)
2		(none)
1	DS2	Drive select 2
0	DS1	Drive select 1

*Table 3-5. Head Select

Head Select Bits		Head Number
HS1	HS2	Selected SA1004
0	0	0
0	1	1
1	0	2
1	1	3

3.2 Formatting.

Since the SA1000 drive is soft-sectored, an entire track must be formatted at one time to maintain the proper timing relationship among the sectors. The heads must be positioned to the desired cylinder using the SEEK command. Then a header image consisting of four bytes, an 0FEH, cylinder number, head number, and sector number must be placed in memory and written out to the disk by the DMA. This is done as each sector arrives under its head during one rotation of the disk. The cylinder number in the header must agree with the cylinder on which the heads are positioned. The head number must agree with the selected head. The sector number does not have to correspond to any system, allowing for staggering of the sectors if required. The DMA must be programmed for a four-byte continuous transfer. Table 3-6 lists and describes the byte header image.

Table 3-6. Header Image

Byte	Description
Sync	ØFEH
Cylinder	Low-order bits (7-0) of the cylinder number
Head	Head bits (3-0) in the top four bits, a bad sector flag at bit 3, and high order cylinder bits (A-8) at the bottom three bits
Sector	Sector number in hex

The FORMAT command must be issued to write a header. When that header has been written, an interrupt is generated. Then the header image must be updated to the next sector number (only the sector numbers change down the track), and a new FORMAT command issued before the next sector arrives at the head (464 μ seconds for a 256-byte sector). The program must also keep count of the number of sectors that have been formatted and stop issuing the FORMAT command when the last command for that track has been written. When the interrupt occurs following the writing of the last sector's header, the status must be read and when the next interrupt occurs, the track is completely formatted and another command may be issued. (Following the next to last interrupt, a dummy or null command may be issued if necessary).

To format the entire disk the above procedure must be repeated for each head of each cylinder.

256 and 512 byte sector sizes are provided for. One track will accommodate 31 sectors at 256 bytes or 17 sectors at 512 bytes. Sector size is determined by jumper S2 on the controller. Two jumpers are used. Both must be in either the 256 or the 512 byte position.

The controller fills in every byte of the data field with Ø4EH while formatting. Following the formatting of a track, any attempt to read a sector on that track that has not been specifically written to will result in a RECORD NOT FOUND (RNF) since the sync bytes will be missing for these sectors. Each sector must subsequently be written to with some other data, (e.g., ØE5H to initialize the sector for CP/M or MP/M. Any data stored on a track is destroyed when that track is formatted.

3.2 --Continued.

The sequence of sectors on a track is under control of the formatting program. Physically adjacent sectors should not be read or written sequentially, because the data is transferred between disk and main memory under DMA control. System memory, composed of dynamic RAM, requires periodic clocking to maintain its data. This refresh is normally done by the CPU, but when the DMA is active, the CPU's refresh cycles are held off. To allow the memory to be properly refreshed, the CPU must regain control and generate the refresh cycles.

Soft sectoring the drive prevents performance of a specific READ ID command since the location of the sector on a track is unknown. When READING or WRITING, a sector is located by reading all the headers encountered along the track until the correct header is found. In a READ command, when the correct header is found, the header bytes are read off the disk and transferred into memory. As a diagnostic this verifies that the data read was from the specified sector.

3.3 Reading or Writing a Sector.

Assuming the drive has been properly initialized following power on by selecting and RECALing the drive, SEEK the desired cylinder loading the old cylinder number at port 021H (following a RECAL this would be 000H), loading the new cylinder number at port 022H, then issuing a SEEK command. An interrupt will occur when the head has arrived at the new cylinder and settled down (no additional head settle time is required).

To write or read a sector the sector must first be found. The controller does this by comparing the header images (written on the disk during formatting) as they pass under the head, to the bytes programmed into ports 020H-022H (020H has the head number, 021H has the sector number and 022H has the new cylinder number). The sector register gets written-over by data during a write. Before the next read or write command the sector number must be reissued to port 021H. Also, in switching between drives, even if a seek is not necessary, port 022H must be reloaded with the new cylinder number.

3.3.1 Reading a Sector.

To read a sector follow the procedure below:

- a. Prepare a buffer area in main memory, to which the data from disk can be placed.

3.3.1 --Continued.

- b. Program the DMA to transfer the desired number of bytes, either 256 or 512 for WRITE, or 259 or 515 for READ, from the controller's I/O port, 021H, to the buffer in memory using the CONTINUOUS mode and standard memory, and I/O timing (to properly pace the FIFO). When doing a READ, three additional bytes of header information that precede the data, cylinder, head/drive and sector are read off the disk. Just as they are written out during formatting. Along with 256 or 512 bytes of data these three bytes must be transferred by the DMA. There are also two bytes of CRC that follow the data. These may be transferred but it is not a requirement. Also, the DMA transfers one more byte than programmed for. Thus, the number of bytes the DMA is programmed to transfer will end up being two or four bytes longer than the sector length.
- c. Load the address, cylinder, head/drive and sector, of the sector to be read. The cylinder number should already be correct from having done a SEEK.
- d. Load the head number to port 020H without changing the drive number (they share the same byte).
- e. Load the sector number at port 021H. A 20- μ second delay is required between selecting a drive or a head and issuing a read or write command, but the inherent programming delays normally take care of this.
- f. Issue the READ command. When the drive/controller locates the desired sector, the controller signals the DMA and the data transfer is carried out by the DMA directly into memory. When the transfer is complete, the controller generates another interrupt and clears out the READ command. The status register must then be read. If a RNF is indicated, the data was not transferred to memory. If a CRC ERR for BAD SECTOR is indicated, the data was transferred but its accuracy is questionable.

3.3.2 Writing a Sector.

To write to a sector follow the procedure given below:

- a. Fill the buffer area with data to be written to the disk. The header and CRC bytes are provided by the hardware, so only the data bytes must be transferred by the DMA.

3.3.2 --Continued.

- b. Read the status register. If a RNF, CRC ERR, or BAD SECTOR is indicated, the data was not written to the disk. When writing, all the sync bytes are provided by the controller (in contrast with the technique used for the SA4000 which required a sync byte ahead of the data). However, when FORMATTING the drive, a sync byte of 0FEH must precede the header bytes.

3.4 Controller Responses.

If a command is issued before a drive is ready or selected, the controller will wait until the selected drive is ready before carrying out the operation. An interrupt is generated when the operation is completed.

Pressing RESET does not generate an interrupt; neither does selecting or deselecting a drive.

Reading from, and writing to the disk cannot be done by the CPU because of the high data rate. Except for some diagnostic tests, the data must be transferred by the DMA.

To prevent extraneous writes to the disk when the power goes off, the controller has a sensing circuit that de-selects the drives when the +5v supply falls below +4.5V. This circuit does not, however, guarantee that data being written to a sector will be retained if power goes off. To insure data retention, power down the system only when no writing is being done to the disk.

3.5 Shugart Eight-inch Soft-sectored drive.

- a. Logical Drives E and F are associated with the first hard disk. Drive E has a formatted capacity of approximately 8 Mbytes. Drive F has a formatted capacity of approximately 500 Kbytes.
- b. Logical Drives G and H are associated with the second hard disk. Drive G has a formatted capacity of Approximately 8 Mbytes. Drive H has a formatted capacity of approximately 500 Kbytes.

Table 3-7. DISK DRIVE SPECIFICATIONS

Nominal track capacity	10416 bytes
Min track capacity (-3% speed)	10102 bytes
Formatted capacity (at 512 bytes)	8,912,896 bytes
Transfer Rate	230 nsec/bit 1.84 μ sec/byte
Access Time	
Track to track	19 ms
Average	70 ms
Maximum	150 ms
Average latency	9.6 ms

Table 3-8. Format for Soft-sectored eight-inch Hard Disk

Start at:	Index Pulse	Character(s) Written	
	16	4E	
	14	00	Repeated 17 times for 512 byte sectors when the cylinder is formatted
	1	A1*	
	1	FE	
	1	[cylinder no.]	
	1	[head no.]	
	1	[sector no.]	
	2	[CRC character]	
	10	00	
	12	00	
	1	A1*	
	1	F8	Written out when a sector is written to
	512	[Data character]	
	2	[CRC character]	
	3	00	
	15	4E	
	(as required)	<or>	
Stop at:	until sub- sequent Index pulse	4E	

* Character written with one missing clock pulse.

3.6 Magnetic Tape Controller.

Figure 3-3 is the MTU Controller Matrix Map. Table 3-9 lists the signal-pin connections for the cable from the MTU Controller to the DEI tape drive.

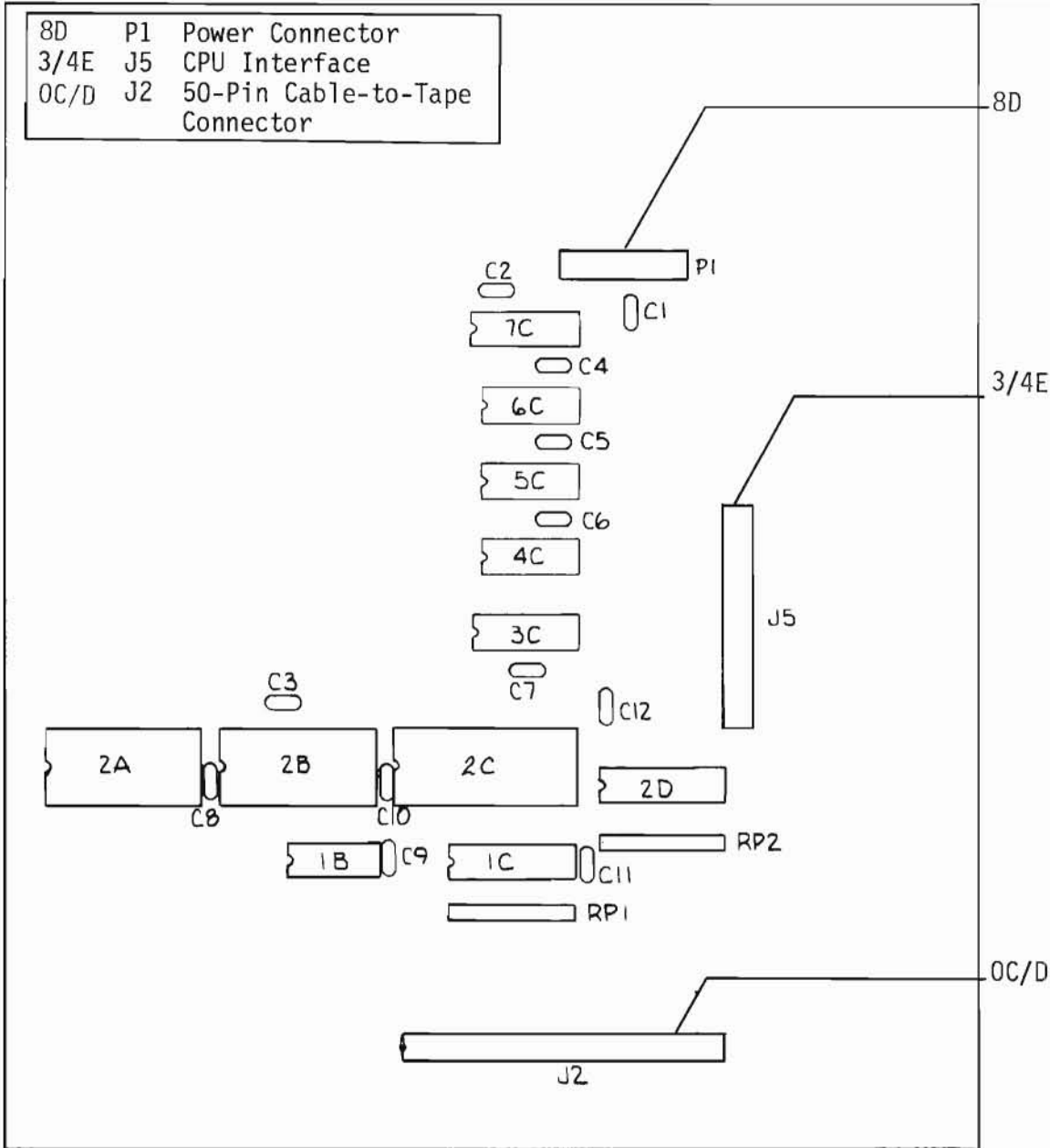


Figure 3-3. MTU Controller Board Matarix Map

Table 3-9. MTU Controller to DEI Drive
Signal Pin Assignments

PIN #	SIGNAL	FROM	COMMENTS
2	SLD-	Drive	Selected
4	RDY-	Drive	Ready
6	WND-	Drive	Write Enabled
8	FLG-	Drive	Flag
10	LPS-	Drive	Load Point Sensed
12	FUP-	Drive	File Unprotected
14	BSY-	Drive	Busy
16	EWS-	Drive	Early Warning Sensed
18	RWD-	Controller	Rewind
20	REV-	Controller	Reverse
22	FWD-	Controller	Forward
24	HSP-	Controller	High Speed
26	WEN-	Controller	Write Enable
28	SL1-	Controller	Unit Select 2 ⁰
30	SL2-	Controller	Unit Select 2 ¹
32	SL4-	Controller	Unit Select 2 ²
34	SLG-	Controller	Select Gate
36	RNZ-	Drive	Read NRZ Data
38	RDS-	Drive	Read Data Strobe
40	DAD-	Drive	Data Detected
42	WDE-	Controller	Write Data Enabled
44	WNZ-	Controller	Write NRZ Data
46	TR2-	Controller	Track Select 2 ¹
48	WDS-	Drive	Write Data Strobe
50	TR1-	Controller	Track Select 2 ⁰

NOTE: 1) All odd numbered pins are returns.

2) Mating connector: 3M Part Number 3425-3000 or equivalent.